Implementing the TL431 feedback loop

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This paper details the numerous ways to implement a feedback network with an optocoupler and a TL431 when implementing shunt regulators. Depending on the configuration of the devices and the method used to measure the open-loop response, some unusual results may appear.

The shunt regulator

The optocoupler is used alone and delivers some current to a shunt regulator such as implemented by the MC3337X series or the MC44608. In these devices, the duty-cycle DC is adjusted by injecting a current into a feedback pin (FB). When the current is low or zero, the duty-cycle is pushed to the max (74% for the MC33370, 80% for the MC44608). If more current is pushed into the pin, the duty-cycle goes toward a few percents. The amount of current needed to go from full DC to null DC determines the PWM gain, assuming the measurement is carried upon a linear portion on the curve DC versus I_{FB}. According to these remarks, there are two ways to model the PWM chain but only one is valid to calculate the pole and zeroes created by the primary compensation network (MC3337X series only). **Figure 1** details how the duty-cycle conversion takes place :

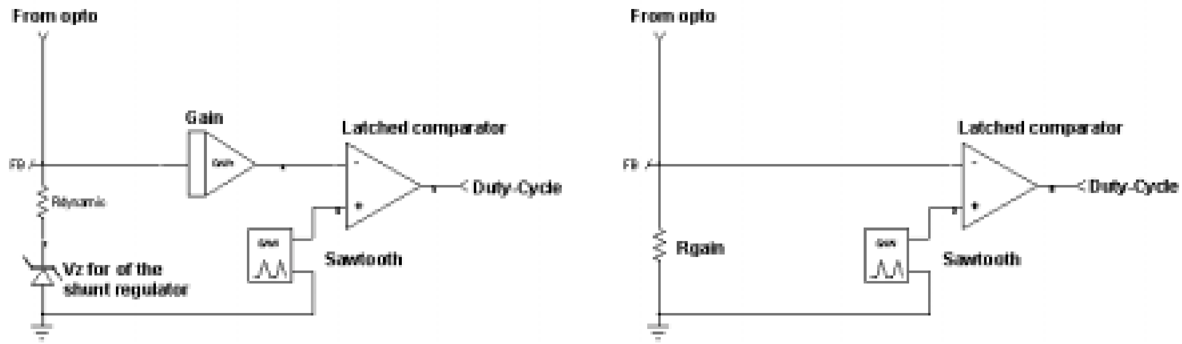


Figure 1
The complete PWM chain in a shunt regulator

As previously said, the FB corresponds to the input of a shunt regulator. To better understand the way it works, you can replace the shunt regulator by a power zener: when the voltage you apply on the FB pin is below the shunt breakdown level, no current flows into the pin and DC is maximum. When the FB level reaches the zener threshold, a current circulates in the pin and is converted into a lowering duty-cycle. First remark, in steady-state operation, the FB pin is at the shunt level as given in the data-sheet: 8.6V for the MC3337X series or 5V for the MC44608. You shall then provide the feedback current through a source whose value is, at least, two or three volts above the shunt value. Otherwise you will not reach the appropriate level to regulate and you will force the optocoupler to operate in low V_{CE}s region where the conductance d_{IC}/dV_{CE} is rather poor.

For AC analysis, the FB pin can be replaced by the dynamic resistor of the power zener, dVzener/dIdiode: 18Ω for the MC3337X series, 20Ω for the MC44608. This value gives you the AC impedance seen from the FB pin. On MC3337X series, it will dictate the locations of the pole and zeroes you create by adding capacitors around this pin. This is NOT the PWM gain, but rather an intermediate current/voltage conversion gain. The complete gain, as highlighted by figure 1, depends on the internal sawtooth amplitude (1.6Vpp for the 44608, 1.4Vpp for the MC3337X) and the maximum duty-cycle. The calculation of G is easily done following the steps:

MC44608	**MC3337X**
ΔI_{FB} of 2mA → ΔDC of 80%	ΔI_{FB} of 6mA→ΔDC of 74%
2mA • 20Ω = 40mV	6mA • 18Ω = 108mV
80% over 1.6Vpp = 1.28V	74% over 1.4Vpp = 1.036V

$$G = 20 \cdot Log\left(\frac{1.28}{40m}\right) = 30.1dB \qquad G = 20 \cdot Log\left(\frac{1.036}{108m}\right) = 19.63dB$$

Finally since the internal FB dynamic impedance also participates to the gain, the complete PWM chain exhibits the following values:

MC44608: 30.1dB + $26dB_{20\Omega}$ = 56.1dB
MC3337X: 19.63dB + $25.1dB_{18\Omega}$ = 44.73dB

These results could also be simply replaced by some equivalent resistor R_{GAIN} that would perform the complete I/V translation to the latched comparator (right portion of figure 1 drawing):

Duty-Cycle of MC44608 = 80% (1.6Vpp) – R_{GAIN} . I_{FB} → R_{GAIN} = 640Ω (20.Log 640 = 56.1dB)
Duty-Cycle of MC3337X = 74% (1.4Vpp) – R_{GAIN} . I_{FB} → R_{GAIN} = 172.66Ω (20 . Log 172.66 = 44.7dB)

However, on the MC3337X series, we can place some capacitors across the FB pin to the ground in order to introduce pertinent poles and zeroes. The resistive value that shall be taken for the calculation is 18Ω. For the 44608, you can take either values 20Ω or 640Ω to evaluate the complete gain chain (FLYBACK + PWM + Compensation) since no other elements are disposed around the FB pin.

First case: the optocoupler is alone

This is the most economic case where the output voltage does not require a tight regulation. The optocoupler Light Emitting Diode (LED) is simply inserted in series with a zener diode. The output level is then close to Vz + Vf, with Vz the zener voltage and Vf the forward level of the LED. **Figure 2a** depicts this situation when a compensation network made of Rs and C1 is added (MC3337X case).

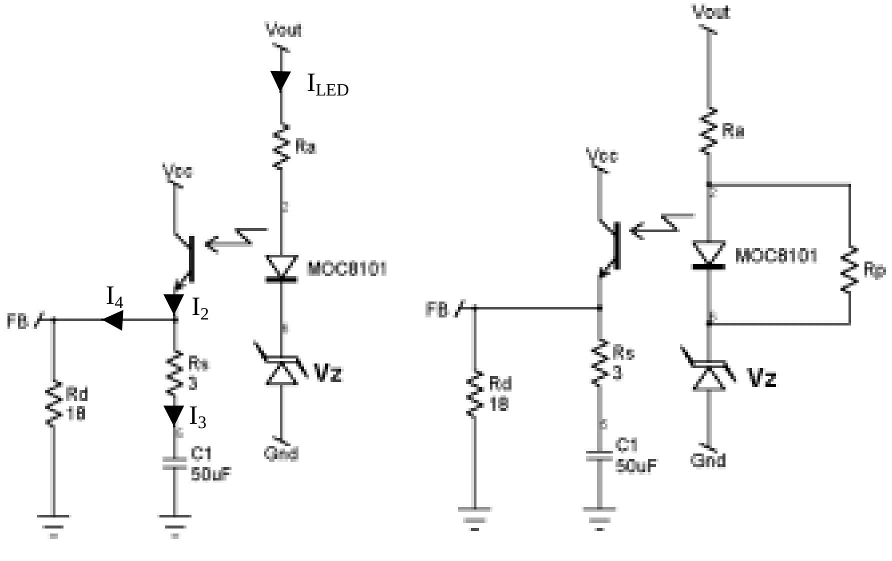


Figure 2a and 2b
On the right side, a resistor Rp is added to refine the stabilization but it also ***slightly*** decreases the loop gain

The calculation steps are rather easy and will be reproduced all along this document. It consists in a) evaluating the LED current b) finding its relationship with I_{FB} or V_{PWM} c) derive the result to obtain the small-signal gain. However, in a so simple schematic, we can highlight the parasitic element the LED and the zener are made of (**figure 3a**). Taking into account that the perfect sources Vf and Vz do not move with Vout, the final equation for the LED current reduces to: $I_{LED} = \frac{Vout}{R_A + Rd_{LED} + Rd_Z}$.

$$I_2 = I_{LED} \cdot C\mathrm{TR}$$

$$V_{PWM} = I_4 \cdot Rd = I_2 \cdot \frac{Z1 \cdot Rd}{Z1 + Rd} = I_{LED} \cdot C\mathrm{TR} \cdot \frac{Z1 \cdot Rd}{Z1 + Rd}$$

$$V_{PWM} = \frac{Vout}{Ra + Rd_{LED} + Rd_Z} \cdot CTR \cdot Rd \cdot \frac{1 + \frac{1}{Rs \cdot C1 \cdot p}}{1 + \frac{1}{(Rs + Rd) \cdot C1 \cdot p}}$$

$$\frac{dV_{PWM}}{dVout} = [Rd // Rs] \cdot \frac{CTR}{Ra + Rd_{LED} + Rd_Z} \cdot \frac{1 + \frac{1}{Rs \cdot C1 \cdot p}}{1 + \frac{1}{(Rs + Rd) \cdot C1 \cdot p}}$$

we then define a zero f_Z and a pole f_P: $f_Z = \frac{1}{2 \cdot \pi \cdot Rs \cdot C1}$ and, $f_P = \frac{1}{2 \cdot \pi \cdot (Rd + Rs) \cdot C1}$

In DC, the gain simplifies to: $DCgain = \frac{Rd \cdot CTR}{Ra + Rd_{LED} + Rd_Z}$ while in high-frequency, when C1 is a complete short: $HFgain = \frac{[Rd // Rs] \cdot CTR}{Ra + Rd_{LED} + Rd_Z}$

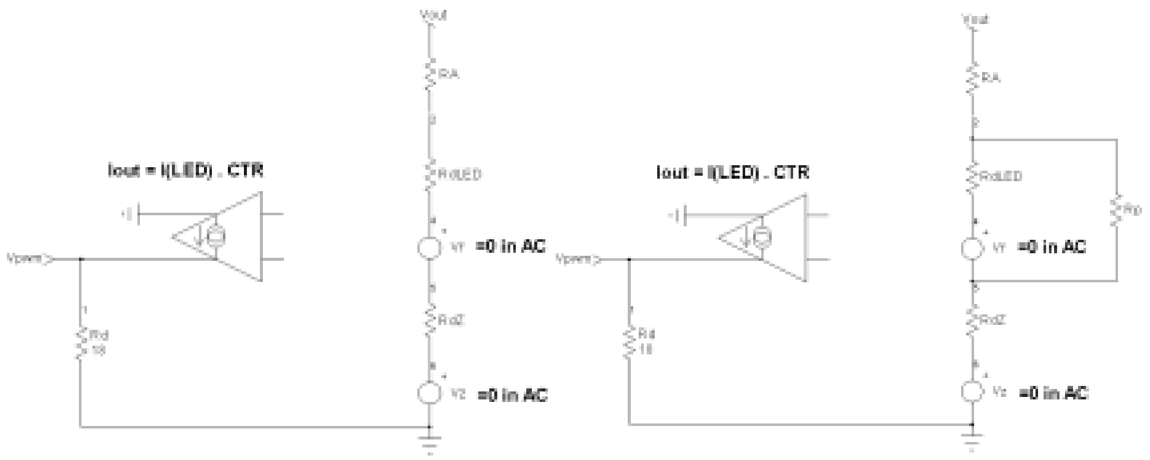


Figure 3a and 3b

Since Vf and Vz do not vary in AC, we can put them to zero for the analysis

In some applications, it is interesting to increase the current flowing into the zener to gain in precision: the zener operates far away from its knee where dVz/dIzener is rather high. To implement this option, simply wire a resistor in parallel with the LED as **figure 2b** and **3b** show. In AC, Rp now comes in parallel with Rd and affects the DC gain by: $DC_{gain} = \frac{1}{RA + Rd_{LED} // Rp + Rd_Z} \cdot \frac{Rp}{Rp + Rd_{LED}} \cdot CTR \cdot Rd$. When Rp becomes infinite, this formula simplifies to the previous one. As we can imagine, with rather low values of Rd_{LED}, the gain is *slightly* degraded by the presence of Rp.

Numerical application for figure 2a example:

Rd = 18Ω	CTR = 1.8 (180%)
Cs = 50µF	R_A = 270Ω
Rs = 3Ω	Rd_{LED} and Rd_Z are neglected.

DC_{gain} = -18.41dB
HF_{gain} = -35.32dB
1st pole = 151Hz
1st zero = 1.061kHz

The very low static-gain engendered by this configuration is not compatible with a good audiosusceptibility. The TL431 will help us to raise this poor value.

An integrator with the TL431 to boost the DC gain

By wiring a TL431 as depicted by **figure 4a**, we will offer better ripple rejection by rising the DC gain. We have removed the previous passive RC network, but their action is similar as the one calculated. Please note that Vo is split in two values: Vo and k x Vo. In FLYBACK converters operating in Discontinuous Conduction Mode (DCM), the high secondary peak current generates a thin output spike when combined with the output capacitor's ESR. To fight against this problem, you can add a small series inductor of a few µH. Unfortunately, it also adds a second order high-frequency pole that you won't take into the final feedback path. You then split the feedback in two ways: a fast one with low gain through the LED anode (k x Vo) and a low-frequency with high gain on the resistive divider (Vo). As a first remark, we can see that when either the TL431's gain or the network across it roll its gain to zero, we come back to figure 2a configuration. Therefore we cannot really roll the whole loop gain to zero! That is a typical pain of the TL431 but we can also turn it into an advantage as we will see later on.

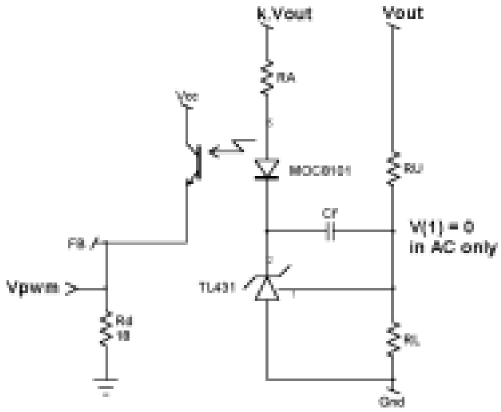


Figure 4a

A TL431 helps to rise the gain in DC

Let us start by the DC analysis where Cf is open and in lack of feedback on the TL431, the node 1 is NOT at zero:

$$I_{LED} = \frac{k \cdot Vout - (Vf + Vz)}{R_A}$$ with Vz = TL431'Anode-Cathode voltage.

$Vz = -Vout \cdot \frac{RL}{RU + RL} \cdot Av_{TL431}$ and $Vpwm = I_{LED} \cdot C\mathrm{TR} \cdot Rd$. The final equation for Vpwm is then:

$$Vpwm = \frac{k \cdot Vout - \left(Vf - \frac{Vout \cdot RL}{RL + RU}\right) \cdot Av_{TL431}}{R_A} \cdot C\mathrm{TR} \cdot Rd$$

$$\frac{dVpwm}{Vout} = \frac{k \cdot (RL + RU) + RL \cdot Av_{TL431}}{R_A \cdot (RL + RU)} \cdot C\mathrm{TR} \cdot Rd \rightarrow \text{DCgain.}$$

In AC, the first I_{LED} equation still holds. But this time Cf closes the TL431 feedback path and maintains a true virtual ground on node 1: V(1) = 0 in AC. Cf creates an integrator with RU (RL does not play in AC because of the virtual ground) and the Vz parameter is expressed by:

$$Vz = -Vo \cdot \frac{1}{RU \cdot Cf \cdot p}$$

$$I_{LED} = \frac{k \cdot Vout - \left(Vf - Vout \cdot \frac{1}{RU \cdot Cf \cdot p}\right)}{R_A}$$

$\frac{dVpwm}{dVout} = \frac{(k \cdot RU \cdot Cf + 1)}{RU \cdot Cf \cdot p} \cdot \frac{CTR \cdot Rd}{R_A}$ → ACgain with a pole $fp = \frac{1}{2 \cdot \pi \cdot RU \cdot Cf}$ and a zero located at $fz = \frac{1}{2 \cdot \pi \cdot k \cdot RU \cdot Cf \cdot p}$.

To verify our calculations, a Spice engine is a very good tool. **Figure 4b** depicts an INTUSOFT's IsSpice4 (San-Pedro, CA) simulation schematic of the TL431 architecture.

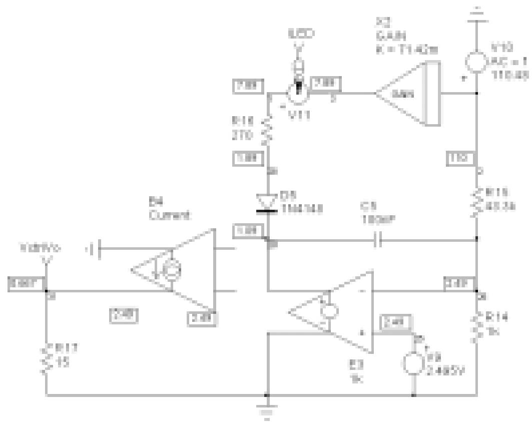


Figure 4b
A Spice simulation schematic of the TL431 structure

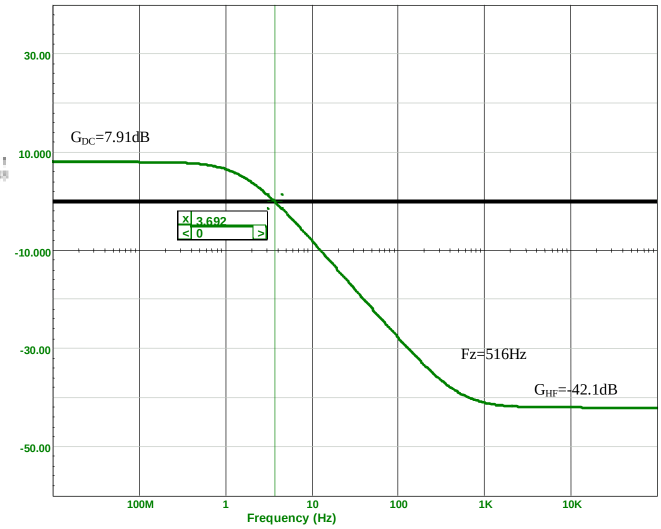


Figure 4c
The Bode plot revealed after simulation

This example simulates a FLYBACK converter delivering a 112V level (e.g. in a TV application) while the LED is biased through an 8V winding. Therefore k = 8/112 = 71.42m. The optocoupler is replaced by a current-controlled current source with a gain of 2 (CTR = 200%) for simpler calculations. V10 is adjusted to keep a correct DC point (as the schematic values testify) and is AC modulated to draw the output Bode plot.

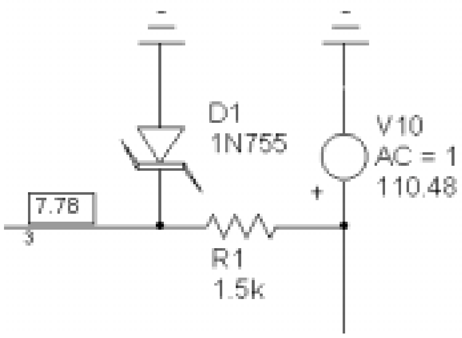


Figure 4c
A zener and a resistor is added

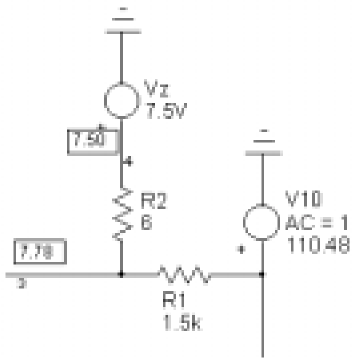


Figure 4d
and can be transformed into this network

Numerical application for figure 4b example:

Rd = 15Ω	CTR = 2 (200%)
R_A = 270Ω	TL431 gain = 1000
RU = 43.3kΩ	RL = 1kΩ
Cf = 100nF	k = 71.42m

DC_{gain} = 8dB
HF_{gain} = -42dB

1^{st} pole x $\dfrac{CTR \cdot Rd}{R_A}$ = fc @ 0dB = 4.08Hz (the small mismatch is due to the natural low Av_{TL431} of 55dB)
1^{st} zero = 514.6Hz

As we said, the presence of the zero at 514Hz can certainly help to boost the phase before the final 0dB cross-over approaches. But, this zero is a function of the coupling between the 112V and the 8V (where the LED is biased from). What is going on if we now remove the biasing from the 8V and add a resistor + zener network directly from the 112V. In this case, we have the sketch depicted by **figure 4c** and **figure 4d**. The k coefficient is now dependent upon R1 but also R2 which is actually the dynamic impedance of the zener. If we now sweep R1 from 300Ω up to 1.5kΩ, we observe a displacement of the zero toward high frequencies. It typically starts from 1.87kHz (k = 19.6m with 300Ω) and grows up to 9.2kHz (k = 3.98m with 1.5kΩ). The evaluation is not easy because R1 fixes a portion of the k coefficient but also makes the dVz/dId rolls over the zener characteristic. The lower the current, the higher the dynamic impedance of the zener (you approach the breakdown knee). As a conclusion, you thought by implementing a zener diode you would improve the regulation but you lost a useful zero that was surely helping to cross the 0dB with a –1 slope.

The TL431 with a DC feedback

We now add a simple feedback resistor between the TL431's cathode and its reference pin (**figure 5a**).

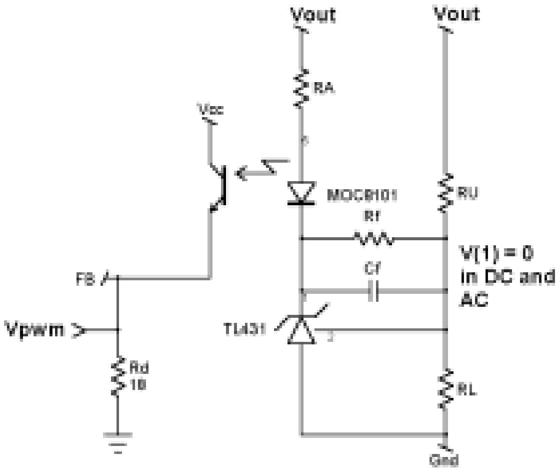


Figure 5a
The DC is no longer in open-loop for the TL431 thanks to Rf

This time, we have a virtual ground in DC and AC. The expression of the LED current changes a bit as RL no longer acts:

$$I_{LED} = \frac{Vout - \left(Vf - Vout \cdot \frac{Rf}{RU}\right)}{RA} \text{ and } Vpwm = I_{LED} \cdot CTR \cdot Rd$$

$$\frac{dVpwm}{Vout} = \frac{RU + Rf}{RU \cdot R_A} \cdot CTR \cdot Rd \rightarrow \text{DCgain}$$

In AC, $Vz = -Vout \cdot \dfrac{Rf}{RU \cdot (1 + Rf \cdot Cf \cdot p)}$ and the final gain becomes:

$$\frac{dVpwm}{dVout} = \frac{(RU + Rf) \cdot \left(1 + \frac{RU \cdot Rf}{RU + Rf} \cdot Cf \cdot p\right)}{RU \cdot RA \cdot (1 + Rf \cdot Cf \cdot p)} \cdot CTR \cdot Rd \rightarrow \text{ACgain expression}$$

Measuring the open-loop gain of the SMPS

The usual method consists in opening the loop at a place where ALL the feedback paths are gathered. The most difficult thing is to keep the operating point corresponding to the application. Various methods including injection transformers have been extensively described and relevant information can be found on Venable’s Web site [1]. As long as you are able to open the loop and provide an AC modulated DC bias, you can generate a Bode plot of the SMPS with a network analyzer. **Figure 6a** depicts a multi-output SMPS using an MC44608 in a FLYBACK configuration. The loop has been purposely opened and the correct DC point is given by V10. Once the simulation has completed, we can a) see that the operating point is correct by printing the OP values in the schematic b) directly draw a Bode plot of the signal available at node 9 (feedback divider). The plot is available on **figure 6b**.

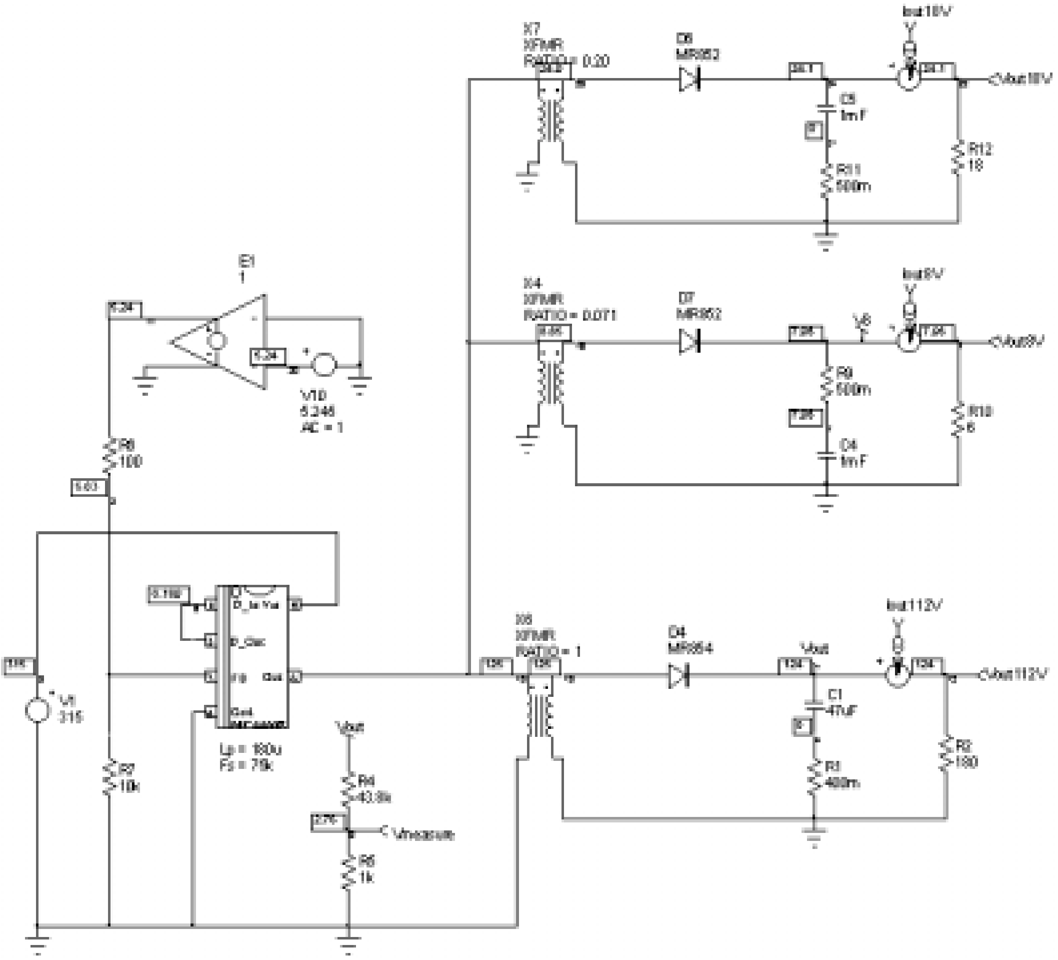
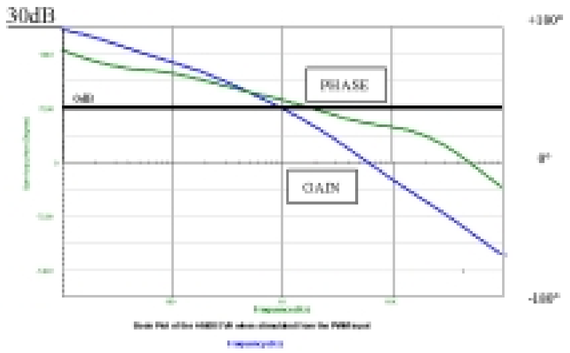


Figure 6a
The multi-output FLYBACK converter

To verify the validity of our approach, a real Bode plot has been measured using a network analyzer, as presented by **figure 6c**. The results are very similar.



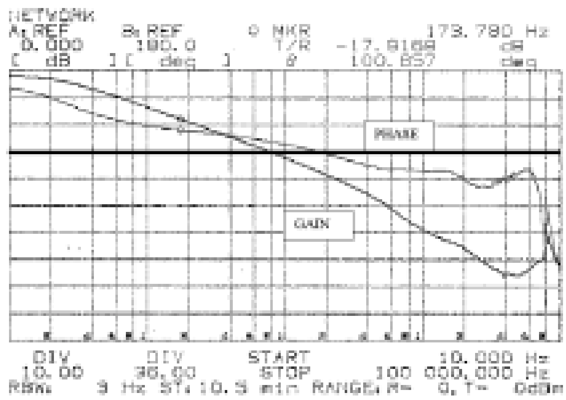


Figure 6b
IsSpice4 simulation results

Figure 6c
A real Bode plot measurement

If we now add a simple optocoupler following **figure 7a** sketch, we should normally include the (low) gain associated to this network. However, the new gain plot measured at node 9 highlights a loss of more than –40dBs compared to the previous sweep! What append? The optocoupler used as in figure 7a implements a negative feedback coming from the auxiliary winding. As a matter of fact, if Vmodulation goes down, I_{LED} goes up as I_{FB}. But Vauxiliary or (k **.**Vout) goes up and tries to oppose the previous action. If things were well equilibrated, ΔVaux could perfectly compensate for ΔVmodulation and the corresponding ΔI_{FB} would be invariant. Actually, the system can be reduced to the following closed-loop configuration (**figure 7b**):

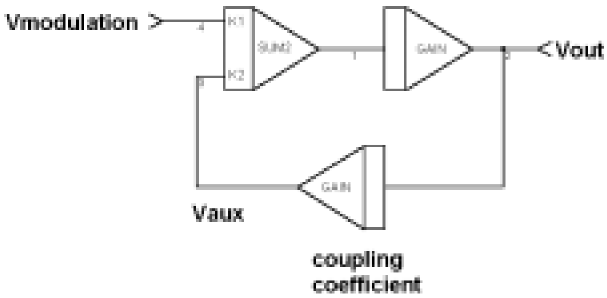


Figure 7b
The closed-loop system corresponding to figure 7a's sketch

The classical closed-loop equation can be used to describe the system: $G_{CL} = \frac{G_{OL}}{1 + k \cdot G_{OL}}$. Since GOL is rather big, this equation simply reduces to $\frac{1}{k}$. With a feedback on the 8V and regulating the 112V, the final gain is $20Log\left(\frac{1}{0.071}\right)$or 22.94dB (-33dB since we measure on node 9) . If we now use the 18V, k becomes 0.2 and the new gain is 13.97dB. Figure 7c and 7c respectively compare the real measurement while using figure 7a sketch and the simulated results with a fixed bias voltage, a bias coming from the 8V and a bias coming from the 18V. With a fixed bias, k goes down to zero and the loop gain stays unchanged at G_{OL}.

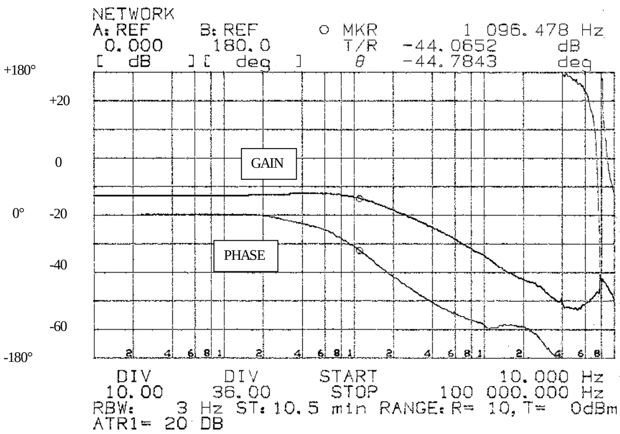


Figure 7b
Measurements on node 9 with figure 7a technique

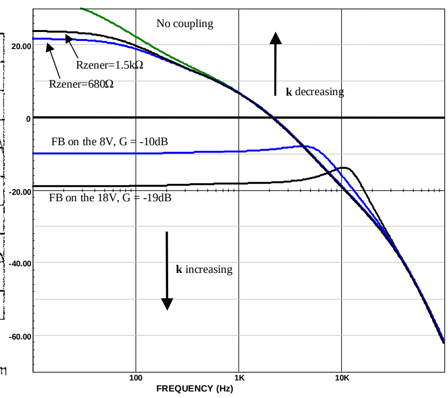


Figure 7c
The simulation shows a slight peaking due to CCM

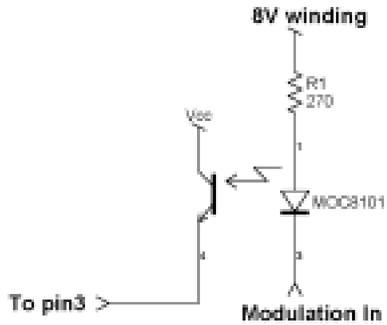


Figure 7a
Implementing the optocoupler

The simulations show a slight gain peaking because the model has entered a light Continuous Conduction Mode (CCM) what the MC44608 naturally prevents by implementing a demag pin.

Deriving the bias level with a zener diode

Decoupling the 8V winding with a zener diode (figure 4c) certainly brings some benefits. The lowest k coefficient we have, the better it is to lower the influence of the LED anode circuit (gain G2 closer to 0dB). Two measurements have been carried with a 7.5V zener and a series resistor R1 of 680Ω and 1.5kΩ. Derived from the 14V rail we impose a bias current of 9.5mA in the first case, while it drops to 4.3mA in the second one. By looking at figure 7d chart, we can deduce both zener dynamic impedances:

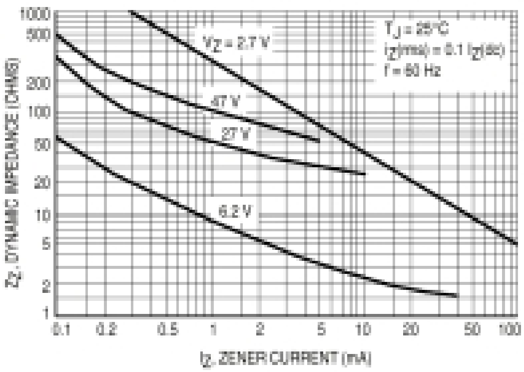


Figure 7d
Dynamic zener impedance variations with bias current

With 680Ω, we impose 9.5mA and Rdzener equals: 2Ω. With the 1.5kΩ, we move a little bit back to the zener knee and Rd rises at 3.8Ω (Id = 4.3mA). In the first case, k is evaluated at $\frac{Rd_{zener}}{Rd_{zener}+R1} = 2.93m$ while in the second case, k drops to 2.5m. The simulation results show higher gains probably because of the dynamic impedance of the zener model which is a bit smaller than in reality. However, the plot confirms that lowering the biasing resistance accordingly lowers the gain (k increases).

How these results impact the closed-loop system

In **figure 8a**, we have added the TL431 and the all the circuitry to make a complete closed-loop SMPS. We easily open the loop by inserting a 1kH inductor which opens in AC but keeps the DC point at the good value. An AC source is then coupled via a 1kF capacitor to actually sweep the SMPS.

When the continuous point is automatically kept at the right value, it is a child play to modify the parameters and watch how they affect the curves. Figure 8b has gathered various results where we see that changing the auxiliary winding from 8V to 18V changes the cross-over frequency but the phase margin is still good. The insertion of a 1.5kΩ + 7.5Vzener drastically degrades the transfer function. As we said, decreasing k pushes the zero toward higher frequencies and it does no longer provide a phase boost at low frequencies. As a result, the phase margin has vanished to a poor value and the supply is unstable. With a 8V feedback, the bandwidth is around 5kHz with a phase margin of 45°. The immediate benefit of Spice simulations is the ability given to the designer to play with the parameters affecting the SMPS performance: ESRs, input voltage, loads etc.

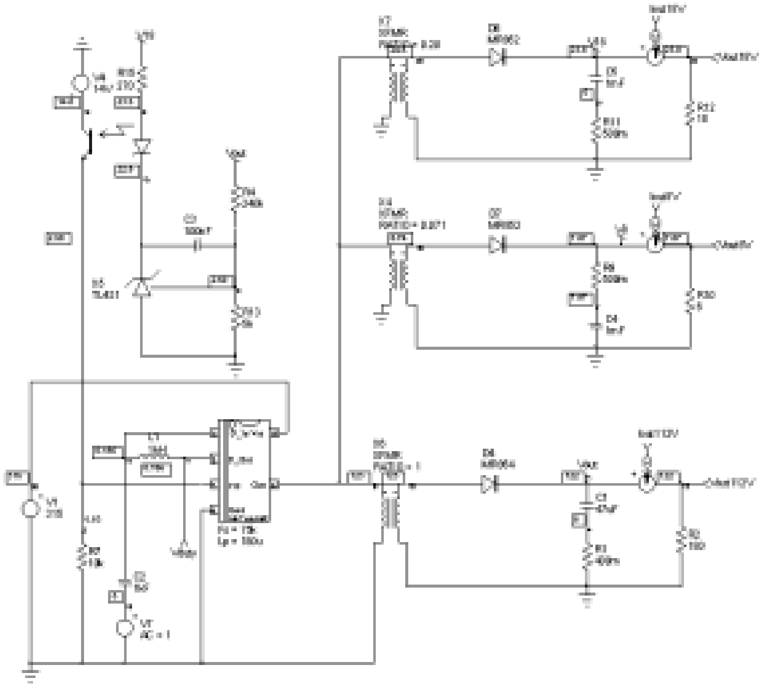


Figure 8a
The complete closed-loop system

Another comfortable advantage lies in the facility with which the final bandwidth can be tailored to the designer needs.

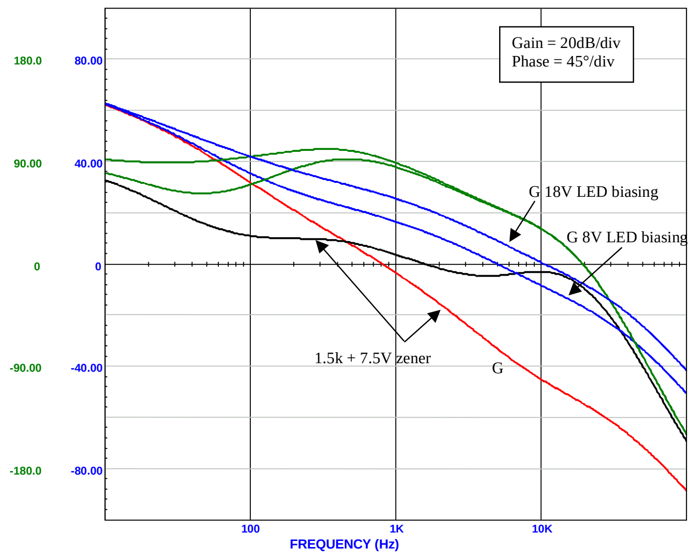


Figure 8b
The closed-loop Bode plot of the FLYBACK SMPS

Conclusion

This paper has tried to gather some typical TL431 configurations. It shows how some anodyne configurations can drastically change the final system performance either in good or in bad. It also confirms the power of a simulation engine to help adapting the system performance to the application needs in a minimum of time.

1. http://www.venableind.com/