ACT361

Rev 1, 24-Jun-09

High Performance *ActivePSR*™ Primary Switching Regulator

FEATURES

- **Patented Primary Side Regulation Technology**
- **No Opto-Coupler**
- **Best-in-Class Constant Voltage, Constant Current Accuracy**
- **Low EMI**
- **Proprietary Fast Startup Circuit**
- **Built-in Soft-Start Circuit**
- **Integrated Line and Primary Inductance Compensation**
- **Integrated Programmable Output Cord Resistance Compensation**
- **Line Under-Voltage, Output Over-Voltage, Output Short-Circuit and Over-Temperature Protection**
- **Complies with all Global Energy Efficiency and CEC Average Efficiency Standards**
- **Adjustable power from 2W to 7W**
- **Minimum External Components**
- **Tiny SOT23-6 Package**

APPLICATIONS

- **Chargers for Cell Phones, PDAs, MP3, Portable Media Players, DSCs, and Other Portable Devices and Appliances**
- **RCC Adapter Replacements**
- **Linear Adapter Replacements**
- **Standby and Auxiliary Supplies**

GENERAL DESCRIPTION

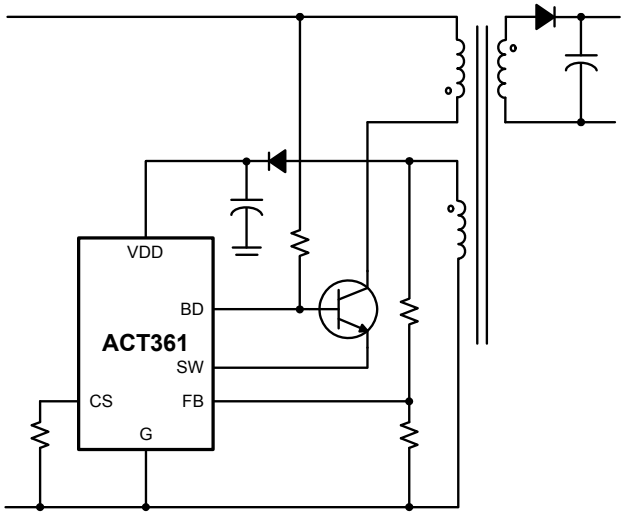
The ACT361 belongs to the high performance patented *ActivePSR*™ Family of Universal-input AC/DC off-line controllers for battery charger and adapter applications. It is designed for flyback topology working in discontinuous conduction mode (DCM). The ACT361 meets all of the global energy efficiency regulations (CEC, European Blue Angel, and US Energy Star standards) while using very few external components.

The ACT361 ensures safe operation with complete protection against all fault conditions. Built-in protection circuitry is provided for output short-circuit, output over-voltage, line under-voltage, and over temperature conditions.

The ACT361 *ActivePSR*™ is optimized for high performance, cost-sensitive applications, and utilizes Active-Semi's proprietary primary-side feedback architecture to provide accurate constant voltage, constant current (CV/CC) regulation without the need of an opto-coupler or reference device. Integrated line and primary inductance compensation circuitry provides accurate constant current operation despite wide variations in line voltage and primary inductance. Integrated output cord resistance compensation further enhances output accuracy. The ACT361 achieves excellent regulation and transient response, yet requires less than 150mW of standby power.

The ACT361 is optimized for 2W to 7W applications. It is available in space-saving 6 pin SOT23-6 package.

Figure 1:
Simplified Application Circuit



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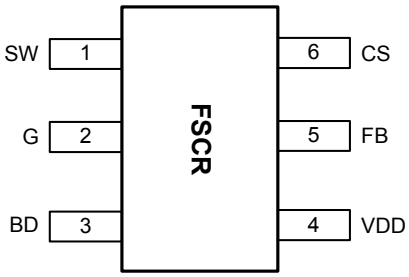
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT361US-T	-40°C to 85°C	SOT23-6	6	TAPE & REEL	FSCR

PIN CONFIGURATION



SOT23-6
ACT361US-T

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	SW	Switch Drive. Switch node for the external NPN transistor. Connect this pin to the external power NPN's emitter. This pin also supplies current to VDD during startup.
2	G	Ground.
3	BD	Base Drive. Base driver for the external NPN transistor.
4	VDD	Power Supply. This pin provides bias power for the IC during startup and steady state operation.
5	FB	Feedback Pin. Connect this pin to a resistor divider network from the auxiliary winding.
6	CS	Current Sense Pin. Connect an external resistor (R_{CS}) between this pin and ground to set peak current limit for the primary switch. The peak current limit is set by (0.4V × 0.9) / R_{CS}. For more detailed information, see Application Information.

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ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VDD, BD, SW to G	-0.3 to +28	V
Maximum Continuous VDD Current	100	mA
FB, CS to G	-0.3 to +6	V
Continuous SW Current	Internally limited	A
Maximum Power Dissipation (derate 4.5mW/˚C above T_A = 50˚C)	0.45	W
Junction to Ambient Thermal Resistance (θ_{JA})	220	˚C/W
Operating Junction Temperature	-40 to 150	˚C
Storage Junction	-55 to 150	˚C
Lead Temperature (Soldering, 10 sec)	300	˚C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 14V, V_{OUT} = 5V, L_P = 2.3mH, N_P = 140, N_S = 10, N_A = 27, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising from 0	17.6	18.6	19.6	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling after Turn-on	5.25	5.5	5.75	V
Supply Current	I_{DD}	V_{DD} = 14V, after Turn-on		1	2	mA
Start Up Supply Current	I_{DDST}	V_{DD} = 14V, before Turn-on		25	45	μA
BD Current during Startup	I_{BDST}				1	μA
Internal Soft Startup Time				10		ms
Oscillator						
Switching Frequency	f_{SW}	100% V_{OUTCV} @ full load		40	45	kHz
		25% V_{OUTCV} @ full load		20		
Maximum Duty Cycle	D_{MAX}		70	75	80	%
Feedback						
Effective FB Voltage	V_{FB}		2.176	2.200	2.224	V
FB Leakage Current					100	nA
Output Cable Resistance Compensation	DV_{COMP}	No R_{CORD} between VDD and SW		0		%
		R_{CORD} = 330k		3		
		R_{CORD} = 160k		6		
		R_{CORD} = 82k		9		
		R_{CORD} = 39k		12		

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ELECTRICAL CHARACTERISTICS CONT'D

(V_{DD} = 14V, V_{OUT} = 5V, L_P = 2.3mH, N_P = 140, N_S = 10, N_A = 27, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit						
SW Current Limit Range			100		600	mA
CS Current Limit Threshold	V_{CSLIM}	t_{OFF_DELAY} = 0	380	396	412	mV
Leading Edge Blanking Time			200	300		ns
Driver Outputs						
Switch ON-Resistance	R_{ON}	I_{SW} = 50mA		1.6	3.0	Ω
SW Off Leakage Current		V_{SW} = 22V			1	μA
Protection						
VDD Latch-Off Voltage	V_{DDOVP}		V_{DDON} +2	V_{DDON} +3	V_{DDON} +4	V
Thermal Shutdown Temperature				135		˚C
Thermal Hysteresis				20		˚C
Line UVLO	I_{FBUVLO}	R_{FB1} = 53.6kΩ		0.12		mA

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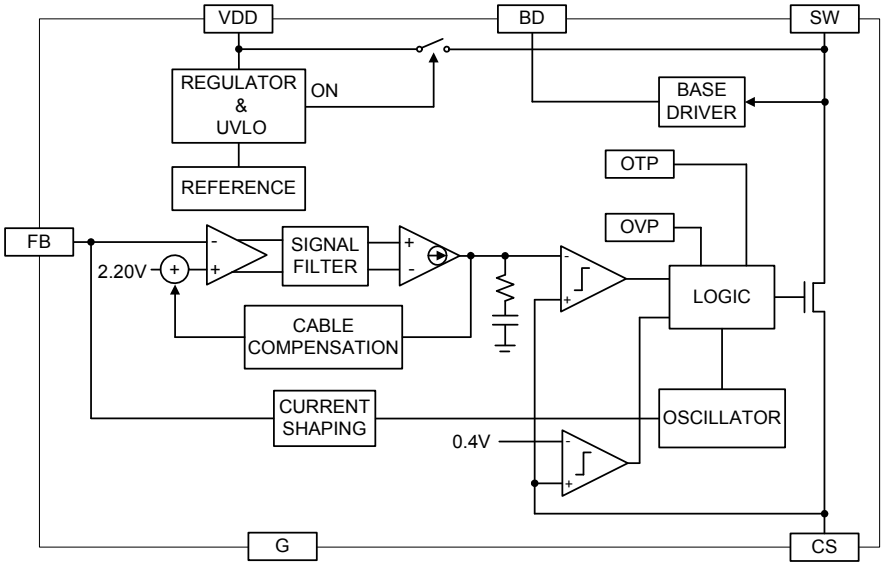
FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As shown in the *Functional Block Diagram,* to regulate the output voltage in CV (constant voltage) mode, the ACT361 compares the feedback voltage at FB pin to the internal reference and generates an error signal to the pre-amplifier. The error signal, after filtering out the switching transients and compensated with the internal compensation network, modulates the external NPN transistor peak current at CS pin with current mode PFWM (Pulse Frequency and Width Modulation) control. To regulate the output current in CC (constant current) mode, the oscillator frequency is modulated by the output voltage.

SW is a driver output that drives the emitter of an external high voltage NPN transistor. This base-emitter-drive method makes the drive circuit the most efficient.

Fast Startup

VDD is the power supply terminal for the ACT361. During startup, the ACT361 typically draws only 20μA supply current. The startup resistor from the rectified high voltage DC rail supplies current to the base of the NPN transistor. This results in an amplified emitter current to VDD through the SW pin via Active-Semi's proprietary fast-startup circuitry until it exceeds the V_{DDON} threshold 19V. At this point, the ACT361 enters internal startup mode with the peak current limit ramping up in 10ms. After switching starts, the output voltage begins to rise. The VDD bypass capacitor must supply the ACT361 internal circuitry and the NPN base drive until the output voltage is high enough to sustain VDD through the auxiliary winding. The V_{DDOFF} threshold is 5.5V; therefore, the voltage on the VDD capacitor must remain above 5.5V while the output is charging up.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT361 captures the auxiliary flyback signal at FB pin through a resistor divider network R8 and R9 in Figure 2. The signal at FB pin is pre-amplified against the internal reference voltage, and the secondary side output voltage is extracted based on Active-Semi's proprietary filter architecture.

This error signal is then amplified by the internal error amplifier. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = 2.20V \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times \frac{N_S}{N_A} - V_D \qquad (1)$$

where R_{FB1} (R8) and R_{FB2} (R9) are top and bottom feedback resistor, N_S and N_A are numbers of

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FUNCTIONAL DESCRIPTION CONT'D

transformer secondary and auxiliary turns, and V_D is the rectifier diode forward drop voltage at approximately 0.1A bias.

Standby (No Load) Mode

In no load standby mode, the ACT361 oscillator frequency is further reduced to a minimum frequency while the current pulse is reduced to a minimum level to minimize standby power. The actual minimum switching frequency is programmable with an output preload resistor.

Loop Compensation

The ACT361 integrates loop compensation circuitry for simplified application design, optimized transient response, and minimal external components.

Output Cable Resistance Compensation

The ACT361 provides programmable output cable resistance compensation during constant voltage regulation, monotonically adding an output voltage correction up to predetermined percentage at full power. There are four levels to program the output cable compensation by connecting a resistor (R4 in Figure 2) from the SW pin to VDD pin. The percentage at full power is programmable to be 3%, 6%, 9% or 12%, and by using a resistor value of 330k, 160k, 82k or 39k respectively. If there is no resistor connection, there is no cord compensation.

This feature allows for better output voltage accuracy by compensating for the output voltage droop due to the output cable resistance.

Constant Current (CC) Mode Operation

When the secondary output current reaches a level set by the internal current limiting circuit, the ACT361 enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting in a constant secondary side output current profile. The energy transferred to the output during each switching cycle is $½(L_P \times I_{LIM}^2) \times \eta$, where L_P is the transformer primary inductance, I_{LIM} is the primary peak current, and η is the conversion efficiency. From this formula, the constant output current can be derived:

$$I_{OUTCC} = \frac{1}{2} \times L_P \times \left(\frac{0.4V \times 0.9}{R_{CS}} \right)^2 \times \left(\frac{\eta \times f_{SW}}{V_{OUTCV}} \right) \qquad (2)$$

where f_{SW} is the switching frequency and V_{OUTCV} is the nominal secondary output voltage.

The constant current operation typically extends down to lower than 40% of nominal output voltage regulation.

Primary Inductance Compensation

The ACT361 integrates a built-in proprietary (patent-pending) primary inductance compensation circuit to maintain constant current regulation despite variations in transformer manufacturing. The compensated range is ±7%.

Primary Inductor Current Limit Compensation

The ACT361 integrates a primary inductor peak current limit compensation circuit to achieve constant input power over line and load ranges.

Protection

The ACT361 incorporates multiple protection functions including over-voltage, over-current and over-temperature.

Output Short Circuit Protection

When the secondary side output is short circuited, the ACT361 enters hiccup mode operation. In this condition, the VDD voltage drops below the V_{DDOFF} threshold and the auxiliary supply voltage collapses. This turns off the ACT361 and causes it to restart. This hiccup behavior continues until the short circuit is removed.

Output Over Voltage Protection

The ACT361 includes output over-voltage protection circuitry, which shuts down the IC when the output voltage is 40% above the normal regulation voltage for 4 consecutive switching cycles. The ACT361 enters hiccup mode when an output over voltage fault is detected.

Over Temperature Shutdown

The thermal shutdown circuitry detects the ACT361 die temperature. The typical over temperature threshold is 135°C with 20°C hysteresis. When the die temperature rises above this threshold the ACT361 is disabled until the die temperature falls by 20°C, at which point the ACT361 is re-enabled.

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TYPICAL APPLICATION

Design Example

The design example below gives the procedure for a DCM flyback converter using the ACT361. Refer to Application Circuit in Figure 2, the design for a charger application starts with the following specification:

Input Voltage Range	$85V_{AC}$ – $265V_{AC}$, 50/60Hz
Output Power	3.5W
Output Voltage	5.0V
OCP Current	0.78A

The operation for the circuit shown in Figure 2 is as follows: the rectifier bridge D1−D4 and the capacitor C1/C2 convert the AC line voltage to DC. This voltage supplies the primary winding of the transformer T1 and the startup resistor R1/R2. The primary power current path is formed by the transformer's primary winding, the NPN transistor, the ACT361 internal MOSFET and the current sense resistor R7. The resistor R6 and capacitor C4 create a snubber clamping network that protects Q1 from voltage spikes due to the transformer primary winding leakage inductance. The network consisting of capacitor C3 and diode D5 provides a VDD supply voltage for ACT361 from the auxiliary winding of the transformer. C3 is the decoupling capacitor of the supply voltage and energy storage component for startup. The diode D7 and the capacitor C7 rectifies and filters the output voltage. The resistor divider consisting of R8 and R9 programs the output voltage.

The minimum and maximum DC input voltages can be calculated:

$$V_{INDCMIN} = \sqrt{2V_{ACMIN}^2 - \frac{2P_{OUT}(\frac{1}{2f_L} - t_C)}{\eta \times C_{IN}}}$$

$$= \sqrt{2 \times 85^2 - \frac{2 \times 3.5(\frac{1}{2 \times 50} - 3.5ms)}{75\% \times 2 \times 4.7\mu F}} \approx 90V \quad (3)$$

$$V_{INDCMAX} = \sqrt{2} \times V_{ACMAX} = \sqrt{2} \times 265 = 375V \quad (4)$$

where η is the estimated circuit efficiency, f_L is the line frequency, t_C is the estimated rectifier conduction time, C_{IN} is empirically selected to be 2 × 4.7μF electrolytic capacitors based on the 3μF/W rule of thumb.

When the transistor is turned off, the voltage on the transistor's collector consists of the input voltage and the reflected voltage from the transformer's secondary winding. There is a ringing on the rising top edge of the flyback voltage due to the leakage inductance of the transformer. This ringing is clamped by a RCD network if it is used. Design this clamped voltage as 50V below the breakdown of the NPN transistor. The flyback voltage has to be considered with selection of the maximum reverse voltage rating of secondary rectifier diode. If a 40V Schottky diode is used, then the flyback voltage can be calculated:

$$V_{RO} = \frac{V_{INDCMAX} \times (V_{OUTCV} + V_D)}{V_{DREV} - V_{OUTCV}} = \frac{375 \times (5 + 0.37)}{40 \times 0.8 - 5} = 74.6V \quad (5)$$

where V_D is the Schottky diode forward voltage, V_{DREV} is the maximum reverse voltage rating of the diode and V_{OUTCV} is the output voltage.

The maximum duty cycle is set to be 35% at low line voltage $85V_{AC}$ and the circuit efficiency is estimated to be 72%. Then the maximum average input current is:

$$I_{IN} = \frac{V_{OUTCV} \times I_{OUTCC}}{V_{INDCMIN} \times \eta} = \frac{5 \times 0.78}{90 \times 72\%} = 60mA \quad (6)$$

The maximum input primary peak current:

$$I_{PK} = \frac{2 \times I_{IN}}{D_{MAX}} = \frac{2 \times 60}{35\%} = 343\ mA \quad (7)$$

The primary inductance of the transformer:

$$L_P = \frac{V_{INDCMAX} \times D_{MAX}}{I_{PK} \times f_{SW}} = \frac{90 \times 35\%}{300mA \times 40kHz} = 2.3mH \quad (8)$$

The primary to secondary turns ratio N_P/N_S:

$$\frac{N_P}{N_S} = \frac{V_{RO}}{V_{OUTCV} + V_D} = \frac{75}{5 + 0.37} = 14 \quad (9)$$

The auxiliary to secondary turns ratio N_A/N_S:

$$\frac{N_A}{N_S} = \frac{V_{DD} + V_D}{V_{OUTCV} + V_D + V_{CODE}} = \frac{14 + 0.37}{5 + 0.37 + 0.3} = 2.53 \quad (10)$$

An EE16 transformer gapped core with an effective inductance A_{LE} of $117nH/T^2$ is selected. The number of turns of the primary winding is:

$$N_P = \sqrt{\frac{L_P}{A_{LE}}} = \sqrt{\frac{2.3mH}{117\ nH\ /\ T^2}} = 140 \quad (11)$$

The number of turns of secondary and auxiliary windings can be derived accordingly:

$$N_S = \frac{N_S}{N_P} \times N_P = \frac{1}{14} \times 140 = 10 \quad (12)$$

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TYPICAL APPLICATION CONT'D

$$N_A = \frac{N_A}{N_S} \times N_S = 2.53 \times 10 \approx 27 \quad (13)$$

The current sense resistance (R7) determines the current limit value based on the following equation:

$$R_{CS} = \frac{V_{CSLIM} \times 0.9}{I_{PK}} = \frac{0.4V \times 0.9}{343mA} = 1.05\Omega \quad (14)$$

The voltage feedback resistors are selected according to the design. The upper feedback resistor is a fixed value determined by the ACT361 design as 53.6k. The lower feedback resistor is selected as:

$$R_{FB2} = \frac{V_{FB}}{(V_{OUTCV} + V_D)\frac{N_A}{N_S} - V_{FB}} R_{FB1}$$

$$= \frac{2.20}{(5 + 0.37) \times 2.53 - 2.20} \times 53.6 = 9.76k \quad (15)$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUTCC}}{F_{SW} \times V_{RIPPLE}} = \frac{0.7}{40kHz \times 50mV} = 350\mu F \quad (16)$$

A 470µF electrolytic capacitors are used to keep the ripple small.

PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C3), current sense resistor (R7) and feedback resistor (R8/R9) should be placed close to VDD, CS and FB pins respectively. There are two main power path loops. One is formed by C1/C2, primary winding, NPN transistor and the ACT361. The other is the secondary winding, rectifier D7 and output capacitors (C7/C8). Keep these loop areas as small as possible. Connect high current ground returns, the input capacitor ground lead, and the ACT361 G pin to a single point (star ground configuration).

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Figure 2:

Universal VAC Input, 5V/0.7A Output Charger

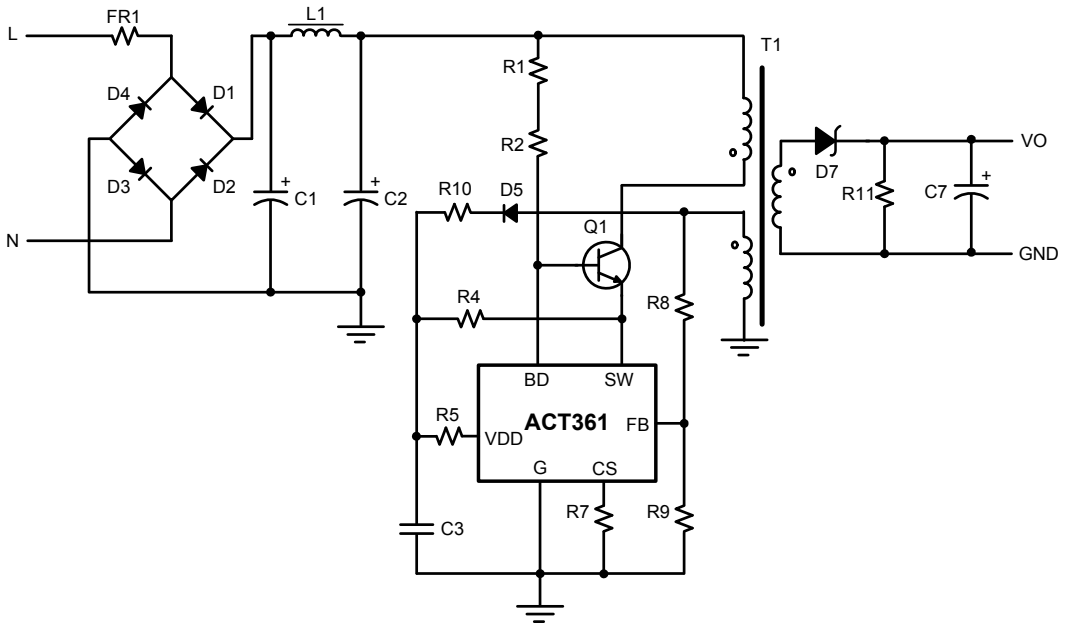

Table 1:

ACT361 Bill of Materials

ITEM	REFERENCE	DESCRIPTION	QTY	MANUFACTURER
1	U1	IC, ACT361US-T, SOT23-6	1	Active-Semi
2	C1, C2	Capacitor, Electrolytic, 4.7μF/400V, 8 × 12mm	2	KSC
3	C3	Capacitor, Ceramic, 2.2μF/35V, 1206, SMD	1	POE
4	C7	Capacitor, Electrolytic, 470μF/10V, 8 × 12mm	1	KSC
5	D1-D4	Diode, Rectifier, 1000V/1A, 1N4007, DO-41	4	Good-Ark
6	D5	Diode, Ultra Fast, FR102,100V/1.0A, DO-41	1	Good-Ark
7	D7	Diode, Schottky, 40V/2A, SB240, DO-15	1	Good-Ark
8	L1	Axial Inductor, 1.5mH, 0410, DIP	1	Amode Tech
9	Q1	Transistor, NPN, 700V,1.5A, KSB13003AR, TO-92	1	Semi How
10	RF1	Fusible Resistor, 1W, 10Ω, 5%	1	TY-OHM
11	R1, R2	Chip Resistor, 10MΩ, 1206, 5%	2	TY-OHM
12	R4	Chip Resistor, 162k, 0805, 5%	1	TY-OHM
13	R5	Chip Resistor, 22Ω, 0603, 5%	1	TY-OHM
14	R7	Chip Resistor, 1.07Ω, 1206, 5%	1	TY-OHM
15	R8	Chip Resistor, 53.6k, 0805, 1%	1	TY-OHM
16	R9	Chip Resistor, 9.76k, 0805, 1%	1	TY-OHM
17	R10	Chip Resistor, 10Ω, 0805, 5%	1	TY-OHM
18	R11	Chip Resistor, 1.1k, 0805, 5%	1	TY-OHM
19	T1	Transformer, L_P = 2.3mH±7%, EE16	1	

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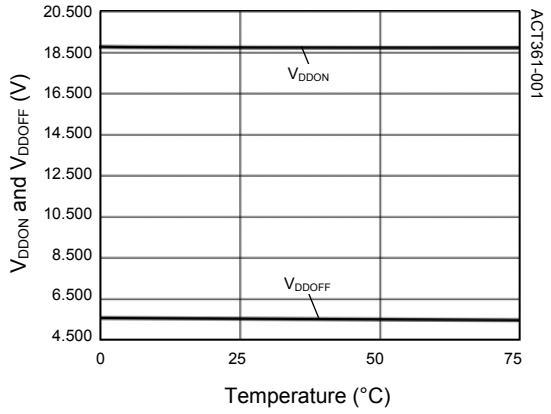
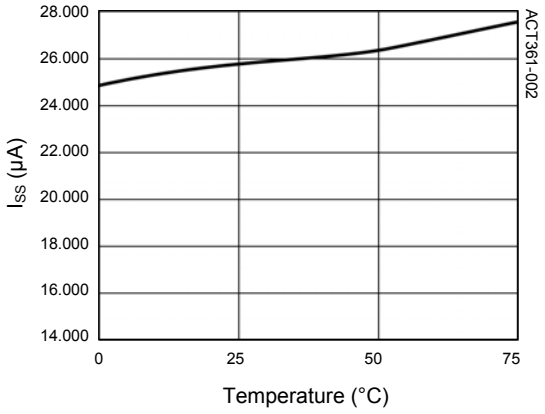
TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of Figure 2, unless otherwise specified.)

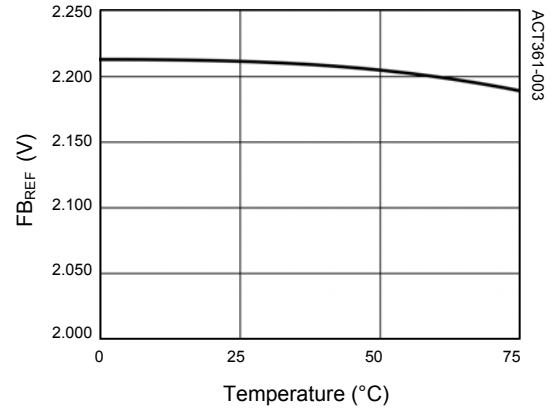
VDD ON/OFF Voltage vs. Temperature



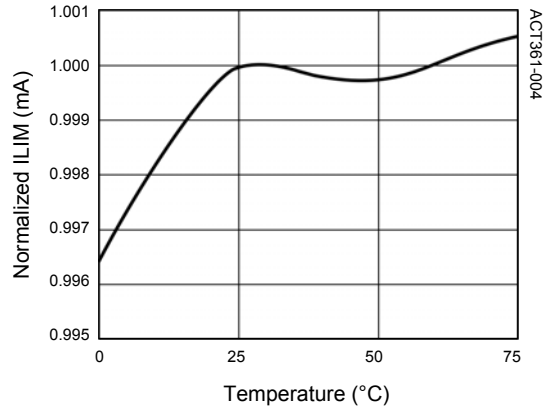
Start Up Supply Current vs. Temperature



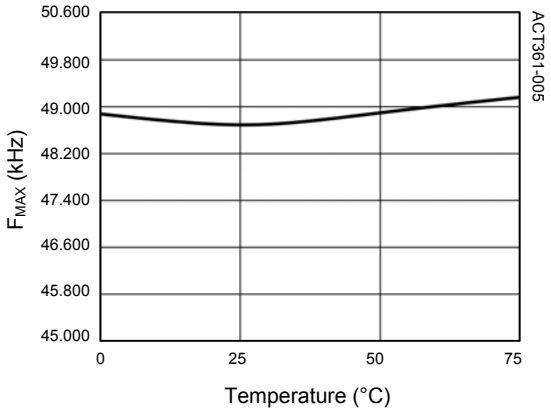
FB Voltage vs. Temperature



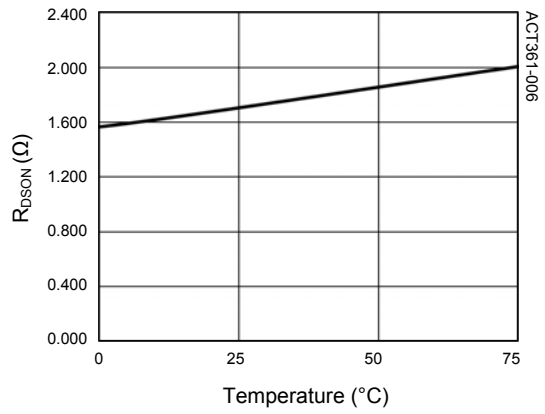
Normalized ILIM vs. Temperature



Max. Switching Frequency vs. Temperature



Internal MOSFET R_{DSON} vs. Temperature



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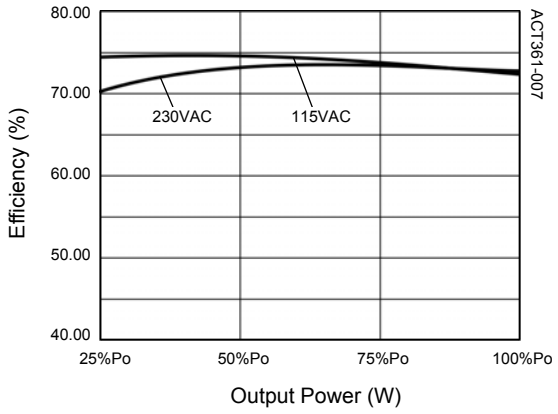
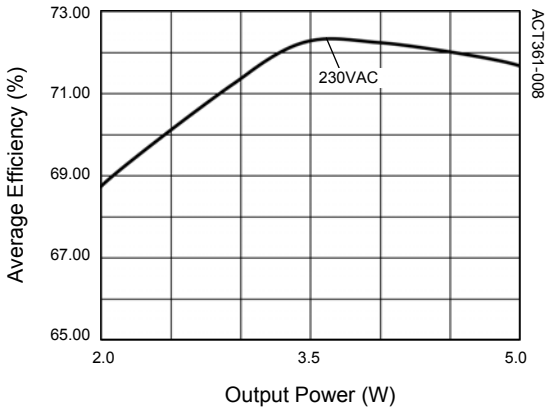
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Circuit of Figure 2, unless otherwise specified.)

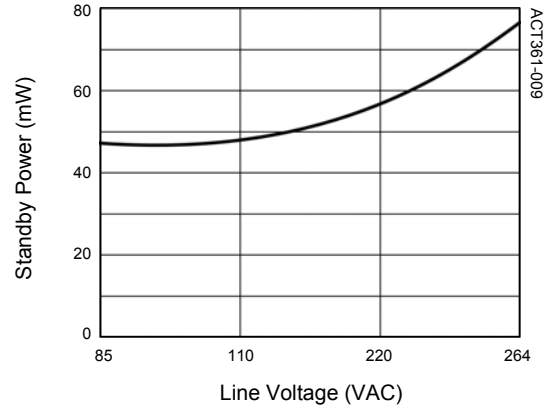
Efficiency vs. Output Power



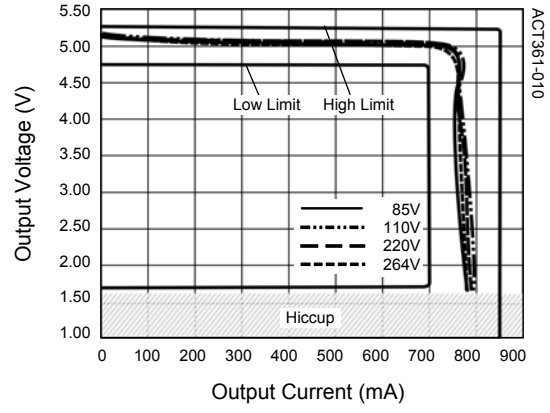
Average Efficiency vs. Output Power



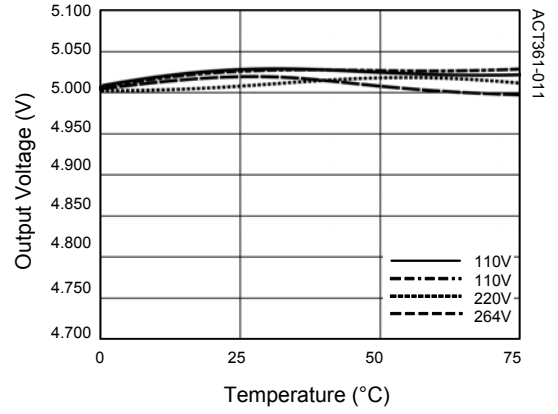
Standby Power vs. Line Voltage



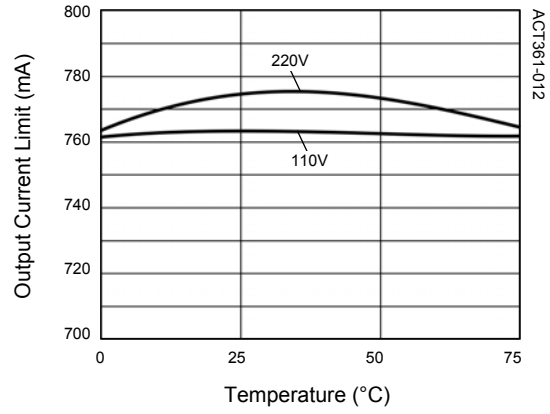
Output Voltage and Current Characteristics



Output Voltage vs. Temperature



Output Current Limit vs. Temperature



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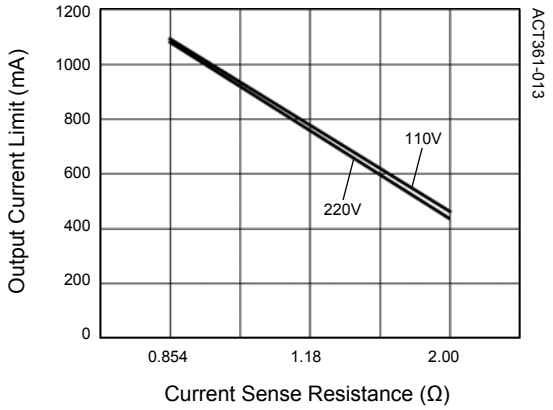
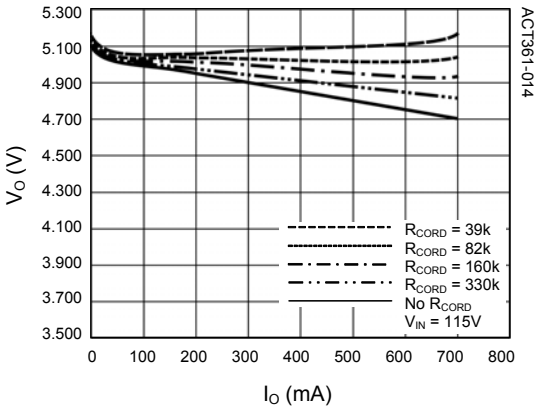
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Circuit of Figure 2, unless otherwise specified.)

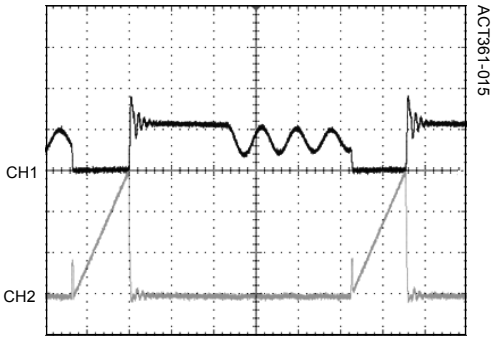
Output Current Limit vs. R_{CS}



Output Cable Resistance Compensation vs. Output Current

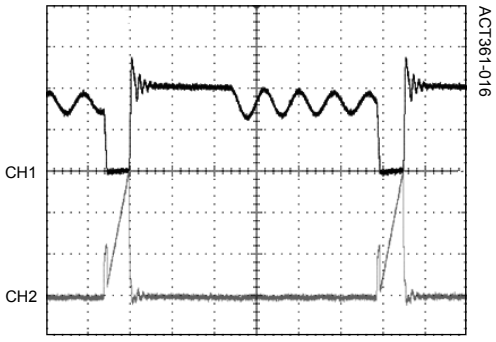


Switching Wareform at 115VAC (Full Load)



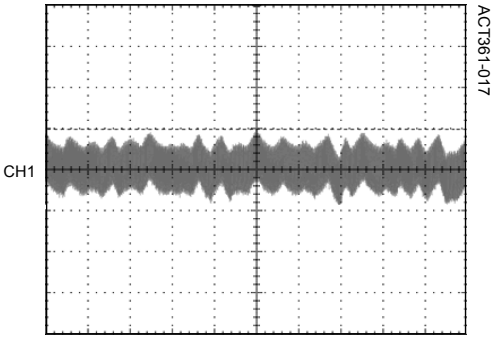
CH1: $V_{COLLECTOR}$, 200V/div
CH2: $I_{COLLECTOR}$, 100mA/div
TIME: 4.00μs/div

Switching Wareform at 230VAC (Full Load)



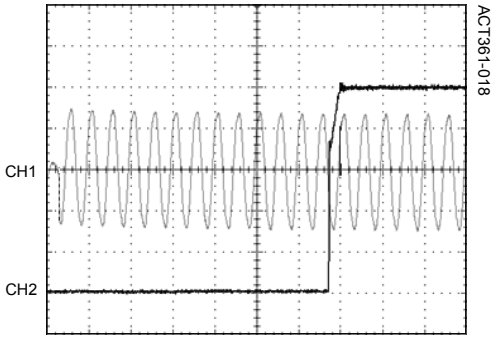
CH1: $V_{COLLECTOR}$, 200V/div
CH2: $I_{COLLECTOR}$, 100mA/div
TIME: 4.00μs/div

Output Voltage Ripple at 115VAC (Full Load)



CH1: 50.0mV/div
TIME: 4.00ms/div

Startup at 115VAC (Full Load)



CH1: $V_{IN(AC)}$, 100V/div
CH2: V_{OUT}, 1V/div
TIME: 40.0ms/div

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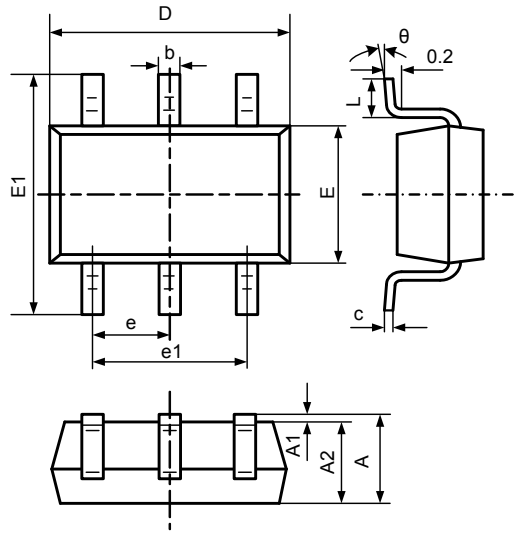
PACKAGE OUTLINE

SOT23-6 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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