

## NCE N-Channel Enhancement Mode Power MOSFET

### DESCRIPTION

The NCE30H21 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### GENERAL FEATURES

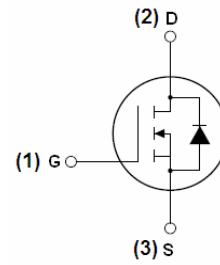
- $V_{DS} = 30V, I_D = 210A$   
 $R_{DS(ON)} < 2.5m\Omega @ V_{GS} = 10V$  (Typ:1m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

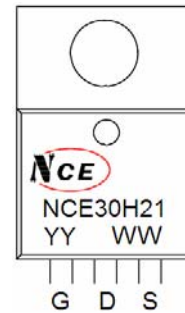
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

**100% UIS TESTED!**

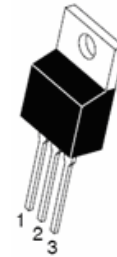
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin Assignment



TO-220 top view

### Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE30H21	NCE30H21	TO-220	-	-	-

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	210	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	100	A
Pulsed Drain Current	$I_{DM}$	1000	A
Maximum Power Dissipation	$P_D$	230	W
Derating factor		1.5	W/°C
Single pulse avalanche energy (Note 5)	$E_{AS}$	1800	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	°C

## Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	0.65	$^{\circ}C/W$
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## Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$		1	2.5	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=24V, I_D=40A$	160			S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$		8200		PF
Output Capacitance	$C_{oss}$			3000		PF
Reverse Transfer Capacitance	$C_{rss}$			280		PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=40A$ $V_{GS}=10V, R_{GEN}=1.8\Omega$		18		nS
Turn-on Rise Time	$t_r$			120		nS
Turn-Off Delay Time	$t_{d(off)}$			50		nS
Turn-Off Fall Time	$t_f$			25		nS
Total Gate Charge	$Q_g$	$V_{DS}=24V, I_D=40A,$ $V_{GS}=10V$		210		nC
Gate-Source Charge	$Q_{gs}$			64		nC
Gate-Drain Charge	$Q_{gd}$			40		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=40A$		0.85	1.2	V
Diode Forward Current (Note 2)	$I_S$				40	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = 40A$ $di/dt = 100A/\mu s(\text{Note3})$		80	120	nS
Reverse Recovery Charge	$Q_{rr}$			180	250	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}C, V_{DD}=15V, V_G=10V, L=1mH, R_g=25\Omega$

## Test circuit

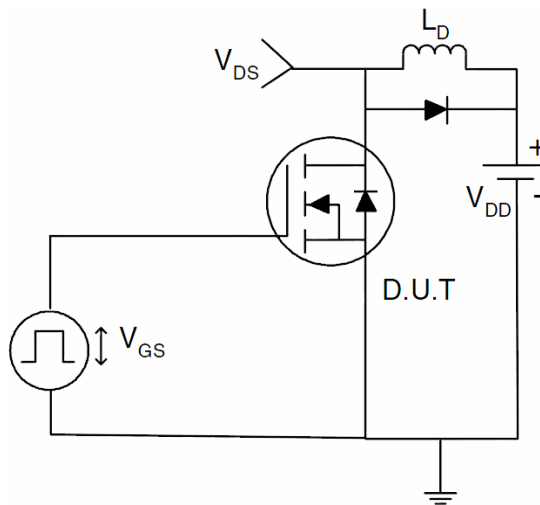
### 1) $E_{AS}$ test Circuits



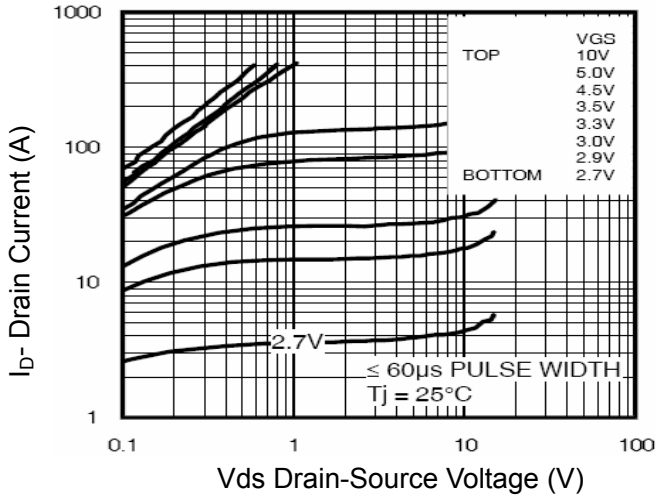
### 2) Gate charge test Circuit:



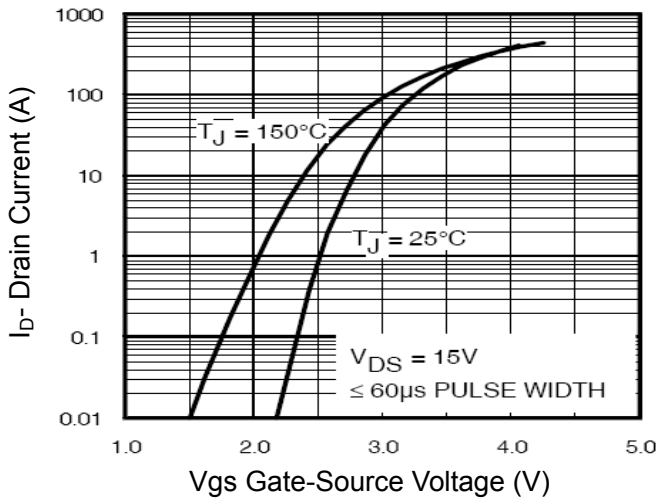
### 3) Switch Time Test Circuit:



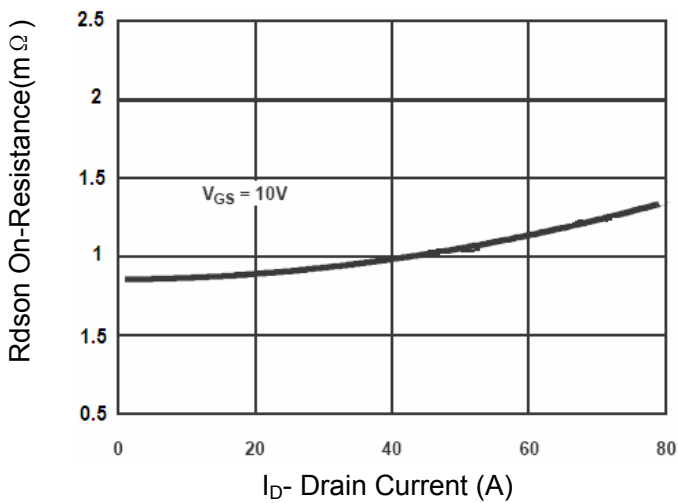
## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)



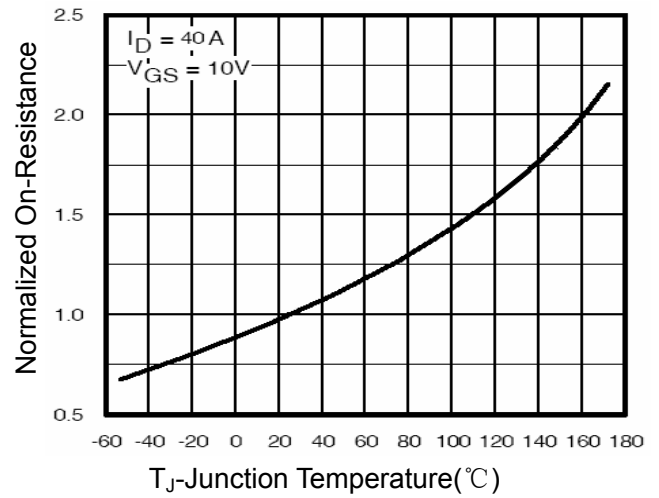
**Figure 1 Output Characteristics**



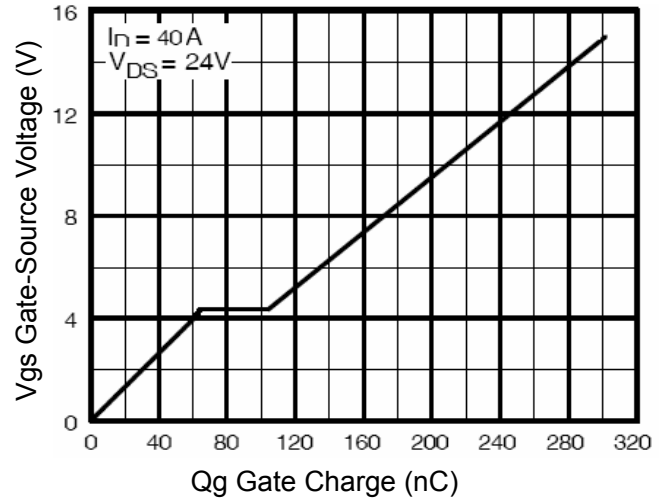
**Figure 2 Transfer Characteristics**



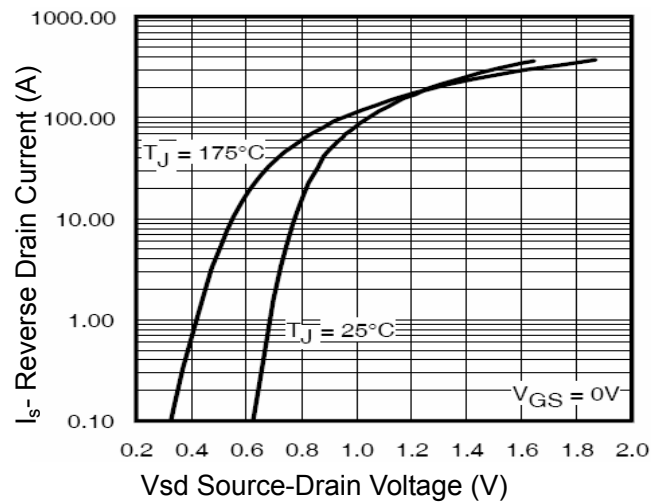
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

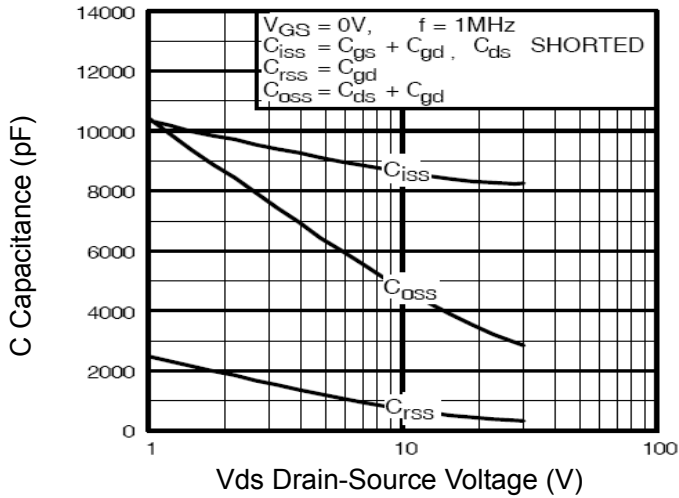


Figure 7 Capacitance vs Vds

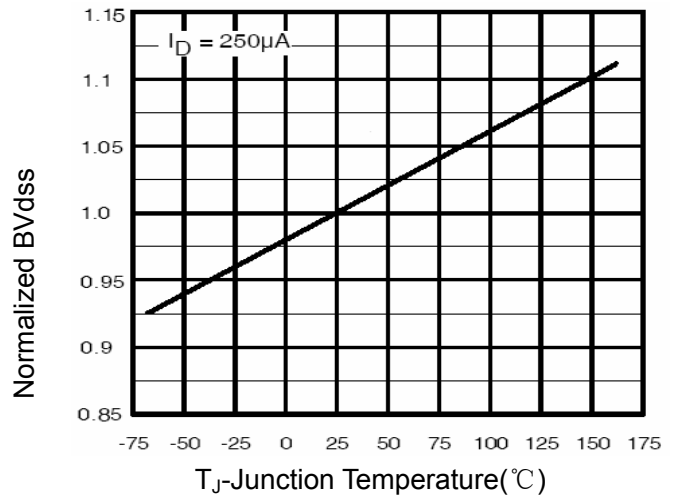


Figure 9  $BV_{DSS}$  vs Junction Temperature

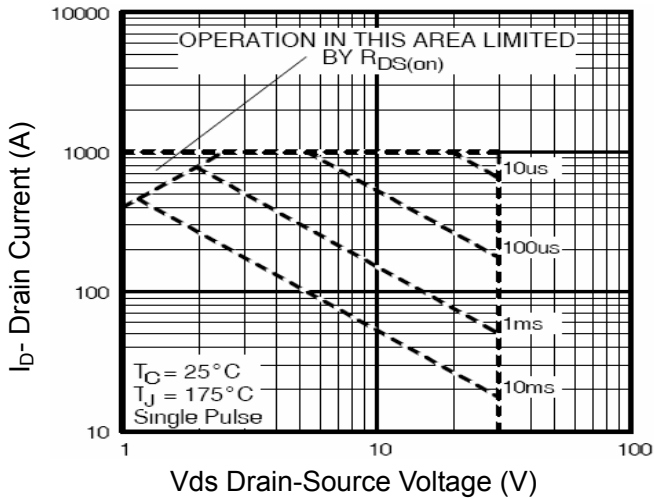


Figure 8 Safe Operation Area

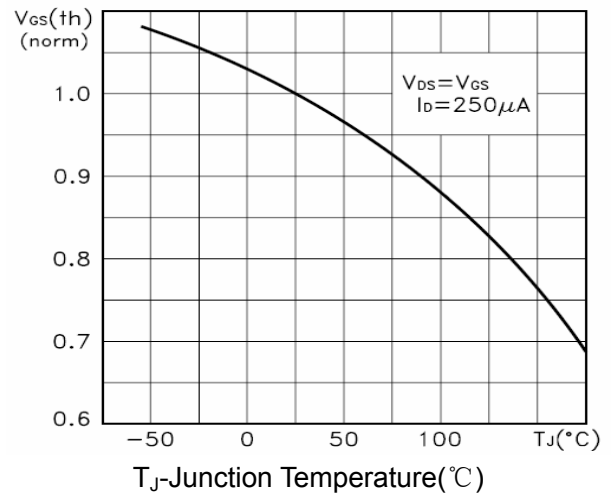


Figure 10  $V_{GS(th)}$  vs Junction Temperature

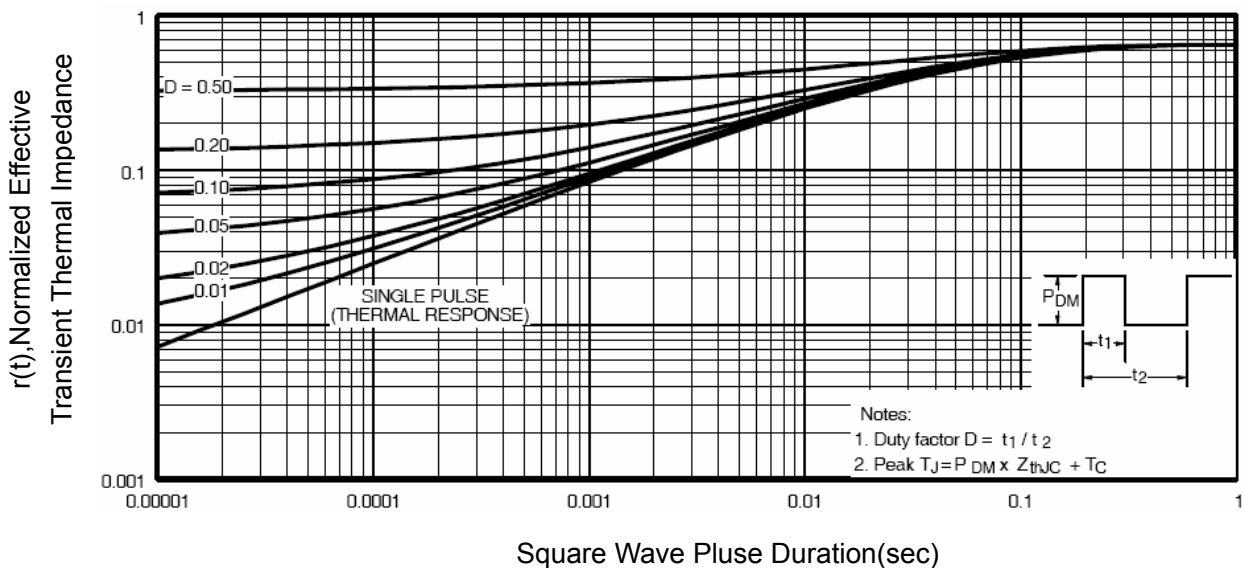
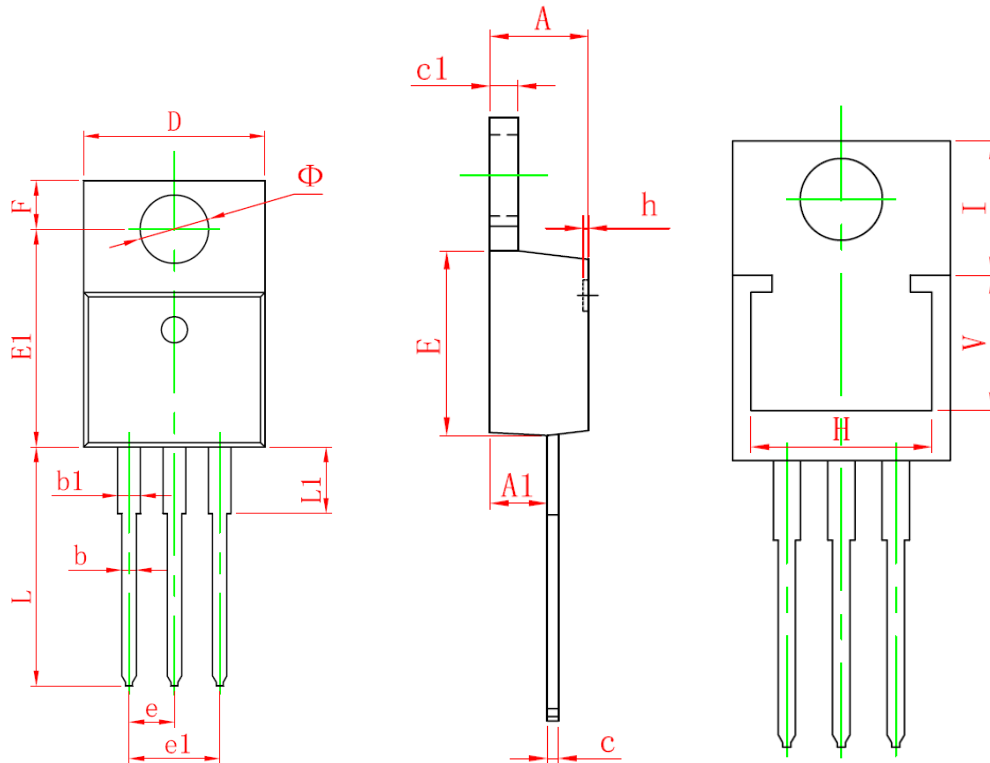


Figure 11 Normalized Maximum Transient Thermal Impedance

## TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	10.010	10.350	0.394	0.407
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 (TYP.)		0.100 (TYP.)	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
H	8.440 REF.		0.332 REF.	
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
V	6.360 REF.		0.250 REF.	
I	6.300 REF.		0.248 REF.	
Φ	3.735	3.935	0.147	0.155

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