

NCE N-Channel Enhancement Mode Power MOSFET

DESCRIPTION

The NCE75H21T uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

GENERAL FEATURES

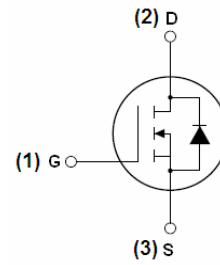
- $V_{DSS} = 75V, I_D = 210A$
 $R_{DS(ON)} < 4m\Omega @ V_{GS} = 10V$
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized Avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Automotive applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin Assignment



TO-247 top view

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE75H21T	NCE75H21T	TO-247	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	75	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	210	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D(100^\circ C)$	150	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	470	W
Derating factor		3.2	W/°C

Single pulse avalanche energy (Note 3)	E_{AS}	2200	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	0.315	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

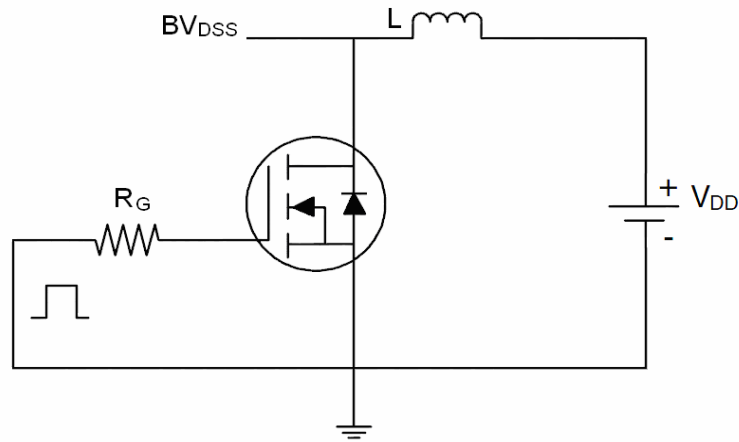
Parameter	Symbol	Condition	Min	Typ	Max	Unit	
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	75	86	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=75V, V_{GS}=0V$	-	-	1	μA	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 200	nA	
On Characteristics							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	25°C	-	2.9	4	m Ω
			125°C	-	4.7	6.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=40A$	100	165	-	S	
Dynamic Characteristics							
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	12100	-	PF	
Output Capacitance	C_{oss}		-	2000	-	PF	
Reverse Transfer Capacitance	C_{rss}		-	480	-	PF	
Switching Characteristics							
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=38V, I_D=40A$ $V_{GS}=10V, R_{GEN}=1.2\Omega$ (Note2)	-	20	-	nS	
Turn-on Rise Time	t_r		-	190	-	nS	
Turn-Off Delay Time	$t_{d(off)}$		-	130	-	nS	
Turn-Off Fall Time	t_f		-	120	-	nS	
Total Gate Charge	Q_g	$V_{DS}=60V, I_D=40A,$ $V_{GS}=10V$ (Note2)	-	410	620	nC	
Gate-Source Charge	Q_{gs}		-	90	140	nC	
Gate-Drain Charge	Q_{gd}		-	140	210	nC	
Drain-Source Diode Characteristics							
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V	
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C, I_F = 40A$ $di/dt = 100A/\mu s$ (Note2)	-	120	210	nS	
Reverse Recovery Charge	Q_{rr}		-	860	1300	nC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)					

Notes:

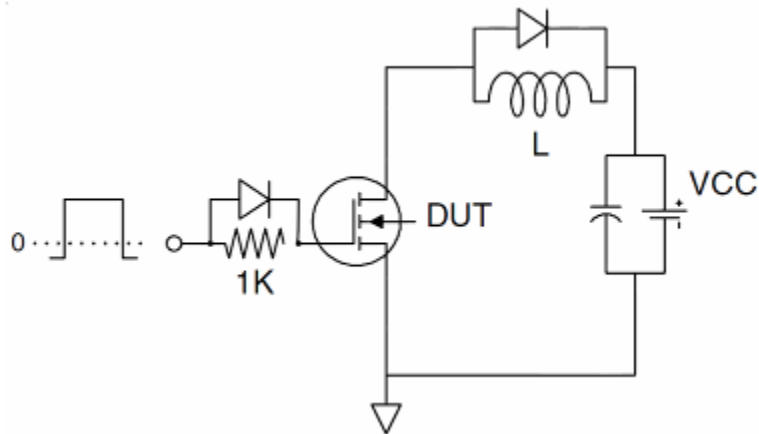
- Surface Mounted on FR4 Board, $t \leq 10$ sec.
- Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
- EAS condition: $T_J=25^\circ C, V_{DD}=37.5V, V_G=10V, L=2mH, R_g=25\Omega, I_{AS}=37A$
- $I_{SD} \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ C$

Test circuit

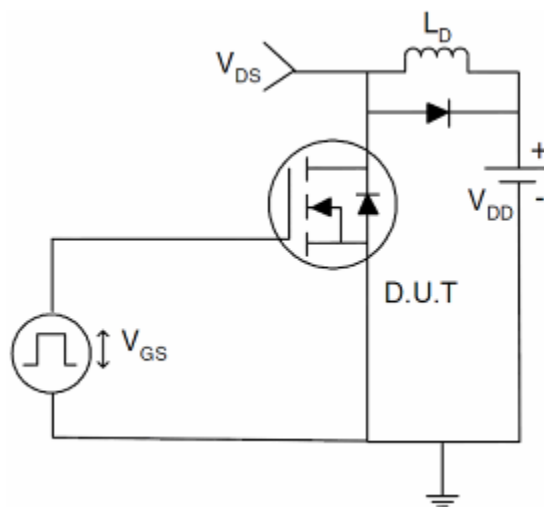
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

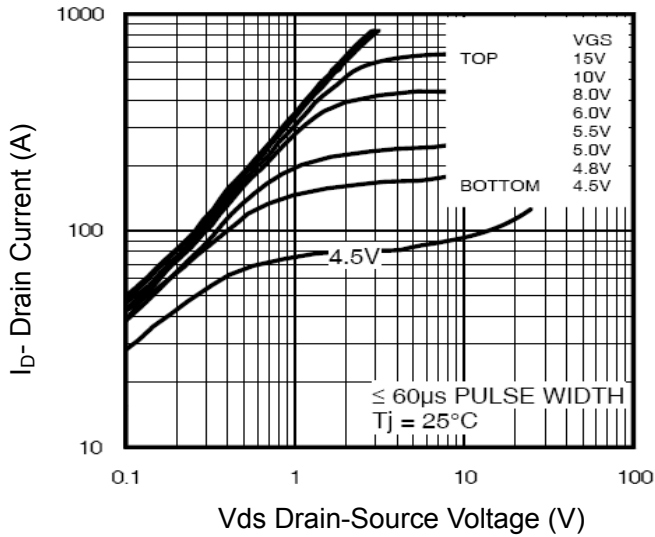


Figure 1 Output Characteristics

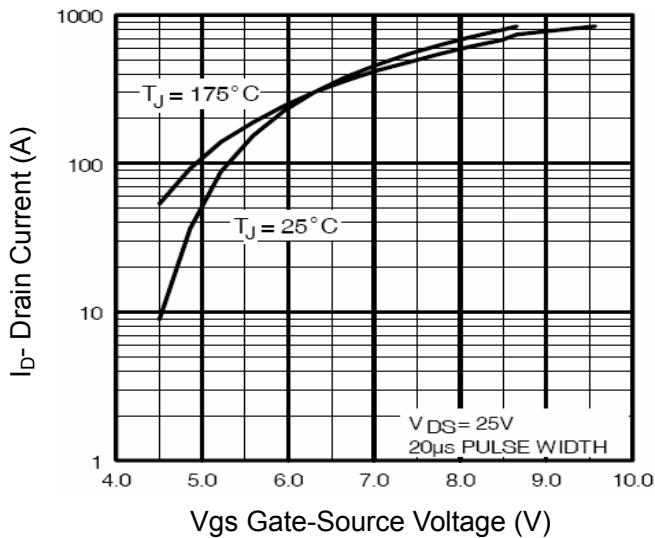


Figure 2 Transfer Characteristics

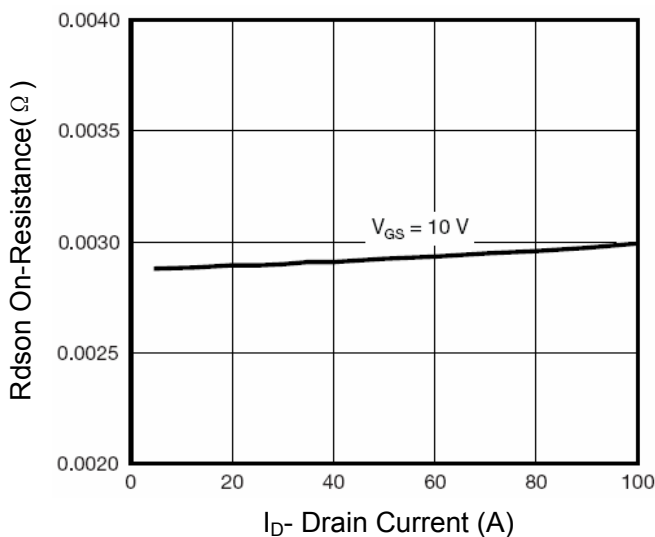


Figure 3 $R_{DS(on)}$ - Drain Current

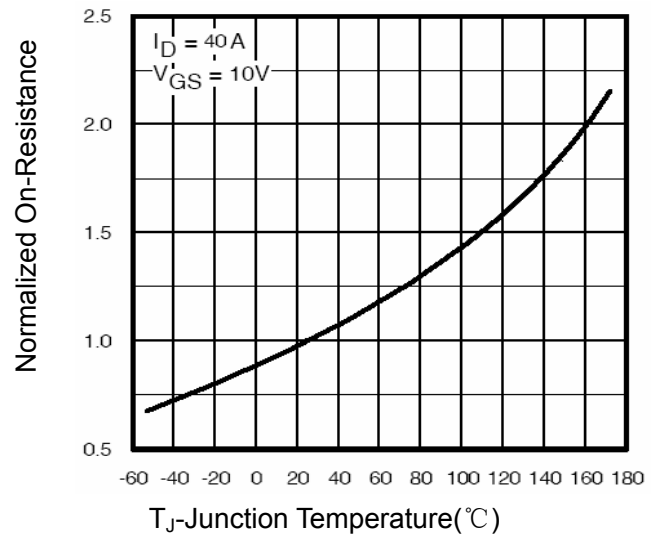


Figure 4 $R_{DS(on)}$ -Junction Temperature

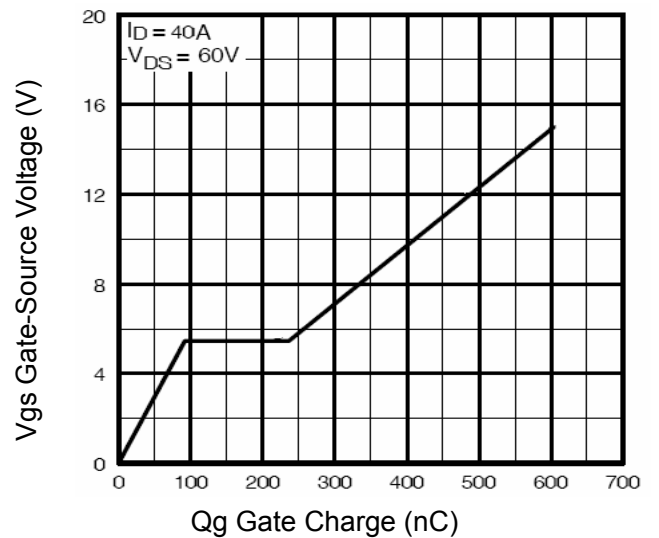


Figure 5 Gate Charge

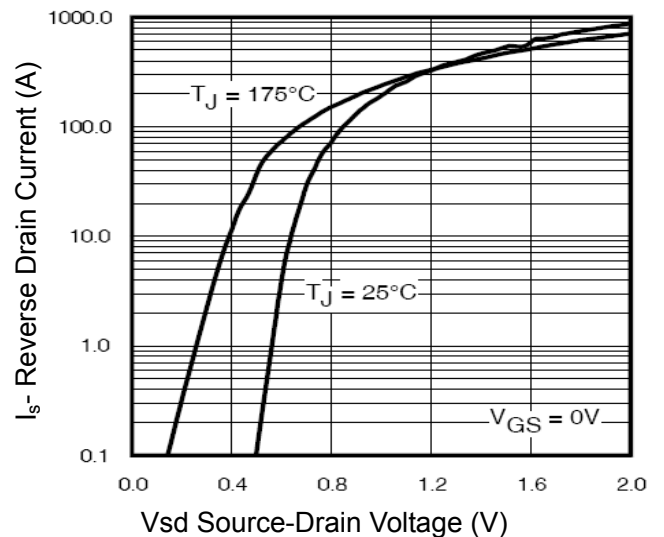


Figure 6 Source- Drain Diode Forward

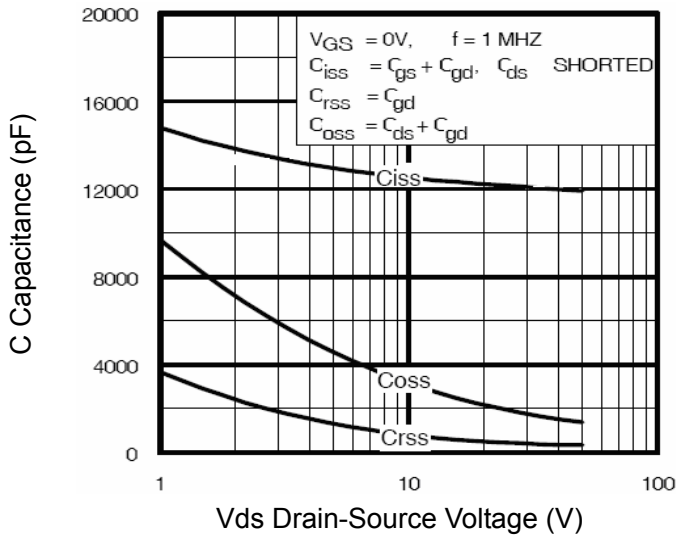


Figure 7 Capacitance vs Vds

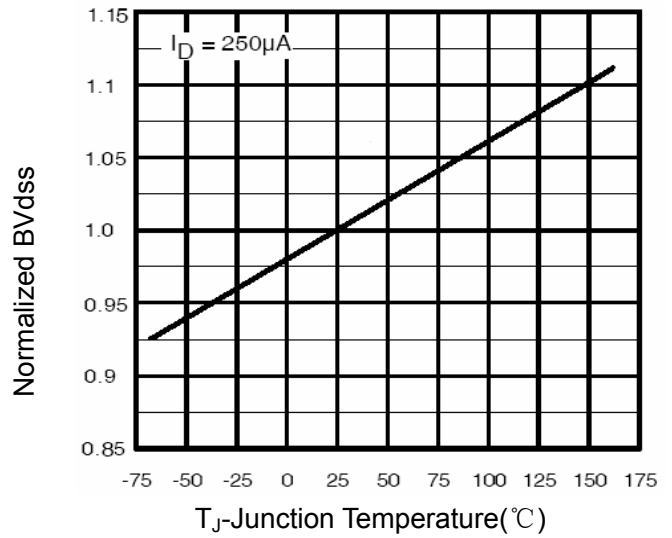


Figure 9 BV_{DSS} vs Junction Temperature

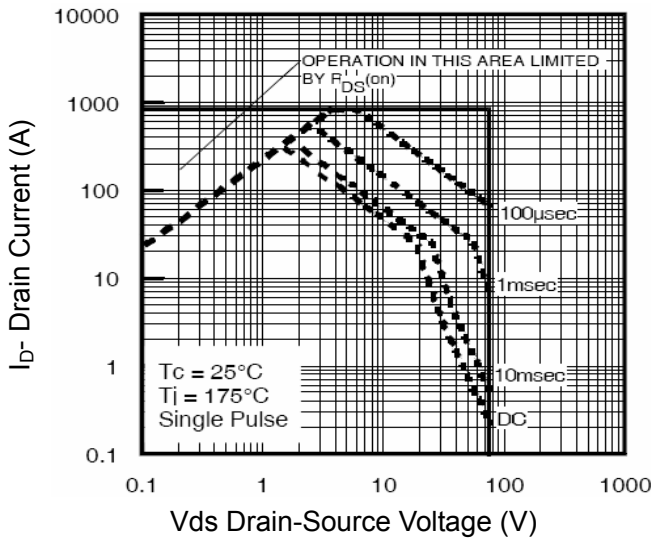


Figure 8 Safe Operation Area

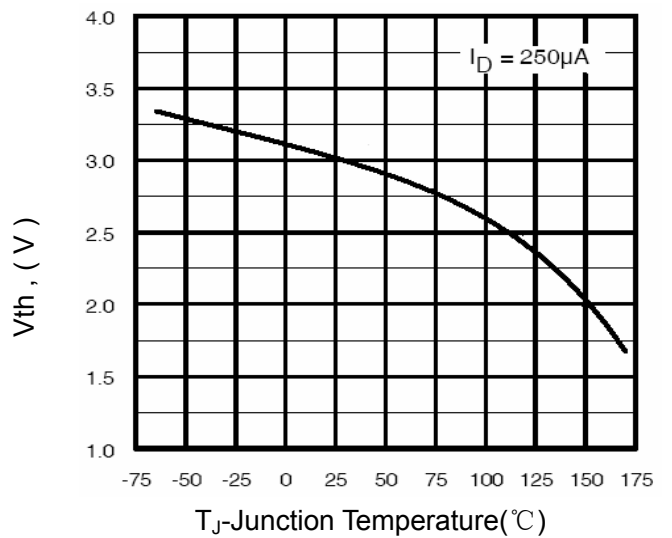


Figure 10 V_{GS(th)} vs Junction Temperature

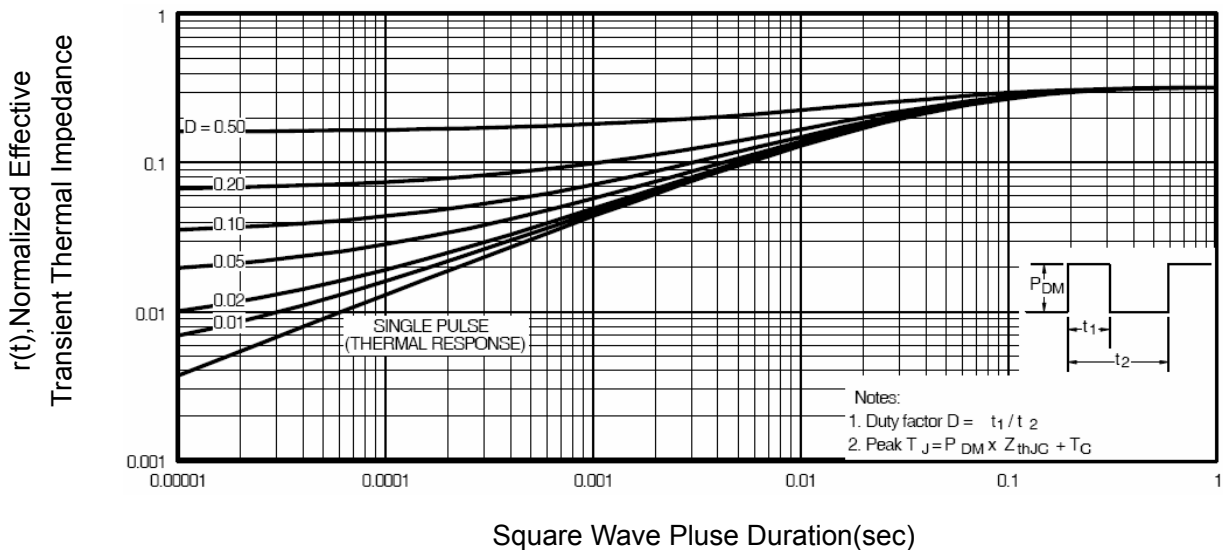
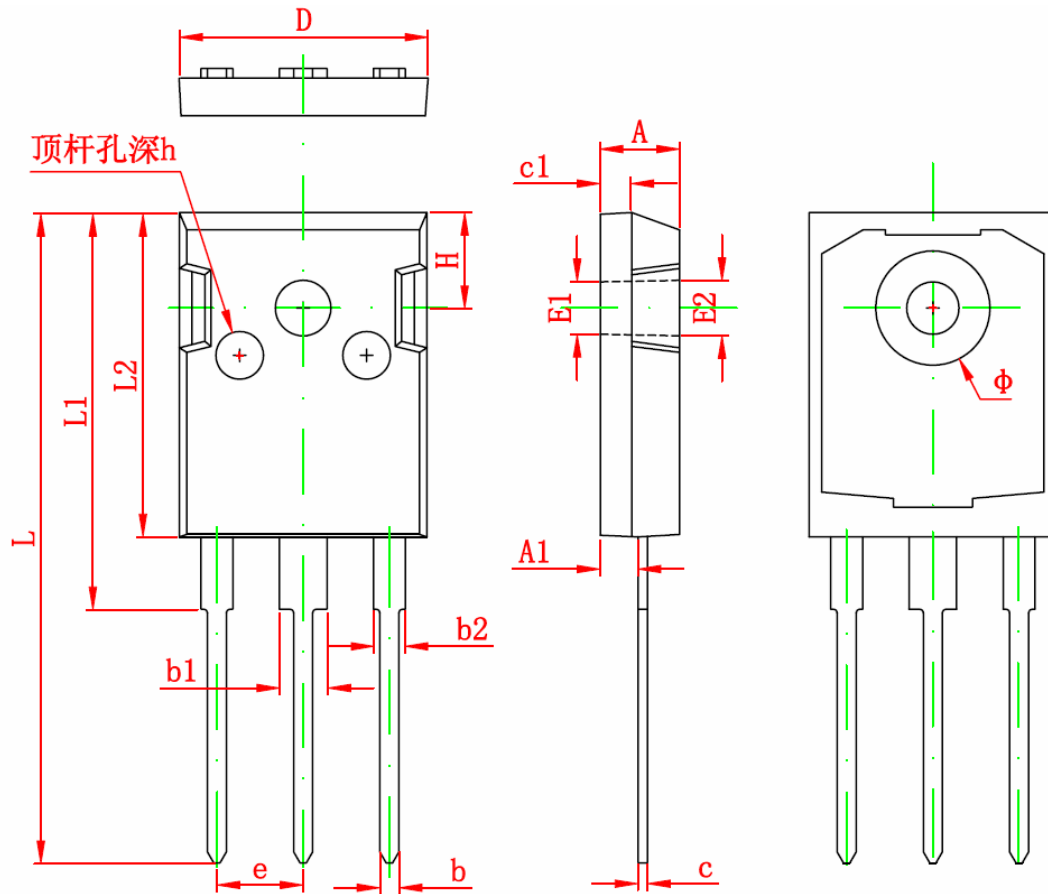


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-247 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500REF		0.138REF	
E2	3.600REF		0.142REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450TYP		0.215TYP	
H	5.980TYP		0.235 REF	
h	0.000	0.300	0.000	0.012

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