

APBADC015 (TEA1750T+TEA1761T, 90W Adaptor)

OVERVIEW

This report describes an universal input, 19.5V, 4.62A single output power supply using TEA1750T and TEA1761T devices from the GreenChip™ family of NXP semiconductor ICs. It contains the specification of the power supply, block diagram, circuit diagram, the component list to build the supply, documentation of the PFC choke and transformer, along with test data and oscillographs of the most important electrical waveforms.

By combining the control and drive for the PFC and the flyback stages into a single device, the TEA1750T provides complete control functionality to comply with the IEC61000-3-2 harmonic current emission requirements, obtain a significant reduction of components, save PCB space and give a cost benefit. It also offers extremely low power consumption in no-load mode so that it is suitable for the low-power consumer markets. The special built-in green functions allow a high efficiency at all power levels that results in a design which can easily satisfy all existing and proposed harmonized energy efficiency standards including CoC (Europe), Energy Star (US), CEC (California), MEPS (Australian & New Zealand), CECP (China)....

The GreenChip SR, TEA1761T, is the only secondary control IC available to integrate both synchronous rectification and primary feedback/control functionality. Used in notebook adapter designs, the GreenChip SR offers a wide operation range of 8.5 to 38V, minimizing the number of external components required and enabling simpler designs. In addition, the high driver output voltage (10V) makes the GreenChip SR compatible with all brands of MOSFETs.

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Summary and Features:

- AC Input Voltage: $90V_{AC}$ to $264V_{AC}$, 47Hz-63Hz
- DC Output: $19.5V_{DC} \pm 2\%$
- Output Current: 4.62A (max.) & 0A (min.)
- Efficiency > 86% at maximum load
- CEC Active-Mode Efficiency > 85%
- No-Load Mode $P_{IN} < 0.5W$
- Dynamic Load Response < +1V/-0.5V
- Ripple & Noise: 200mVp-p (max.)
- EN61000-3-2 A14 (Harmonics) compliance
- SCP, OCP, OTP & FLR

Block Diagram:

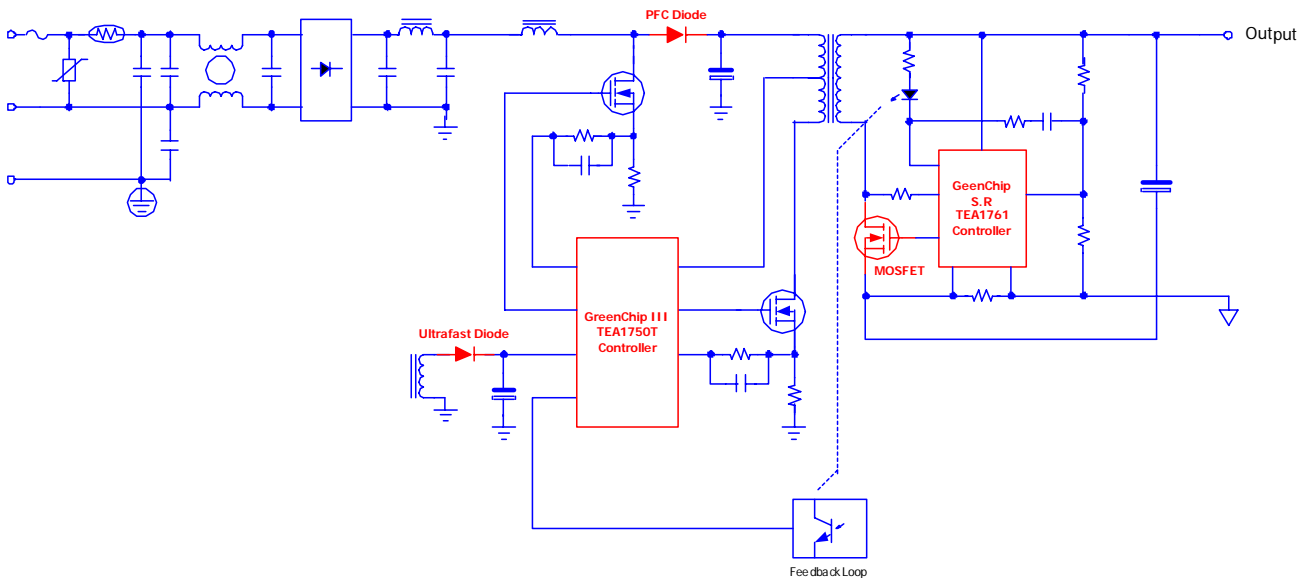


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Test Facility

- Programmable AC Source: Chroma, Model 61503
- Power Hitester: Hioki, Model 3332
- DC Electronic Load: Chroma, Model 63030
- Digital Phosphor Oscilloscope: Tektronix, Model TDS5104B
- Current Probe/Amplifier: Tektronix, Model TCP305/TCPA300
- 100MHz, High Voltage Differential Probe: Tektronix, Model P5205
- 6 ½ Digit Multimeter: Agilent, Model 34401A

Test Conditions

- Unit on the lab-table with the heat sinks on top
- No casing was present on the unit
- Lab temperature between 20°C and 25°C
- Measurements were made with an output cable (2.5 ϕ dc plug, 1-meter length, 16AWG/UL1571)
- Measurements were made after stabilization of temperature according "test method for calculating the efficiency of single-voltage external AC-DC and AC-AC power supplies" of Energy Star

1.0 INPUT CHARACTERIZATION

1.1 PFC Stage Efficiency/Power Factor

Test Condition :

Placing a 100KΩ resistor between the FBctrl and FBaux pin to stop the flyback converter switching, then apply an external power supply (>15V) via a diode on the V_{CC} pin of U1 to resume the PFC converter activated. The unit is set at maximum load & well-heated condition and the input voltage is varied from the minimum to the maximum value. Efficiency is computed and power factor is measured.

Note: The output voltage is measured at the bulk capacitor, C3, terminals on PCB.

Input Voltage (V _{AC} /Hz)	V _{BULK} (V _{DC})	P _{OUT} (W)	P _{IN} (W)	Efficiency (%)	Power Factor
90/60	383	100.73	106.41	94.66	0.992
115/60	383	100.73	104.53	96.36	0.975
132/60	383	100.73	103.94	96.91	0.968
180/50	383	100.73	103.00	97.80	0.944
230/50	383	100.73	102.50	98.27	0.912
264/50	383	100.73	102.27	98.49	0.892

1.2 PFC+Flyback Efficiency/Power Factor

Test Condition :

The unit is set at maximum load & well-heated condition and the input voltage is varied from the minimum to the maximum value. Efficiency is computed and power factor is measured.

Note: The output voltage is measured at the end of the output cable.

Criteria: The efficiency must be > 86% under maximum load operation.

Test Result:

Input Voltage (V _{AC} /Hz)	I _{IN_rms} (A)	P _{IN} (W)	P _{OUT} (W)	Efficiency (%)	Power Factor
90/60	1.136	101.30	88.46	87.32	0.992
115/60	0.888	99.50	88.45	88.89	0.974
132/60	0.778	98.98	88.45	89.36	0.964
180/50	0.580	98.10	88.45	90.16	0.938
230/50	0.467	97.72	88.45	90.51	0.910
264/50	0.425	97.58	88.45	90.64	0.868

1.3 Active & No-Load Mode CEC Measurements

In the state of California, after January 1, 2008, all single-output EPS adaptors – including those sold with the products they power – must meet the California Energy Commission (CEC) requirement for minimum active-mode efficiency and no-load input power consumption. Minimum active-mode efficiency is defined as the average efficiency at 25%, 50%, 75% and 100% of rated load output power printed on the nameplate of the supply:

Standards for Power Supplies Effective January 1, 2008

Nameplate Output Power (Po)	Minimum Average Efficiency in Active Mode
< 1W	0.5 * Nameplate Output
≥ 1 and ≤ 49W	0.09 * Ln(Nameplate Output) + 0.5
> 49W	0.85
	Maximum Energy Consumption in No-Load Mode
Any Output	0.5Watts

Where Ln (Nameplate Output) = Natural Logarithm of the nameplate output expressed in Watts.

Active-Mode Efficiency

Test Condition :

For adaptors that are single input voltage only, the measurements are to be made at the nominal rated input voltage (115V_{AC} or 230V_{AC}). For universal input adaptors, the measurements are to be made at both nominal input voltages (115V_{AC} and 230V_{AC}).

Criteria: To comply with the standard, the average of the four efficiency measurements must be greater than or equal to the efficiency specified by the standard.

115V_{AC}/60Hz

Percent of Full Load, I _{OUT}	V _{OUT} (V)	P _{OUT} (W)	P _{IN} (W)_Total	Eff_Total (%)	PF	P _{LOSS} (W)
100%, 4.620A	19.145	88.45	99.40	88.98	0.974	10.95
75%, 3.466A	19.216	66.60	74.62	89.25	0.963	8.02
50%, 2.313A	19.286	44.61	50.53	88.28	0.967	5.92
25%, 1.156A	19.343	22.36	27.37	81.70	0.937	5.01

Avg.

87.05

230V_{AC}/50Hz

Percent of Full Load, I _{OUT}	V _{OUT} (V)	P _{OUT} (W)	P _{IN} (W)_Total	Eff_Total (%)	PF	P _{LOSS} (W)
100%, 4.620A	19.143	88.44	97.70	90.52	0.910	8.03
75%, 3.466A	19.218	66.61	73.56	90.55	0.884	6.26
50%, 2.313A	19.286	44.61	49.93	89.35	0.861	5.00
25%, 1.156A	19.343	22.36	27.11	82.48	0.760	4.65

Avg. 88.23

From these results it is apparent that the efficiency of this design easily exceeds the required 85%. More states within the USA, and many other countries around the world are adopting similar energy efficiency standards (based on the original Energy Star standard). For the latest, up-to-date information on energy efficiency regulations, please visit the CEC or Energy Star Program website at: <http://www.energy.ca.gov/> or <http://www.energystar.gov/>

No-Load Mode

Test Condition :

The unit is set at no load mode and the input voltage is varied from the minimum to the maximum value.

Criteria: The input power shall be less than 0.5W at both 115V_{AC}/60Hz and 230V_{AC}/50Hz.

Test Result:

Input Voltage (V _{AC} /Hz)	90/60*	115/60*	132/60*	180/50*	230/50	264/50
Pin (W)	0.18	0.24	0.24	0.24	0.268	0.288

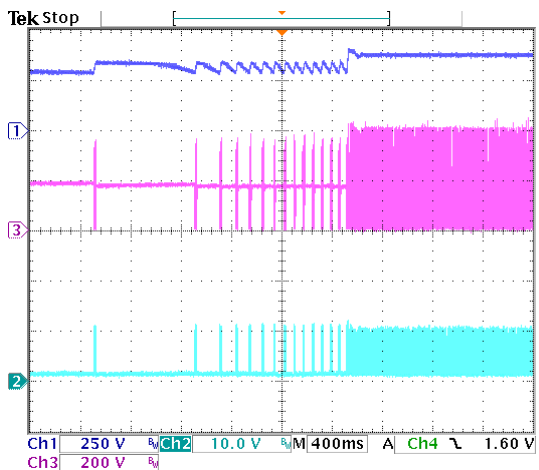
*: The power meter is set at the integration mode for the duration of 60 seconds.

1.4 PFC Burst Mode and Normal Operations

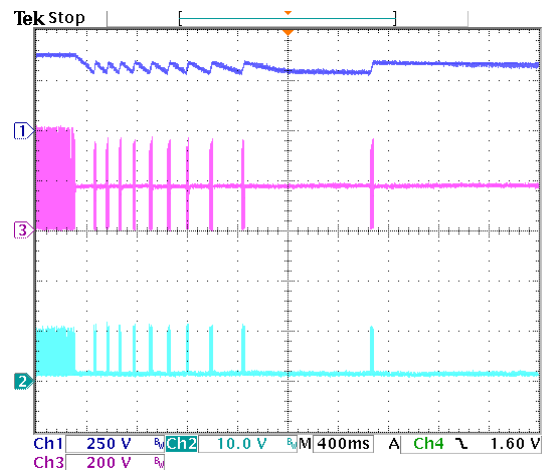
Test Condition :

When the output power of the flyback converter is low, the flyback converter switches over to VCO mode. When VCO mode is entered by the flyback controller, the power factor correction circuit switches to burst mode control. In burst mode control, switching of the power factor correction circuit is inhibited until the voltage on the VoSense pin has dropped to Vburst,low.

AC Mains	Output Current Rating	
	Burst Mode ⇒ Normal Operation	Normal Operation ⇒ Burst Mode
90V/60Hz	0.935A	0.6A
115V/60Hz	0.935A	0.635A
132V/60Hz	0.98A	0.545A
180V/50Hz	0.92A	0.575A
230V/50Hz	1.25A	0.545A
264V/50Hz	1.342A	0.528A

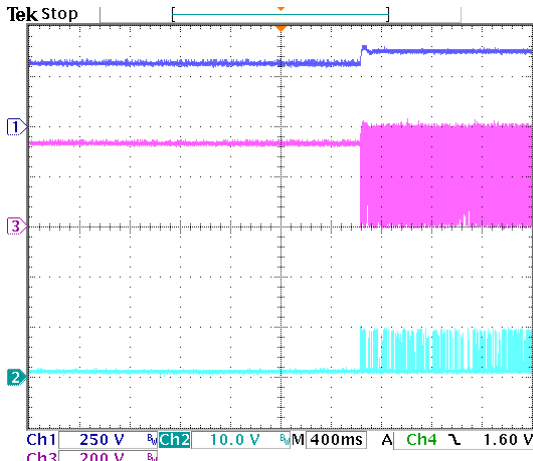


115V_{AC}/60Hz, Burst Mode to Normal Operation¹

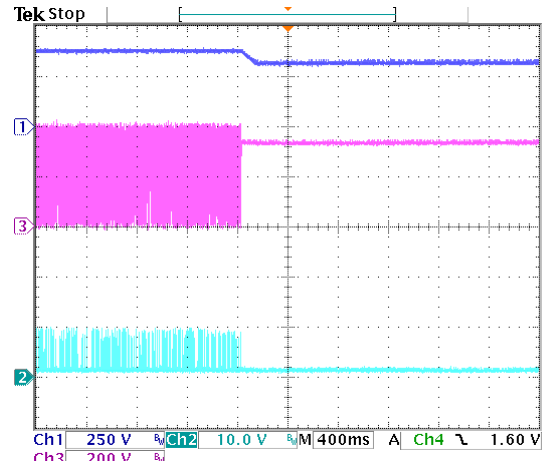


115V_{AC}/60Hz, Normal Operation to Burst Mode¹

CH1: V_{BULK} CH2: V_{GS}/Q1 CH3: V_{DS}/Q1

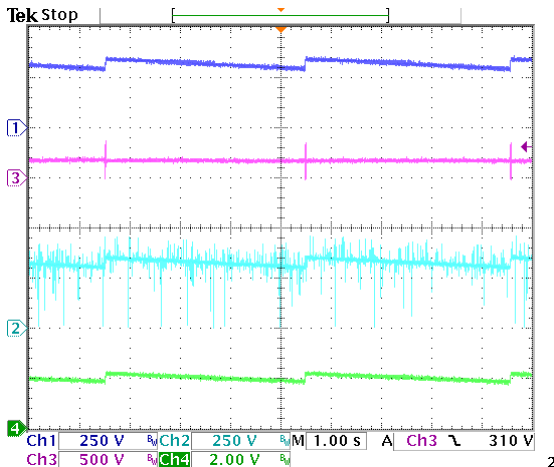


230V_{AC}/50Hz, Burst Mode to Normal Operation ^{Note}

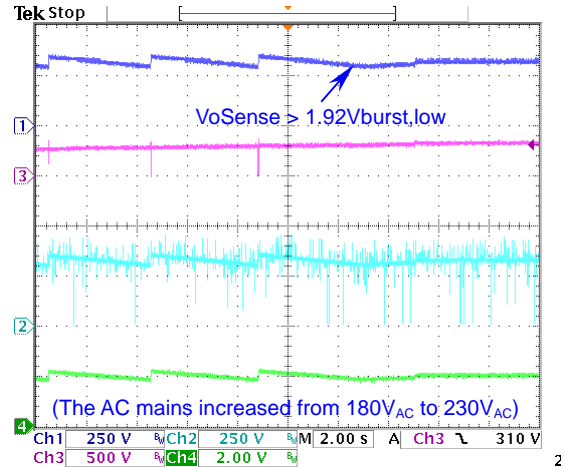


230V_{AC}/50Hz, Normal Operation to Burst Mode ^{Note}

CH1: V_{BULK} CH2: V_{GS/Q1} CH3: V_{DS/Q1}



Burst mode at 115V_{AC}/60Hz, No Load ^{Note}



Burst mode at 210V_{AC} to stop, No Load ^{Note}

CH1: V_{Bulk} CH2: V_{DS_Q2} CH3: V_{DS_Q1} CH4: V_{O_sense}

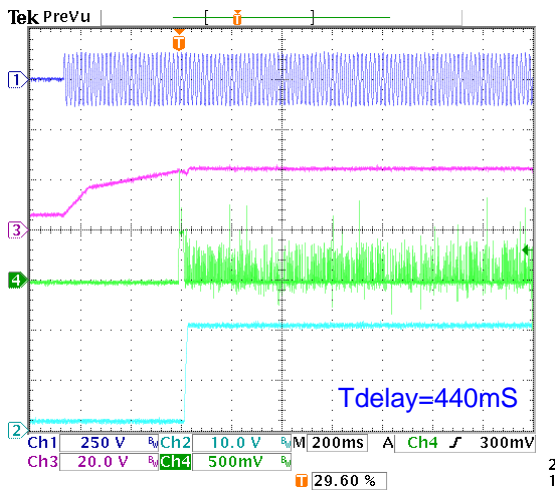
Note: It's stopped of the burst mode at approx. line voltage of 210V_{AC}, this is because of the bulk capacitor voltage, $V_{C3} = 210V_{AC} \times \sqrt{2} = 297V_{DC}$, presented on the VoSense pin $[(297V_{DC} \times R7)/R5+R6+R7]$ to be larger than the level of Vburst,low (1.92V) that will result in the burst mode stopping.

1.5 Timing

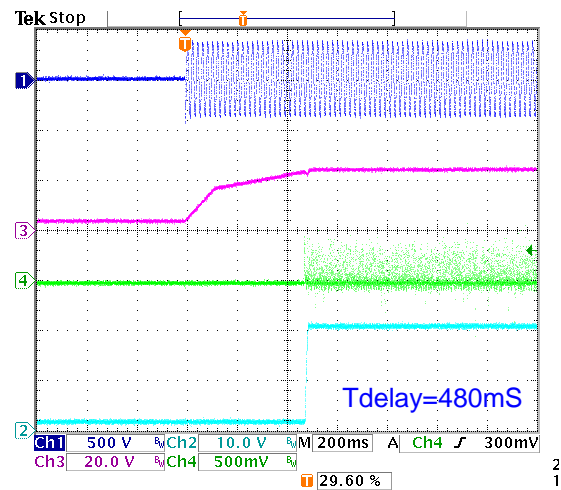
The following timings are measured:

1. Delay after AC applied: 2 second maximum after the AC is externally applied to the time when the output is within the regulation limit.
2. Soft-start interval.
3. Output rise time: The output voltage shall rise from 10% of nominal to the regulation limit within 30mS.

Criteria: There must be a smooth and continuous ramp of output voltage and no voltage of opposite polarity shall be present on output during start-up.

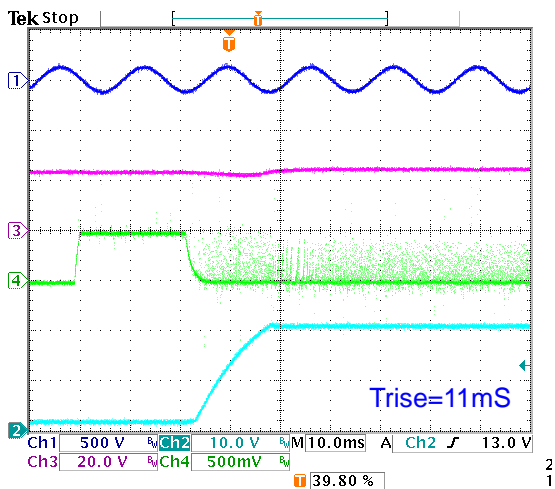


Delay Time, 90V_{AC}/60Hz, Full Load

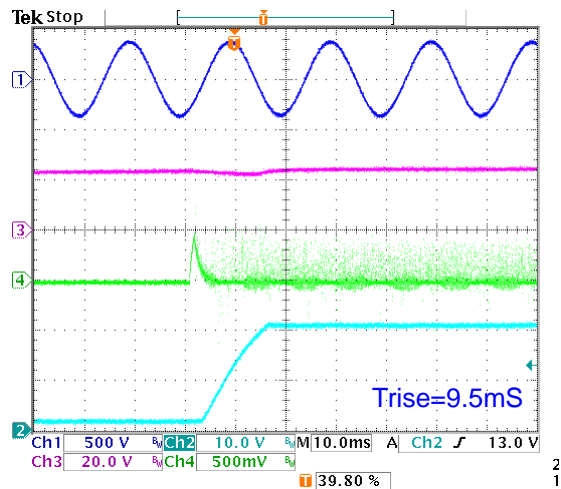


Delay Time, 264V_{AC}/50Hz, Full Load

CH1: AC Mains CH2: V_{OUT} CH3: V_{CC} CH4: V_{FB_sense}



Rise Time, 90V_{AC}/60Hz, Full Load



Rise Time, 264V_{AC}/50Hz, Full Load

CH1: AC Mains CH2: V_{OUT} CH3: V_{CC} CH4: V_{FB_sense}

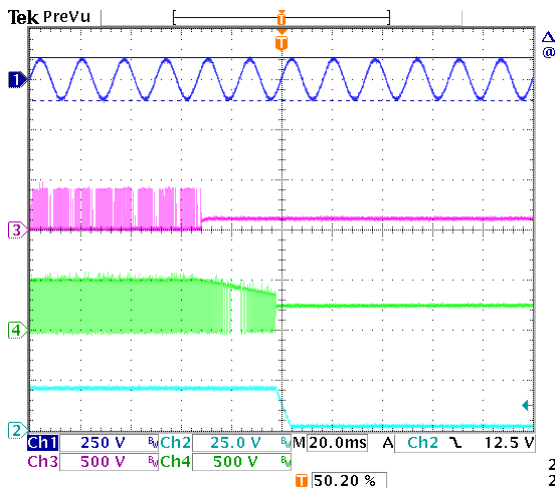
1.6 Brownout/Brownout Recovery

The voltage on the VinSense pin is sensed continuously to prevent the PFC to operate at very low mains input voltages.

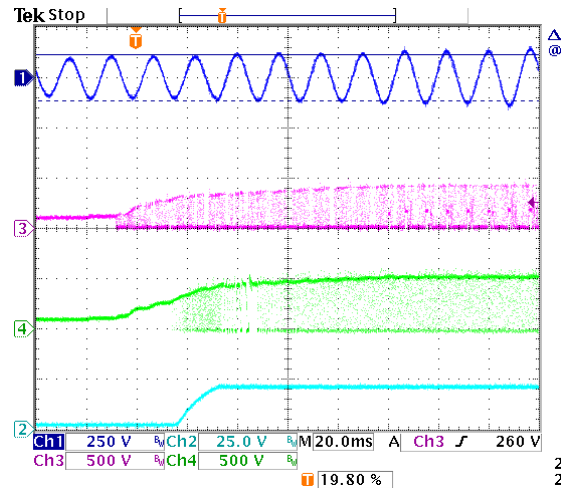
Test Condition :

The input voltage decreased from 90V_{AC} down to zero, and then recovers back to 90V_{AC}. The output is fully loaded.

Criteria: The unit shall survive over specified operating temperature test limits. The unit shall power up by the time the input AC line voltage reach 85V_{AC}(max.).



AC Mains from 90V_{AC} to 0V, Full Load



AC Mains from 0V to 90V_{AC}, Full Load

CH1: AC Mains CH2: V_{OUT} CH3: V_{DS_Q1} CH4: V_{DS_Q2}

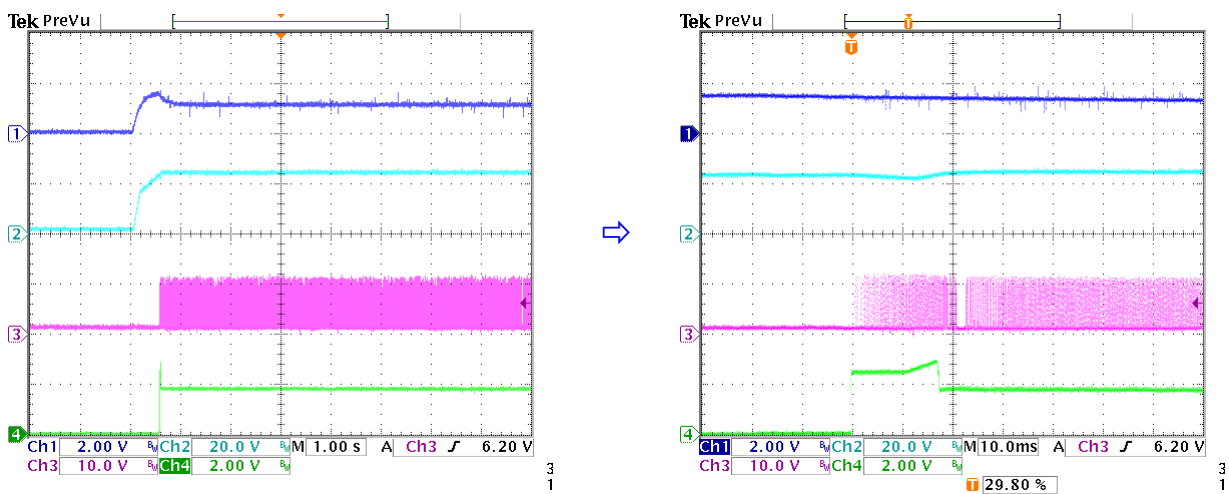
Note:

The input voltage was measured at approx. of 77V_{AC} for both brownout & brownout recovery operations. The output voltage shall stay within the specified regulation limits or switch-off. No output bounce or hiccup is allowed during switch-on or switch-off.

1.7 Time-Out Feature

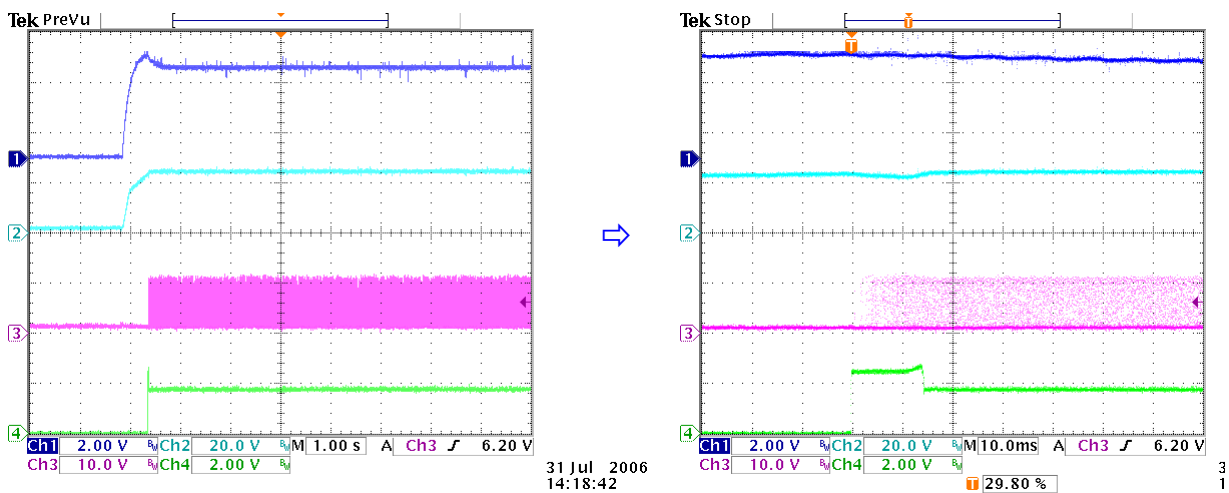
When the voltage on FBctrl pin rises above 4.5V (typ.), a fault is assumed and switching is inhibited. When a small capacitor is connected to this pin, a time-out function can be realized to protect for an open control loop situation. The time-out function can be disabled by placing a resistor (100KΩ) to ground on the FBctrl pin. If the pin is shorted to ground, switching of the flyback controller is inhibited.

90V_{AC}/60Hz, Normal Start-Up, Full Load



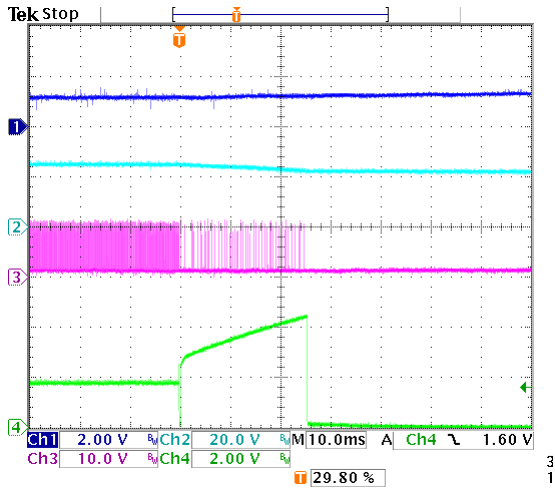
CH1: VinSense CH2: V_{CC} CH3: FB_driver CH4: FBctrl

264V_{AC}/50Hz, Normal Start-Up, Full Load

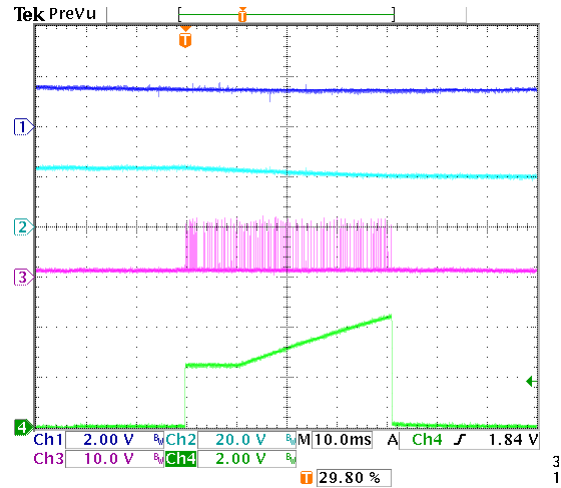


CH1: VinSense CH2: V_{CC} CH3: FB_driver CH4: FBctrl

90V_{AC}/60Hz, Abnormal Operations, Full Load



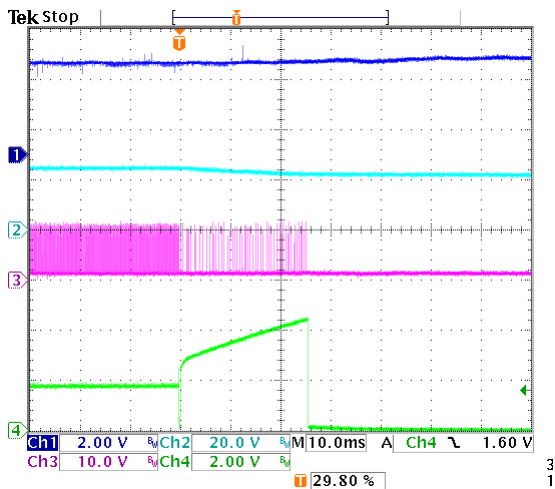
Power-up then output short-circuit



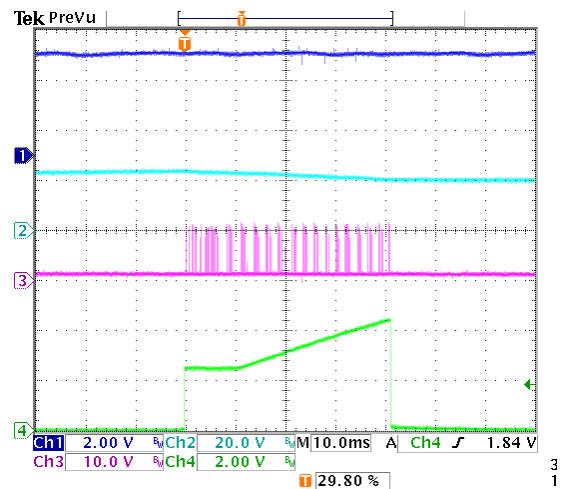
Output short-circuit then power-up

CH1: VinSense CH2: V_{CC} CH3: FB_driver CH4: FBctrl

264V_{AC}/50Hz, Abnormal Operations, Full Load



Power-up then output short-circuit



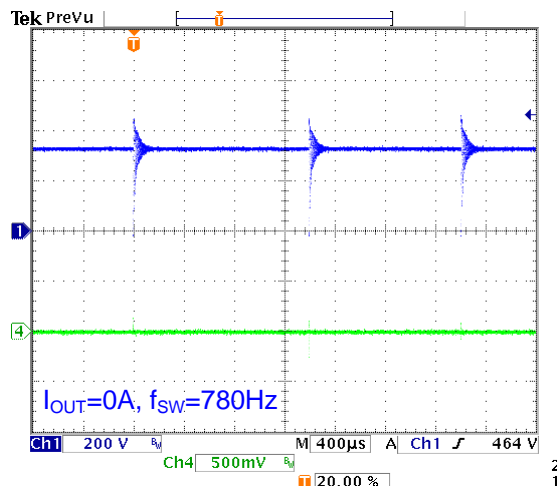
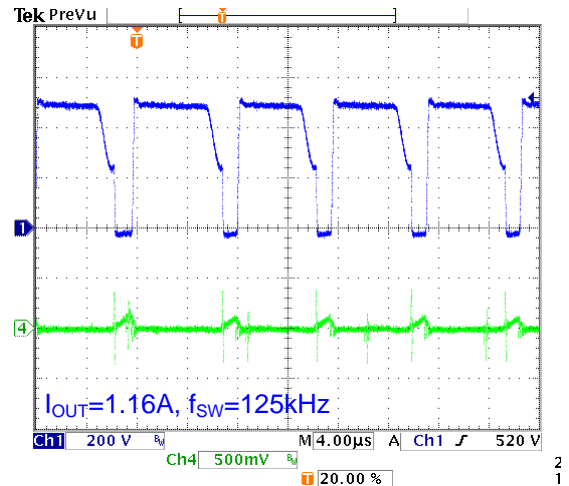
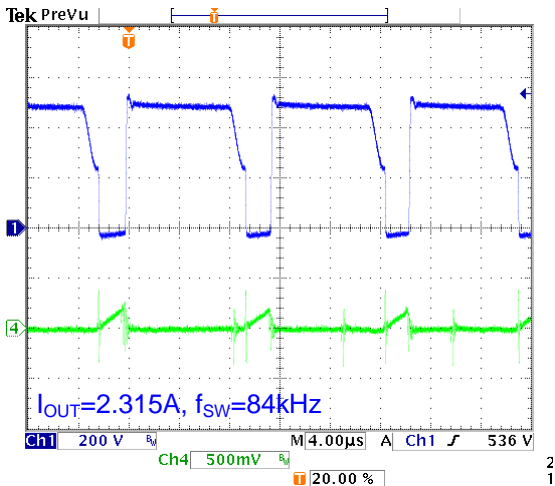
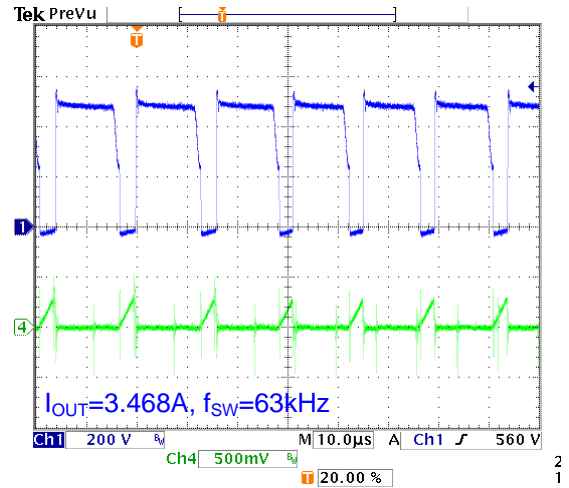
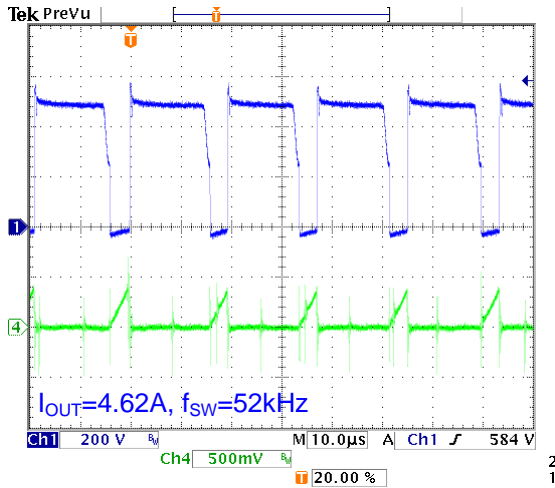
Output short-circuit then power-up

CH1: VinSense CH2: V_{CC} CH3: FB_driver CH4: FBctrl

1.8 Normal Mode Operation

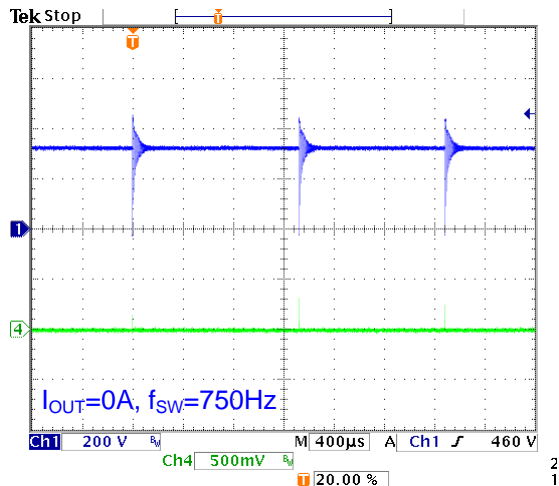
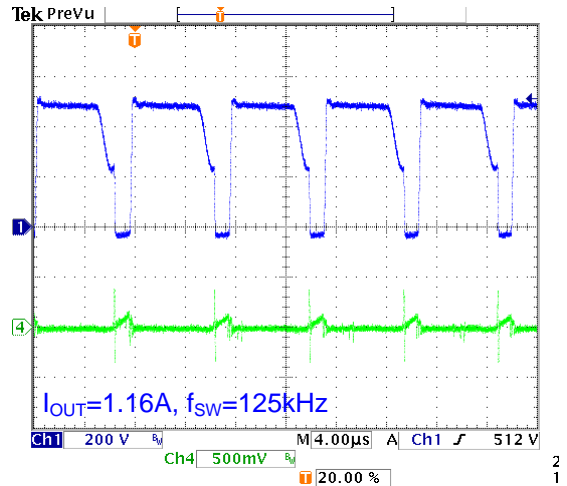
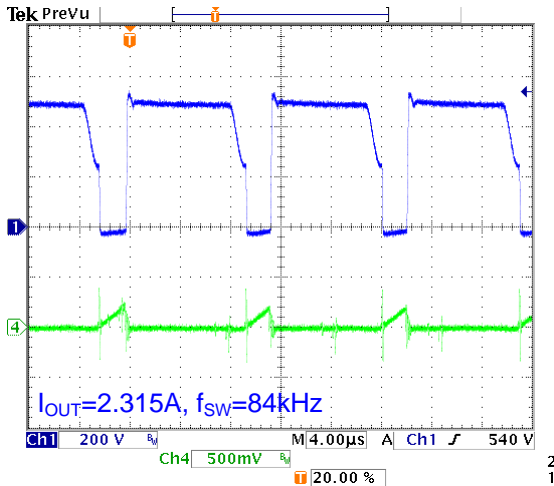
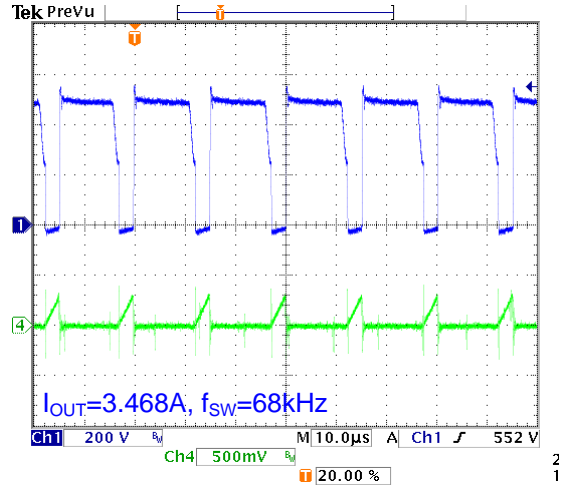
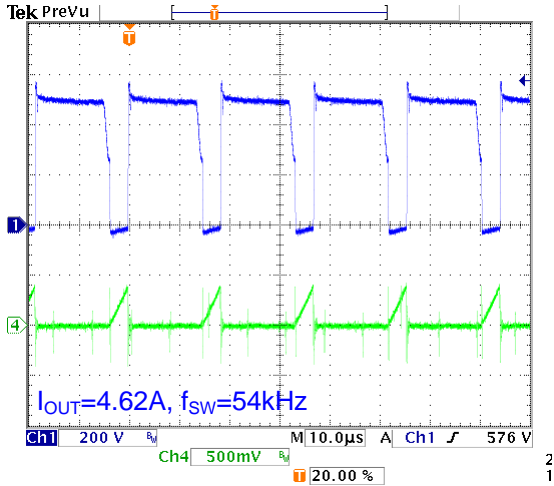
By observing the switching waveform (V_{DS} of Q2) to verify the unit can be operated in multi modes along with 25%, 50%, 75% and 100% load conditions respectively. Test is repeated from different input voltages.

- 115V_{AC}/60Hz -



CH1: $V_{DS}/Q2$ CH2: $V_{FBsense}$

- 230V_{AC}/50Hz -



CH1: V_{DS}/Q2 CH2: V_{FBsense}

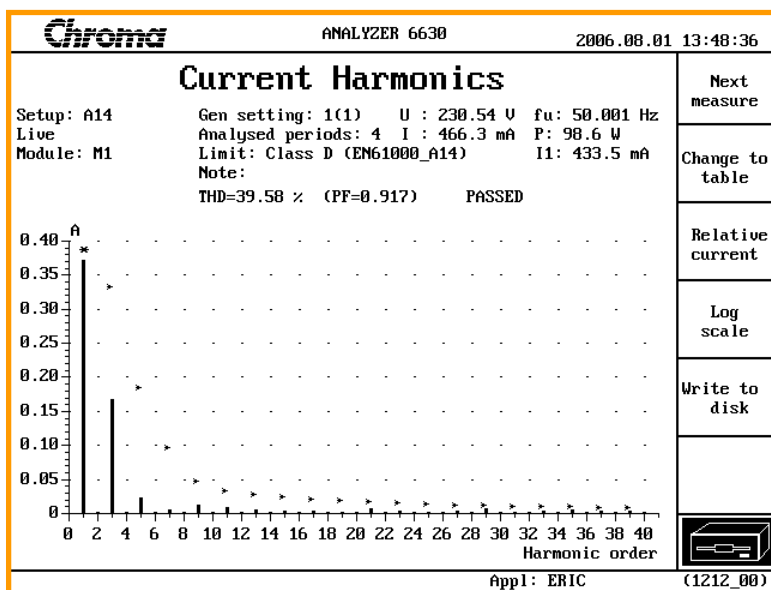
1.9 Harmonics per EN61000-3-2 A14

The purpose of this measurement is to know if the unit goes to comply with the harmonics per EN61000-3-2 A14 requirements.

Test Condition :

The unit is set at maximum load and the input voltage is applied to 230V_{AC}/50Hz.

Test Result : PASSED



Chroma ANALYZER 6630 2006.08.01 13:53:33

Current Harmonics

Setup: A14 Gen setting: 1(1) U : 230.54 V fu: 50.001 Hz
 Live Analysed periods: 4 I : 466.3 mA P: 98.6 W
 Module: M1 Limit: Class D (EN61000_A14) I1: 433.5 mA
 Note:
 THD=39.58 % (PF=0.917) PASSED

No	mA	Lim mA	No	mA	Lim mA	No	mA	Lim mA
1	433.5		15	4.4	25.2	29	7.2	13.1
2	0.4		16	0.1		30	0.1	
3	168.1	334.3	17	3.9	22.3	31	1.1	12.2
4	0.1		18	0.0		32	0.1	
5	23.3	186.8	19	2.0	19.9	33	4.0	11.5
6	0.1		20	0.1		34	0.1	
7	7.0	98.3	21	7.2	18.0	35	5.4	10.8
8	0.1		22	0.1		36	0.1	
9	13.3	49.2	23	4.2	16.5	37	4.1	10.2
10	0.1		24	0.2		38	0.2	
11	9.2	34.4	25	3.0	15.1	39	4.0	9.7
12	0.1		26	0.1		40	0.1	
13	7.0	29.1	27	5.2	14.0			
14	0.2		28	0.0				

Current range: 1 Ap

Next measure
 Change to bar graph
 Relative current
 Write to disk

Appl: ERIC (1212_01)

2.0 OUTPUT CHARACTERIZATION

2.1 Load/Line Regulation

Test Condition :

While the load on output is increased from the minimum to the maximum given values, the output voltage deviation is plotted. Test is repeated from different input voltages.

Note: The output voltage is measured at the end of the output cable.

Criteria:

The output shall remain within the specified limits over its minimum to maximum load range.

Test Result:

Line Regulation

- a). Line Regulation = $(V_{MAX.} - V_{MIN.}) / V_{NORMINAL} * 100\%$, where $V_{NORMINAL} = 19.5V$
- b). Line regulation shall less than 0.05%
- c). $I_{OUT} = 4.62A$

Input Voltage (V _{AC} /Hz)	90/60	115/60	132/60	180/50	230/50	264/50
V _{OUT}	19.149V	19.149V	19.148V	19.148V	19.148V	19.147V
Line Regulation	$(19.149V - 19.147V) / 19.5V * 100\% = 0.01\%$					

Load Regulation

- a). Load Regulation = $(V_{MAX.} - V_{MIN.}) / V_{NORMINAL} * 100\%$, where $V_{NORMINAL} = 19.5V$
- b). Load regulation shall less than 2%

90Vac/60Hz

Load	0A	4.62A
V _{OUT}	19.453V	19.149V
Load Regulation	$(19.453V - 19.149V) / 19.5V * 100\% = 1.56\%$	

264Vac/50Hz

Load	0A	4.62A
V _{OUT}	19.450V	19.147V
Load Regulation	$(19.450V - 19.147V) / 19.5V * 100\% = 1.55\%$	

2.2 Ripple & Noise (P.A.R.D.)

Test Condition :

Ripple and noise are defined as periodic or random signal over a frequency band of 10Hz to 20MHz. Measurement shall be made with an oscilloscope with 20MHz bandwidth. Outputs should be bypassed at the end of the output cable with a 0.1 μ F ceramic disk capacitor and a 22 μ F electrolytic capacitor to simulate loading.

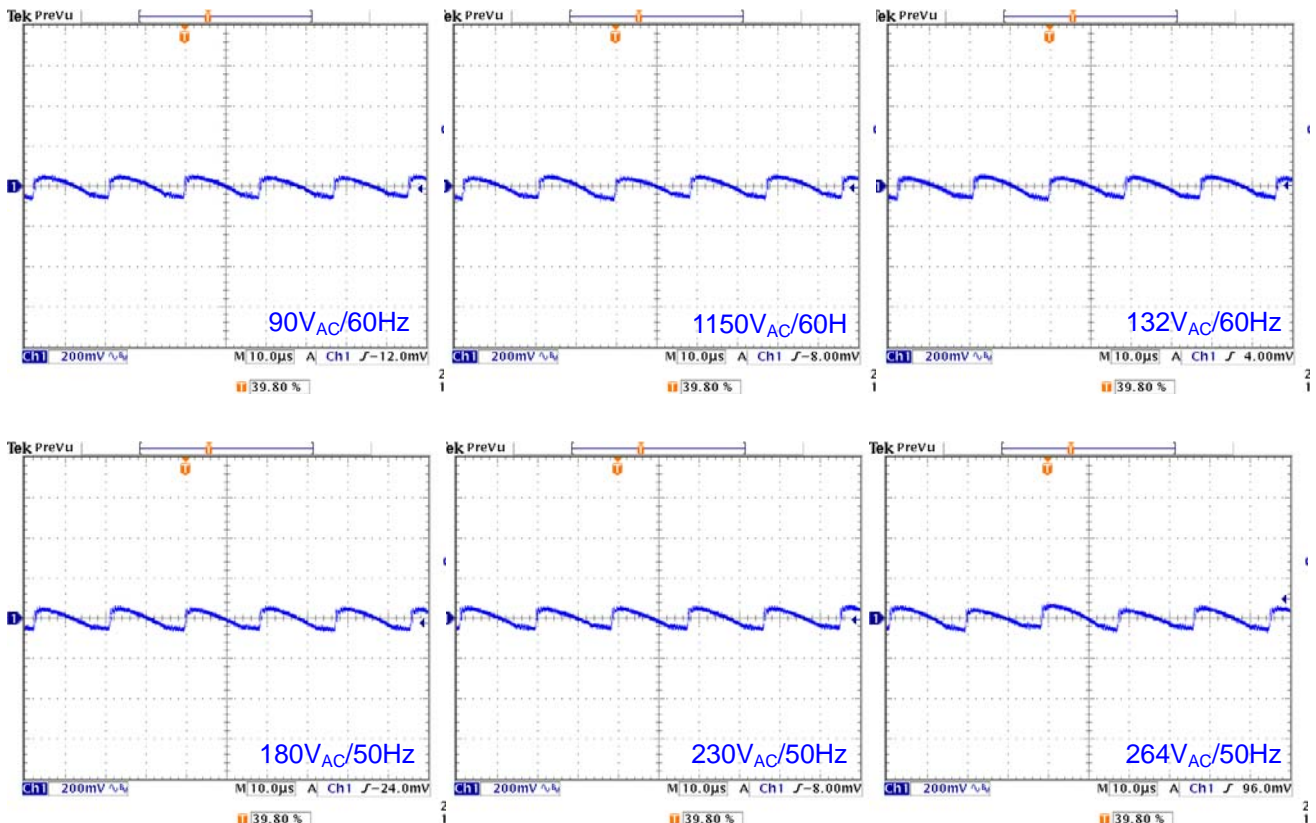
- a). $V_{IN} = 90V_{AC}$ to $264V_{AC}$ as indicated below
- b). $I_{OUT} = 4.62A$

Criteria:

P.A.R.D. on output shall remain within the specified limits (200mVp-p) at maximum load.

Test Result:

Input Voltage (V_{AC}/Hz)	90/60	115/60	132/60	180/50	230/50	264/50
R&N (mV)	132	144	140	136	136	152



2.3 Dynamic Load Response

Test Condition :

The unit is subjected to a load change from 0% to 100% at a rate of 1A/ μ sec. The frequency of change is set to give the best readability of the deviation and setting time.

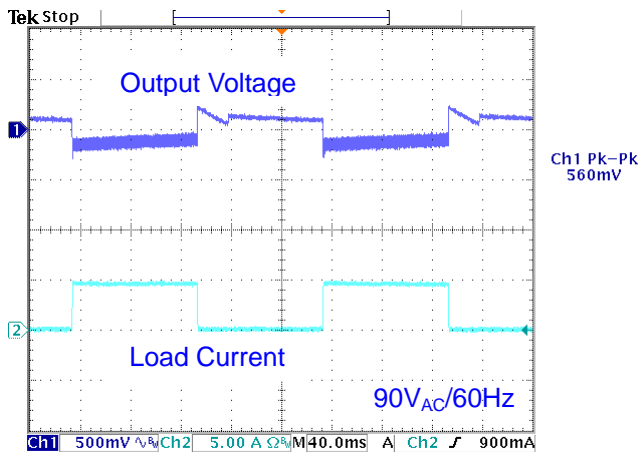
Note: The voltage is measured at the end of the output cable.

Criteria:

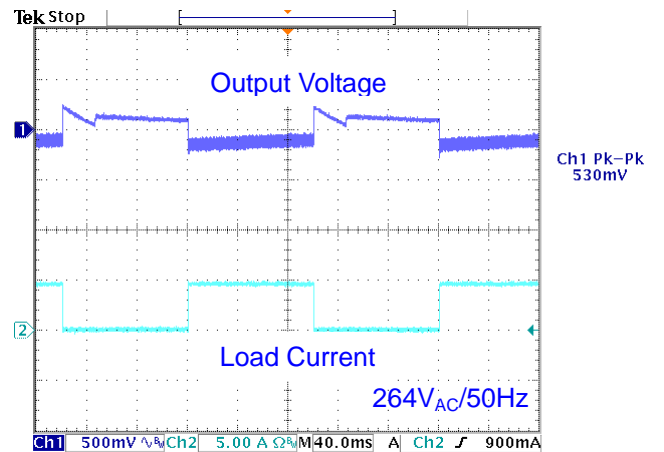
The unit output shall not undershoot or overshoot beyond the specified limits (+1V/-0.5V) after applying load changes.

Test Result:

Input Voltage (V_{AC}/Hz)	90/60	264/50
Deviation Voltage V_{p-p} (mV)	560	530



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3.0 Protection

3.1 Short-Circuit Protection

An output short circuit is defined as the output impedance of less than 0.1ohms.

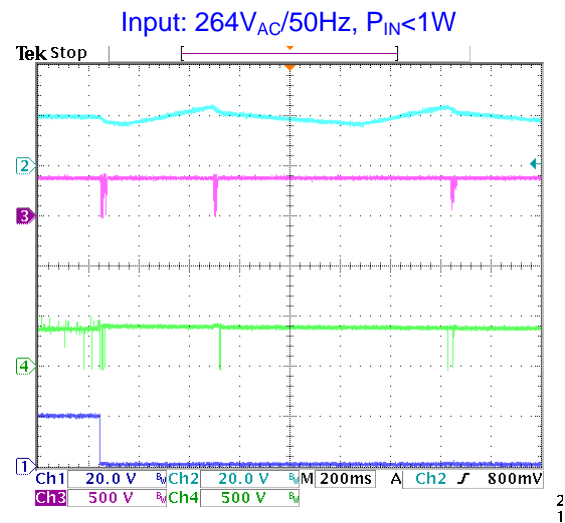
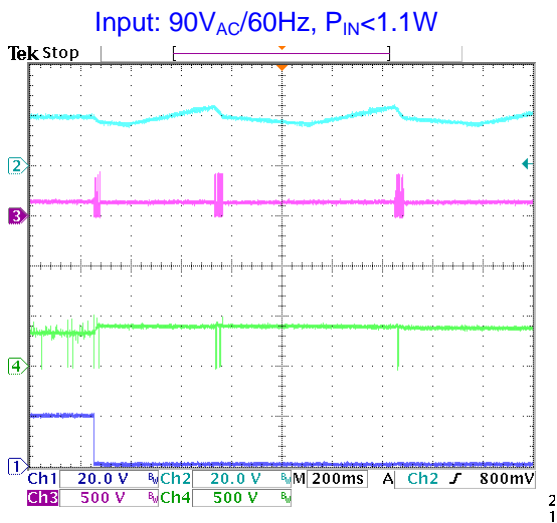
Test Conditions :

It is a manual test where short circuit is applied to output while the unit is at no load. The AC line voltages are chosen in order to obtain the worst case condition. The unit shall fold back while shorting, but when the short is removed the unit shall recover automatically. The unit shall be capable of withstanding a continuous short-circuit to the output without damage or overstress to the unit under any input conditions.

Criteria:

No damage shall result during the test.

Test Result:



CH1: V_{OUT} CH2: V_{CC} CH3: V_{DS_Q1} CH4: V_{DS_Q2}

3.2 Over-Current Protection

Overload currents applied to output rail will cause the output to trip before reaching or exceeding 240VA.

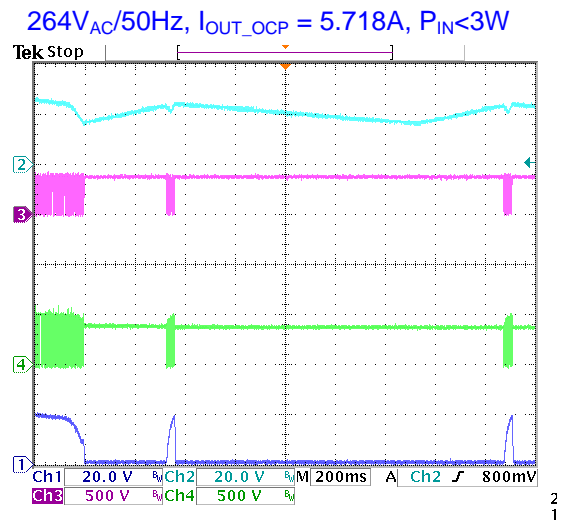
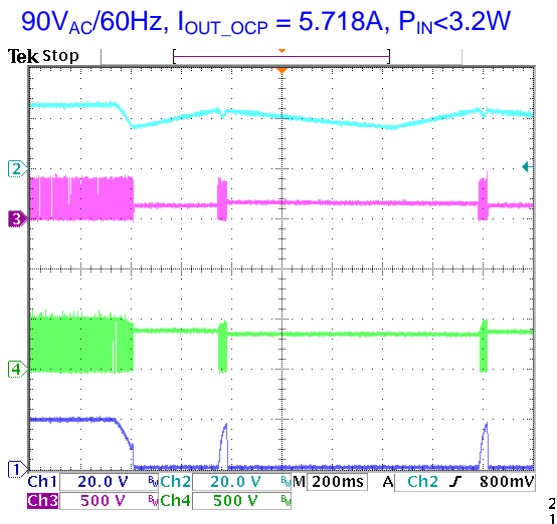
Test Conditions :

The load is increased on output from its maximum value to an estimated over-current value in several steps. The test is repeated at different input voltages.

Criteria:

The output shall be limited and shall not exceed 240VA.

Test Result:



CH1: V_{OUT} CH2: V_{CC} CH3: V_{DS_Q1} CH4: V_{DS_Q2}

3.3 Over-Voltage Protection

Test Conditions :

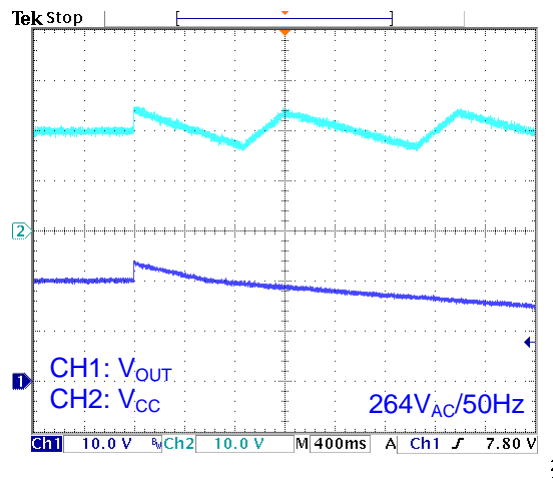
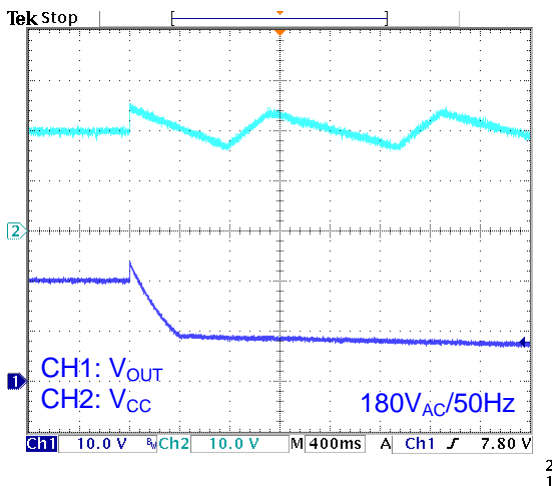
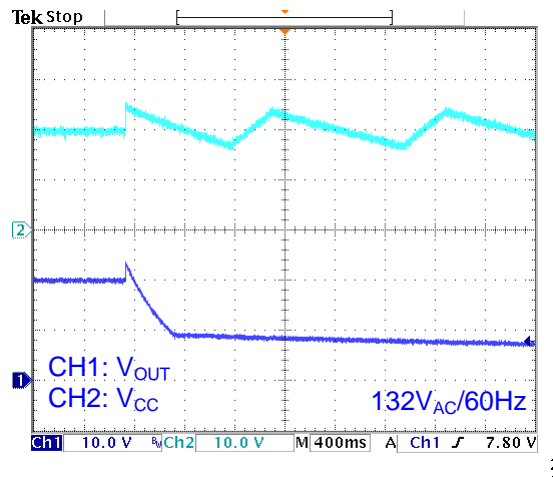
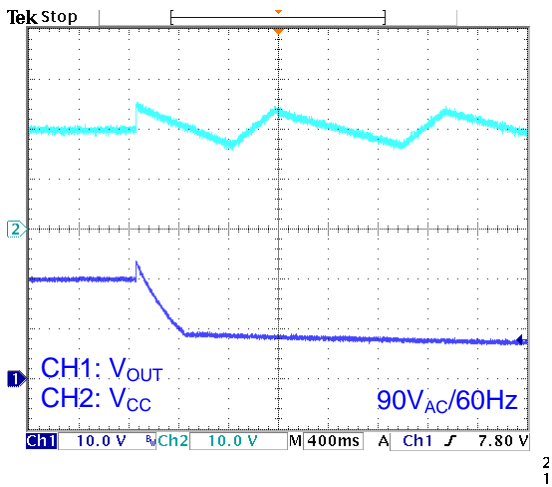
It is performed by fooling the feedback loops of the output voltage. The AC line voltages are chosen in order to obtain the worst case condition and the output is at no load.

Criteria:

The unit shall provide latch-mode over-voltage protection within 25V, and no single point fault shall be able to cause a sustained over-voltage condition on output.

Test Result:

Input Voltage (V_{AC}/Hz)	90/60	132/60	180/50	264/50
Trip Point (V)	23.8	23.8	24.0	24.0
Protection Mode	Latch	Latch	Latch	Latch



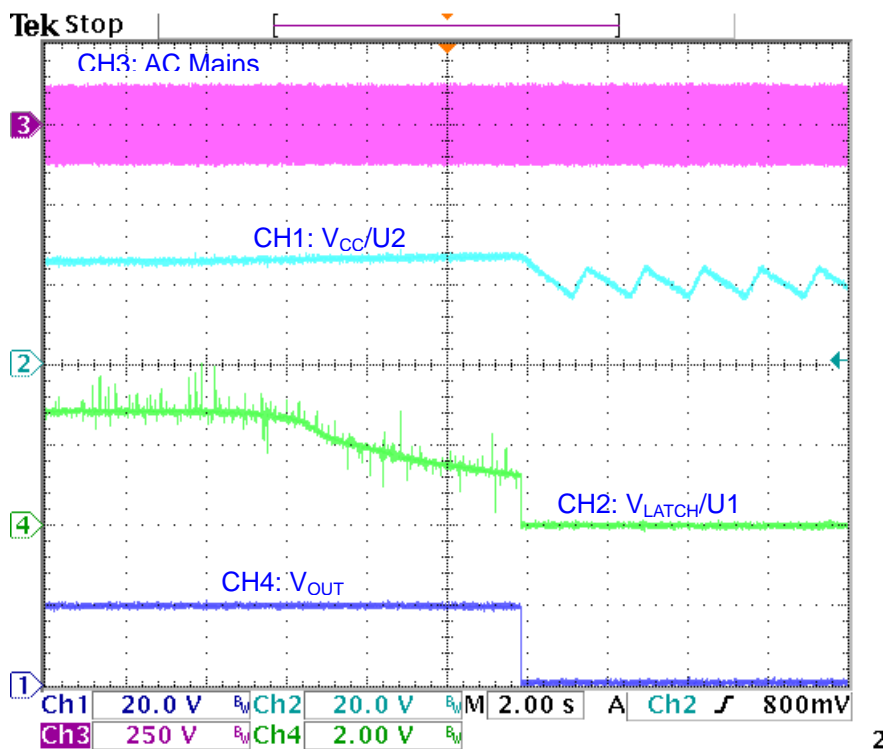
3.4 Over-Temperature Protection

Test Conditions :

An accurate temperature protection is provided in the circuit (U1, TR2, R26 and C19). When the junction temperature of TR2 exceeds the thermal shutdown temperature and the voltage on the LATCH pin raise above 1.25V, the unit will be latched off immediately. The voltage on the V_{CC} pin will cycle between V_{CC(START)} and V_{CC(UVLO)}, and the U1 will not start switching again until the latch function is reset.

Criteria:

The IC should latch off the output at a V_{LATCH} trip level of 1.25V. No output bounce or hiccup is allowed.



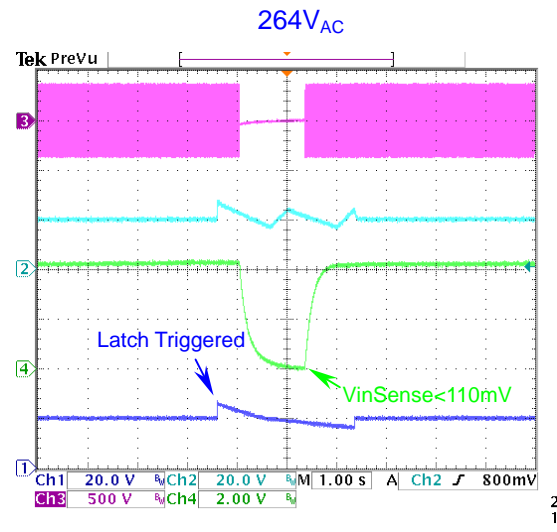
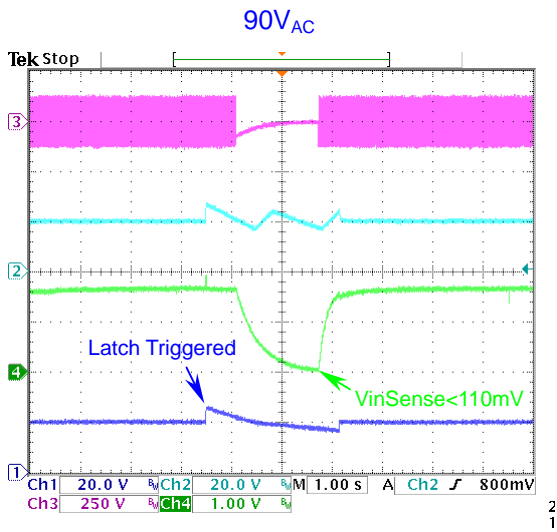
Note:

OTP≅108°C in this case.

3.5 Fast Latch Reset

Test Conditions :

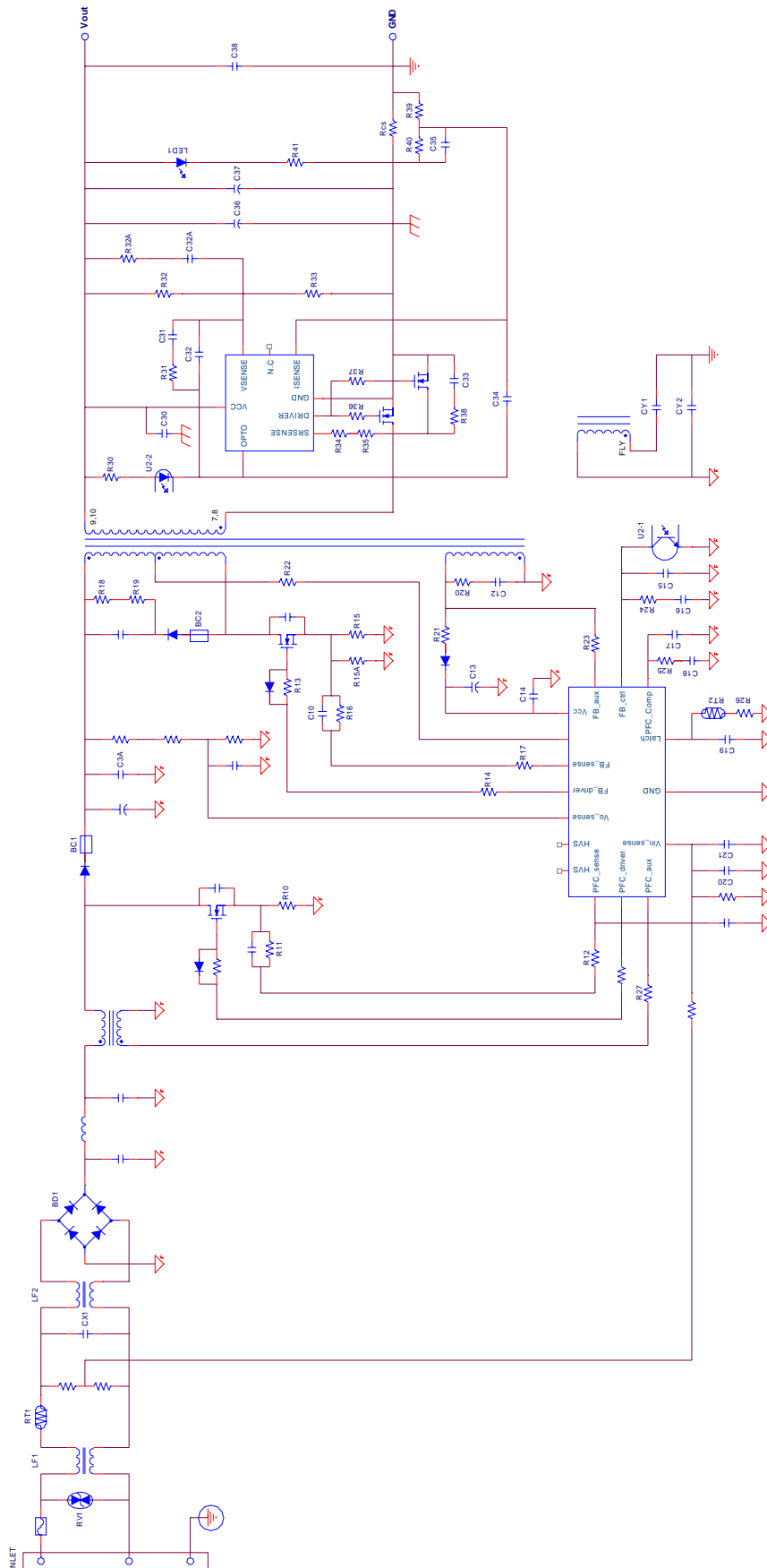
The latched protection will be reset as soon as the voltage on VinSense pin drops below 110mV (typ.) and after that is raised to 225 mV (typ.), the latched protection is fast reset accordingly.



CH1: V_{OUT} CH2: V_{CC} CH3: AC Mains CH4: Vin_sense

Appendix

Schematic:





Component List:

Item	Description	Designation	Q'ty
Resistor			
1	Resistor, SMD 1206 Thin Film Chip, 2M ohm, 5%	R1,R2	2
2	Resistor, SMD 0805 Thin Film Chip, 560K ohm, 5%	R3	1
3	Resistor, SMD 0805 Thin Film Chip, 47K ohm, 5%	R4	1
4	Resistor, Axial Lead, 1/4W, 4.7M ohm, 1%	R5	1
5	Resistor, SMD 1206 Thin Film Chip, 4.7M ohm, 1%	R6	1
6	Resistor, SMD 0805 Thin Film Chip, 62K ohm, 1%	R7	1
7	Resistor, SMD 0805 Thin Film Chip, 10 ohm, 5%	R8,R9,R14,R36	4
8	Resistor, Axial Lead, MOF, 0.1 ohm, 1W(S), 5%	R10	1
9	Resistor, SMD 0805 Thin Film Chip, 12K ohm, 5%	R11	1
10	Resistor, SMD 0805 Thin Film Chip, 1K ohm, 5%	R12,R17,R30,R35	4
11	Resistor, SMD 0805 Thin Film Chip, 47 ohm, 5%	R13,R20,R38	3
12	Resistor, Axial Lead, MOF, 0.15 ohm, 1W(S), 5%	R15	1
13	Resistor, SMD 0805 Thin Film Chip, 15K ohm, 5%	R16	1
14	Resistor, SMD 1206 Thin Film Chip, 43K ohm, 5%	R18,R19	2
15	Resistor, SMD 0805 Thin Film Chip, 0 ohm, 5%	R21	1
16	Resistor, SMD 0805 Thin Film Chip, 10K ohm, 5%	R22,R26,R31,R32A,R39,R41	6
17	Resistor, SMD 0805 Thin Film Chip, 71.5K ohm, 1%	R23	1
18	Resistor, SMD 0805 Thin Film Chip, 39K ohm, 5%	R24	1
19	Resistor, SMD 0805 Thin Film Chip, 33K ohm, 5%	R25	1
20	Resistor, SMD 0805 Thin Film Chip, 4.7K ohm, 5%	R27	1
21	Resistor, SMD 0805 Thin Film Chip, 35.7K ohm, 1%	R32	1
22	Resistor, SMD 0805 Thin Film Chip, 5.23K ohm, 1%	R33	1
23	Resistor, SMD 1206 Thin Film Chip, 0 ohm, 5%	R34	1
24	Resistor, SMD 0805 Thin Film Chip, 51K ohm, 5%	R40	1
25	NTC Resistor, Axial Lead, 5φ, 100K ohm, 5%, TTC05104/Thinking	RT2	1
Capacitor			
1	Film Capacitor, Axial Lead, 0.47μF/450V, 5%, MMX/Arcotronics Nissei	C1,C2	2
2	E/C, Radial Lead, 68μF/400V, 105°C, 16x30mm, TY/LTEC	C3	1
3	Ceramic, Disc, 11.5φ, 10000pF/1KV, Z5U	C3A	1
4	MLCC, SMD 0805, 0.01μF/50V, X7R	C4,C15,C19,C31,C32A	5
5	MLCC, SMD 1206, 220pF/630V, NPO	C5	1
6	MLCC, SMD 0805, 0.047μF/50V, X7R	C6	1
7	Ceramic, Disc, 8.5φ, 3300pF/1KV, Z5U	C8	1
8	MLCC, SMD 1206, 100pF/630V, NPO	C9	1
9	MLCC, SMD 0805, 0.1μF/50V, X7R	C10	1
10	MLCC, SMD 0805, 220pF/100V, NPO	C12,C33	2
11	E/C, Radial Lead, 47μF/35V, 105°C, 5x11mm, LZP/LTEC	C13	1
12	MLCC, SMD 0805, 1μF/50V, Y5V	C14,C21,C30	3
13	MLCC, SMD 0805, 0.33μF/16V, X7R	C16	1
14	MLCC, SMD 0805, 0.15μF/16V, X7R	C17	1
15	MLCC, SMD 0805, 0.47μF/16V, X7R	C18	1
16	MLCC, SMD 0805, 2.2μF/10V, X7R	C20,C35	2
17	MLCC, SMD 0805, 470pF/50V, X7R	C34	1
18	E/C, Radial Lead, 680μF/25V, 105°C, 10x16mm, LZP/LTEC	C36,C37	2
19	MKP, X2 Cap, Axial Lead, 0.33μF/275Vac, R46/Arcotronics Nissei	CX1	1
20	Ceramic, Y1 Cap, Disc 7φ, 150pF/400Vac, CD/TDK	CY1	1
21	Ceramic, Y1 Cap, Disc 8.5φ, 1000pF/400Vac, CD/TDK	CY2	1



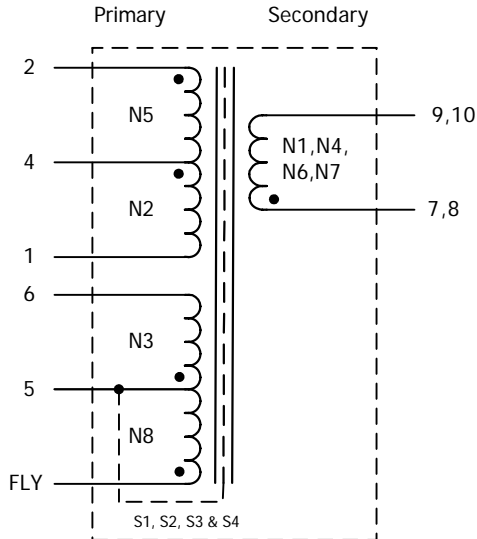
APBADC015 Test Report

APB_ADC

Item	Description	Designation	Q'ty
Diode			
1	Bridge Diode, Flat/Mini, 8A/600V, GBU806/Lite-On	BD1	1
2	Ultra Fast Diode, Axial Lead, DO-201AD, 5A/600V, SF50JG/Lite-On	D1	1
2	Ultra Fast Diode, TO-220AC, 5A/600V, BYC5-600/NXP	D1 (Alternate Source)	1
2	Ultra Fast Diode, TO-220AC, 9A/600V, BYV29-600/NXP	D1 (Alternate Source)	1
2	Ultra Fast Diode, SOD113, 9A/600V, BYV29X-600/NXP	D1 (Alternate Source)	1
3	Switching Diode, SMD SOD-80, 0.2A/75V, PMLL4148/NXP	D2,D4	2
4	General Purpose Diode, Axial Lead, SOD-57, 2A/1KV, LT2A07/Lite-On	D3	1
5	Ultra-Fast Diode, SMD SOD-80, 0.25A/250V, BAV103/NXP	D5	1
6	LED, 5φ*25mm, Green	LED1	1
MOSFET			
1	MOSFET, TO-220F, 12A/500V, 0.52/15p-typ, 2SK3568/Toshiba	Q1	1
2	MOSFET, TO-220F, 10A/600V, 0.75/15p-typ, 2SK3569/Toshiba	Q2	1
3	MOSFET, TO-220, 75A/100V, 0.015/220p-typ, PSMN015-100P/NXP	Q3	1
IC			
1	GreenChip III SMPS Controller IC, SO-16, TEA1750/NXP	U1	1
2	Optocoupler, CTR=130~260, LTV-817B/Lite-On	U2	1
3	Synchronous Rectifier Controller IC, SO-8, TEA1761T/NXP	U3	1
Inductor			
1	Transformer, PQ-3220, 560μH, APBADC015/Sendpower	T1	1
2	Line Choke, T12*6*4, 0.6φx2 (3L), 10T, 1mH, SP05D100/S.P	LF1	1
3	Line Choke, T16*12*8 A10, 0.55φx2, 62.5Ts, 12.8mH, SP06Z181/S.P	LF2	1
4	Choke, T60-52, 0.7φ, 65Ts, 220μH, SP05Z369/Sendpower	L1	1
5	PFC Choke, RM-10, 40:2, 250μH, PFC-APBADC015/Sendpower	L2	1
6	Bead Core, RH4*6*2, K5B(King-Core)/XP, N4/AMAX	BC1 for D1	1
7	Bead Core, RH3.5*4.2*1.3, S6H/JK,H6H/AH, N6/AMAX	BC2 for D3	1
Others			
1	Jumper Wire, 0.6φ*10mm	J1,J3,	2
2	Jumper Wire, 0.6φ*7.5mm	J2,J4,J6	3
3	Jumper Wire, 0.6φ*5mm	J5,J8	2
4	Jumper Wire, 1φ*10mm	J9	1
5	Jumper Wire, 0.6φ*12.5mm	J11	1
6	Jumper Wire, 1φ*7.5mm	RT1	1
7	Mu-Cu Wire, 1.2φ*8mm, Kink Type, 10m ohm	Rcs	1
8	Heatsink, L-Shape, 89.5*25.5*25mm, t=2mm, Cu-Tinned, WD	For Q1,Q2	1
9	Heatsink, L-Shape, 91.5*19.5*25mm, t=2mm, Cu-Tinned, WD	For Q3	1
10	PCB, Single Side, CEM-3, 2-OZ, 126*59.6*1.6mm, APBADC015 Ver. B	Main PCB	1
11	Fuse, Axial Lead, Time Lag, T3.15A/250V, LT-5/Littlefuse	F1	1
12	Screw, M3*8, Pan Head, NI Shouh-Pin	For BD1	1
13	Screw, M3*10, Flat Head 5.0, NI Shouh-Pin	For Q1,Q2,Q3	3
14	Nut, HEX/GW, M3, NI Shouh-Pin, LF	For Q1,Q2,Q3	3
15	Silicon Tube, 1φ*15mm, A(Kurabe)/LC, Nikkan	For TR1	2
16	Silicon Rubber, 18*13mm, TO-2203/Pingood	For Q3	1
17	Bushing, TO-220, A427(Imperial), Toray/Everfame	For Q3	1
18	LED Holder, 5φ*11mm, LED-11/PinGood	For LED1	1
19	Inlet, L3P, TU-333-BZ-315-P3D/TECX	Inlet	1
20	Cable, 16AWG/1571, 2.5*5.5*12 (kk,fk), L=1000mm	Output	1

Transformer Specification:

1. Transformer Schematic Diagram



2. Winding Specification

No.	Pin		Wire	Turns	Winding Method	Margin Tape		Insulation	
	Start	Finish				Pri.	Sec.	Turn	Width
N1	9	7	0.3φ(3L) X 2	6	Center	-	-	1	10mm
S1		5	0.025t*8mm	1	Center	-	-	1	10mm
N2	1	4	0.5φ X 1	16	Center	-	-	1	10mm
S2		5	0.025t*8mm	1	Center	-	-	1	10mm
N3	6	5	0.25φ X 2	6	Center	-	-	1	10mm
N4	10	8	0.3φ(3L) X 2	6	Center	-	-	1	10mm
S3		5	0.025t*8mm	1	Center	-	-	1	10mm
N5	4	2	0.5φ X 1	16	Center	-	-	1	10mm
S4		5	0.025t*8mm	1	Center	-	-	1	10mm
N6	9	7	0.3φ(3L) X 2	6	Center	-	-	1	10mm
N7	10	8	0.3φ(3L) X 2	6	Center	-	-	1	10mm
N8	5	FLY	0.25φ X 1	5	Center	-	-	1	10mm
Outer-Wrapped of Core								2	10mm

3. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1 - 2	560μH ± 5%	60KHz, 1V
Leakage Inductance	1 - 2	6μH	2 nd all short

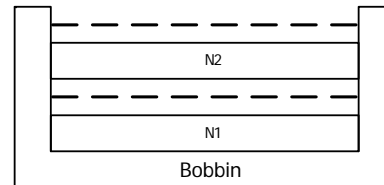
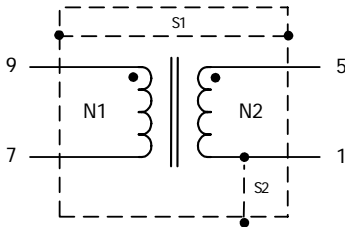
4. Core & Bobbin

Core: PQ-3220 (TDK PC44 or Equiv.)
 Bobbin: PQ-3220 (12Pin, Vertical Type)
 Ae: 170mm²

5. Marking: APBADC015

PFC Choke Specification:

1. Transformer Schematic Diagram



2. Winding Specification

No.	Pin		Wire	Turns	Winding Method	Margin Tape		Insulation	
	Start	Finish				Pri.	Sec.	Turn	Width
N1	9	7	0.1 ϕ X 30	40	Center	-	-	1	10mm
N2	5	1	0.22 ϕ X 2	2	Center	-	-	1	10mm
S1			0.05t*14mm	1	Center	-	-		
S2		1	0.05t*14mm	1	Center	-	-		
Outer-Wrapped of Core								1	14mm (S2)
								1	14mm (S1)

3. Electrical Characteristics

	Pin	Specification	Remark
Inductance	9 – 7	250 μ H \pm 10%	60KHz, 1V
Leakage Inductance	9 – 7	N/A	

4. Core & Bobbin

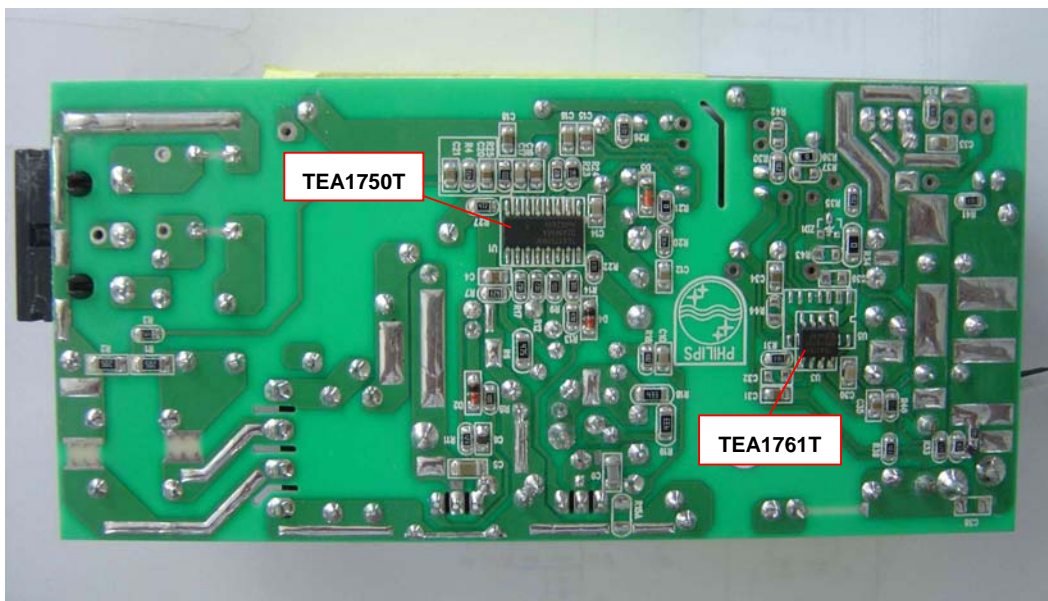
Core: RM-10 (Ferroxcube RM/I or Equiv.)
 Bobbin: RM-10 (12Pin, Vertical Type)
 Ae: 96.6mm²

5. Marking: PFC-APBADC015

Evaluation Board:



(Top View)



(Bottom View)