

NCP1901

Advance Information

Primary Side Combination Resonant and PFC Controllers

The NCP1901 is a combination of PFC and half-bridge resonant controllers optimized for off-line adapter applications. This device includes all the features needed to implement a highly efficient and small form factor adapter. It integrates a critical conduction mode (CrM) power factor correction (PFC) controller and a half-bridge controller with a built-in 600 V driver. The half-bridge stage operates at a fixed frequency. Regulation is achieved by adjusting the PFC stage output voltage.

This device includes an enable input on the PFC feedback pin, open feedback loop protection and PFC overvoltage and undervoltage detectors. Other features included in the NCP1901 are a 600 V startup circuit and an adjustable frequency oscillator. The controllers are properly sequenced, simplifying system design.

Features

- Adjustable Half-Bridge Frequency up to 75 kHz
- Open Feedback Loop Protection
- CrM Power Factor Correction Controller
- PFC Undervoltage Detector
- PFC Overvoltage Detector
- Half-Bridge Controller with 600 V High Side Gate Drive
- State Machine Ensures Proper Turn-on and Turn-off of Half-Bridge Stage
- Enable Input on the PFC Feedback Pin Disables Controllers and Reduces Power
- Controllers are Properly Sequenced for Fault Free Operation
- Internal 600 V Startup Circuit
- This is a Pb-Free Device

Typical Applications

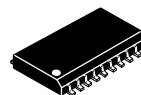
- High Efficiency Notebook Adapter
- Solid State Lighting

This document contains information on a new product. Specifications and information herein are subject to change without notice.

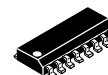


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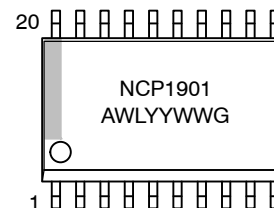
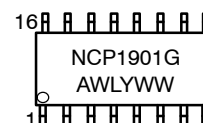


SO-20 WB
DW SUFFIX
CASE 751D



SOIC-16
D SUFFIX
CASE 751B

MARKING DIAGRAM



NCP1901 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y or YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-----------------------|------------------|
| NCP1901DR2G | SOIC-16 (Pb-Free) | 2500/Tape & Reel |
| NCP1901DWR2G | SO-20 WB (Pb-Free) | 1000/Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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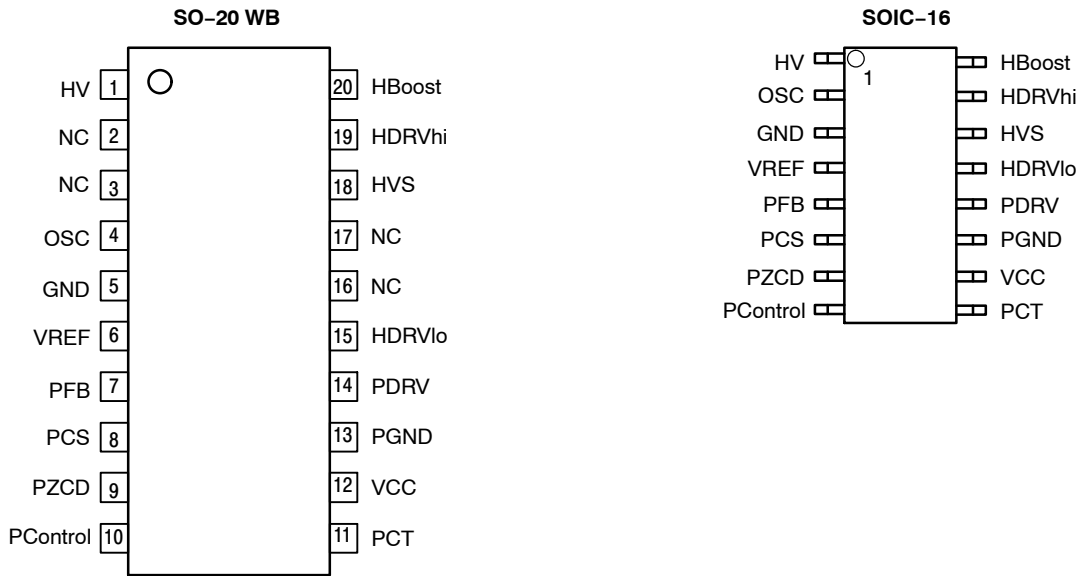


Figure 1. Pin Connections

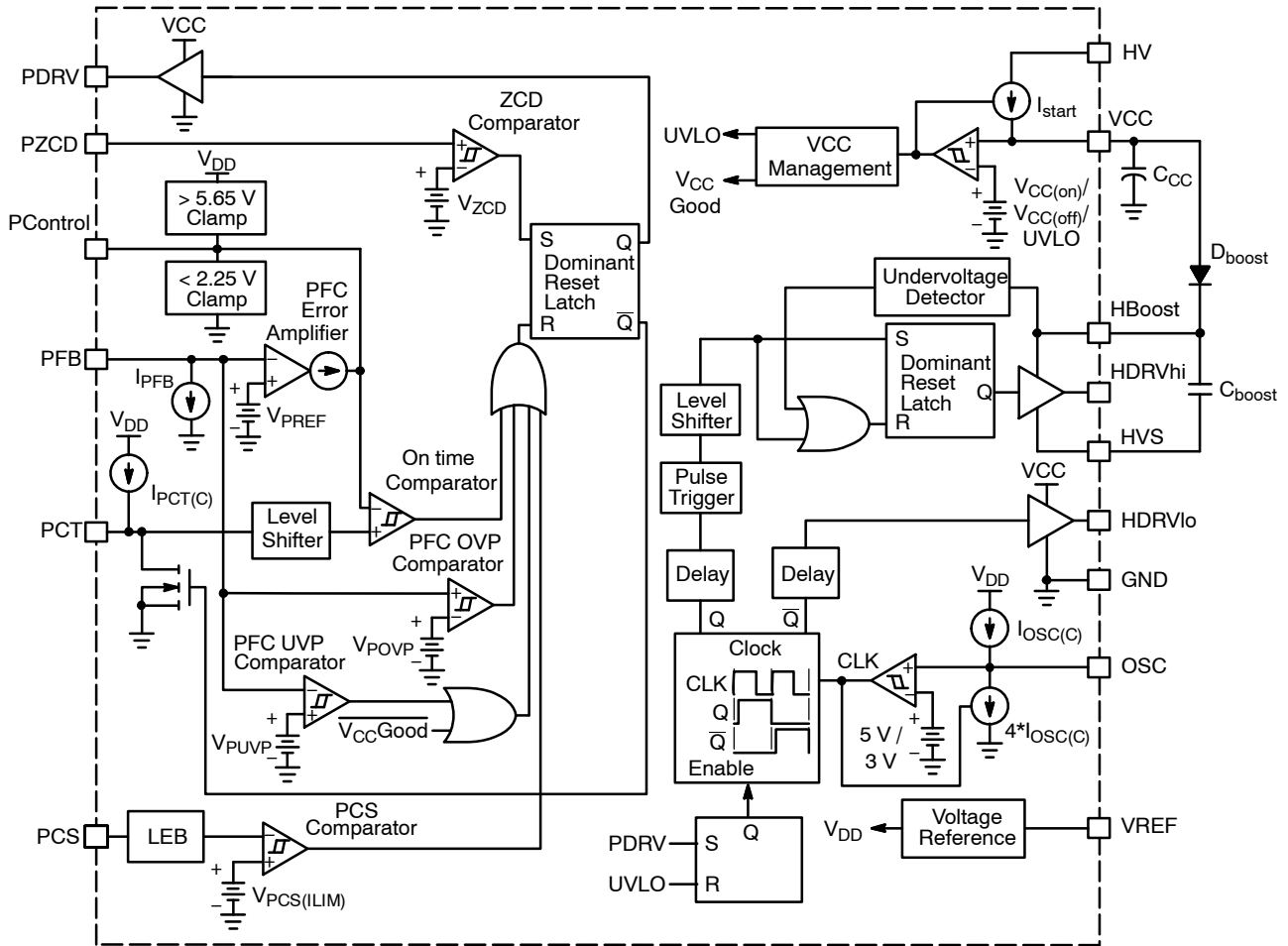


Figure 2. Functional Block Diagram

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Table 1. PIN FUNCTION DESCRIPTION

| 20 Pin | 16 Pin | Name | Description |
|--------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | 1 | HV | This is the input of the high voltage startup regulator and connects directly to the bulk voltage. A constant current source supplies current from this pin to the V_{CC} capacitor, eliminating the need for an external startup resistor. The charge current is 7.5 mA (typical). |
| 4 | 2 | OSC | A capacitor on this pin adjusts the frequency of the internal oscillator. The oscillator sets the frequency of the half-bridge controller. The half-bridge operates at half the oscillator frequency. |
| 5 | 3 | GND | Analog ground. |
| 6 | 4 | VREF | Reference voltage. The capacitor on this pin decouples the internal reference. A 0.1 μ F capacitor needs to be connected between this pin and ground. |
| 7 | 5 | PFB | PFC voltage feedback input. The voltage on this pin is compared to a 2.5 V reference (typical) to regulate the PFC output voltage. The voltage on this pin is also used to detect PFC undervoltage and overvoltage conditions. |
| 8 | 6 | PCS | PFC regulator current sense input. A voltage ramp proportional to the PFC switch current is applied to this pin. The current sense threshold, $V_{PCS(LIM)}$, is typically 0.84 V. A 110 ns (typical) leading edge blanking circuit filters the current sense signal at the start of each cycle. |
| 9 | 7 | PZCD | PFC inductor zero current detector. The inductor current is monitored using an auxiliary winding on the PFC inductor. The PFC drive signal is enabled during a high to low transition on the PZCD pin. A series resistor limits the current into the PZCD pin. |
| 10 | 8 | PControl | PFC control voltage. This pin connects to the output of the PFC error amplifier. The error amplifier is a transconductance amplifier. A compensation network between this pin and grounds sets the PFC loop bandwidth. The PFC control voltage is compared to a level shifted version of V_{PCT} to control the PFC duty ratio. |
| 11 | 9 | PCT | PFC on time control capacitor. A 270 μ A (typical) current source charges a capacitor connected between this pin and ground. Once the level shifted PCT voltage reaches $V_{PControl}$, the PFC drive signal is disabled and the PCT capacitor is discharged. |
| 12 | 10 | VCC | Positive input supply. This pin connects to an external capacitor for energy storage. An internal current source supplies current from HV to this pin. Once the V_{CC} voltage reaches $V_{CC(on)}$ (15.3 V typical), the current source turns off and the controller is enabled. The current source turns on once V_{CC} falls to $V_{CC(off)}$ (9.3 V typical). During normal operation, power is supplied to the IC via this pin by means of an auxiliary winding. |
| 13 | 11 | PGND | Ground connection for PDRV and HDRVlo. Tie to the power stage return with a short trace. |
| 14 | 12 | PDRV | PFC switch gate drive control signal. The source and sink drive capability is limited to 60 Ω and 15 Ω (typical), respectively. A discrete driver may be needed to drive the external MOSFET. |
| 15 | 13 | HDRVlo | Half-bridge low side switch gate drive control signal. The source and sink drive capability is limited to 75 Ω and 15 Ω (typical), respectively. A discrete driver may be needed to drive the half bridge switch. |
| 18 | 14 | HVS | Half-bridge high side driver source connection. This pin connects directly to the bridge terminal and can float up to 600 V. |
| 19 | 15 | HDRVhi | Half-bridge high side switch gate drive control signal. The source and sink drive capability is limited to 75 Ω and 15 Ω (typical), respectively. The supply terminals of the high side driver connect to the HBoost and HVS pins. |
| 20 | 16 | HBoost | Supply voltage of the high side gate driver. A charge pump generates a bootstrap voltage floating on top of the HVS voltage. A diode between the VCC and HBoost pins provides a charge path. The bootstrap voltage is V_{CC} minus a diode drop. |

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Table 2. MAXIMUM RATINGS (Notes 1 and 2)

| Rating | Symbol | Value | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|------|
| High Voltage Input Voltage | V_{HV} | -0.3 to 600 | V |
| High Voltage Input Current | I_{HV} | 10 | mA |
| Supply Input Voltage | V_{CC} | -0.3 to 20 | V |
| Supply Input Current | I_{CC} | 10 | mA |
| Oscillator Input Voltage | V_{OSC} | -0.3 to 10 | V |
| Oscillator Input Current | I_{OSC} | 10 | mA |
| Bandgap Reference Decoupling Output Voltage | V_{REF} | -0.3 to 9 | V |
| Bandgap Reference Decoupling Output Current | I_{REF} | 10 | mA |
| PFC Feedback Voltage Input Voltage | V_{PFB} | -0.3 to 10 | V |
| PFC Feedback Voltage Input Current | I_{PFB} | 10 | mA |
| PFC Current Sense Input Voltage | V_{PCS} | -0.3 to 10 | V |
| PFC Current Sense Input Current | I_{PCS} | 10 | mA |
| PFC Zero Current Detection Input Voltage | V_{PZCD} | -0.3 to 10 | V |
| PFC Zero Current Detection Input Current | I_{PZCD} | 10 | mA |
| PFC Control Input Voltage | $V_{PControl}$ | -0.3 to 10 | V |
| PFC Control Input Current | $I_{PControl}$ | 1.2 | mA |
| PFC On Time Control Input Voltage | V_{PCT} | -0.3 to 10 | V |
| PFC On Time Control Input Current | I_{PCT} | 9 | mA |
| PFC Drive Signal Voltage | V_{PDRV} | -0.3 to V_{CC} | V |
| PFC Drive Signal Current | I_{PDRV} | 100 | mA |
| Half-Bridge Low Side Driver Input Voltage | V_{HDRVlo} | -0.3 to V_{CC} | V |
| Half-Bridge Low Side Driver Input Current | I_{HDRVlo} | 100 | mA |
| Half-Bridge High Side Driver Source Connection Input Voltage | V_{HVS} | -1.0 to 600 | V |
| Half-Bridge High Side Driver Source Connection Input Current | I_{HVS} | 100 | mA |
| Half-Bridge High Side Driver Input Voltage | V_{HDRVhi} | -1.3 to 600 | V |
| Half-Bridge High Side Driver Input Current | I_{HDRVhi} | 100 | mA |
| Half-Bridge High Side Driver Charge Pump Input Voltage | V_{HBoost} | -0.3 to 600 | V |
| Half-Bridge High Side Driver Charge Pump Input Current | I_{HBoost} | 100 | mA |
| High Side Boost Circuit Supply Voltage (between HBoost and HVS pins) | $V_{HBoost(supply)}$ | -0.3 to V_{CC} | V |
| High Side Boost Circuit Supply Current (between HBoost and HVS pins) | $I_{HBoost(supply)}$ | 100 | mA |
| Half-Bridge High Side Driver Source Connection Slew Rate | dV_{HVS}/dt | TBD | V/ns |
| Operating Junction Temperature | T_J | -40 to 150 | °C |
| Storage Temperature Range | T_{stg} | -60 to 150 | °C |
| Power Dissipation ($T_A = 25^\circ\text{C}$, 1 Oz Cu, 0.155 Sq Inch, Printed Circuit Copper Clad) D Suffix, Plastic Package Case 751B-05 (SOIC-16) | P_D | 0.95 | W |
| Thermal Resistance, Junction to Ambient (1 Oz Cu, 0.155 Sq Inch, Printed Circuit Copper Clad) D Suffix, Plastic Package Case 751B-05 (SOIC-16) | $R_{\theta JA}$ | 130 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device(s) contains ESD protection and exceeds the following tests:
 Pins 1, 14, 15 and 16 rated to the maximum voltage of the part, or 600 V.
 All Other Pins: Human Body Model 1500 V per JEDEC Standard JESD22-A114E.
 Machine Model 150 V per JEDEC Standard JESD22-A115-A.
- This device contains Latch-Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.

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Table 3. ELECTRICAL CHARACTERISTICS ($V_{HV} = \text{open}$, $V_{PFB} = 2.4 \text{ V}$, $V_{PCS} = 0 \text{ V}$, $V_{PZCD} = 5 \text{ V}$, $V_{PControl} = \text{open}$, $V_{CC} = 15 \text{ V}$, $V_{PDRV} = \text{open}$, $V_{HDRVlo} = \text{open}$, $V_{HVS} = 0 \text{ V}$, $V_{HDRVhi} = \text{open}$, $V_{HBoost} = 15 \text{ V}$, $C_{OSC} = 2200 \text{ pF}$, $C_{VREF} = 0.1 \mu\text{F}$, $C_{PCT} = 1000 \text{ pF}$, for typical values $T_J = 25^\circ\text{C}$, for min/max values, T_J is -40°C to 125°C , unless otherwise noted)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|-----------------------------------------------------|----------------------------------------------------------------------------------------------|------------------|--------------|-----------|--------------|---------------|
| STARTUP AND SUPPLY CIRCUITS | | | | | | |
| Supply Voltage | | | | | | V |
| Startup Threshold | V_{CC} Increasing | $V_{CC(on)}$ | 14.3 | 15.3 | 16.3 | |
| Minimum Enable Threshold | V_{CC} Decreasing | $V_{CC(enable)}$ | 13.6 | 14.6 | 15.6 | |
| Minimum Operating Voltage | V_{CC} Decreasing | $V_{CC(off)}$ | 8.5 | 9.3 | 10.0 | |
| Supply Current | | | | | | mA |
| Device Disabled/Fault | $V_{PFB} = V_{PUVP(low)}$ | I_{CC1} | 1.0 | 1.4 | 2.0 | |
| Device Switching | (Note 4) | I_{CC2} | 1.5 | 2.4 | 3.0 | |
| Startup Current | $V_{CC} = V_{CC(on)} - 0.2 \text{ V}$, $V_{HV} = 50 \text{ V}$ | I_{start} | 3.0 | 7.5 | 10.5 | mA |
| Startup Circuit Off-State Leakage Current | $V_{HV} = 600 \text{ V}$, $V_{CC} = V_{CC(on)} + 0.2 \text{ V}$ | $I_{HV(off)}$ | – | 15 | 50 | μA |
| BANDGAP REFERENCE | | | | | | |
| Reference Voltage | $C_{REF} = 0.1 \mu\text{F}$ | V_{REF} | 6.605 | 7.000 | 7.295 | V |
| OSCILLATOR | | | | | | |
| Half-Bridge Clock Frequency | $V_{HVS} = 50 \text{ V}$ | f_{clock} | 13.5 | 15.5 | 16.5 | kHz |
| Maximum Half-Bridge Clock Frequency | $C_{OSC} = \text{open}$ | $f_{clock(MAX)}$ | 75 | – | – | kHz |
| PFC ERROR AMPLIFIER | | | | | | |
| PFC Feedback Voltage Reference | $0^\circ\text{C} < T_J < 125^\circ\text{C}$ $-40^\circ\text{C} < T_J < 125^\circ\text{C}$ | V_{PREF} | 2.42 2.40 | 2.50 – | 2.58 2.60 | V |
| PFC Feedback Voltage Reference Regulation with Line | $V_{CC(on)} + 0.2 \text{ V} < V_{CC} < 20 \text{ V}$ | $V_{PREF(line)}$ | –15 | – | 15 | mV |
| Error Amplifier Drive Capability | | | | | | μA |
| Sink | $V_{PControl} = 4 \text{ V}$, $V_{PFB} = 5 \text{ V}$ | $I_{EA(SNK)}$ | 60 | 80 | – | |
| Source | $V_{PControl} = 4 \text{ V}$, $V_{PFB} = 0.5 \text{ V}$ | $I_{EA(SRC)}$ | –60 | –80 | – | |
| Open Loop Error Amplifier Transconductance | $V_{PControl} = 4 \text{ V}$, $V_{PFB} = 2.4 \text{ V}$ and 2.6 V | G_m | 60 | 95 | – | μS |
| Feedback Input Pulldown Current Source | $V_{PFB} = 3 \text{ V}$ | I_{PFB} | 0.5 | 1.2 | 1.5 | μA |
| Error Amplifier Maximum Output Voltage | $I_{PControl} = 10 \mu\text{A}$ | $V_{EA(OH)}$ | 5.30 | 5.65 | 6.00 | V |
| Error Amplifier Minimum Output Voltage | $I_{PControl} = -10 \mu\text{A}$ | $V_{EA(OL)}$ | 2.10 | 2.25 | 2.40 | V |
| Error Amplifier Output Voltage Range | $V_{EA(OH)} - V_{EA(OL)}$ | ΔV_{EA} | 3.1 | 3.4 | 3.7 | V |

3. Resistor/capacitor parallel combination (39 pF || 20 k Ω) between drive pin and driver supply and between xDRVxx and GND pins.

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Table 4. ELECTRICAL CHARACTERISTICS (V_{HV} = open, V_{PFB} = 2.4 V, V_{PCS} = 0 V, V_{PZCD} = 5 V, $V_{PControl}$ = open, V_{CC} = 15 V, V_{PDRV} = open, V_{HDRVlo} = open, V_{HVS} = 0 V, V_{HDRVhi} = open, V_{HBoost} = 15 V, C_{OSC} = 2200 pF, C_{VREF} = 0.1 μ F, C_{PCT} = 1000 pF, for typical values T_J = 25°C, for min/max values, T_J is -40°C to 125°C, unless otherwise noted)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|-----------------|------------|--------|-----|-----|-----|------|
|-----------------|------------|--------|-----|-----|-----|------|

PFC CURRENT SENSE

| | | | | | | |
|----------------------------------|----------------------------------------|------------------|------|------|------|---------|
| Current Sense Threshold Voltage | | $V_{PCS(ILIM)}$ | 0.78 | 0.84 | 0.92 | V |
| Current Sense Input Bias Current | $V_{PCS} = 2\text{ V}$ | I_{PCS} | -1 | 0 | 1 | μ A |
| Leading Edge Blanking Duration | | $t_{PCS(LEB)}$ | 40 | 110 | 200 | ns |
| Propagation Delay | $V_{PCS} = V_{PCS(ILIM)} + 1\text{ V}$ | $t_{PCS(delay)}$ | - | 90 | 250 | ns |

PFC ZERO CURRENT DETECTION

| | | | | | | |
|------------------------|----------------------------------------------------|----------------------------------------|------------|------------|------------|---------|
| ZCD Threshold Voltage | V_{PZCD} increasing V_{PZCD} decreasing | $V_{ZCD(high)}$ $V_{ZCD(low)}$ | 1.9 1.3 | 2.1 1.5 | 2.3 1.7 | V |
| ZCD Voltage Hysteresis | | $V_{ZCD(HYS)}$ | 400 | 600 | 800 | mV |
| ZCD Input Bias Current | $V_{PZCD} = 1\text{ V}$ $V_{PZCD} = 5\text{ V}$ | $I_{PZCD(bias1)}$ $I_{PZCD(bias2)}$ | -1 -1 | - - | 1 1 | μ A |

PFC MAXIMUM OFF TIME

| | | | | | | |
|------------------|--|----------------|----|-----|-----|---------|
| Maximum Off Time | | $t_{PFC(off)}$ | 50 | 180 | 350 | μ s |
|------------------|--|----------------|----|-----|-----|---------|

PFC ON TIME RAMP GENERATOR

| | | | | | | |
|----------------------------------------------------------------------------------------|-----------------------------------------------------------------------|-------------------|-----|-----|-----|---------|
| ON time Capacitor Charge Current | $V_{PCT} = 0\text{ V}$ | $I_{PCT(C)}$ | 220 | 270 | 300 | μ A |
| On Time Capacitor Discharge Time | $C_{PCT} = 1\text{ nF}$, $V_{PCT} = 2.4\text{ V to }0.6\text{ V}$ | $t_{PCT(D)}$ | - | 70 | 300 | ns |
| ON Time Capacitor Peak Voltage | | $V_{PCT(peak)}$ | 2.6 | 3.0 | 3.4 | V |
| Minimum Duty Ratio | $V_{PFB} = 3.0\text{ V}$, $V_{PZCD} = 0\text{ V}$ | D_{PMIN} | 0 | - | - | % |
| Maximum On Time Detect Delay | $V_{PCT} = V_{PCT(peak)} + 1\text{ V}$ | $t_{PCT(delay)}$ | - | 250 | 375 | ns |
| Voltage Delta between PControl Voltage Needed to Generate PDRV Pulses and $V_{EA(OL)}$ | $\Delta V_{EA} - V_{PCT(peak)}$ | $V_{PCT(offset)}$ | 250 | 400 | 550 | mV |

PFC OVERVOLTAGE and UNDERVOLTAGE

| | | | | | | |
|-----------------------------------------|---------------------------------------------------------------------------|-------------------------------------|---------------------|---------------------|---------------------|----|
| Overvoltage Detector Threshold Voltage | Midpoint between high and low threshold, $V_{PControl} = 4\text{ V}$ | V_{POVP} | 1.03* V_{PREF} | 1.05* V_{PREF} | 1.07* V_{PREF} | V |
| Overvoltage Comparator Hysteresis | Between increasing and decreasing thresholds, $V_{PControl} = 4\text{ V}$ | $V_{POVP(HYS)}$ | 5 | 30 | 60 | mV |
| Propagation Delay | $V_{PFB} = V_{PREF} + 1\text{ V}$ | $t_{POVP(delay)}$ | - | 400 | 800 | ns |
| Undervoltage Detector Threshold Voltage | V_{PFB} increasing V_{PFB} decreasing | $V_{PUVP(high)}$ $V_{PUVP(low)}$ | - 175 | 290 230 | 350 - | mV |
| Undervoltage Comparator Hysteresis | V_{PFB} increasing | $V_{PUVP(HYS)}$ | 20 | 60 | 100 | mV |

PFC DRIVER

| | | | | | | |
|-------------------------------|---------------------------|------------------|-------|-------|------|----|
| PFC Driver Rise Time | 10% to 90% (Note 4) | $t_{PDRV(rise)}$ | - | 18 | - | ns |
| PFC Driver Fall Time | 90% to 10% (Note 4) | $t_{PDRV(fall)}$ | - | 9 | - | ns |
| PFC Driver High State Voltage | $I_{PDRV} = -8\text{ mA}$ | $V_{PDRV(OH)}$ | 14.00 | 14.55 | - | V |
| PFC Driver Low State Voltage | $I_{PDRV} = 8\text{ mA}$ | $V_{PDRV(OL)}$ | - | 0.12 | 0.50 | V |

4. Resistor/capacitor parallel combination (39 pF || 20 k Ω) between PDRV and driver supply and between PDRV and GND pins.

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Table 5. ELECTRICAL CHARACTERISTICS (V_{HV} = open, V_{PFB} = 2.4 V, V_{PCS} = 0 V, V_{PZCD} = 5 V, $V_{PControl}$ = open, V_{CC} = 15 V, V_{PDRV} = open, V_{HDRVlo} = open, V_{HVS} = 0 V, V_{HDRVhi} = open, V_{HBoost} = 15 V, C_{OSC} = 2200 pF, C_{VREF} = 0.1 μ F, C_{PCT} = 1000 pF, for typical values T_J = 25°C, for min/max values, T_J is -40°C to 125°C, unless otherwise noted)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|----------------------------------------------------------------|-----------------------------------------------------------------------|--------------------|------|------|-----|---------|
| HALF BRIDGE HIGH SIDE DRIVER | | | | | | |
| Half-Bridge High Side Driver Rise Time | 10% to 90% (Note 5) | $t_{HDRVhi(rise)}$ | – | 18 | – | ns |
| Half-Bridge High Side Driver Fall Time | 90% to 10% (Note 5) | $t_{HDRVhi(fall)}$ | – | 9 | – | ns |
| High State Voltage | $I_{HDRVhi} = -4$ mA | $V_{HDRVhi(OH)}$ | 14.0 | 14.7 | – | V |
| Low State Voltage | $I_{HDRVhi} = 4$ mA | $V_{HDRVhi(OL)}$ | – | 0.06 | 0.5 | V |
| High Side Driver Duty Ratio | 10 to 90% to 10% transitions, $V_{HVS} = 50$ V (Note 5) | $D_{HDRVhiMAX}$ | 44 | 48 | 50 | % |
| Boost Supply Undervoltage Threshold | | $V_{HBoost(UVLO)}$ | 4 | 6.1 | 8.0 | V |
| Boost Current Consumption | HDRVhi switching, between HDRVhi and HVS (Note 5) | $I_{CC(Boost)}$ | – | 0.1 | 0.5 | mA |
| HVS Leakage Current | $T_J = 25^\circ\text{C}$, $V_{HVS} = 600$ V, $V_{HBoost} = 600$ V | $I_{HVS(off)}$ | – | 0.1 | 1 | μ A |
| HALF BRIDGE LOW SIDE DRIVER | | | | | | |
| Half-Bridge Low Side Driver Rise Time | 10% to 90% (Note 5) | $t_{HDRVlo(rise)}$ | – | 18 | – | ns |
| Half-Bridge Low Side Driver Fall Time | 90% to 10% (Note 5) | $t_{HDRVlo(fall)}$ | – | 9 | – | ns |
| Half-Bridge Low Side Driver High State Voltage | $I_{HDRVlo} = -4$ mA | $V_{HDRVlo(OH)}$ | 14 | 14.7 | – | V |
| Half-Bridge Low Side Driver Low State Voltage | $I_{HDRVlo} = 4$ mA | $V_{HDRVlo(OL)}$ | – | 0.06 | 0.5 | V |
| Half-Bridge Low Side Driver Duty Ratio | 10 to 90% to 10% transitions (Note 5) | $D_{HDRVloMAX}$ | 44 | 48 | 50 | % |
| CROSSOVER DEAD TIME | | | | | | |
| Delay from HDRVlo high to low to HDRVhi low to high transition | $V_{HVS} = 50$ V | $t_{HDRVhi(h-l)}$ | 500 | 785 | 950 | ns |
| Delay from HDRVhi high to low to HDRVlo low to high transition | $V_{HVS} = 50$ V | $t_{HDRVlo(h-l)}$ | 500 | 785 | 950 | ns |

5. Resistor/capacitor parallel combination (39 pF || 20 k Ω) between drive pin and driver supply and between xDRVxx and GND pins.

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1901 is a combination of PFC and half-bridge resonant controllers optimized for off-line adapter applications. This device includes all the features needed to implement a highly efficient and small form factor adapter. It integrates a critical conduction mode (CrM) power factor correction (PFC) controller and half-bridge controller with a built-in 600 V driver. The half-bridge stage operates at a fixed frequency. Regulation is achieved by adjusting the PFC stage output voltage.

This device includes an enable input, open feedback loop protection and PFC overvoltage and undervoltage detectors. Other features included in the NCP1901 are a 600 V startup circuit and an adjustable frequency oscillator. The controllers are properly sequenced, simplifying system design.

Supply Sequencing

The PFC controller is enabled once V_{CC} reaches $V_{CC(on)}$ and the PFB voltage exceeds $V_{UVP(high)}$, typically 290 mV. Once the PFC controller is enabled the PControl pin begins to charge. Once the control voltage exceeds $V_{EA(OL)}$ the first PFC drive pulse is observed. The half-bridge driver is enabled once the first PFC drive pulse is generated. This ensures a monotonic output voltage rise as the input voltage to the half bridge stage is regulated.

The controller will not start in the event that V_{CC} falls below $V_{CC(MIN)}$ before PFB goes above $V_{UVP(high)}$. This ensures there is enough time to start the controller before V_{CC} reaches $V_{CC(off)}$.

Output Voltage Regulation

The half-bridge stage operates at a fixed frequency. Output voltage regulation is achieved by adjusting the half-bridge input voltage (PFC output voltage). The PFC output voltage is sensed using a resistor divider. The mid point of the resistor divider connects to the PFB pin. Subtracting current out of the feedback resistor divider increases the PFC output voltage and thus regulation is achieved.

High Voltage Startup Circuit

The NCP1901 internal startup regulator eliminates the need for external startup components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding. The startup regulator consists of a constant current source that supplies current from the high voltage line (V_{in}) to the supply capacitor on the V_{CC} pin (C_{CC}). The startup current (I_{start}) is typically 7.5 mA. The startup circuit is rated at a maximum voltage of 600 V.

Once C_{CC} is charged to 15.3 V ($V_{CC(on)}$), the startup regulator is disabled and the PFC controller is enabled if the PFB voltage exceeds $V_{PUVP(high)}$. The startup regulator

remains disabled until the lower supply threshold, $V_{CC(off)}$, (typically 9.3 V) is reached. Once reached, the drive outputs are disabled and the startup current source is enabled. Once the outputs are disabled, the bias current of the NCP1901 is reduced, allowing V_{CC} to charge back up.

The supply capacitor provides power to the controller while operating in the power up or self-bias mode. During the converter power up, C_{CC} must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the controller will turn off. The IC bias current and gate charge load at the drive outputs must be considered to correctly size C_{CC} . The increase in current consumption due to external gate charge is calculated using Equation 1.

$$I_{CC(gate\ charge)} = f \cdot Q_G \quad (eq. 1)$$

where, f is the operating frequency and Q_G is the gate charge of the external MOSFETs.

Main Oscillator

The oscillator frequency is set by the oscillator capacitor, C_{OSC} , on the OSC pin. The oscillator operates at a fixed 80% duty ratio. A current source charges C_{OSC} to its peak voltage, typically 5 V. Once the peak voltage is reached, the charge current is disabled and C_{OSC} is discharged down to 3 V by another current source. The charge and discharge currents are typically 173 and 692 μA , respectively. The oscillator frequency vs oscillator capacitance graph is shown in Figure 3.

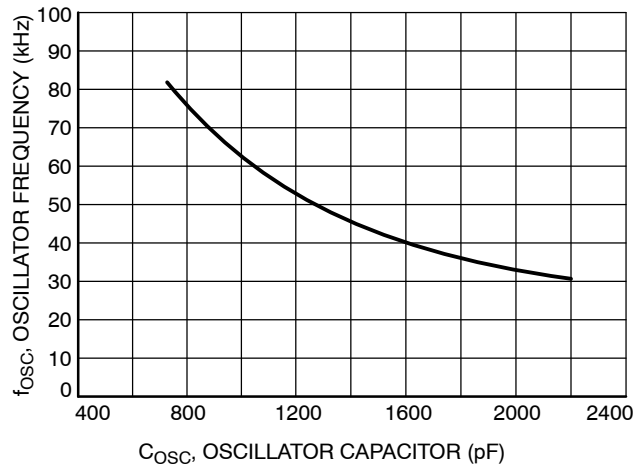


Figure 3. Oscillator Frequency vs. Oscillator Capacitor

An internal clock signal is generated dividing by two the oscillator frequency. This clock signal is used to control the half-bridge controller. The half-bridge duty ratio is limited to 50%. The PFC is not synchronized to the oscillator as it operates in CrM.

Voltage Reference

The internal voltage reference, V_{REF} is brought out of the controller to ease compensation requirements. The reference voltage is typically 7.0 V. A 0.1 μ F is required for stability. The reference should not be loaded with external circuitry.

PFC Regulator

The PFC stage operates in critical conduction mode (CrM). In CrM, the PFC inductor current, $I_L(t)$, reaches zero at the end of the switch cycle as shown in Figure 4. As seen in Figure 4, the average input current, $I_{in}(t)$, is in phase with the ac line voltage, $V_{in}(t)$.

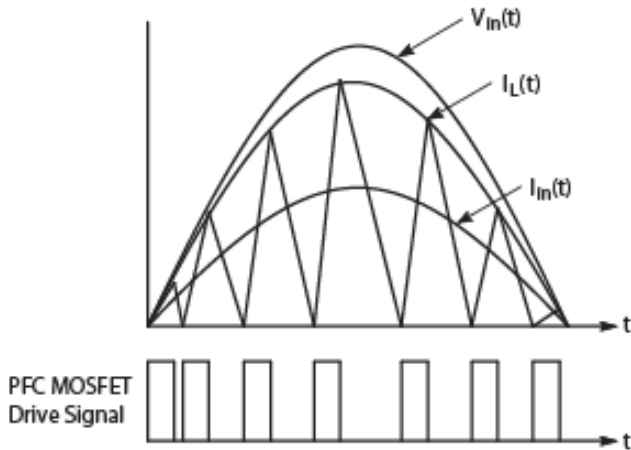


Figure 4. Inductor Current in CrM

High power factor is achieved in CrM by maintaining a constant on time (t_{on}) for a given RMS input voltage ($V_{ac(RMS)}$) and load conditions. Equation 2 shows the relationship between on time and system operating conditions.

$$t_{on} = \frac{2 \cdot P_{out} \cdot L}{\eta \cdot V_{ac(RMS)}^2} \quad (\text{eq. 2})$$

where, P_{out} is the output power, L is the PFC inductor inductance and η is the system efficiency.

On Time Control

The NCP1901 controls the on time by charging an external timing capacitor on the PCT pin, C_T , with a constant current source, $I_{PCT(C)}$. The C_T ramp is then compared to the control voltage, $V_{PControl}$. The control voltage is constant for a given RMS line voltage and output load, satisfying Equation 2. A voltage offset, $V_{PCT(offset)}$, is added to the C_T ramp to account for the control voltage range. The block diagram of the constant on time section is shown in Figure 5.

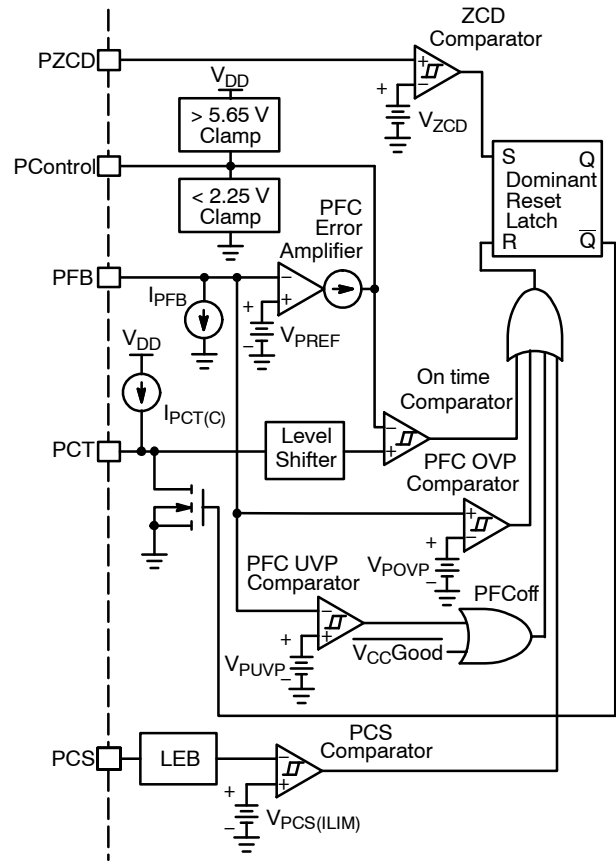


Figure 5. Constant On Time Control Block Diagram

The PControl voltage is internally clamped between 2.25 V and 5.65 V. An offset voltage greater than the minimum PControl clamp voltage is added to the C_T ramp prior to comparing it to the control voltage signal. This allows the PFC stage to stop the drive pulses (0% duty ratio) and regulate at light loads. The delta between the Pcontrol voltage needed to generate a PDRV pulse and the minimum PControl Clamp voltage is $V_{PCT(offset)}$.

The timing capacitor is discharged and held low once the C_T ramp voltage plus offset reaches $V_{PControl}$. The PFC drive pulse terminates once the C_T voltage reaches its peak voltage threshold, $V_{PCT(peak)}$. A new cycle starts once the inductor current reaches zero detected by a transition on the ZCD pin or the maximum off has been reached.

The timing capacitor is sized such that the C_T ramp peak voltage is reached at low line and full load. In this operating mode $V_{PControl}$ is at its maximum. Equation 3 is used to calculate the on time for a given C_T .

$$t_{on(MAX)} = \frac{C_T \cdot V_{PCT(MAX)}}{I_{PCT(C)}} \quad (\text{eq. 3})$$

Substituting t_{on} in Equation 2 with Equation 3 and rearranging Equation 4 provides a maximum value for C_T .

$$C_T \geq \frac{2 \cdot P_{out} \cdot L \cdot I_{PCT(C)}}{\eta \cdot V_{ac(RMS)}^2 \cdot V_{PCT(MAX)}} \quad (\text{eq. 4})$$

where, $V_{PCT(MAX)}$, is the maximum PCT voltage, typically 3.0 V.

Off Time Control

The PFC off time varies with the instantaneous line voltage and it is adjusted every cycle to allow the inductor current to reach zero before the next switch cycle begins. The inductor is demagnetized once its current reaches zero. Once the inductor is demagnetized the drain voltage of the PFC switch begins to drop. The inductor demagnetization is detected by sensing the voltage across the inductor using an auxiliary winding. This winding is commonly known as a zero crossing detector (ZCD) winding. This winding provides a scaled version of the inductor voltage. Figure 6 shows the ZCD winding arrangement.

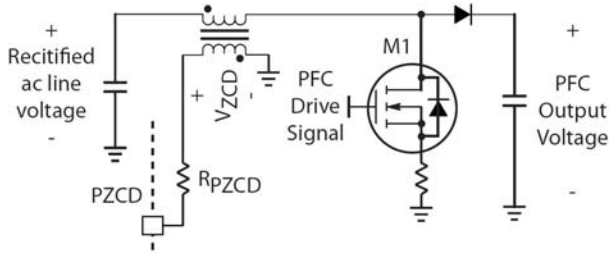


Figure 6. ZCD Winding Implementation

A negative voltage appears on the ZCD winding while the PFC switch is on. The PZCD voltage is positive while the PFC switch is off and current is flowing through the inductor. The PZCD voltage drops to and rings around zero volts once the inductor is demagnetized. Once a negative transition is detected in the PZCD pin the next switch cycle commences. A positive transition (corresponding to the PFC switch turn off) arms the ZCD detector to prevent false triggering. The arming of the ZCD detector is typically 2.1 V (V_{PZCD} increasing) and the triggering is typically 1.5 V (V_{PZCD} decreasing).

The PZCD pin is internally clamped to 10 V with a zener diode. A resistor in series with the ZCD pin is required to limit the current into the PZCD pin. The zener diode prevents the voltage from exceeding the 10 V clamp or going below ground. Figure 7 shows typical ZCD waveforms.

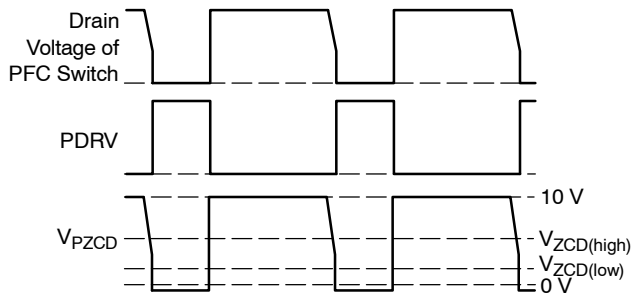


Figure 7. ZCD Winding Waveforms

During startup there are no ZCD transitions to enable the PFC switch. A watchdog timer enables the PFC controller if no switch pulses are detected for a period of 180 μ s (typical). The watchdog is also useful while operating at light load because the amplitude of the ZCD signal may be very small to cross the ZCD thresholds. The watchdog

timer is reset at the beginning of a PFC drive pulse and in a PFC undervoltage fault.

PFC Compensation

A transconductance error amplifier regulates the PFC output voltage, V_{PFC} , by comparing the PFC feedback signal to an internal 2.5 V reference. As shown in Figure 28 a resistor divider from the PFC output voltage consisting of R1 and R2 generates the PFC feedback signal.

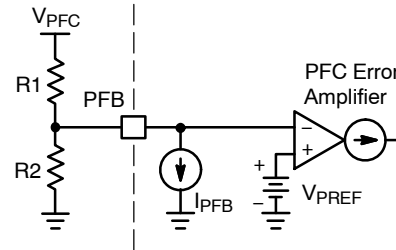


Figure 8.

The feedback signal is applied to the amplifier inverting input. The internal 2.5 V reference, V_{PREF} , is applied to the amplifier non-inverting input. The reference is trimmed during manufacturing to achieve an accuracy of $\pm 3.2\%$. Figure 5 shows the PFC error amplifier and sensing network. Equation 5 is used to calculate the values of the PFC feedback network.

$$V_{PFC} = V_{PREF} \cdot \frac{R_1 + R_2}{R_2} + I_{PFB} \cdot R_1 \quad (\text{eq. 5})$$

A transconductance amplifier has a voltage-to-current gain, gm. That is, the output current is controlled by the differential input voltage. The NCP1901 amplifier has a typical gm of 95 μ S. The PControl pin provides access to the amplifier output for compensation. The compensation network is ground referenced allowing the PFC feedback signal to be used to detect an overvoltage condition.

The compensation network on the PControl pin is selected to filter the bulk voltage ripple such that a constant control voltage is maintained across the ac line cycle. A capacitor between the PControl pin and ground sets a pole. A pole at or below 20 Hz is enough to filter the ripple voltage for a 50 and 60 Hz system. The low frequency pole, f_p , of the system is calculated using Equation 6.

$$f_p = \frac{g_m}{2\pi C_{PControl}} \quad (\text{eq. 6})$$

where, $C_{PControl}$ is the capacitor on the PControl pin to ground.

A key feature to using a transconductance type amplifier, is that the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of the feedback pin by the error amplifier and by the overvoltage comparator.

PFC Undervoltage

The NCP1901 safely disables the controller if the PFB pin is left open. An undervoltage detector disables the controller if the voltage on the PFB pin is below $V_{PUVP(low)}$, typically 0.23 V. A 1.2 μ A (typical) pull down current source, I_{PFB} , ensures V_{PFB} falls below $V_{PUVP(low)}$ if the PFB pin is floating. The PFB pull down current source affects the PFC output voltage regulation setpoint.

PFC Overvoltage

An overvoltage detector monitors the PFC feedback voltage and disables the PFC driver if the PFC output voltage is greater than 5% of its nominal value. PFC drive pulses are suppressed until the overvoltage condition is removed. The overvoltage detector tolerance is better than $\pm 2\%$ across the operating temperature voltage range. The overvoltage comparator hysteresis is typically 30 mV (1.2%).

PFC Overcurrent

The PFC current is monitored by means of an overcurrent detector. The PCS pin provides access to the overcurrent detector. The PFC drive pulse is terminated if the voltage on the PCS pin exceeds the overcurrent threshold, $V_{PCS(ILIM)}$. This comparison is done on a cycle by cycle basis. The overcurrent threshold is typically 0.84 V.

The current sense signal is prone to leading edge spikes caused by the power switch transitions. The NCP1901 has leading edge blanking circuitry that blocks out the first 110 ns (typical) of each current pulse.

PFC Driver

The PFC driver source and sink impedances are typically 60 and 15 Ω , respectively. Depending on the external MOSFET gate charge requirements, an external driver may be needed to drive the PFC power switch. A driver as the one shown in Figure 9 can be easily implemented.

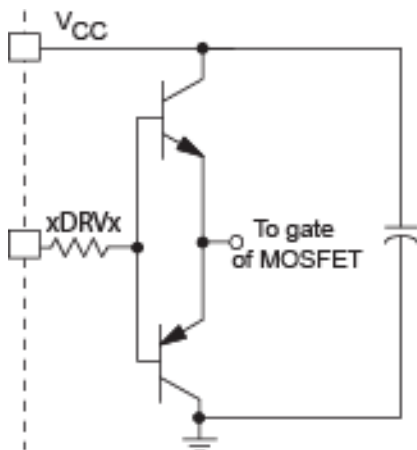


Figure 9. External Driver

Half-Bridge Driver

The half-bridge stage operates at a fixed 50% duty ratio. The oscillator frequency is divided by two before it is applied to the half-bridge controller.

The half-bridge controller has a low side driver, $HDRVlo$, and a 600 V high side driver, $HDRVhi$. The built in high voltage driver eliminates the need for an external transformer or dedicated driver. A built-in delay between each drive transition eliminates the risk of cross conduction. The delay is typically 785 ns. The typical duty ratio of each half-bridge driver is 48%.

The high side driver is connected between the HBoost and the HVS pins as shown in Figure 10.

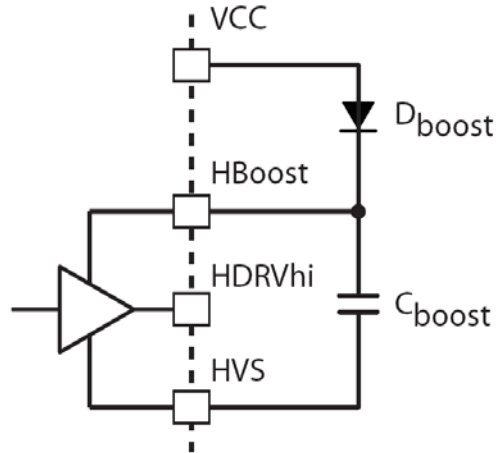


Figure 10. Half-bridge High Side Driver

A boost circuit comprised of D_{boost} and C_{boost} generates the supply voltage for the high side driver. Once $HDRVlo$ turns on, the HVS pin is effectively grounded through the external power switch. This allows C_{boost} to charge to V_{CC} . Once $HDRVlo$ turns off, HVS floats high and D_{boost} is reversed biased. An undervoltage detector monitors the HBoost voltage. Once the HBoost voltage is greater than $V_{Boost(UV)}$, typically, 6.1 V, the high side driver is enabled. The low side driver generally starts before the high side driver because the boost voltage is generated by the low side driver switch transitions.

The half-bridge low side driver source and sink impedances are typically 75 and 15 Ω , respectively. The half-bridge high side driver source and sink impedances are typically 75 and 15 Ω , respectively. Depending on the external MOSFETs gate charge requirements, an external driver may be needed to drive the low and high side power switches.

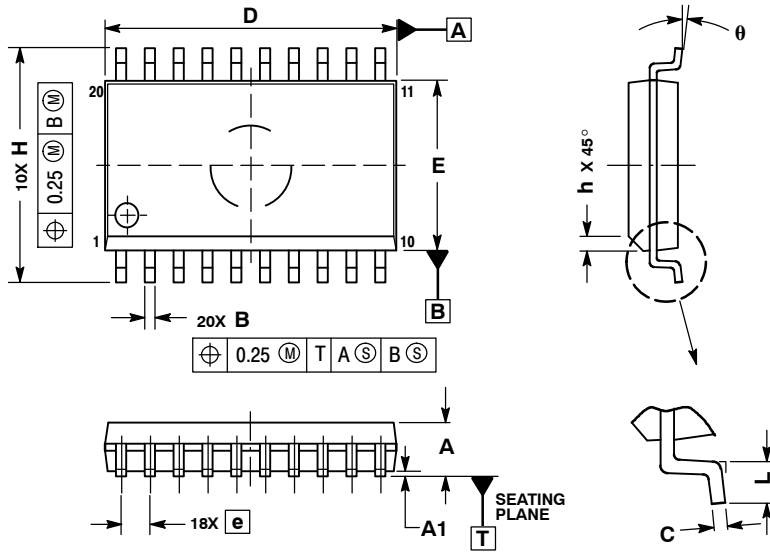
Analog and Power Ground

The NCP1901 has an analog ground, GND, and a power ground, PGND, terminal. GND is used for analog connections such as VREF and OSC. PGND is used for high current connections such as the gate drivers. It is recommended to have independent analog and power ground planes and connect them at a single point, preferably at the ground terminal of the system. This will prevent high current flowing on PGND from injecting noise in GND. The PGND connection should be as short and wide as possible to reduce inductance-induced spikes.

NCP1901

PACKAGE DIMENSIONS

SO-20 WB
CASE 751D-05
ISSUE G



NOTES:

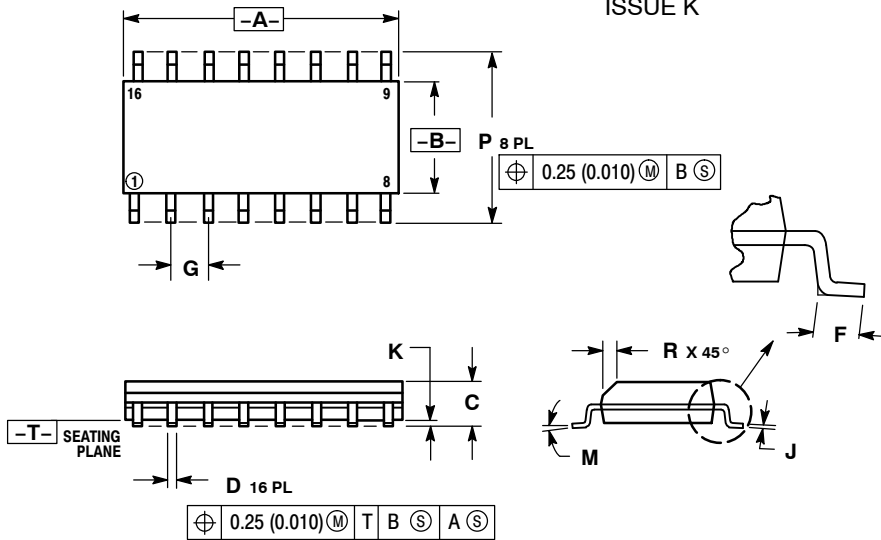
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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|----------|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

NCP1901

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

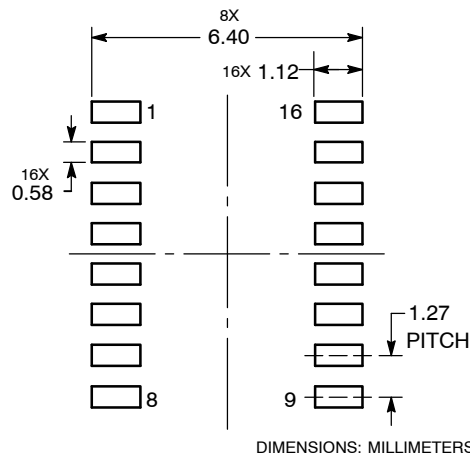


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| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT



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