Virtual Prototyping of Power Supply Designs

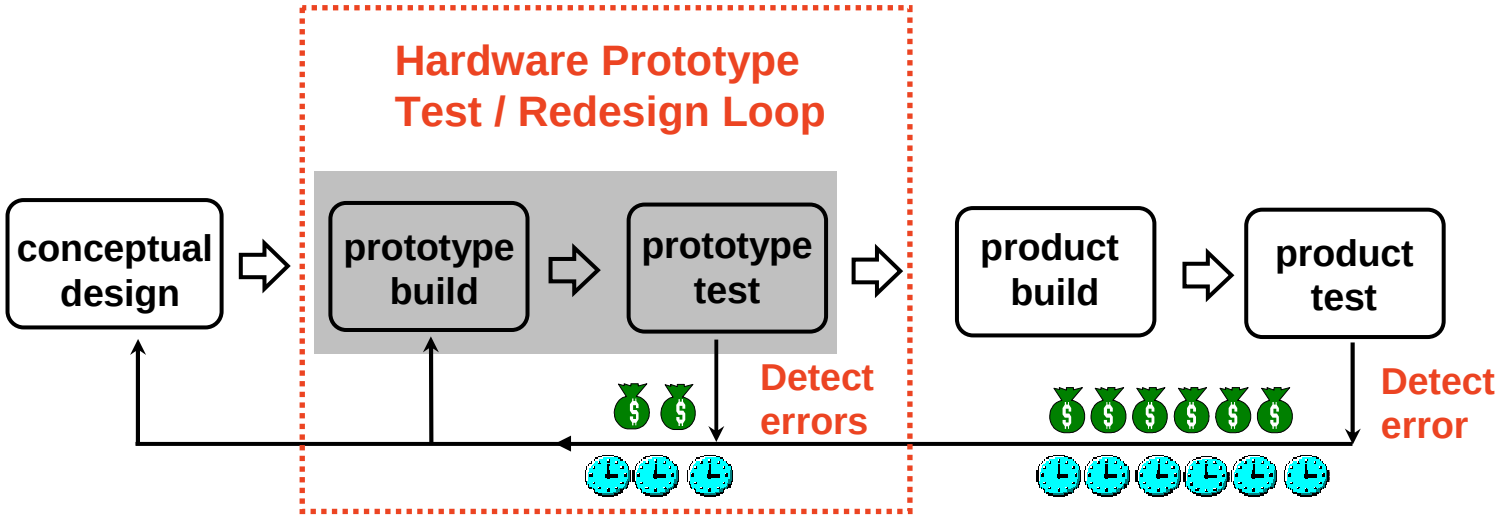
A Practical Guide to Using Circuit Simulation to Reduce Design Cycle Time

APEC 2010
Professional Education Seminar
Thomas G. Wilson, Jr.
SIMPLIS Technologies

SIMPLIS TECHNOLOGIES

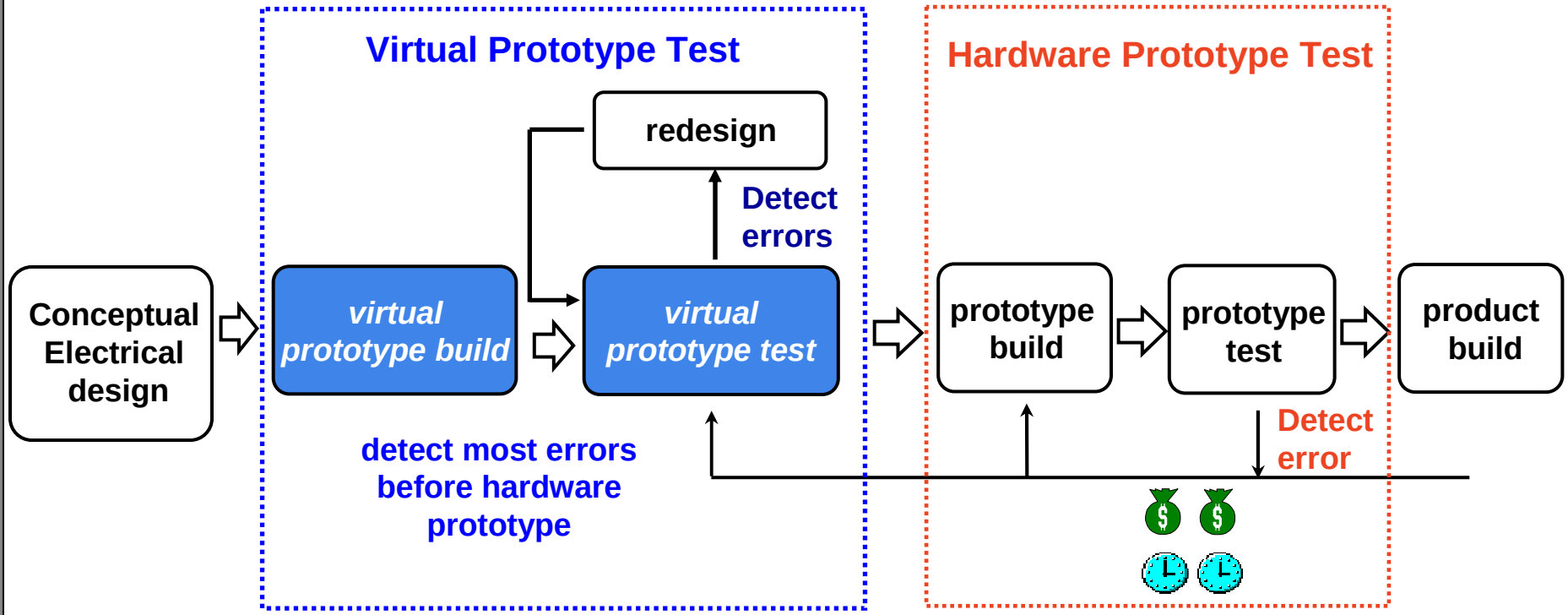
Simulation Software for Power Electronics
Component Design • Circuit Design • System Design

Hardware-Focused Product Development Procedure



SIMPLIS TECHNOLOGIES

Development Process with Virtual Prototype emphasis



Over 50% of all electrical design errors
can be detected by Virtual Prototyping Process
No other single design improvement can achieve more than 2% design error reduction

SIMPLIS TECHNOLOGIES

Virtual Prototyping of Power Supply Designs

- Cost of Design Changes increasing
  - Design Changes delay time to profitable manufacture
  - All Design Changes consume valuable New Product delivery capacity
- Cost of Hardware Iterations increasing
  - Time to market requirements are shrinking
  - As size of power supplies shrink, $$ cost of additional hardware iterations increases
- Cost of correcting Design Errors increases dramatically the later they are discovered in the process

SIMPLIS TECHNOLOGIES

Virtual Prototyping of Power Supply Designs

- Electrical Design Error
  - Design fails to meet design requirements necessitating a design ***change*** after first hardware prototype
- Design “Failure”
  - Electrical Design fails to meet design requirements necessitating an ***additional hardware iteration***

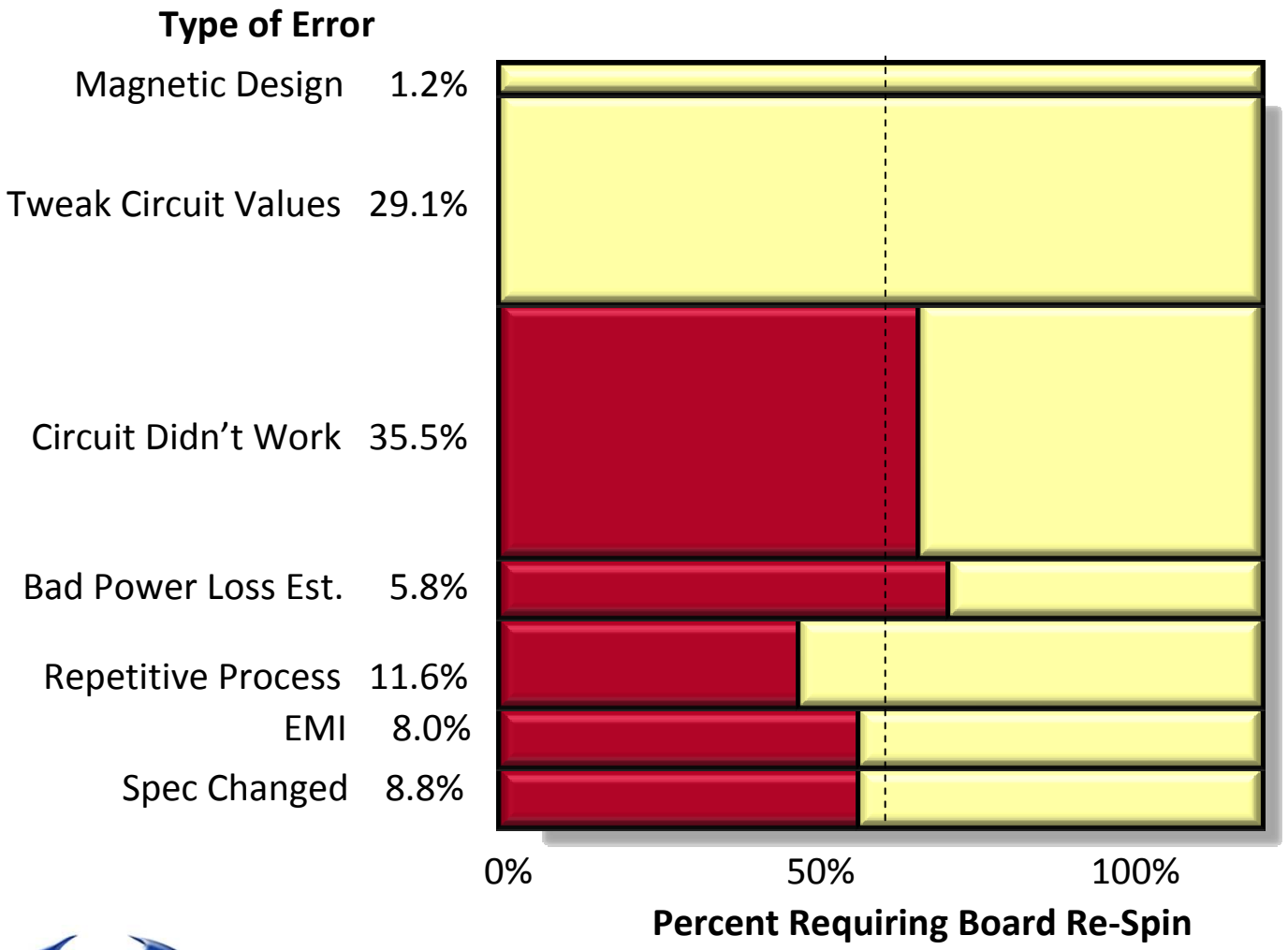
SIMPLIS TECHNOLOGIES

Power Supply Electrical Design Errors

- The following data is the result of in-depth studies of five large design organizations at three major manufacturers of custom and standard power supplies.
- All engineering change orders during the study period (6 to 9 months) were evaluated to determine the nature of the change, whether or not it resulted in a PCB spin, and whether or not it could have been detected with simulation.

SIMPLIS TECHNOLOGIES

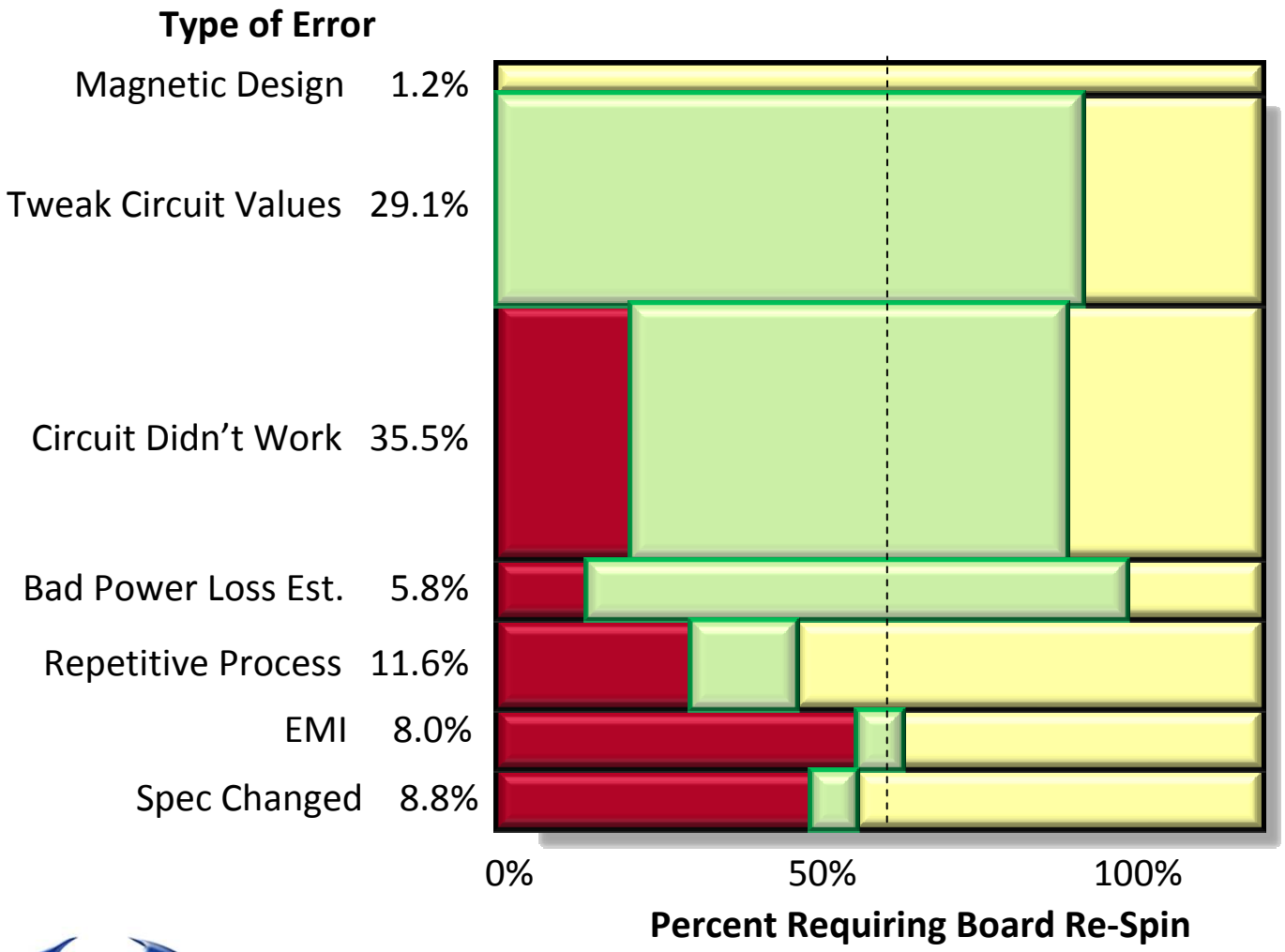
Survey of PS Electrical Design Errors



34% of all design errors in the study required a new PCB spin.

SIMPLIS TECHNOLOGIES

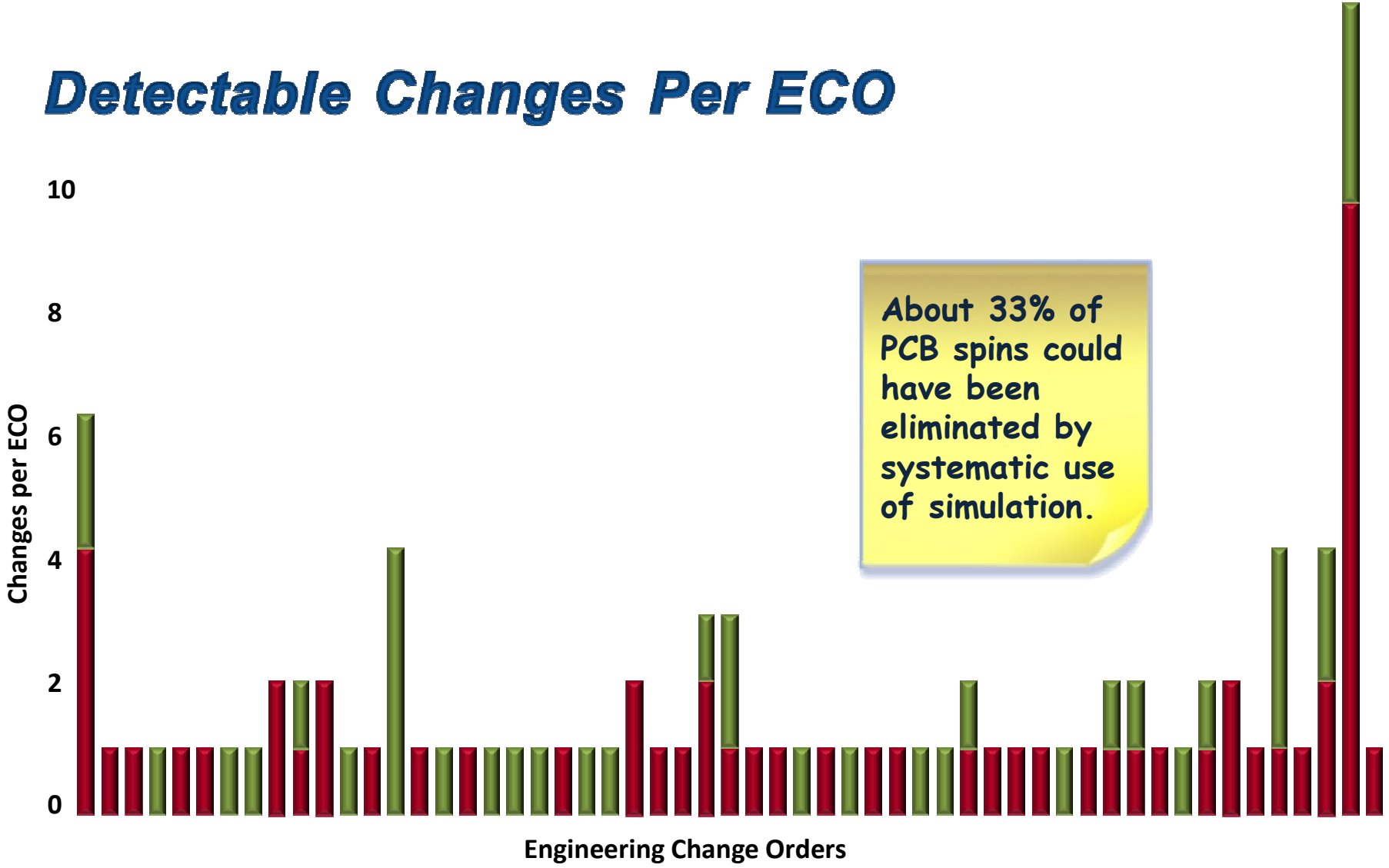
Errors Detectable by Simulation



SIMPLIS could detect 51% of all errors and 56% of errors that required a board spin.

SIMPLIS TECHNOLOGIES

Detectable Changes Per ECO



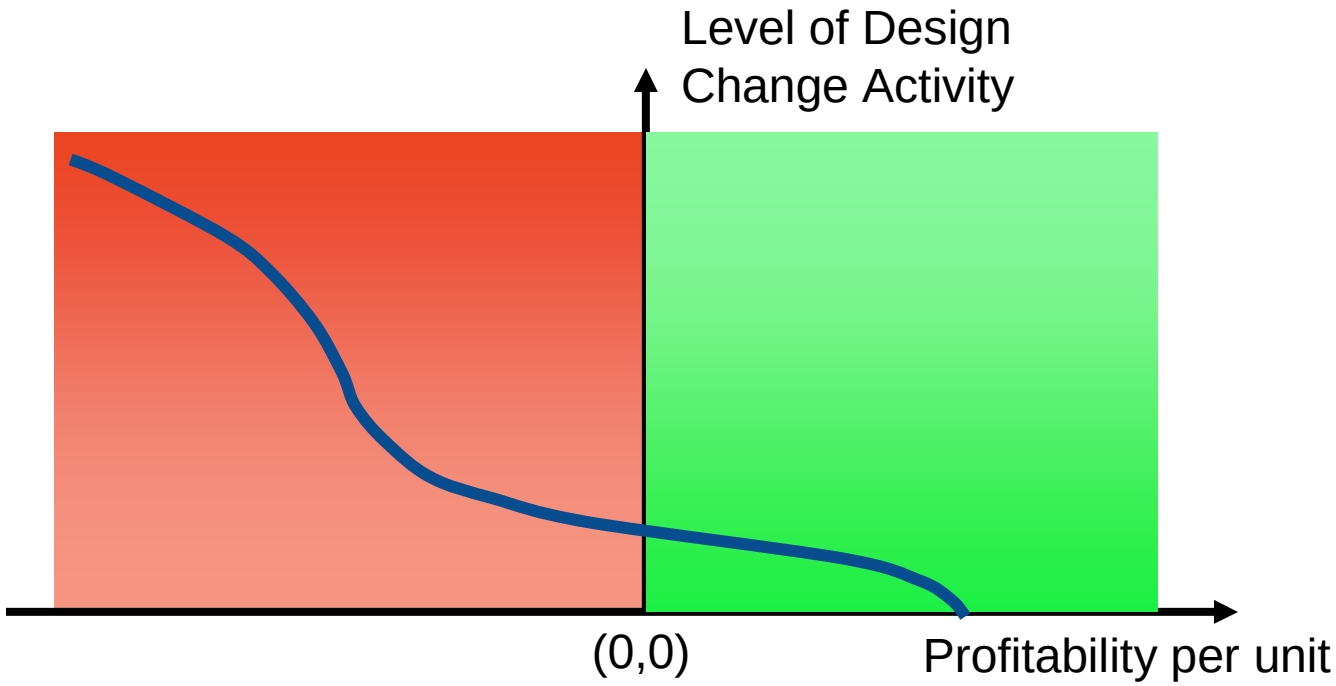
SIMPLIS TECHNOLOGIES

Virtual Prototyping of Power Supply Designs

- Virtual Prototyping Objective
  - Reduce number of latent design errors that are left to be discovered in prototype hardware
    - Reduce number of hardware iterations required to meet design requirements
      - Reduce time before design can be profitably manufactured
  - **Get design into profitable manufacture as soon as possible**

SIMPLIS TECHNOLOGIES

Virtual Prototyping Objective



As a rolling stone gathers no moss,
so a churning design gathers no profits

SIMPLIS TECHNOLOGIES

Virtual Prototyping of Power Supply Designs

Virtual Prototypes will not replace Hardware Prototypes in any reasonable planning horizon, so why bother?

- Benefits of reducing hardware iterations
  - Reduce time to profitable design
  - Reduce development cost
  - Increase effective development capacity
- No other single process improvement comes within an order of magnitude of this level of benefit

SIMPLIS TECHNOLOGIES

Survey -- Time to valuable simulation results

- If you could identify 50% of your latent design errors via simulation before 1st prototype, would you spend
    - 5 minutes
    - 5 hours
    - 5 days
    - 5 weeks
    - 5 months

  on simulation?

SIMPLIS TECHNOLOGIES

Virtual Prototyping – why now?

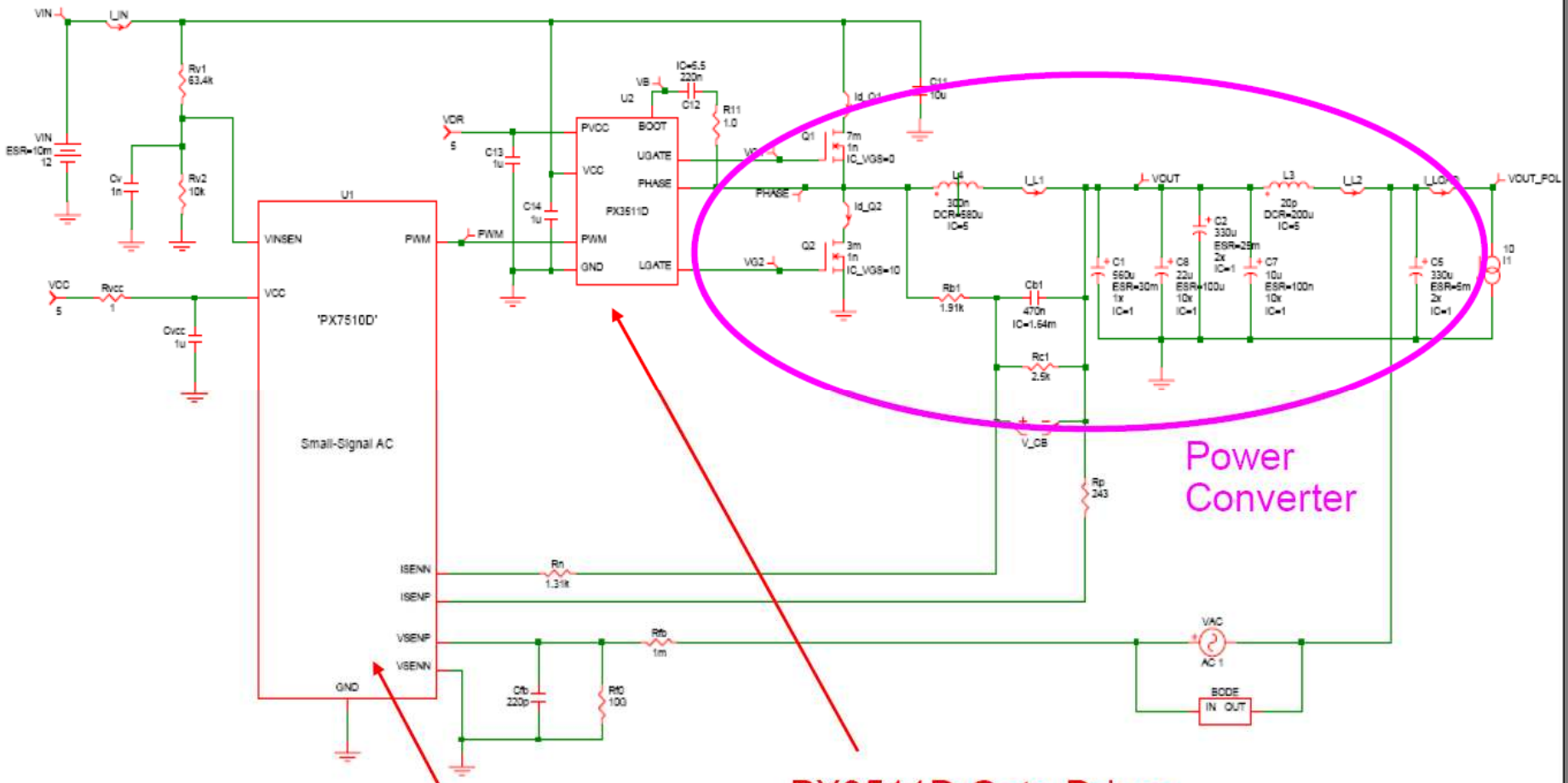
- Costs of failure rising sharply
  - $$
  - Time
- Costs of simulation have fallen
  - $$
  - Time
    - ***Time to valuable simulation results has fallen below critical threshold in many applications***

SIMPLIS TECHNOLOGIES

D14.1 - D14.4

Time-Domain Simulation Model

SIMPLIS Simulation Circuit & IC Model



primarion
Infineon Digital Power

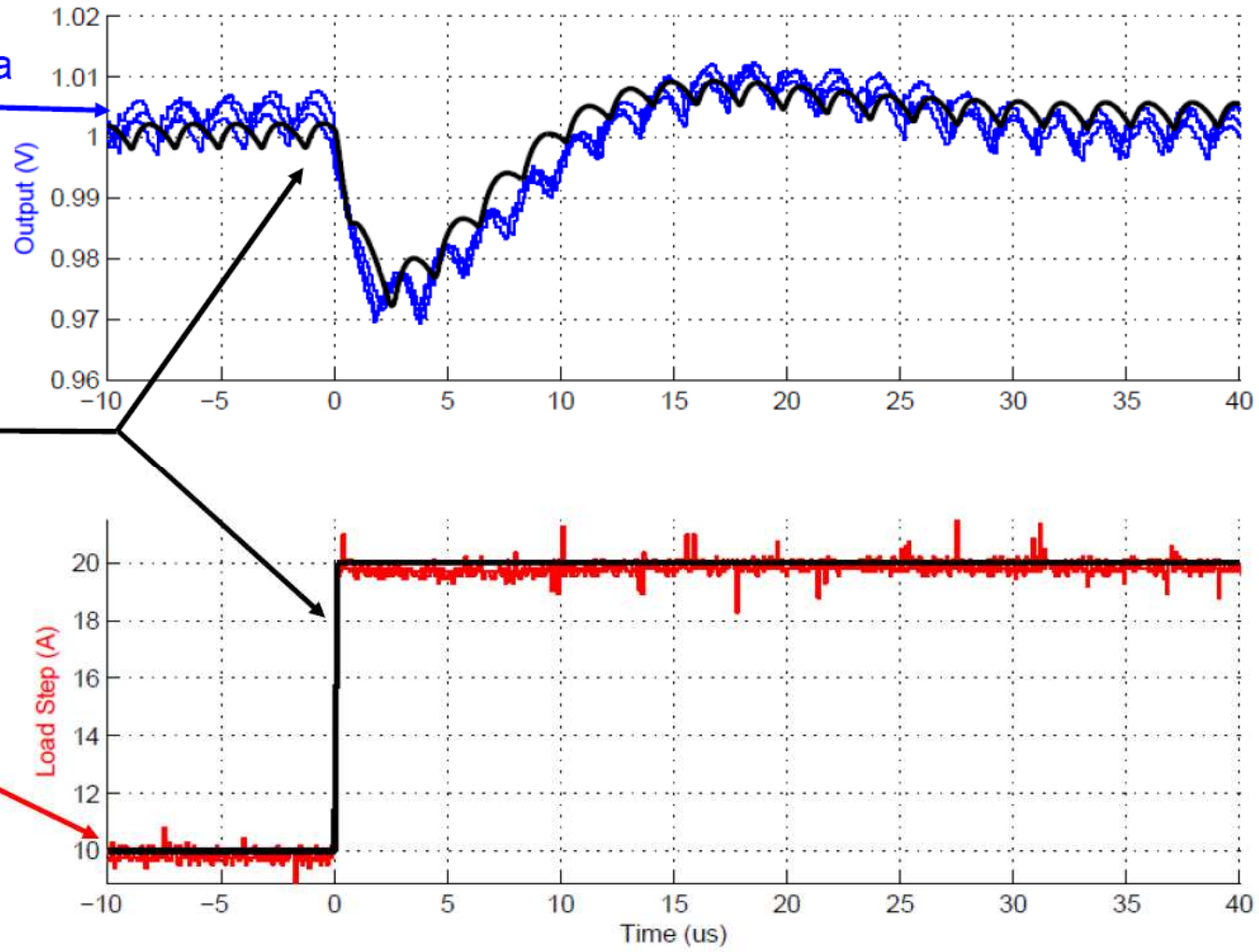
SIMPLIS TECHNOLOGIES

Time-Domain Simulation vs. Experimental Results

Output Voltage
Imported Scope Data
3 Traces

SIMPLIS™
Simulation Model

10 A to 20 A
Load Step
A 10 A Step
with a 10 A
Static Load



primarion
Infineon Digital Power

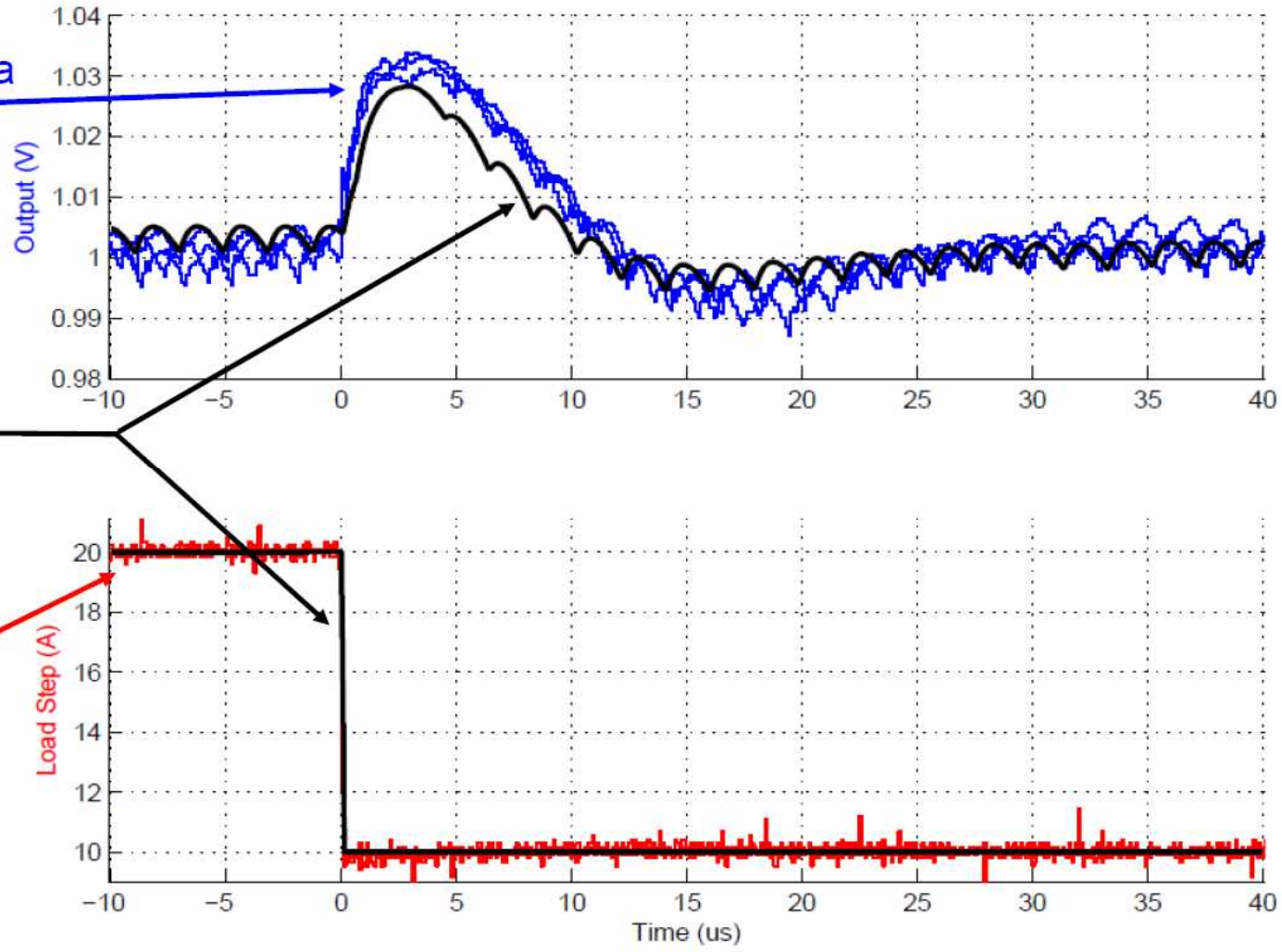
SIMPLIS TECHNOLOGIES

Time-Domain Simulation vs. Experimental Results

Output Voltage
Imported Scope Data
3 Traces

SIMPLIS™
Simulation Model

20 A to 10 A
Load Step
A 10 A Step
with a 10 A
Static Load

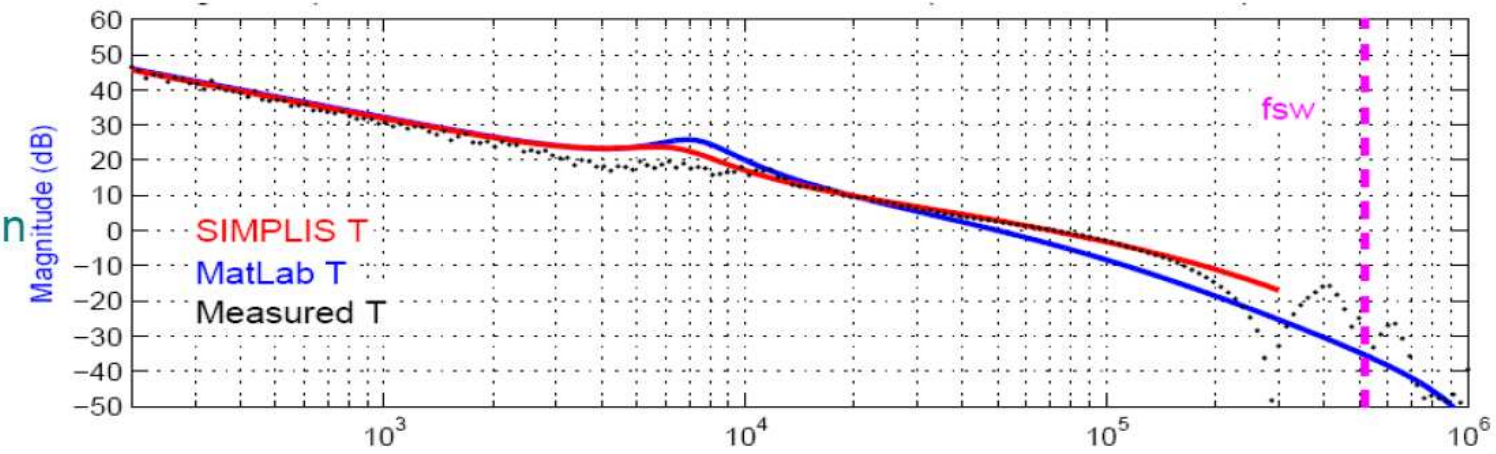


primarion
Infineon Digital Power

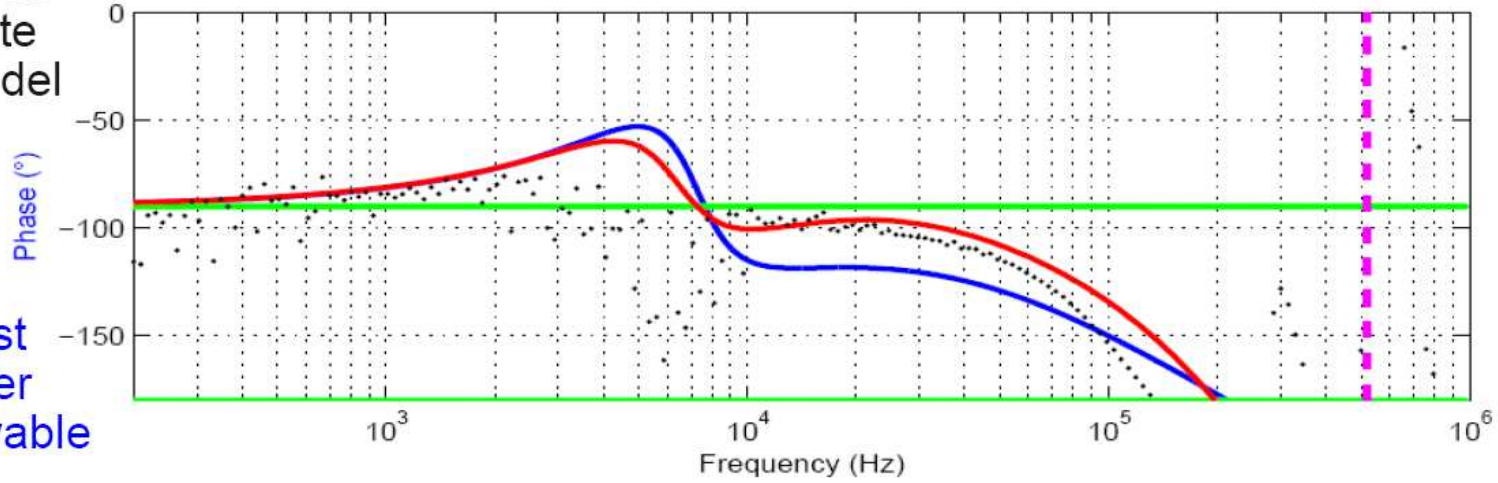
SIMPLIS TECHNOLOGIES

Frequency-Domain Comparison: Complex Zeroes

This is a more aggressive design



The MatLab model shown here uses a more accurate digital loop model

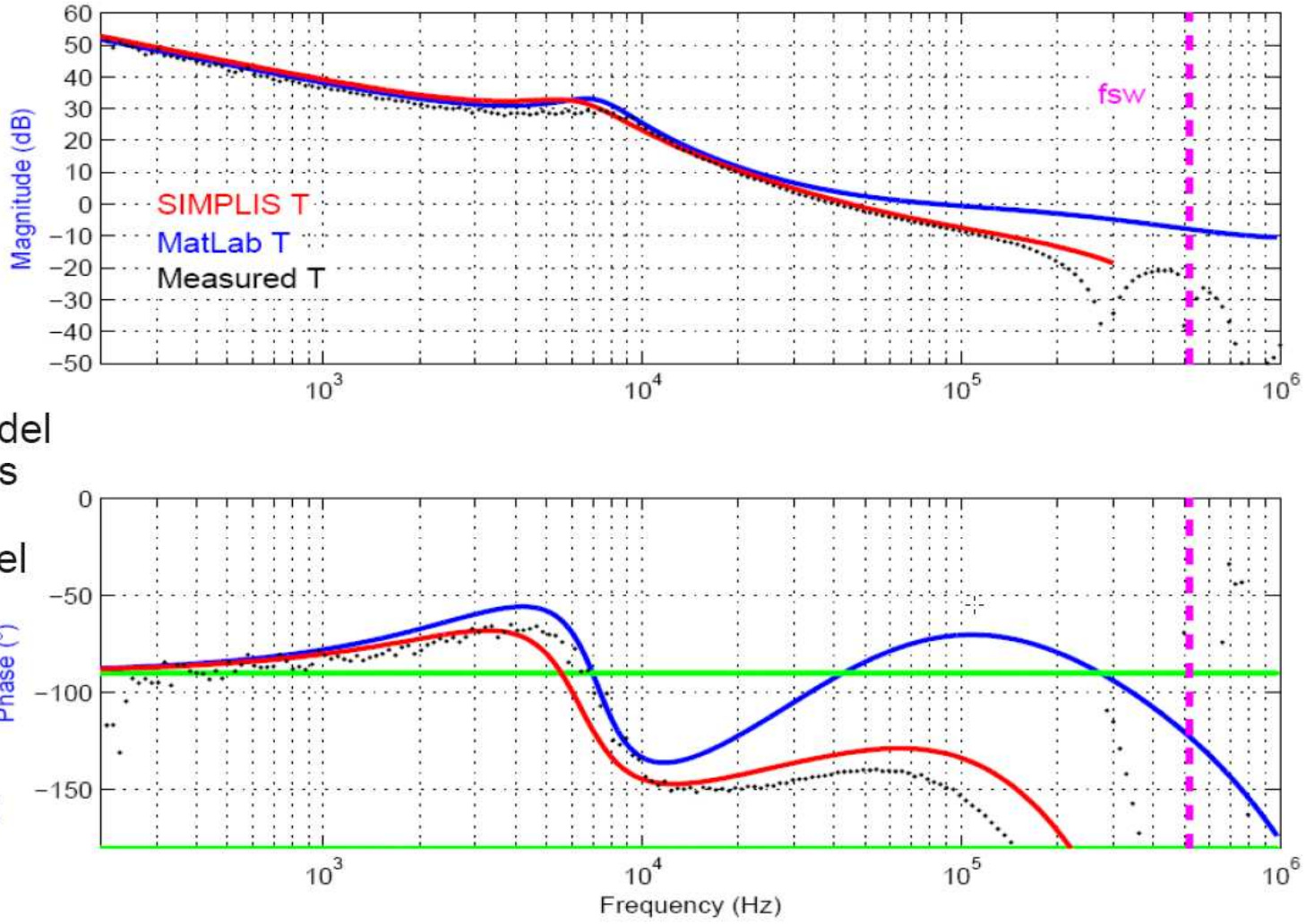


More phase boost throughout, higher crossover achievable

primarion
Infineon Digital Power

SIMPLIS TECHNOLOGIES

Frequency-Domain Comparison: Real Zeroes



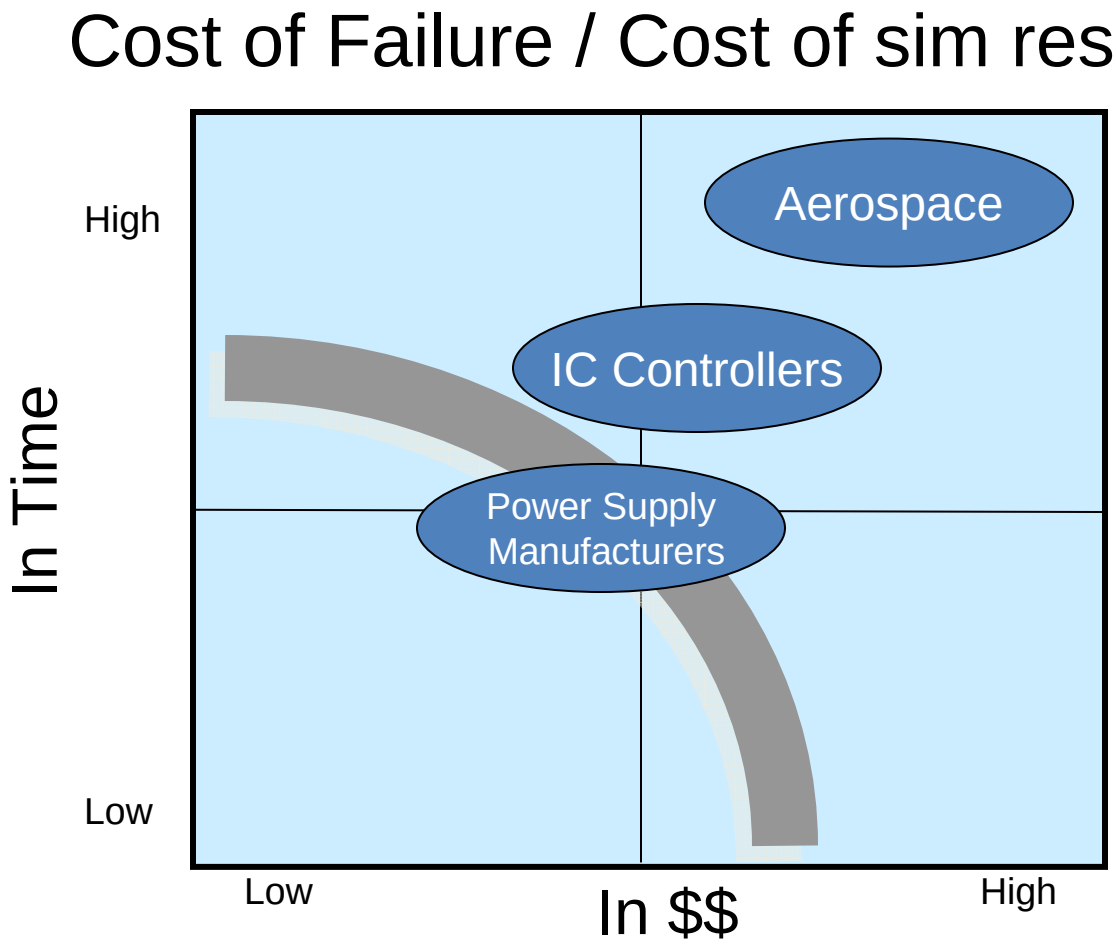
The MatLab model shown here uses a simplified digital loop model

Both the gain and phase are less accurate at the higher frequencies

primarion
Infineon Digital Power

SIMPLIS TECHNOLOGIES

Pain Threshold – when does Virtual Prototyping make sense?



SIMPLIS TECHNOLOGIES

Virtual Prototyping of Power Supply Designs

- Seminar Objective:
  - Provide practical guidance on how to use circuit simulation to detect more Design Errors sooner before they get committed to next hardware iteration
  - Virtual Prototyping
    - Illustrate current capabilities
    - Outline critical success factors
    - Discuss future directions

SIMPLIS TECHNOLOGIES

Different Analysis Types – Definitions

- Periodic Operating Point Analysis
- AC Analysis
- Transient Analysis

SIMPLIS TECHNOLOGIES

Periodic Operating Point (POP) Analysis – What is it?

- POP Analysis finds the steady-state Limit Cycle or the Periodic Operating Point of a periodically switching system
- POP Analysis works on full nonlinear switching time-domain model of circuit
- POP Analysis is typically much faster than running a long time-domain transient

SIMPLIS TECHNOLOGIES

Periodic Operating Point (POP) Analysis – How it works

- Takes snapshot of all inductor currents and capacitor voltages at beginning of a conversion cycle
- Simulates in time domain one conversion cycle
- Takes another snapshot of all inductor currents and capacitor voltages at beginning of next conversion cycle
- Looks at the normalized difference of all capacitor voltages and inductor currents and tries to find a set of initial conditions that will drive this difference to zero
- Will stop when difference diminishes to ~ 10^{-9} %
  - This is miniscule when compared to a Spice rel tol of 10^{-3}

SIMPLIS TECHNOLOGIES

D.24.5

Why Periodic Operating Point (POP) Analysis can fail (in order of frequency)

- Circuit is not stable
- Initial conditions are too far away from steady-state limit cycle
- POP Trigger is not connected to a proper node so that a trigger signal is generated once every complete conversion cycle
- POP analysis settings constrain the analysis so that
  - Max Period is less than conversion period
  - Max Period is much too large
  - Number of POP iterations is too small

SIMPLIS TECHNOLOGIES

POP Analysis enables AC analysis

- Because POP error is so small, we can inject a very small AC signal into a feedback loop and measure a valid small signal AC response – ***in the time domain*** – with very high accuracy
- Level of injected AC signal is automatically controlled to keep AC response of nonlinear circuit in its "linear" small signal region
- AC analysis is performed on full nonlinear time-domain switching model – ***no averaged model required***

SIMPLIS TECHNOLOGIES

D.24.5

Virtual Prototyping of Power Supply Designs

- We will look at Virtual Prototyping Process
  - From 3 Perspectives:
    - Power Supply Designer 90 min
    - Power Management IC Architect 40 min
    - Power System Designer 15 min

  Since all three do power supply design, we will spend ~ 50% our time in that area

SIMPLIS TECHNOLOGIES

Keys to making Virtual Prototyping Practical

- Piecewise Linear (PWL) Modeling & Simulation
  - Enables required speed and accuracy
- Clear & Focused Simulation Strategy
  - Always clear about ***simulation objective***
    - Includes quantities to be measured and required accuracy
  - Aware of required ***level of device modeling*** to achieve simulation objectives
    - **This is where engineers are most likely to fail to achieve benefits of Virtual Prototyping**

SIMPLIS TECHNOLOGIES

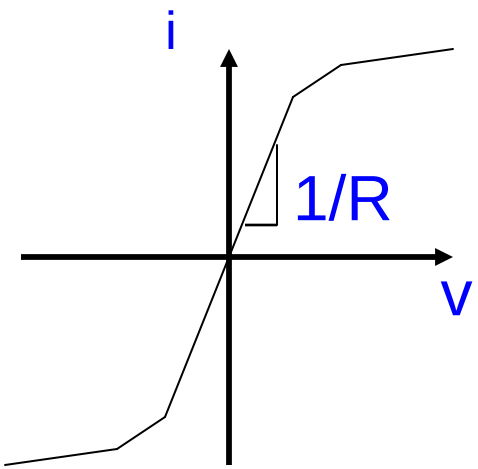
Piecewise Linear Modeling and Simulation

- Simulation Speed ~ 10 – 50 X faster than Spice
- Convergence is qualitatively better than Spice for switching power supplies
- Simulation Speed and Convergence performance dramatically increase the practical scope of power supply designs that can benefit from Virtual Prototyping
-
- To achieve required accuracy, multi-level modeling is managed according to simulation objective

SIMPLIS TECHNOLOGIES

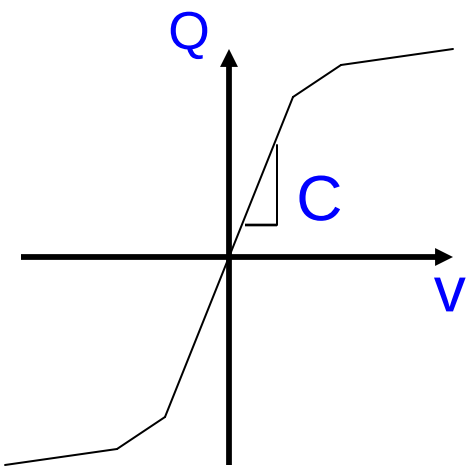
Piecewise Linear Components

Resistors



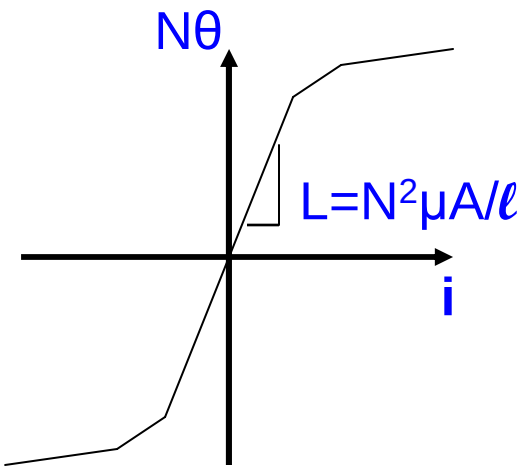
x-value → Voltage
y-value → Current

Capacitors



x-value → Voltage
y-value → Charge

Inductors

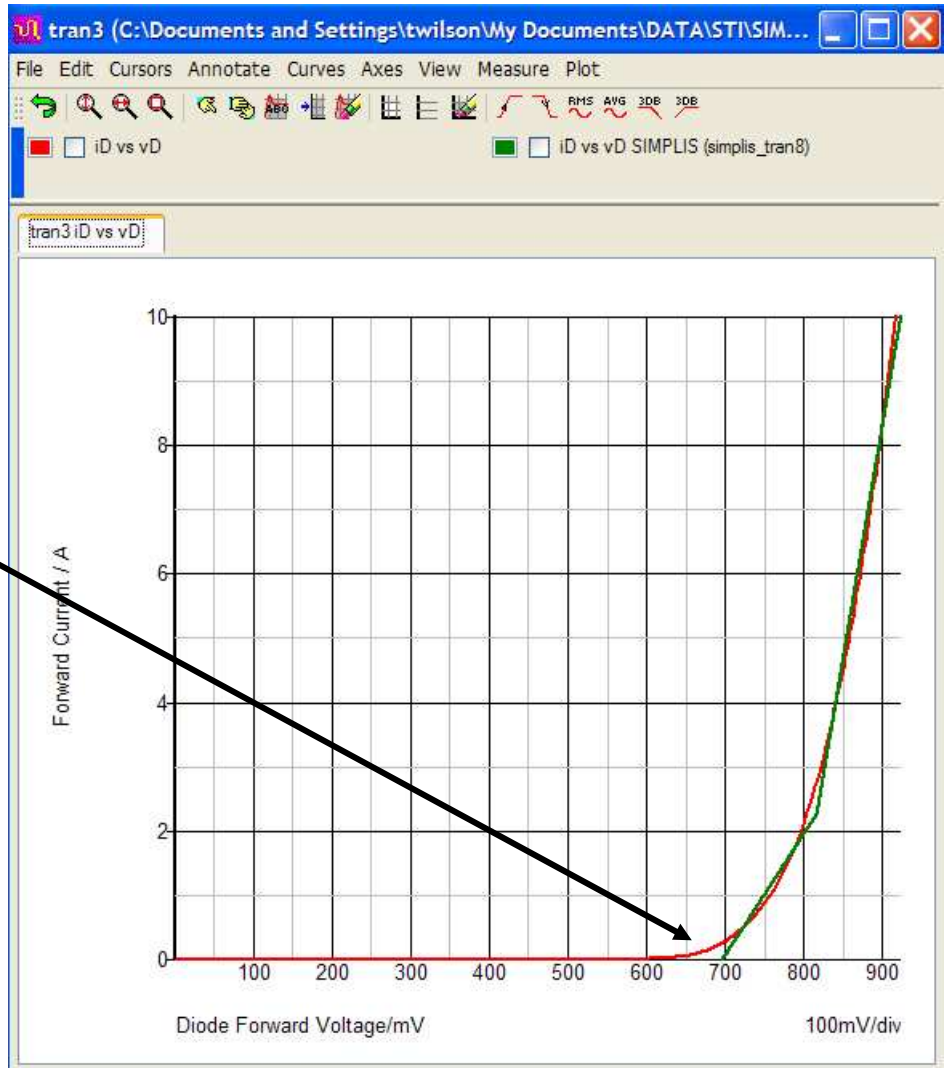


x-value → Current
y-value → Flux Linkages

SIMPLIS TECHNOLOGIES

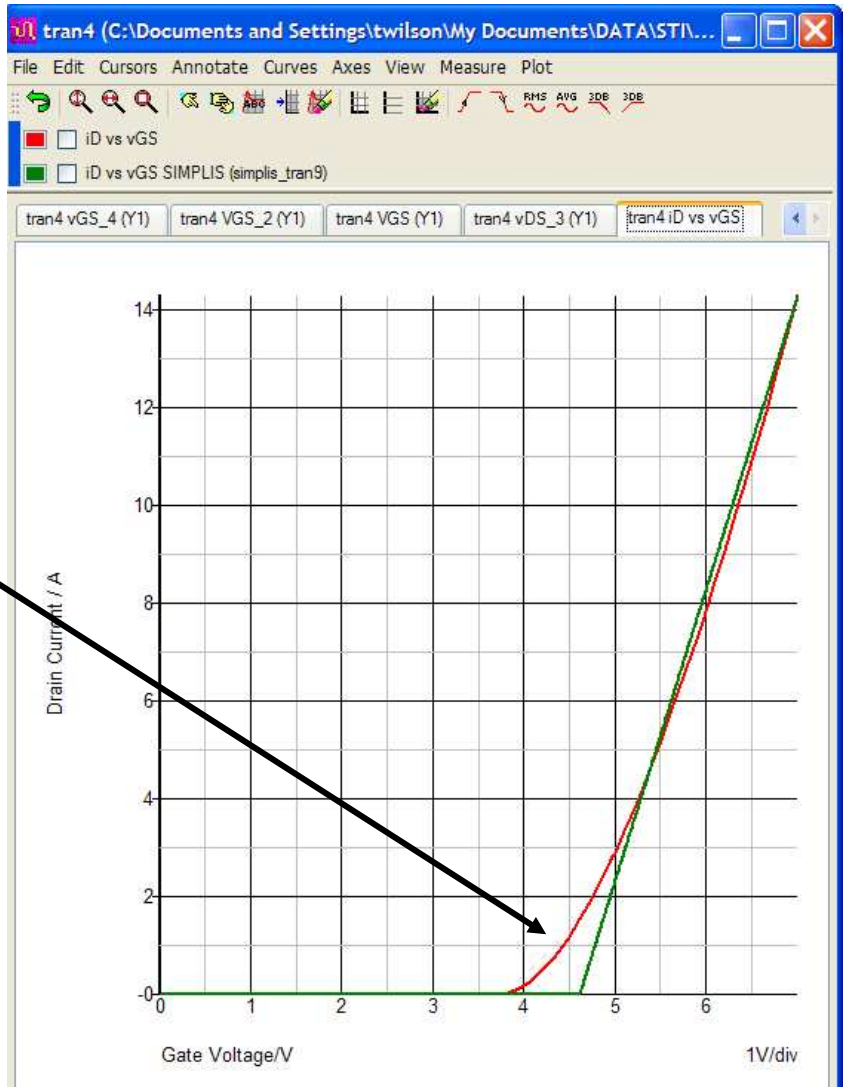
Diode PWL Model

- Three-segment SIMPLIS diode model (green)
- Compared to Spice model (red)
- Fit optimized over 4A – 8A range



FET PWL Model

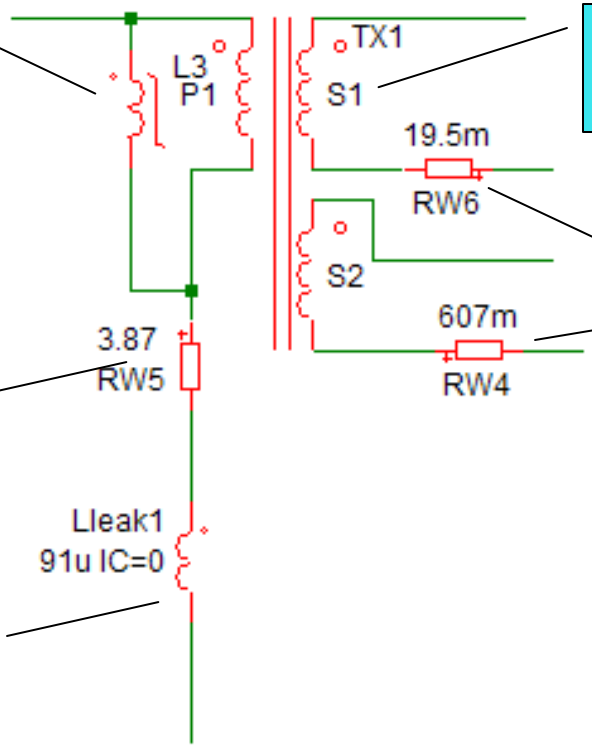
- Two-segment SIMPLIS iD vs. vGS (green)
- Compared to Spice model (red)
- Fit optimized over 33% - 100% of Imax



SIMPLIS TECHNOLOGIES

PWL Transformer model

PWL Inductor
for primary magnetizing inductance – includes any saturation effects



Ideal DC Transformer
(infinite magnetizing inductance)

Secondary winding resistance

Primary winding resistance

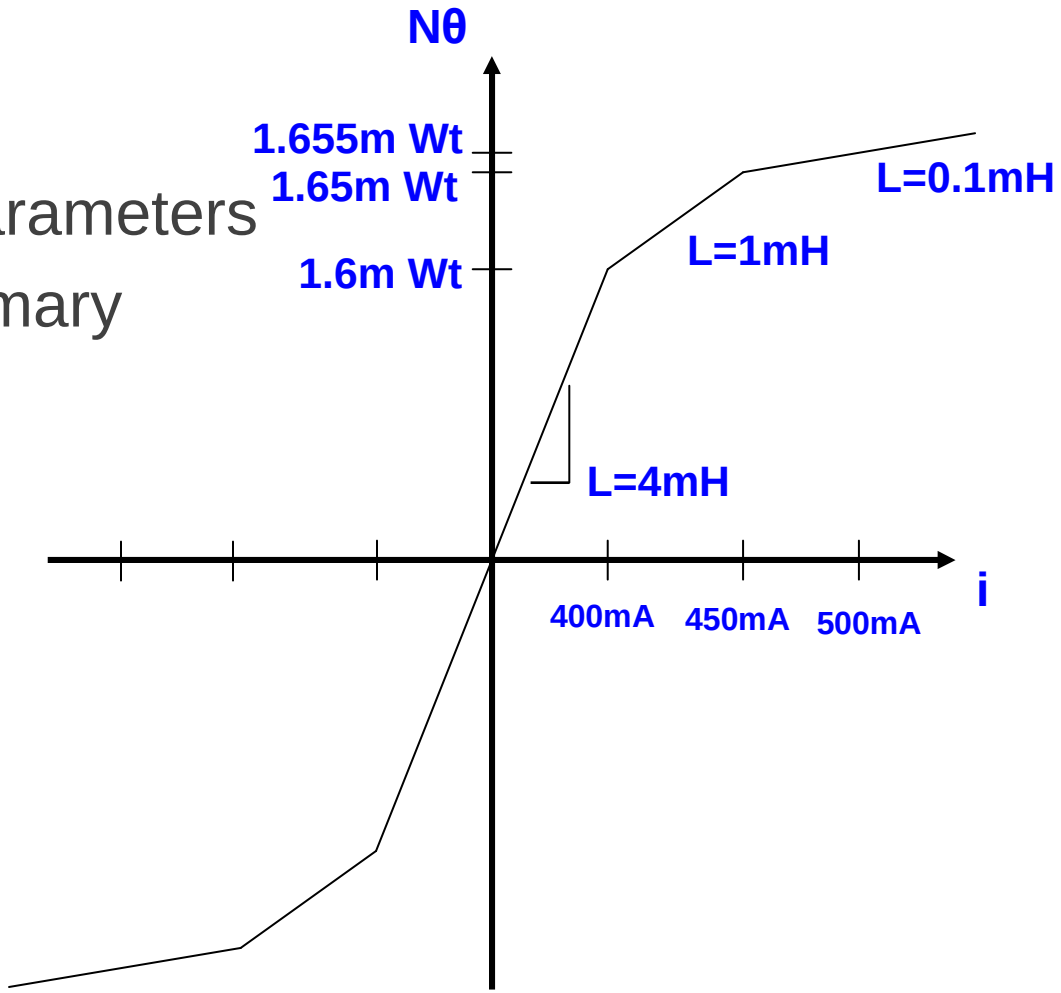
Primary leakage inductance

SIMPLIS TECHNOLOGIES

Saturable Inductor (PWL Inductor)

- Use the following parameters for the saturable primary inductance

- Run simulation.
- Confirm expected saturation at about 400mA



D.24.5

Model Accuracy

- **Accuracy of Physics:** the Physics behind the equations that describe semiconductors
  - Spice - very accurate
  - SIMPLIS – piecewise linear behavioral approximations
- **Accuracy of Parameters:** the value of the constants used in the model
  - Spice – mere mortals cannot typically create their own Spice models
  - SIMPLIS – models are based on data sheet info and can be created by average user in ~20 minutes
- **Accuracy of solution of circuit equations:**
  - Spice – in order to get practical speed, Spice must accept more numerical error (RelTol) per computational step
  - SIMPLIS – takes advantage of piecewise linear system to get extremely accurate numerical solutions of circuit equations

SIMPLIS TECHNOLOGIES

Simulation Accuracy vs. Simulation Time

- What is necessary to achieve required accuracy within reasonable simulation times?
  - PWL modeling and simulation -- Speed
  - Multi-level modeling – Accuracy
  - Clear Simulation Objectives

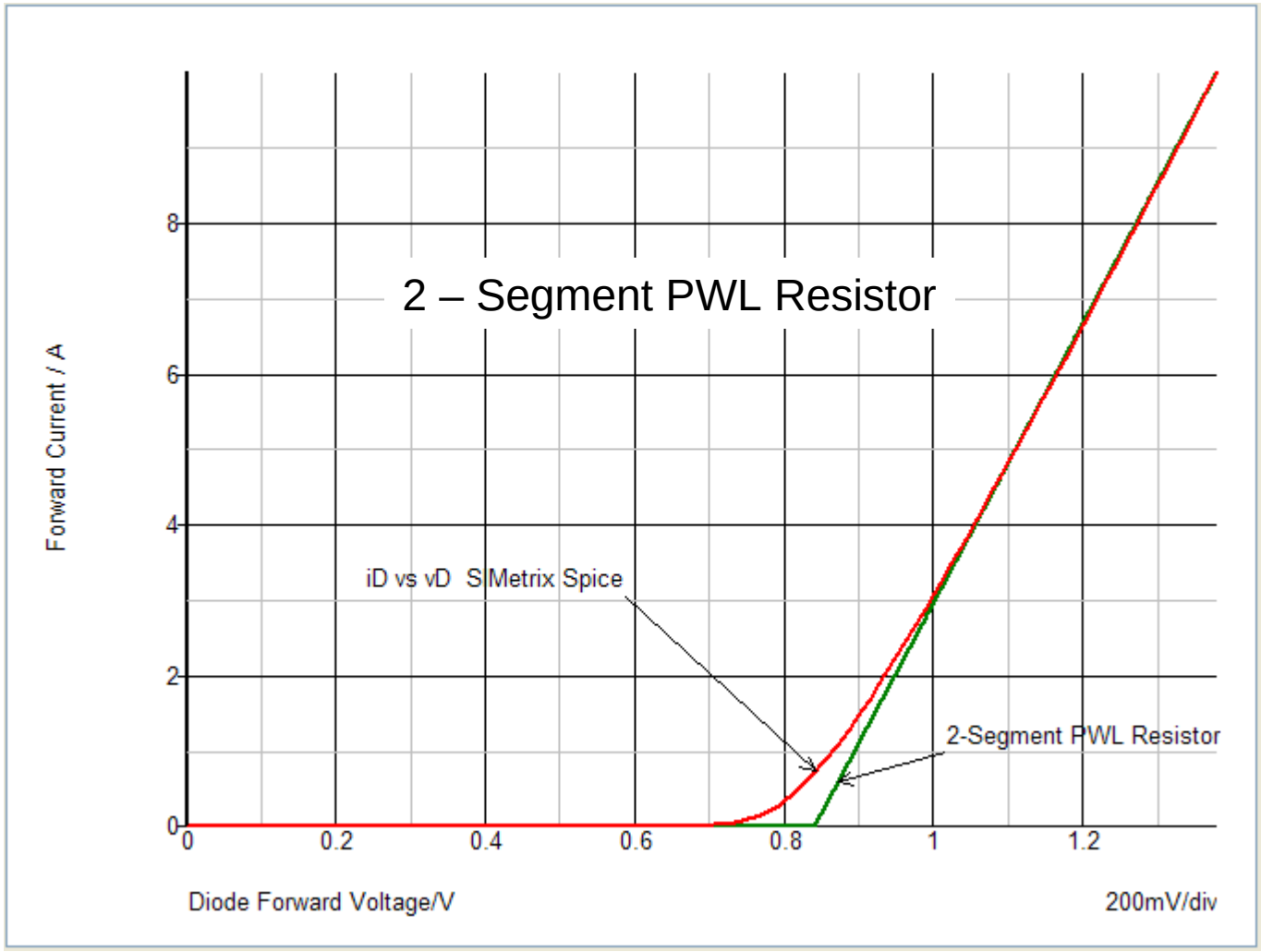
SIMPLIS TECHNOLOGIES

Examples of Multi-level Modeling

- Diode Rectifiers – two or three segment model
- Output Capacitors – add ESR, add ESL
- MOSFETs – with and without switching losses
- Transformer – with and without saturation

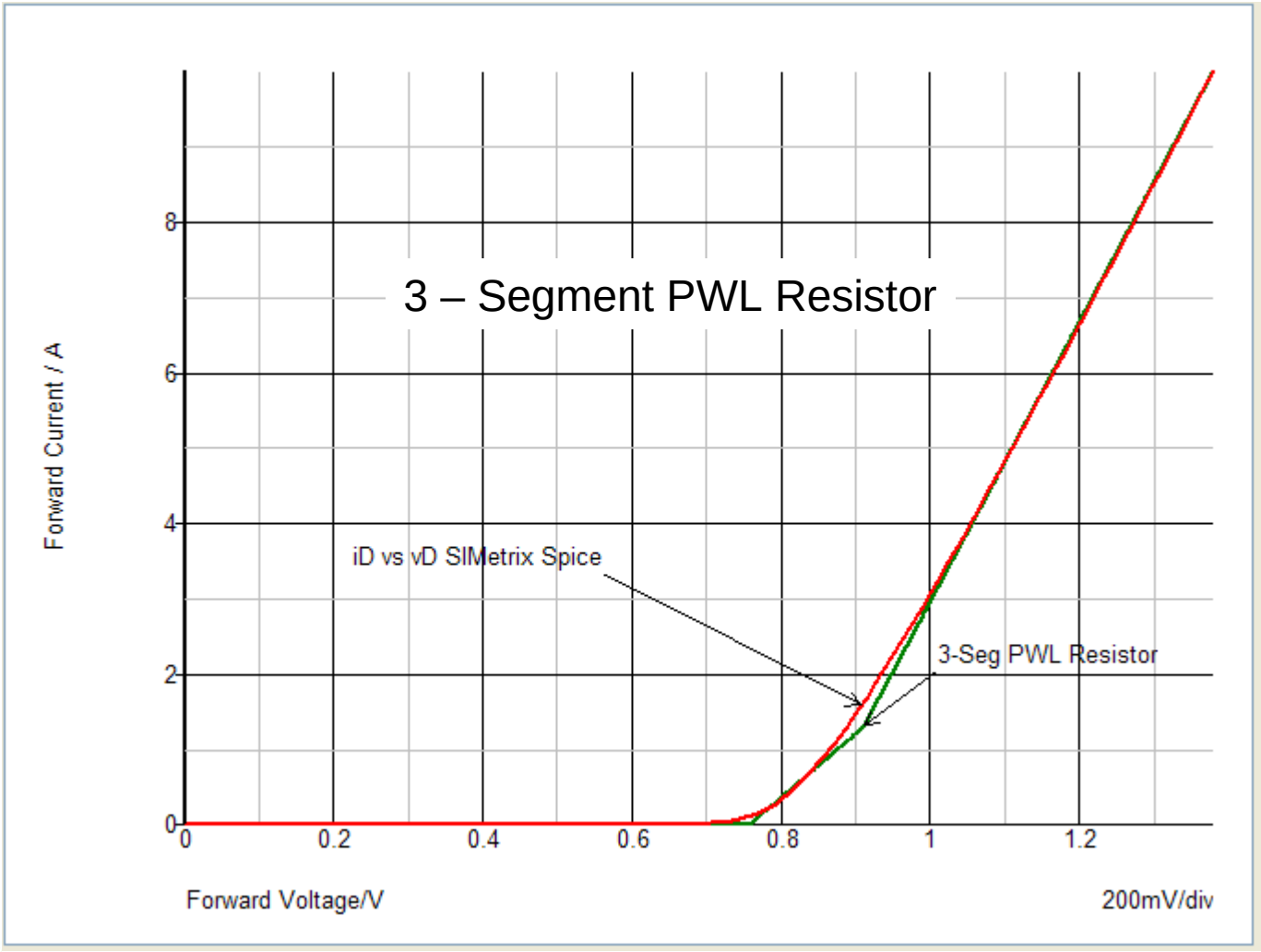
SIMPLIS TECHNOLOGIES

Modeling Diodes with PWL Resistors



SIMPLIS TECHNOLOGIES

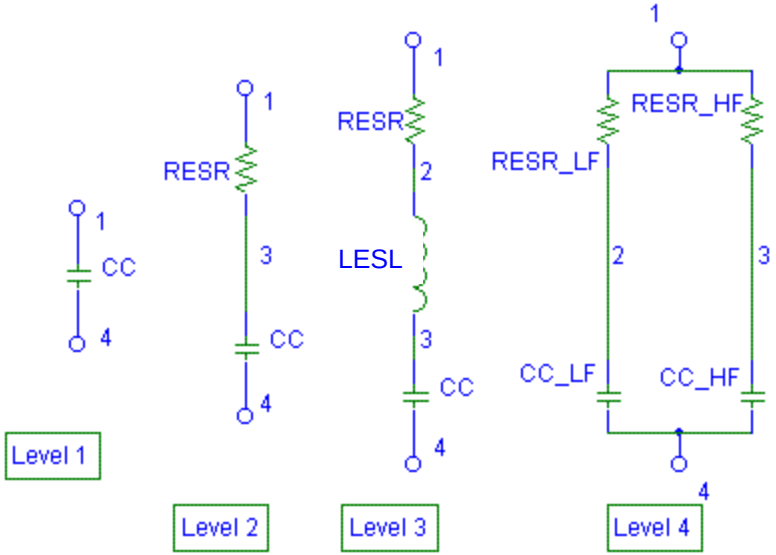
Modeling Diodes with PWL Resistors



SIMPLIS TECHNOLOGIES

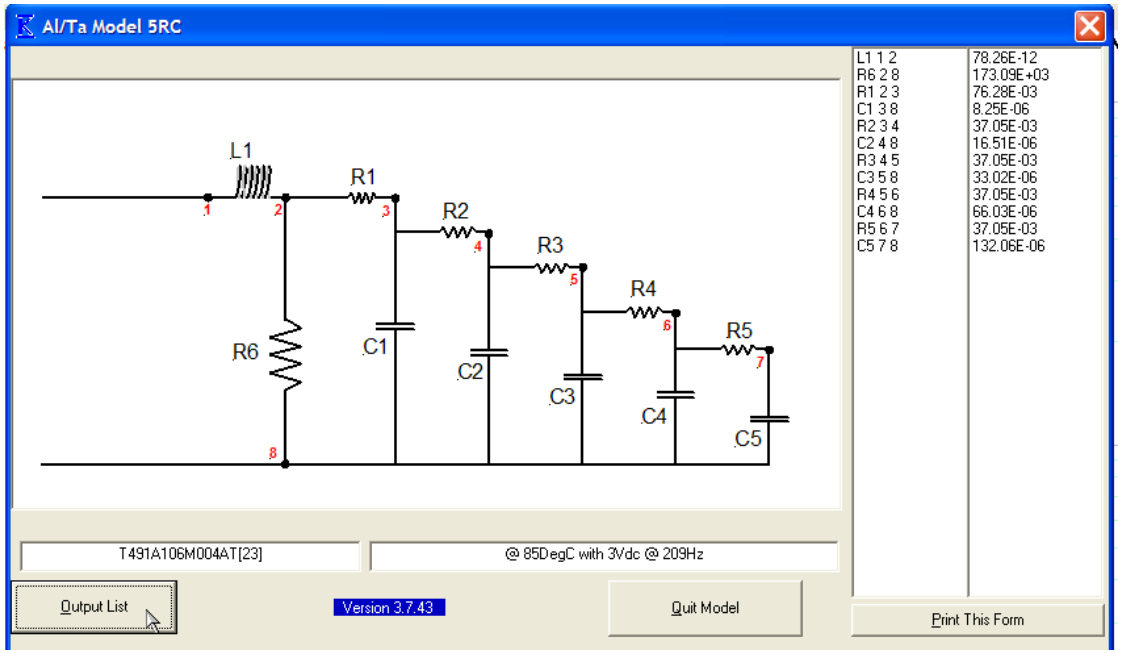
Multi-level modeling

- Select appropriate level of model complexity to optimize simulation accuracy and speed
- Include device parasitics where critical to simulation objectives
  - Example: Output Capacitor
    - Start up
      - Level 2
    - Stability analysis
      - Level 4 or 2
    - High di/dt load transient
      - Level 3



Kemet Capacitor Model Generator

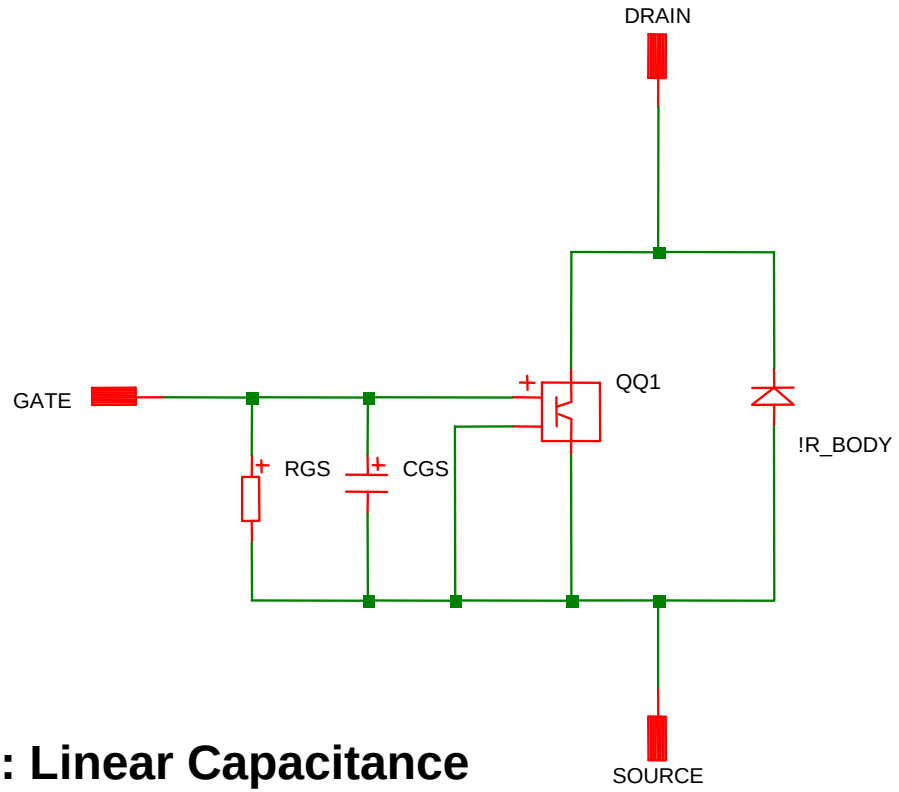
- Adjusts Capacitor models for
  - DC bias
  - Temp
  - Number of Caps in parallel



- http://www.simplistechnologies.com/downloads
- http://www.kemet.com/kemet/web/homepage/kechome.nsf/weben/kemsoftSIMPLIS

SIMPLIS TECHNOLOGIES

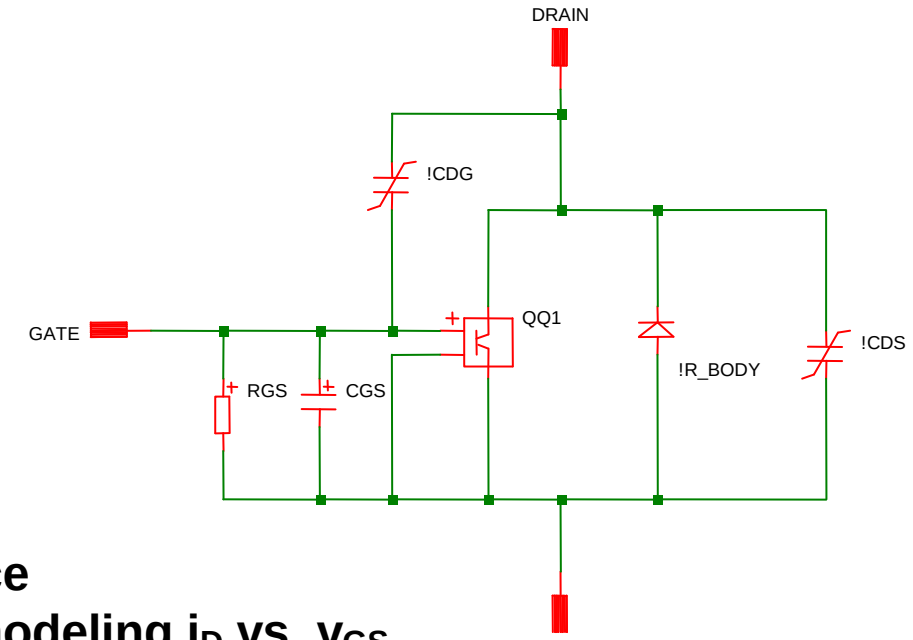
Modeling Level 1 N-channel MOSFET



CGS: Linear Capacitance
QQ1: Switch with On & Off Resistance
IR_BODY: Body diode modeled by PWL Resistor

SIMPLIS TECHNOLOGIES

Modeling Level 3 N-channel MOSFET



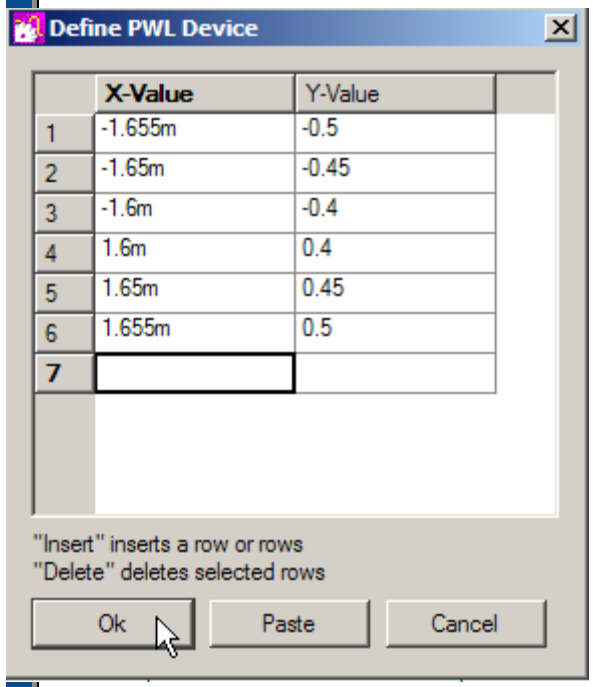
CGS: Linear Capacitance
QQ1: SIMPLIS Switch modeling i_D vs. v_{GS}
proportional to (v_{GS} -VTO)
IR_BODY: Body diode modeled by PWL Resistor
!CDG : PWL capacitance
!CDS : PWL capacitance

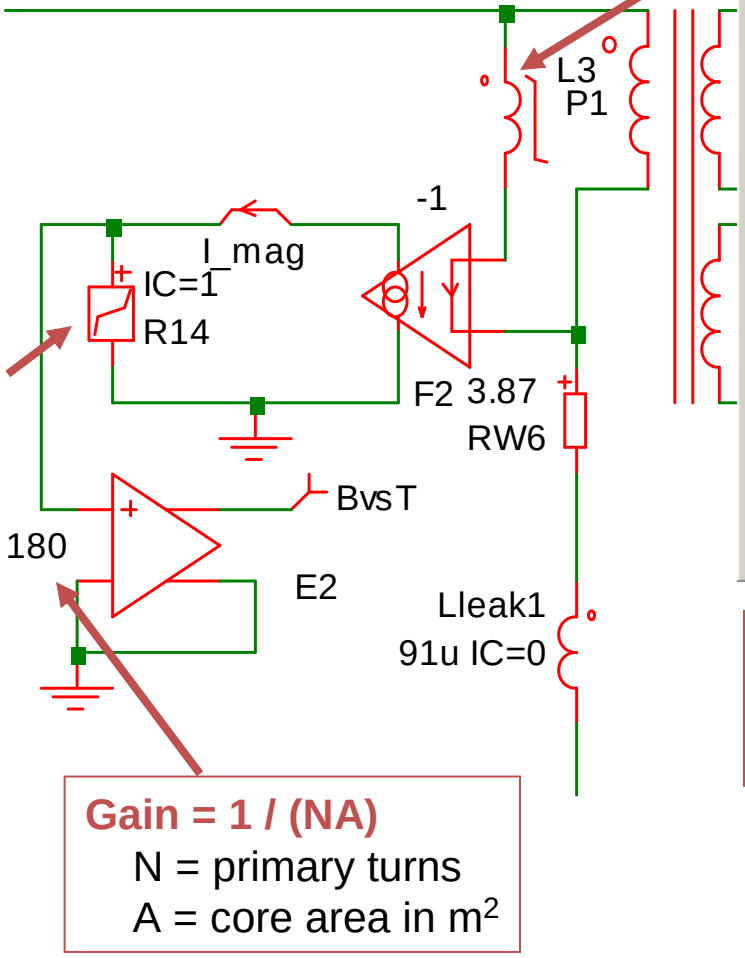
SIMPLIS TECHNOLOGIES

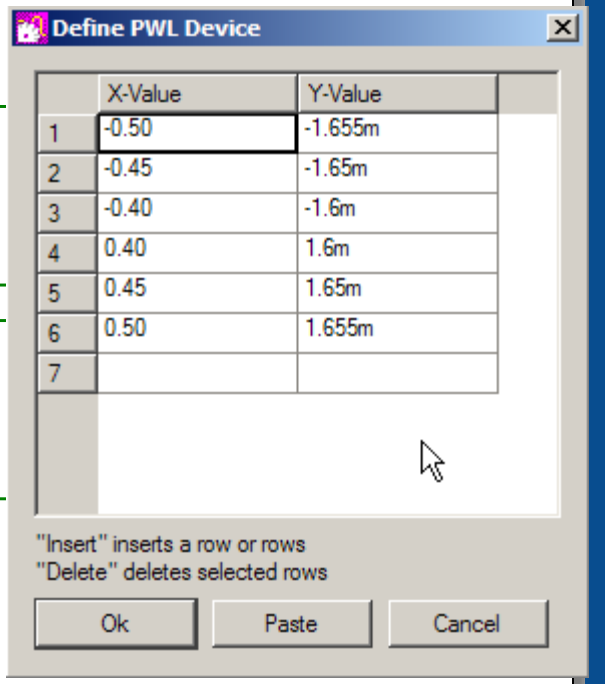
D.24.5

Add B vs. time waveform to transformer model

PWL Resistor
x – voltage=Weber-turns
y – magnetizing current







PWL Inductor
x – magnetizing current
y – Weber-turns

Gain = 1 / (NA)
N = primary turns
A = core area in m^2

Core Loss Model

$$P = \alpha V \left[(\Delta B \, m / (2 t_{ON}) \, n) \, t_{ON} / T_S + (\Delta B \, m / (2 t_{OFF1}) \, n) \, t_{OFF1} / T_S \right]$$

where

t_{ON} is the interval when switch is on and flux density B is increasing;
t_{OFF1} is the interval when switch is off and flux density is decreasing;
t_{OFF2} is the zero-voltage time, the interval when switch is off and flux density is not changing;
T_S is the switching period, which is the sum of t_{ON} , t_{OFF1} , and t_{OFF2};
V is the volume of the core.
α, **m** and **n** are constants for each core material, based on *square wave excitation*

– "**A Method for Inductor Core Loss Estimation in Power Factor Correction Applications"** Jinjun Liu, Thomas G. Wilson, Jr., Ronald C. Wong, Ron Wunderlich, and Fred C. Lee, APEC 2002

SIMPLIS TECHNOLOGIES

Benefits of PWL modeling and simulation

- Much faster time-domain transient simulations
- Ability to find Steady-State limit cycle much faster than long transient simulation
- Ability to do AC analysis on a circuit that is in Steady State time domain operation
  - No average model required
- Speed and Accuracy levels can be achieved with proper attention to
  - multi-level modeling
  - clear simulation objectives

SIMPLIS TECHNOLOGIES

Select Modeling Level based on Simulation Objective

- Example: 3-Phase Synchronous Buck
  - What modeling levels are required for Bode Plot ?
  - What modeling levels are required for Step Load transient with moderate di/dt?
- Issue:
  - Include switching losses of Sync FETs ?
  - Compare simulation times and results

SIMPLIS TECHNOLOGIES

D.14.1

Select Modeling Level based on Simulation Objective

- Example: Self Oscillating Flyback
  - What modeling levels are required for Bode Plot ?

- Issue:
  - With self oscillating converter, the switching frequency is reduced by non-zero switching transitions.
  - Do these losses materially affect Bode Plot?

SIMPLIS TECHNOLOGIES

D.24.5

Simulation Objective = AC Analysis - Bode Plot

- Sync Buck sim times ***without*** Switching losses
  - POP - 6 s
  - AC - 3 s
  - Step Load Tran - 13 s
- Sync Buck sim times ***with*** Switching losses
  - POP - 56 s
  - AC - 13 s
  - Step Load Tran - 103 s

Nearly a **10x** increase in simulation time for ***zero*** benefit

SIMPLIS TECHNOLOGIES

Modeling Level vs. Simulation Objective and Device Type

Device Type / Simulation Objective	Output Diode Rectifier	Output Capacitor (Electrolytic)	Output Capacitor (Ceramic)	Output Inductor	MOSFET Power Switch	
Bode Plot (Steady-State, AC analysis)						
Step Load Transient – moderate di/dt (Steady-State, Transient analysis)						
Step Load Transient – high di/dt (Steady-State, Transient analysis)						
Line and Load Regulation (Steady-State analysis)						

SIMPLIS TECHNOLOGIES

Modeling Level vs. Simulation Objective and Device Type

Simulation Objective \ Device Type	Output Diode Rectifier	Output Capacitor (Electrolytic)	Output Capacitor (Ceramic)	Output Inductor	MOSFET Power Switch	
Bode Plot (Steady-State, AC analysis)	2-seg	Lev 2	Lev 1	Linear Lossy	Lev 1	
Step Load Transient – moderate di/dt (Steady-State, Transient analysis)	2-seg	Lev 2	Lev 1	Linear Lossy	Lev 1	
Step Load Transient – high di/dt (Steady-State, Transient analysis)	2-seg	Lev 3	Lev 1	Linear Lossy	Lev 1	
Line and Load Regulation (Steady-State analysis)	3-seg*	Lev 2	Lev 1	Linear Lossy	Lev 1	

SIMPLIS TECHNOLOGIES

Simulation Accuracy vs. Simulation Time

- What is necessary to achieve required accuracy within reasonable simulation times?
  - PWL modeling and simulation
  - Multi-level modeling
  - Clear Simulation Objectives

SIMPLIS TECHNOLOGIES

Clear & Focused Simulation Strategy

- Two major benefits of being clear and focused
    - You can go farther
    - You can get there much faster

SIMPLIS TECHNOLOGIES

Clear & Focused Simulation Strategy

- Example: Flyback for Adapter
  - What modeling levels are required for device stress and loss measurements?
- Specifically
  - What is needed to get good power loss estimates?
    - Given that switching loss measurements are more challenging than measuring loop response behavior

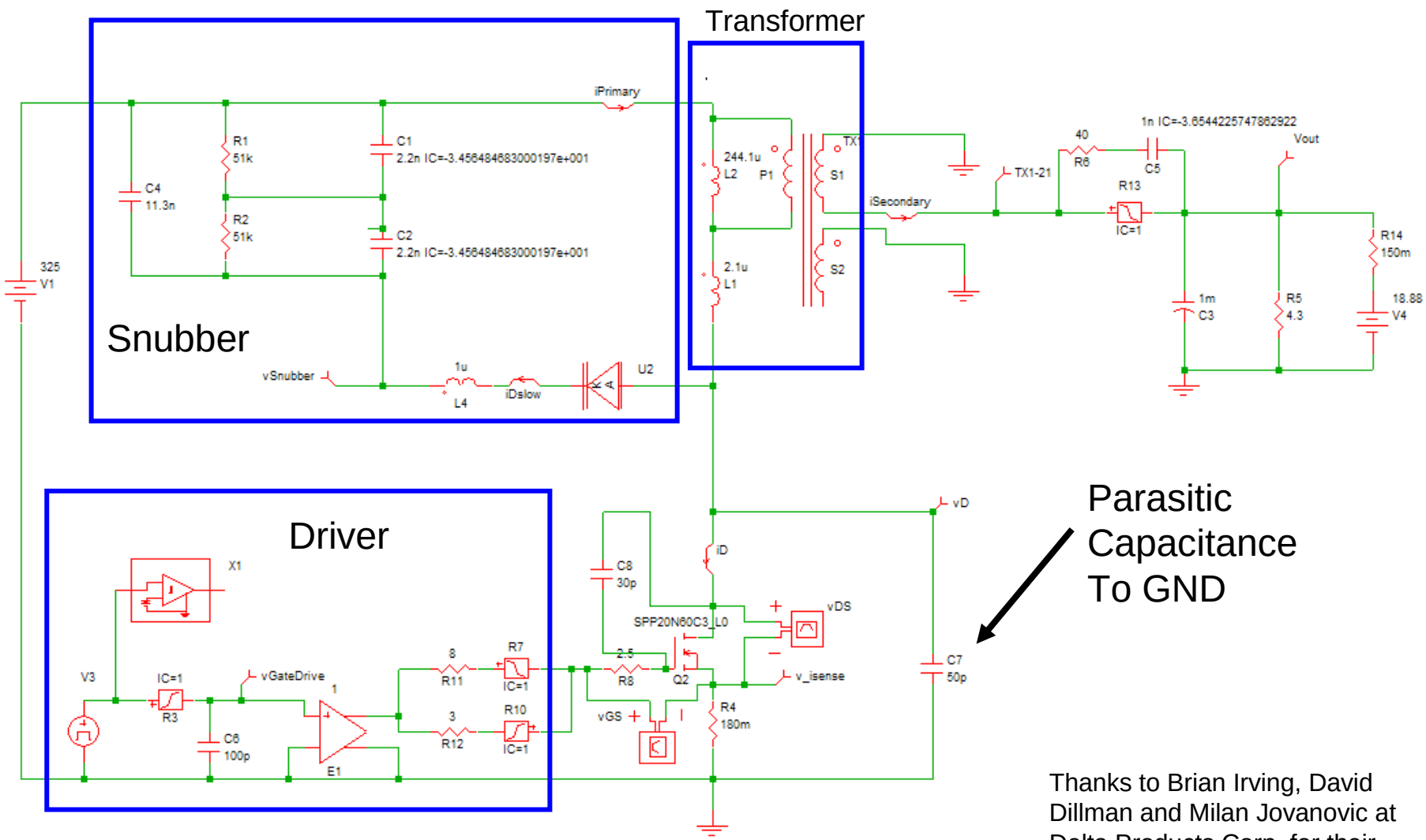
SIMPLIS TECHNOLOGIES

Switching Losses

- Switching losses are very sensitive to
  - Device parasitic elements
  - Layout parasitic elements
- Device parasitics can be characterized in advance
- For maximum benefit, virtual prototyping is done ***before*** a layout exists
  - So there are inherent uncertainties in this effort
- This area of simulation is less mature than simulation of closed loop performance
- Even so, *the initial estimate of switching losses plays a central role in the development process*

SIMPLIS TECHNOLOGIES

Switching Losses – Flyback for Adapter



SIMPLIS TECHNOLOGIES

Thanks to Brian Irving, David Dillman and Milan Jovanovic at Delta Products Corp. for their support in this effort

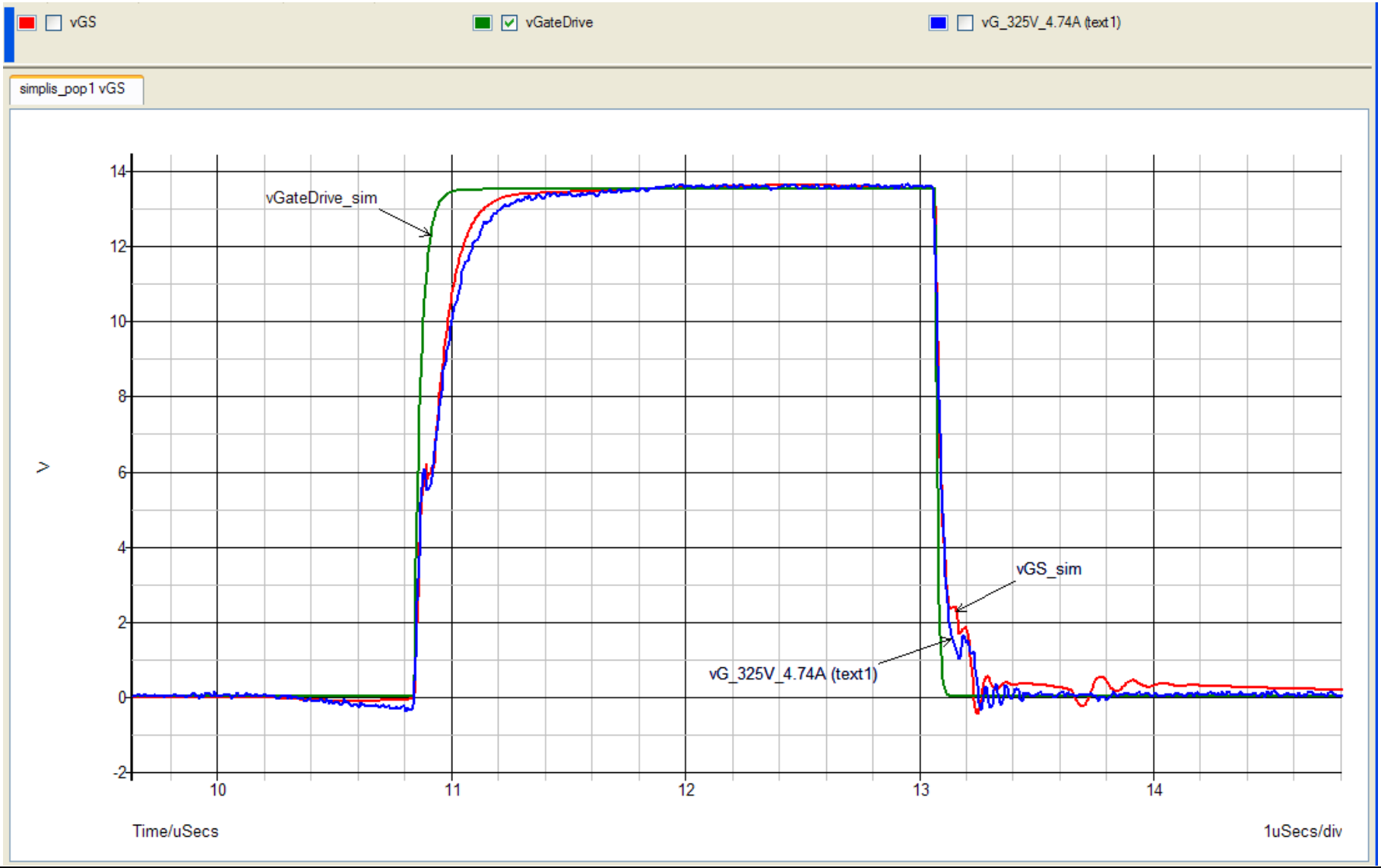
Switching Losses – Flyback for Adapter

- Run simulation test circuit open loop in Steady State
- Adjust Driver, FET and Snubber Diode models to match measured waveforms at Vin = 325V, Vout = 18.88V and Full Load Iout = 4.74A
- Then compare simulated waveforms and measured waveforms at different line and load conditions with “identical” gate drive signals

SIMPLIS TECHNOLOGIES

D.55.1

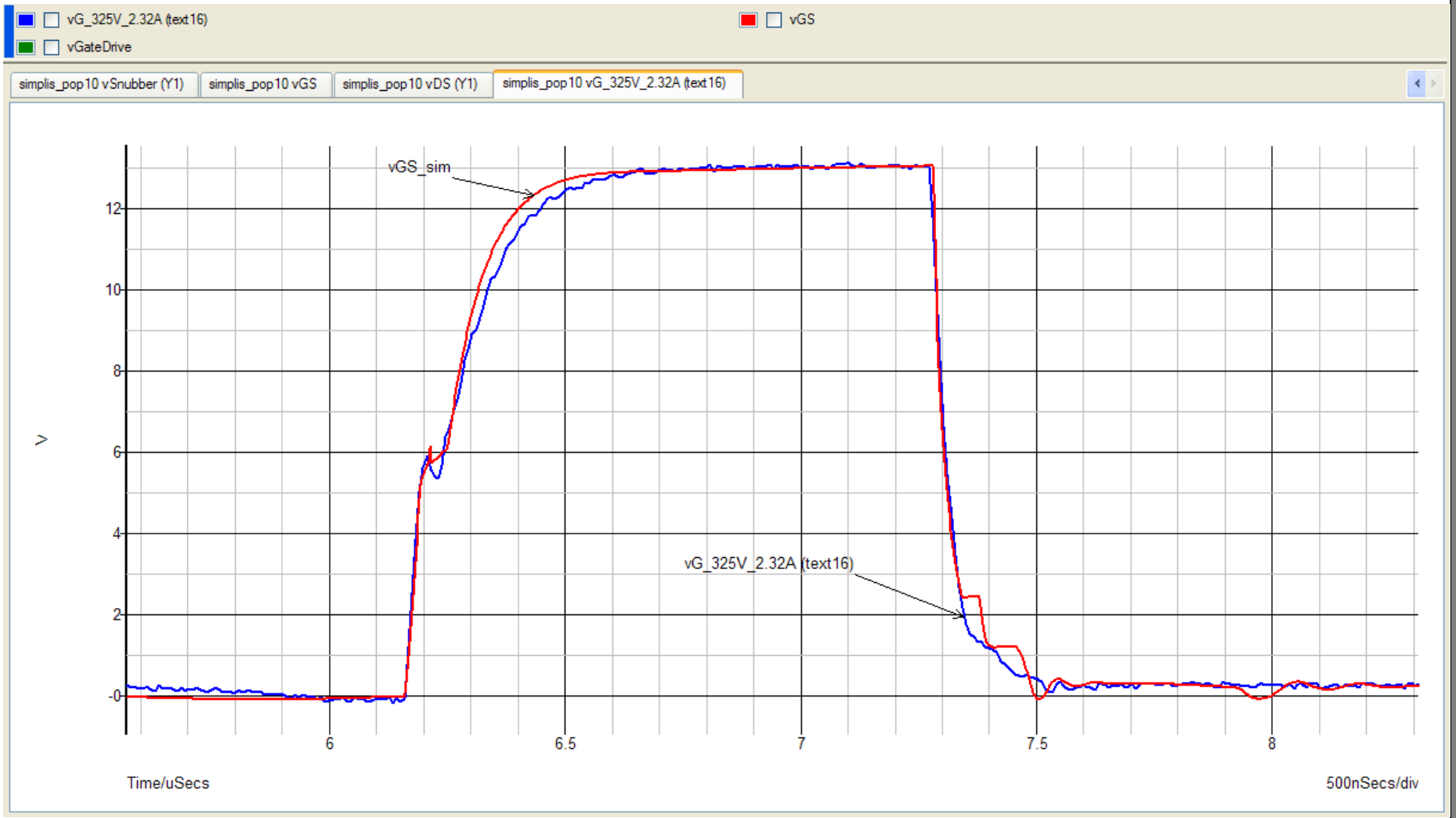
Gate Voltage v_{GS}
(Vin = 325V, Iout = 4.74A)



Drain Voltage v_{DS} and Drain Current i_D

(Vin = 325V, Iout = 4.74A)

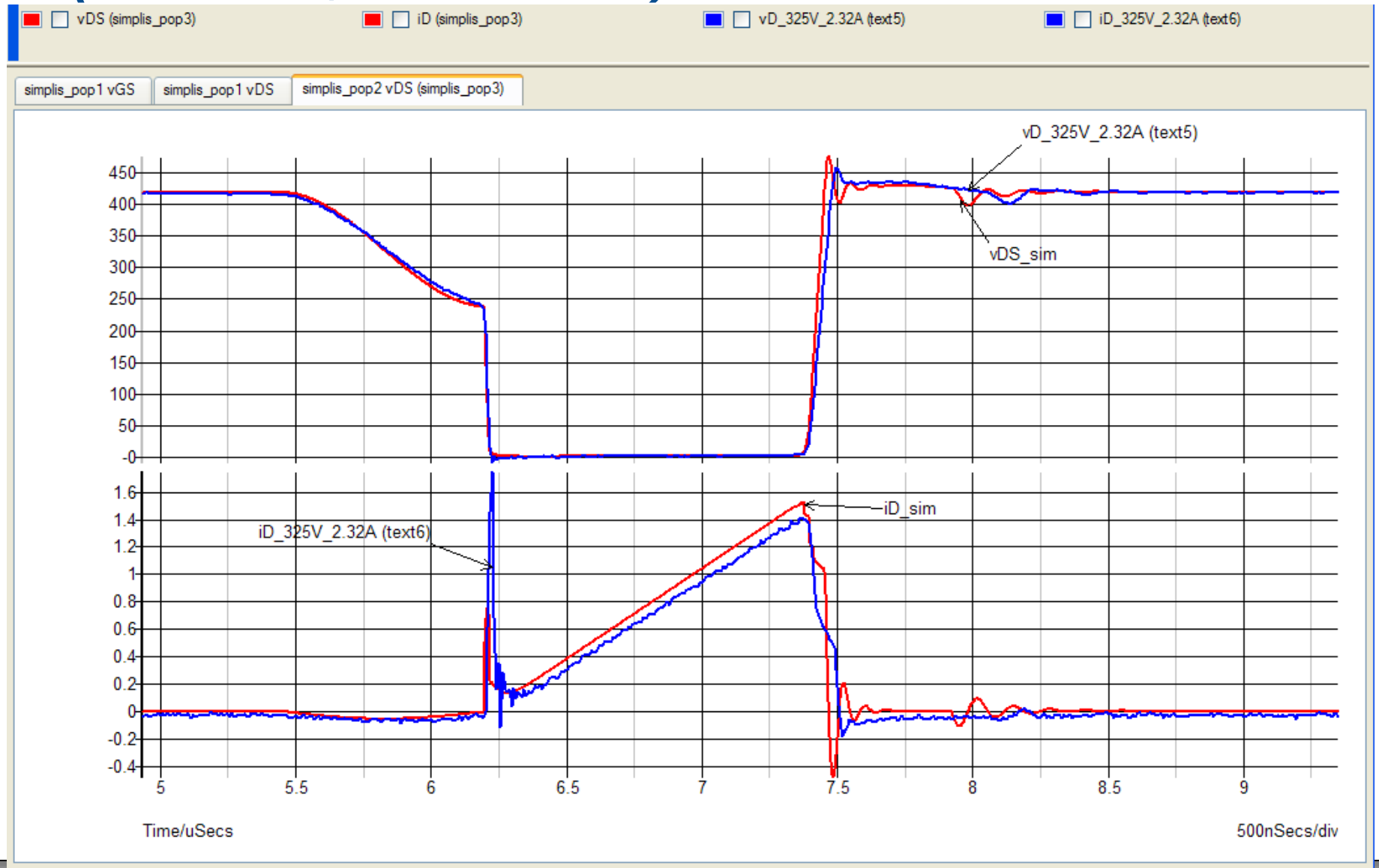
Gate Voltage v_{GS}
(Vin = 325V, Iout = 2.32A)



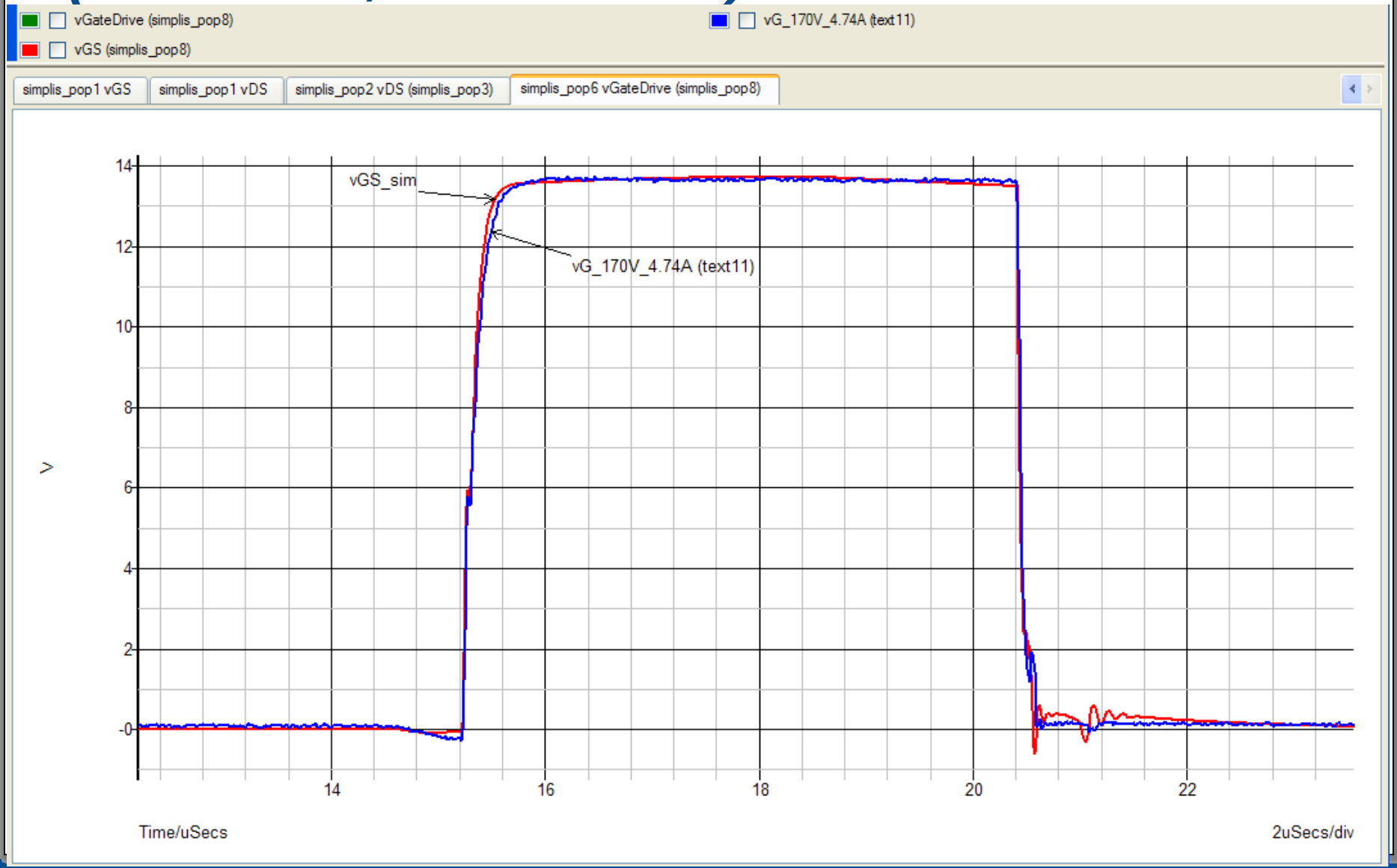
SIMPLIS TECHNOLOGIES

Drain Voltage v_{DS} and Drain Current i_D

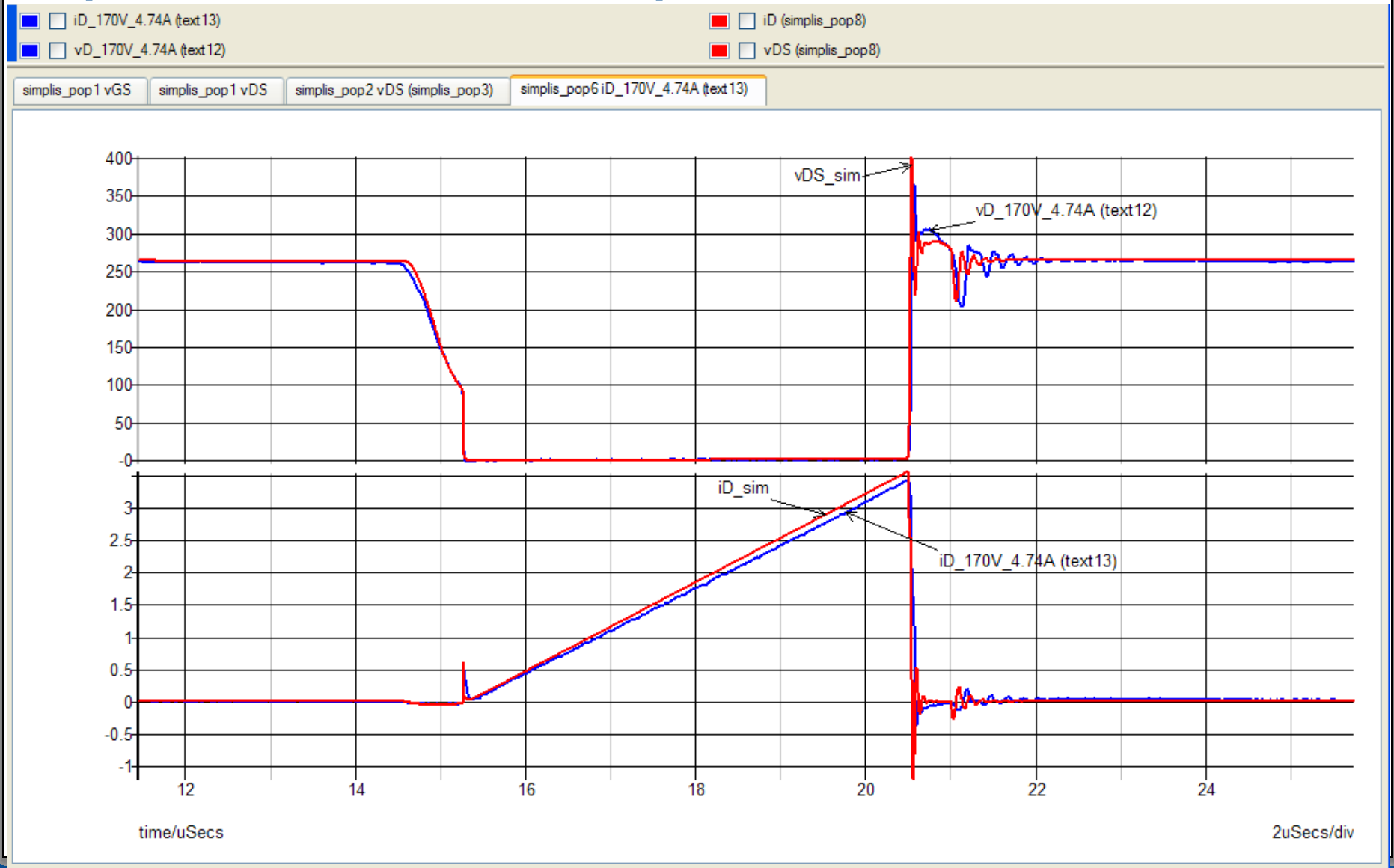
(Vin = 325V, Iout = 2.32A)



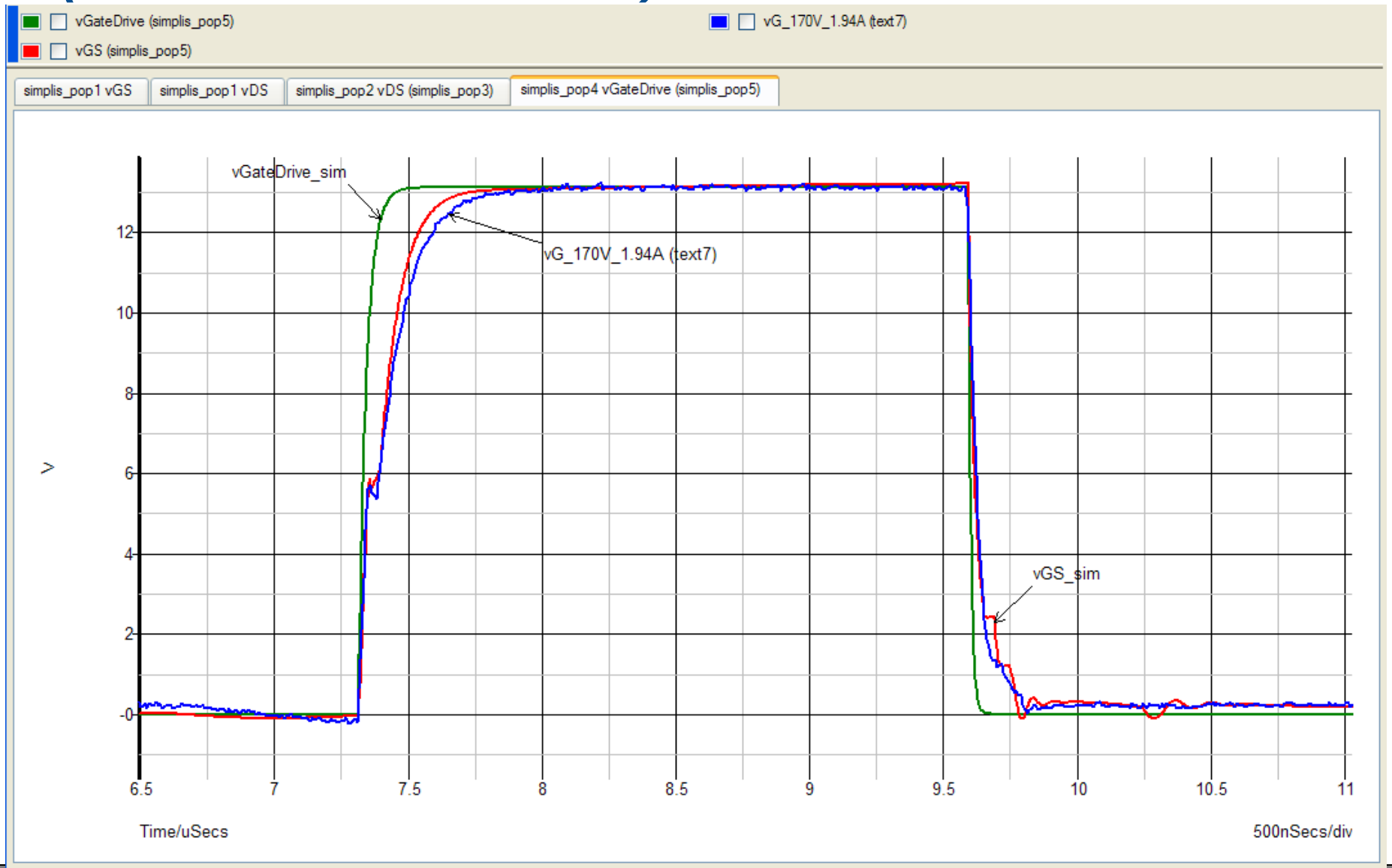
Gate Voltage v_{GS} (Vin = 170V, Iout = 4.74A)



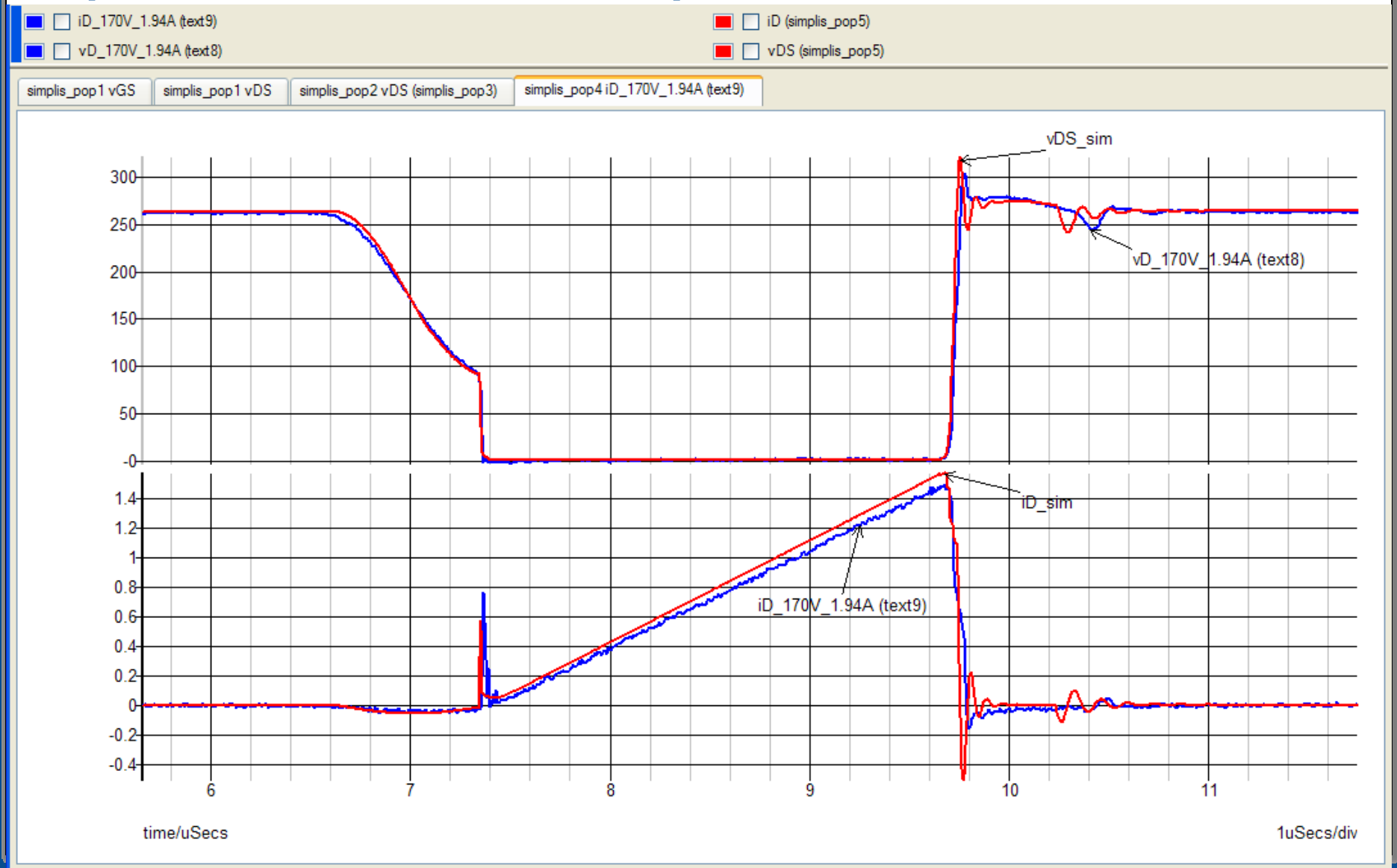
Drain Voltage v_{DS} and Drain Current i_D (Vin = 170V, Iout = 4.74A)



Gate Voltage v_{GS}
(Vin = 170V, Iout = 1.94A)



Drain Voltage v_{DS} and Drain Current i_D (Vin = 170V, Iout = 1.94A)



Switching Losses (1)

- Can get very good matching between simulated and measured waveforms
  - We are capturing the important aspects of FET waveforms pretty well
  - With reasonable measurements of silicon device parasitics
  - With reasonable estimates of
    - layout parasitics
    - magnetic device parasitics

SIMPLIS TECHNOLOGIES

Switching Losses (2)

- Challenging to get sufficiently accurate ***measurements*** of vDS and iD to measure switching losses directly
- Would like better models for reverse recovery
  - First need better characterization data for devices
- Unknown layout parasitic can be estimated if have experience with similar packaging

SIMPLIS TECHNOLOGIES

Switching Losses (3)

Having said all that

- Simulation can do a better and faster job than most hand analysis of estimating:
  - Switching losses before first hardware build
  - Sensitivity of losses to various layout and device parasitics

SIMPLIS TECHNOLOGIES

Modeling Level vs. Simulation Objective and Device Type

Device Type / Simulation Objective	Output Diode Rectifier	Output Capacitor (Electrolytic)	Output Capacitor (Ceramic)	Output Inductor	MOSFET Power Switch	
Switching Losses (FET) (Steady-State)						
Start up Transient (Transient analysis)						
Short Circuit (Steady-State, Transient analysis)						
Short Circuit & Recovery (Steady-State, Transient analysis)						

SIMPLIS TECHNOLOGIES

Modeling Level vs. Simulation Objective and Device Type

Device Type / Simulation Objective	Output Diode Rectifier	Output Capacitor (Electrolytic)	Output Capacitor (Ceramic)	Output Inductor	MOSFET Power Switch	
Switching Losses (FET) (Steady-State)	3-seg	Lev 2	Lev 1	Linear Lossy	Lev 3	
Start up Transient (Transient analysis)	2-seg	Lev 2	Lev 1	Linear Lossy	Lev 1	
Short Circuit (Steady-State, Transient analysis)				Lossy w Sat		
Short Circuit & Recovery (Steady-State, Transient analysis)				Lossy w Sat		

SIMPLIS TECHNOLOGIES

Clear & Focused Simulation Strategy

Critical Success Factor for Virtual Prototyping

- Establish the Matrix showing the appropriate Model Levels for each Simulation Objective
- Verify / Modify Matrix for each new class of circuit

SIMPLIS TECHNOLOGIES

Modeling Level vs. Simulation Objective and Device Type

- This Matrix showing the appropriate Modeling Level for each Device Type for each Simulation Objective is
  - Typically applicable over a broad class of converter topology – control law combinations
  - Easy to summarize and share with larger design team
  - Can save a lot of confusion and bring engineers new to power supply simulation up the learning curve much faster
  - Can save a lot of simulation time and still deliver required simulation accuracy

SIMPLIS TECHNOLOGIES

Time is the most precious resource (1)

- Speed is essential to test for all “known” electrical design errors in a reasonable time
- You won’t find design errors that you don’t look for
- A comprehensive Test Plan includes hundreds of simulation tests.
- Want to invest simulation time where it will do the most good
- Need a clear and focused Test Plan that executes your Simulation Strategy

SIMPLIS TECHNOLOGIES

Time is the most precious resource (2)

- During the course of design and design verification testing you will hit the “Simulate” button ~ thousand times
- Using higher complexity models than you need to achieve your simulation objectives just wastes your time

SIMPLIS TECHNOLOGIES

Modeling Level vs. Simulation Objective and Device Type

Device Type / Simulation Objective	Output Diode Rectifier	Output Capacitor (Electrolytic)	Output Capacitor (Ceramic)	Output Inductor	MOSFET Power Switch	
Bode Plot (Steady-State, AC analysis)	2-seg	Lev 2	Lev 1	Linear Lossy	Lev 1	
Step Load Transient – moderate di/dt (Steady-State, Transient analysis)	2-seg	Lev 2	Lev 1	Linear Lossy	Lev 1	
Step Load Transient – high di/dt (Steady-State, Transient analysis)	2-seg	Lev 3	Lev 1	Linear Lossy	Lev 1	
Line and Load Regulation (Steady-State analysis)	3-seg*	Lev 2	Lev 1	Linear Lossy	Lev 1	

SIMPLIS TECHNOLOGIES

Observations

- Note that many of the Design Verification Tests that you will be doing start out in steady state
- It is often much faster to do more targeted simulations than fewer “Test Everything” simulations
- Some modeling strategies that work well for Spice are counter productive with SIMPLIS

SIMPLIS TECHNOLOGIES

Virtual Prototyping of Power Supply Designs

- Virtual Prototyping Process
  - From 3 Perspectives:
    - Power Supply Designer
    - **Power Management IC Architect**
    - Power System Designer

  Controller IC-centric view of world where customers are Power Supply and Power System Designers

SIMPLIS TECHNOLOGIES

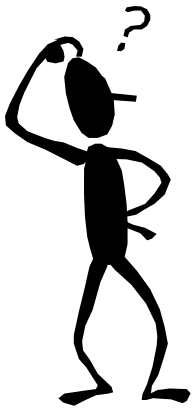
New Product Definition for Power Management ICs

- Significant Process Trend
  - Use of SIMPLIS PWL simulation behavioral model to define new products
  - Create behavioral models that describe all critical features
  - Thoroughly test PWL behavioral model of proposed new product in system application circuit
    - Over whole anticipated application space
    - Compare results with customer system specs

SIMPLIS TECHNOLOGIES

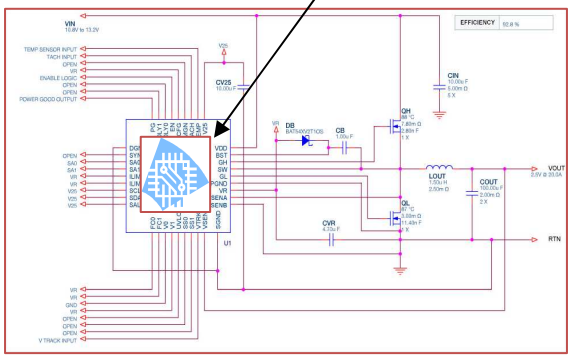
Traditionally

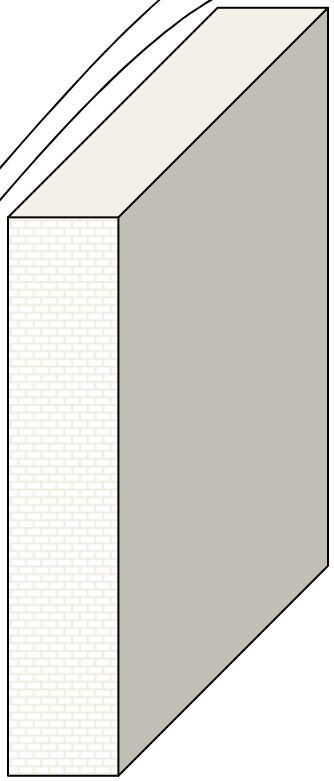
New Product Definition



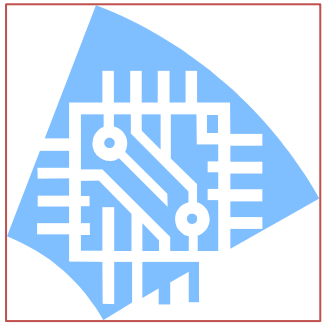
Test & Verification

New Product Architect





IC Designer



IC Design

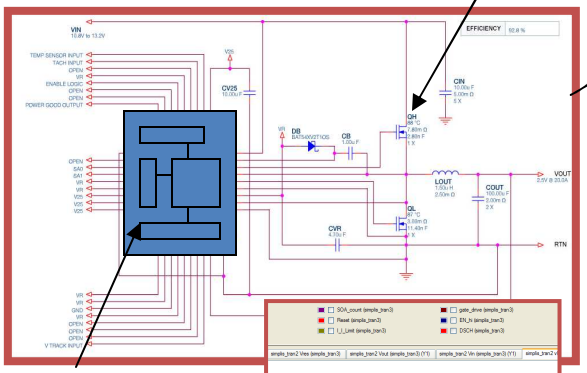
SIMPLIS TECHNOLOGIES

With SIMPLIS PWL Virtual Prototype

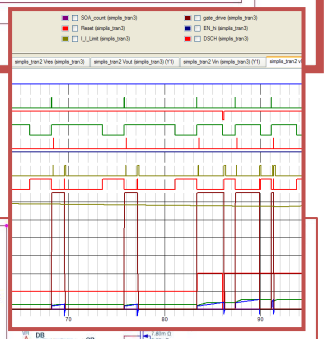
New Product Definition

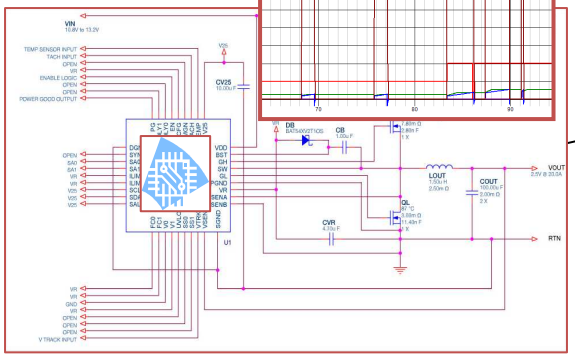
New Product Architect

Application Schematic



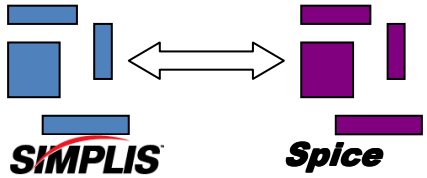
SIMPLIS IC Building blocks



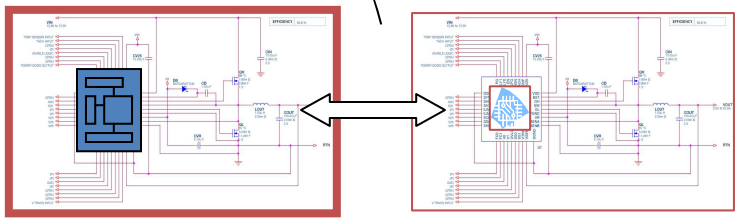


Test & Verification

IC Designer



IP Block Mapping



SIMPLIS TECHNOLOGIES

New Product Definition

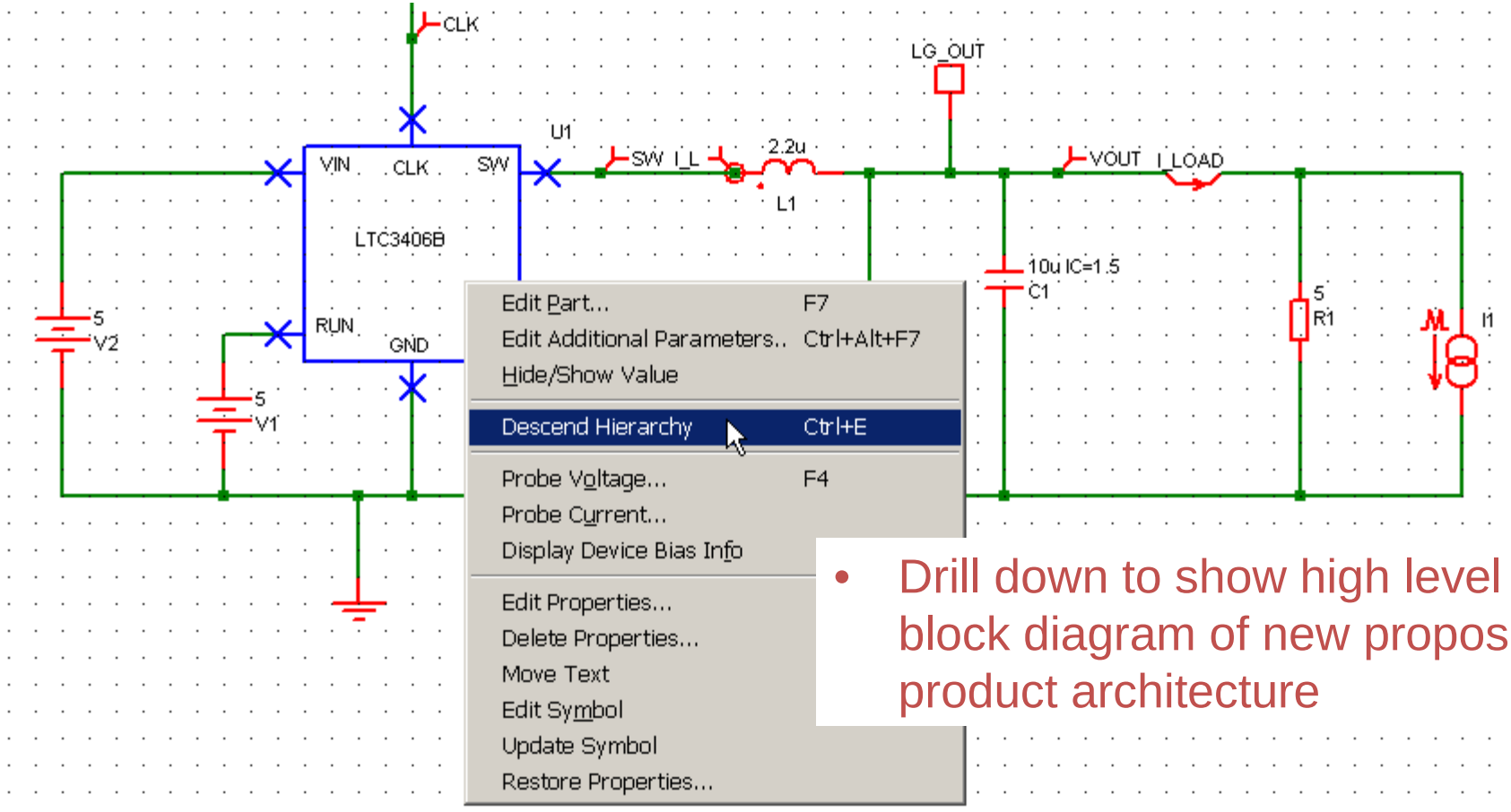
SIMPLIS PWL Behavioral Models

- Provides much crisper new product definition between System Engineer and IC Circuit Designer
- New Product Definition includes:
  - Clear relationship between IC spec and system level performance
  - Clear definition of Top level IC architecture
  - Quantitative specs (delays, waveforms, rise/fall times, bandwidth) of each input/output for each major element in Block Diagram
  - Clear architecture of critical blocks

SIMPLIS TECHNOLOGIES

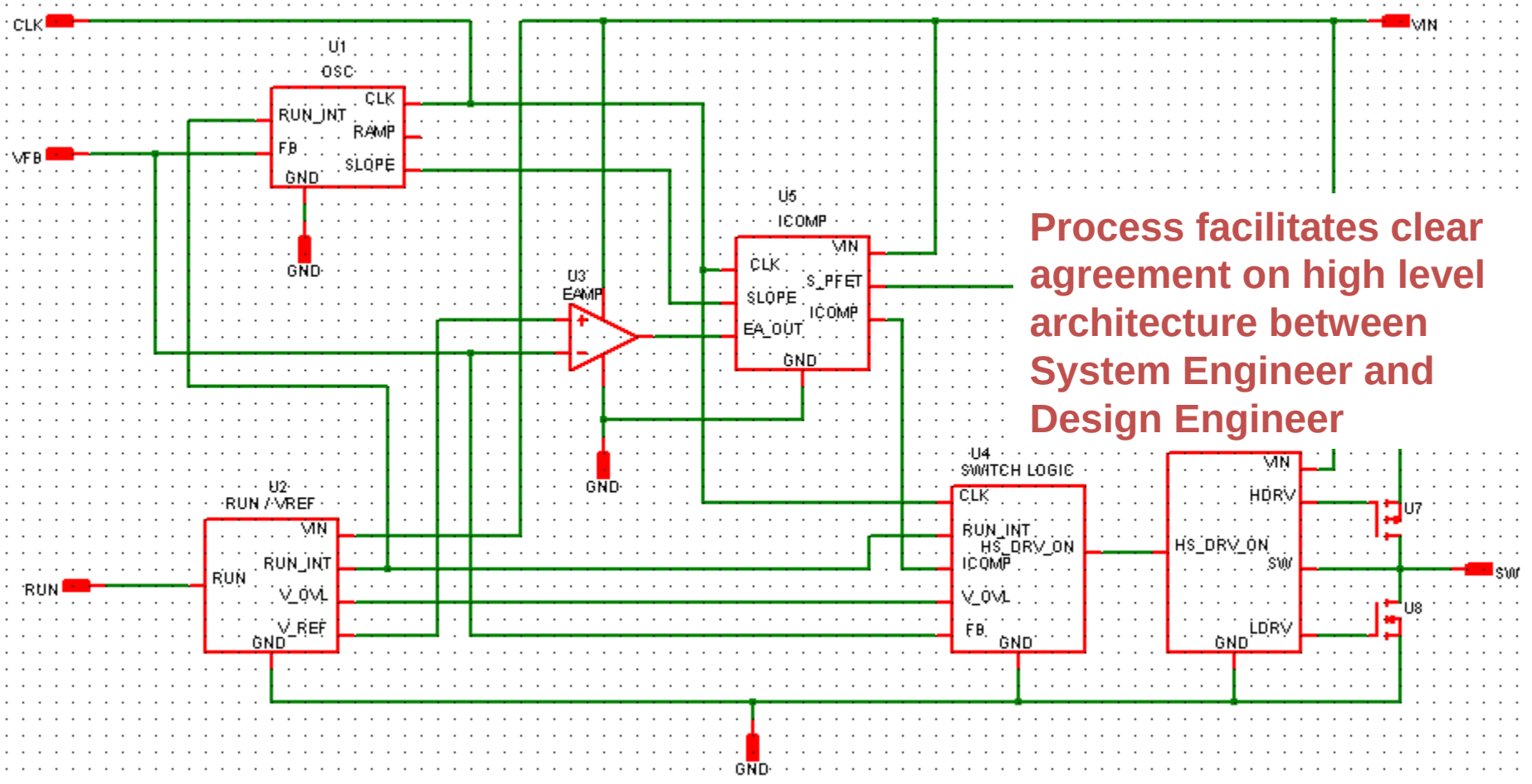
Use SIMPLIS models to define new product architecture at functional block level

- Proposed new product in the target application circuit



- Drill down to show high level block diagram of new proposed product architecture

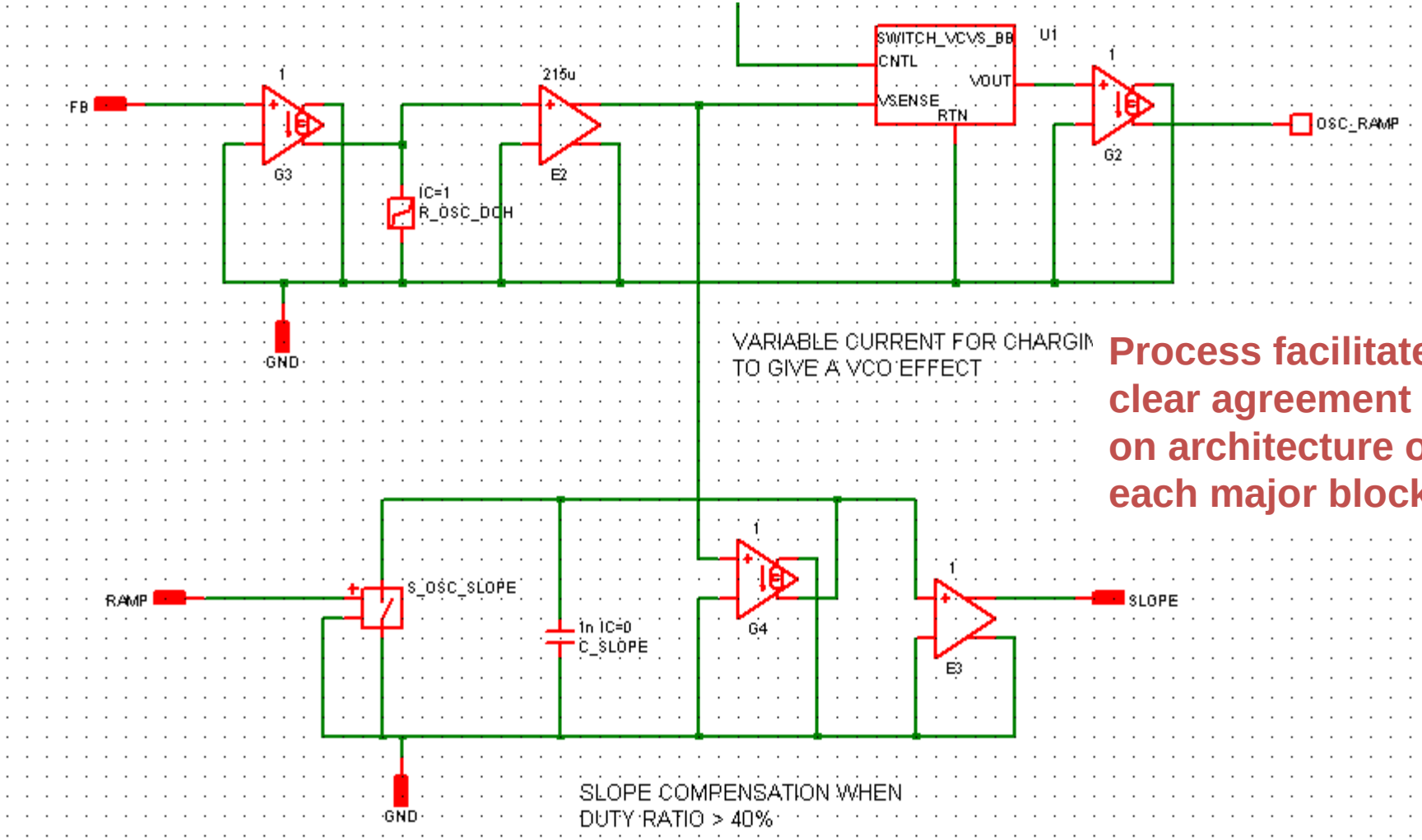
High Level Block Diagram corresponds to desired IC architecture



Process facilitates clear agreement on high level architecture between System Engineer and Design Engineer

SIMPLIS TECHNOLOGIES

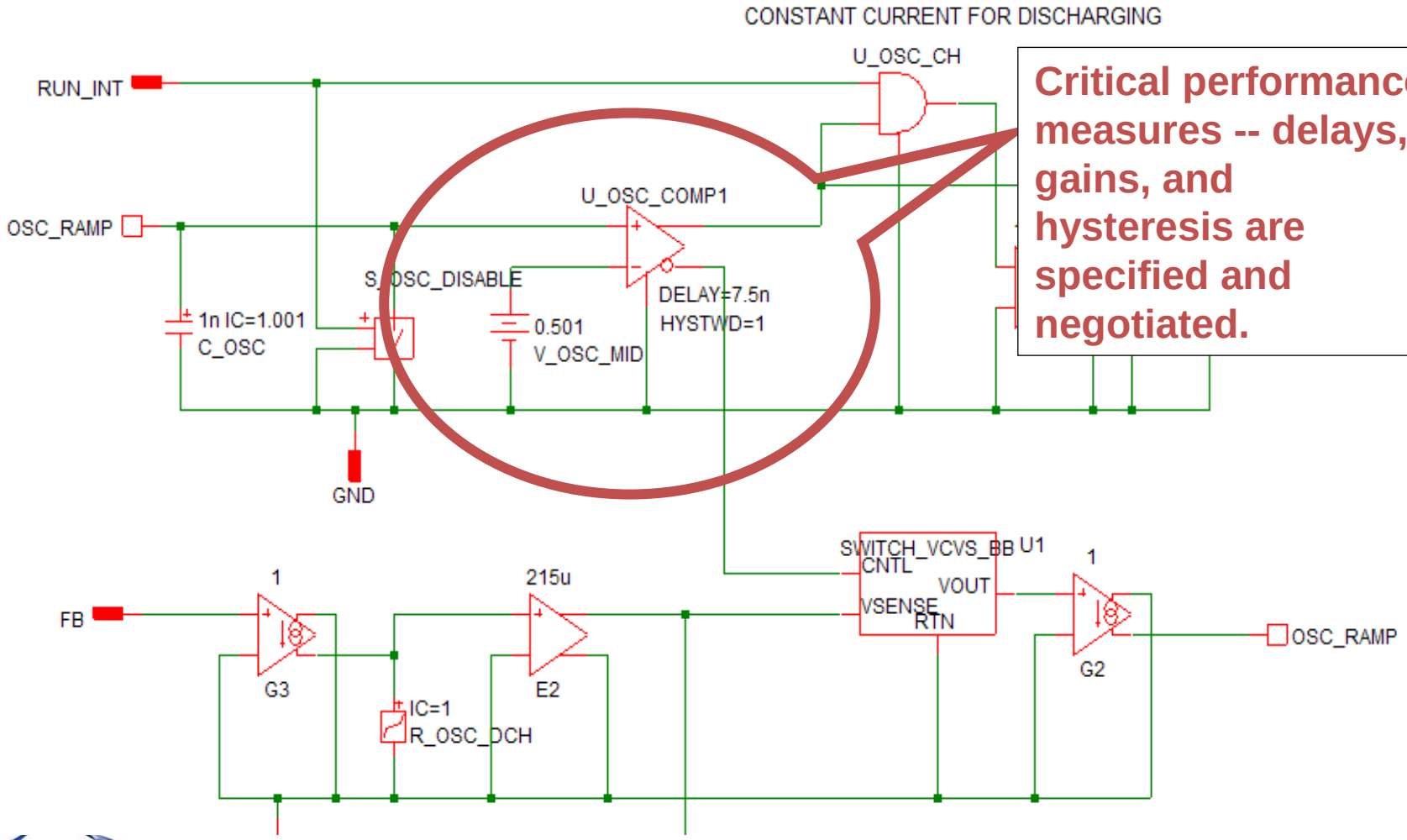
Each Functional Block in the High Level Diagram contains its own Architectural definition



Process facilitates clear agreement on architecture of each major block

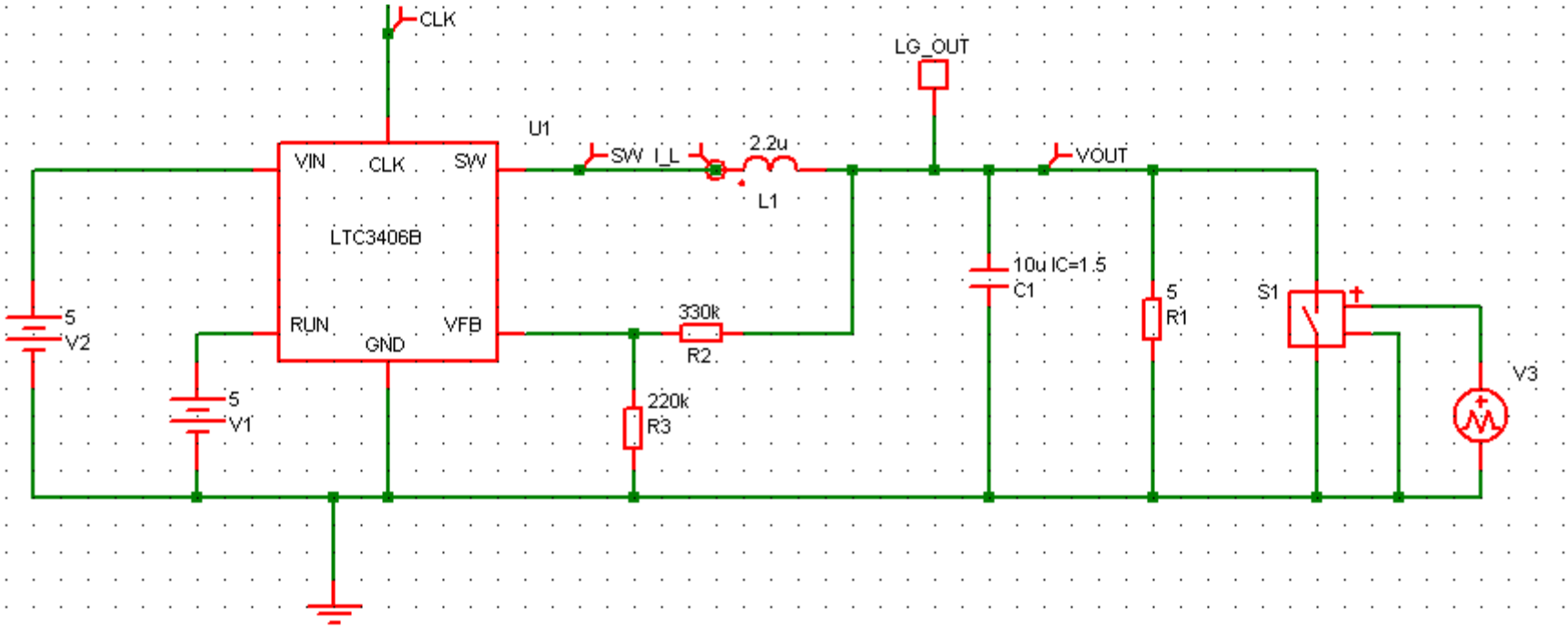
SIMPLIS TECHNOLOGIES

In each Block, Critical Gains, Delays and Hysteresis can be modeled to…



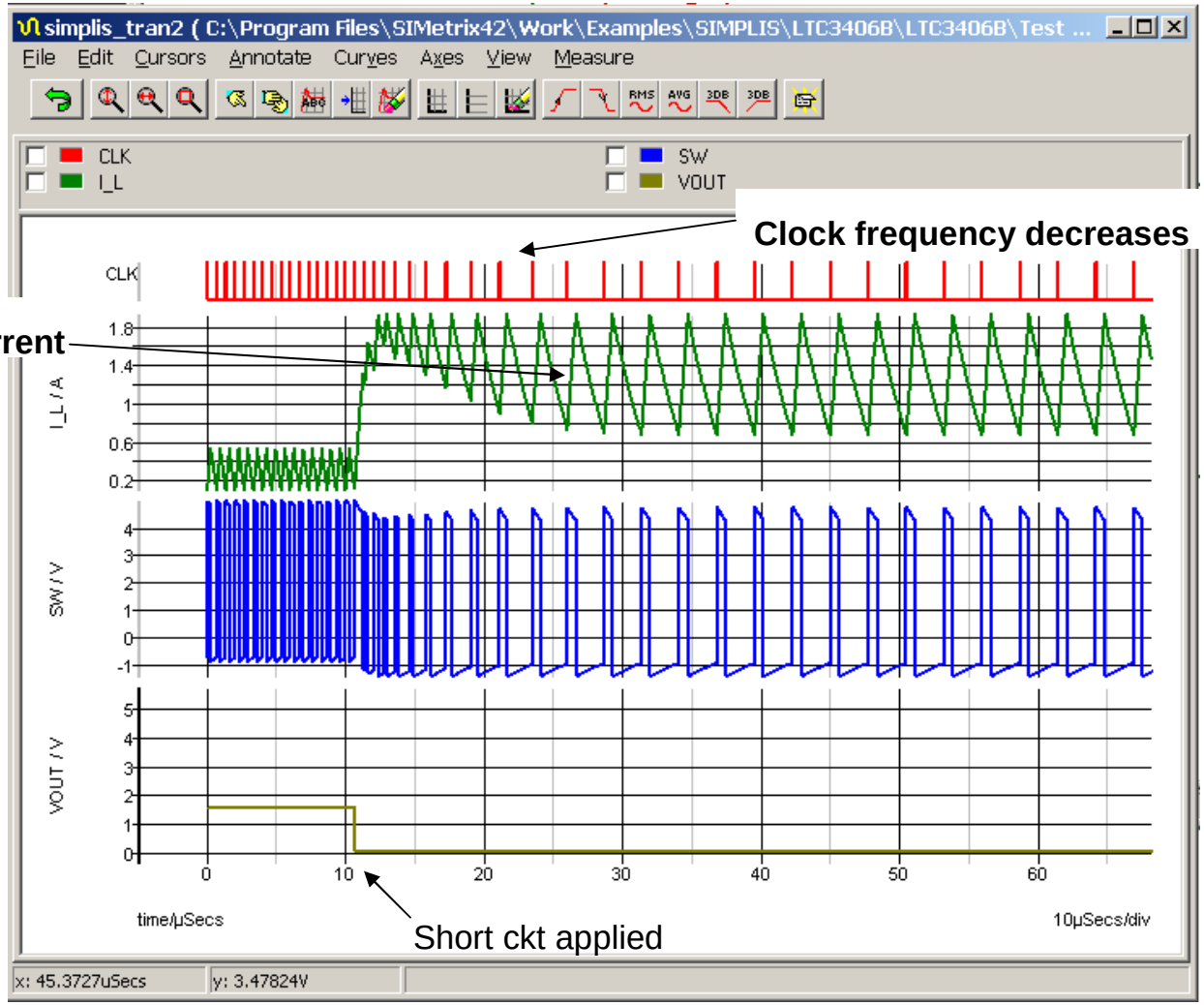
SIMPLIS TECHNOLOGIES

… explore how IC design parameters impact overall system performance of the final application



SIMPLIS TECHNOLOGIES

… under all application conditions, such as short circuit …



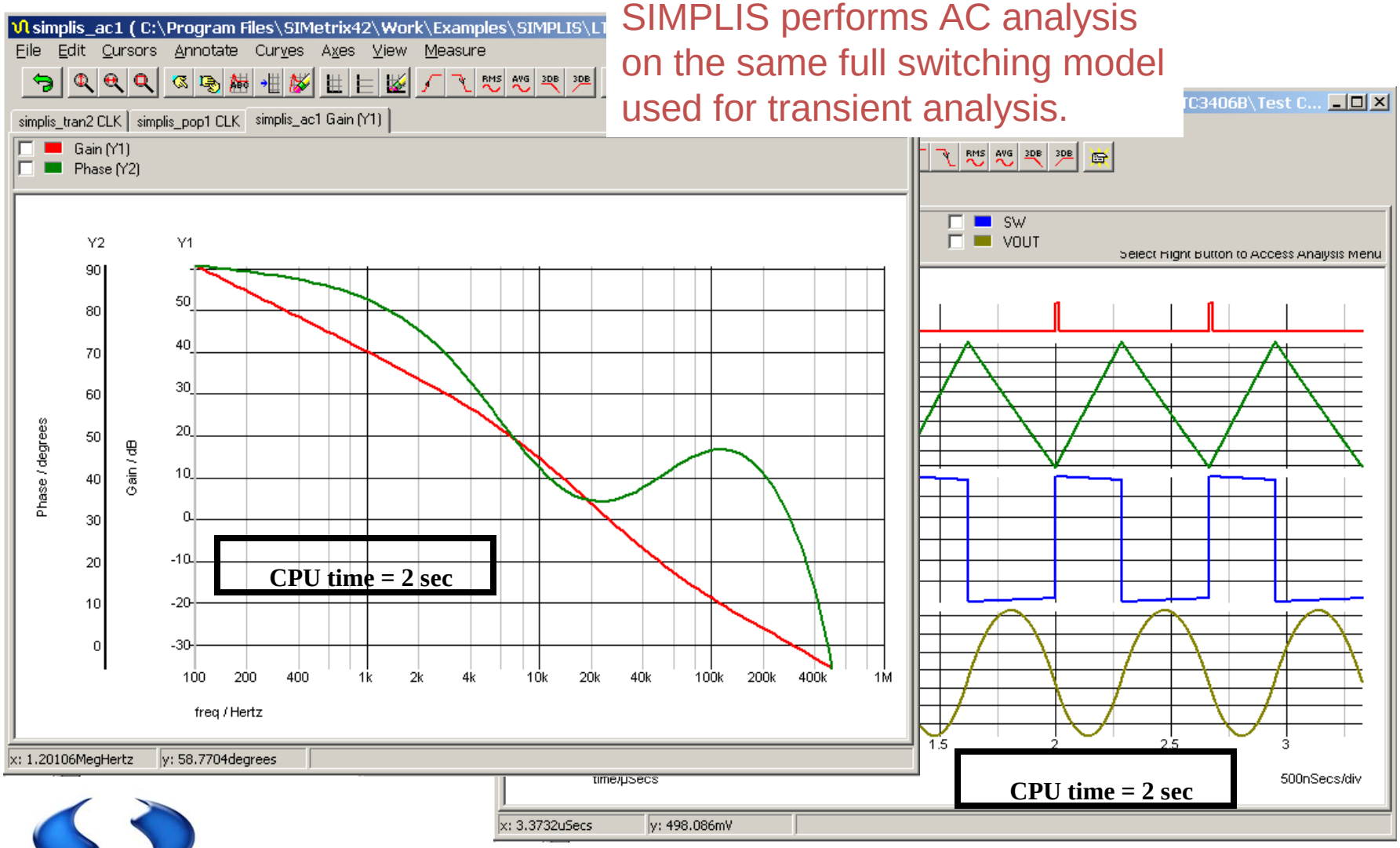
SIMPLIS is very fast

CPU time = 2 sec

SIMPLIS TECHNOLOGIES

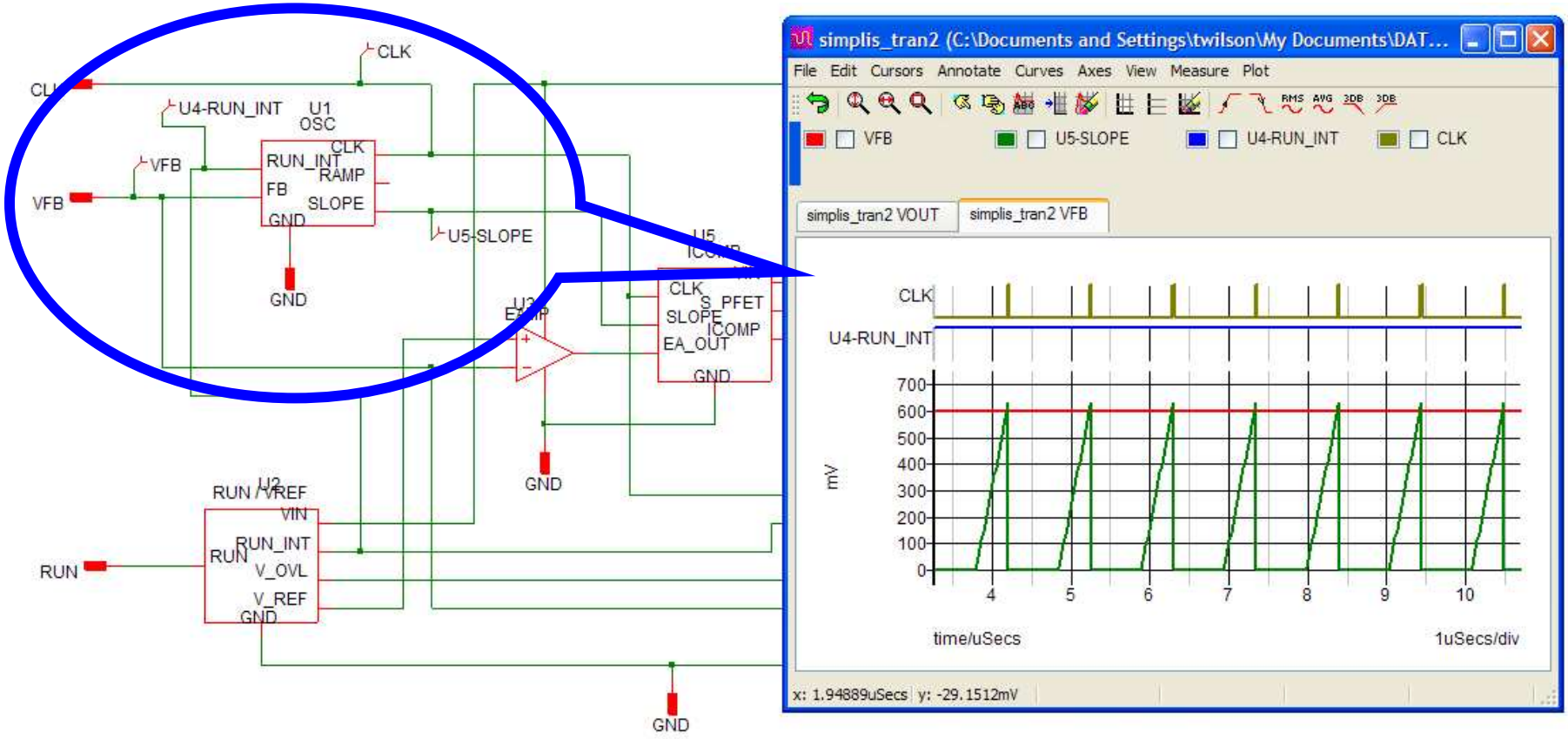
… and small signal stability.

SIMPLIS performs AC analysis on the same full switching model used for transient analysis.



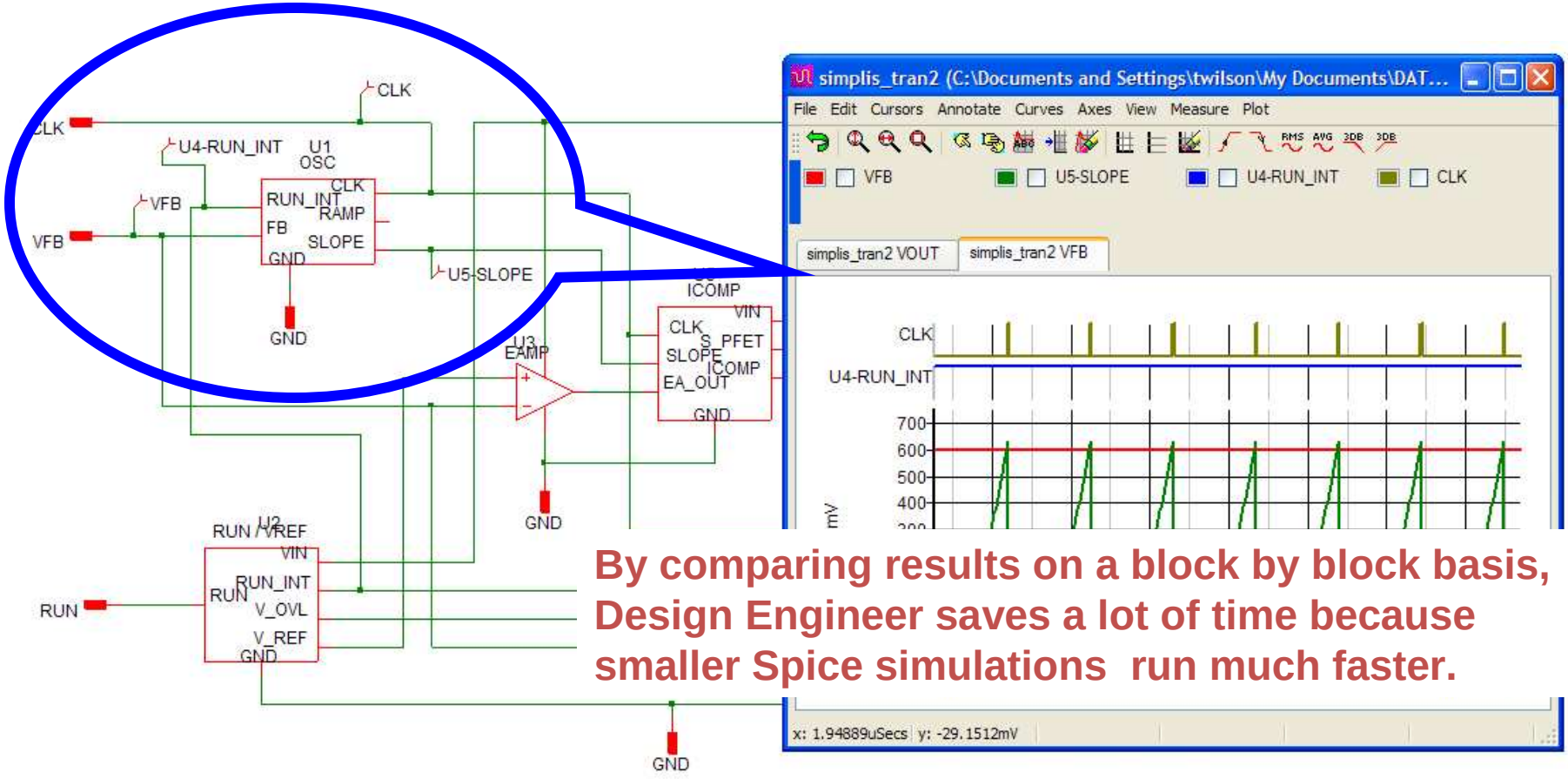
SIMPLIS TECHNOLOGIES

Clear I/O specs are generated for each Functional Block



SIMPLIS TECHNOLOGIES

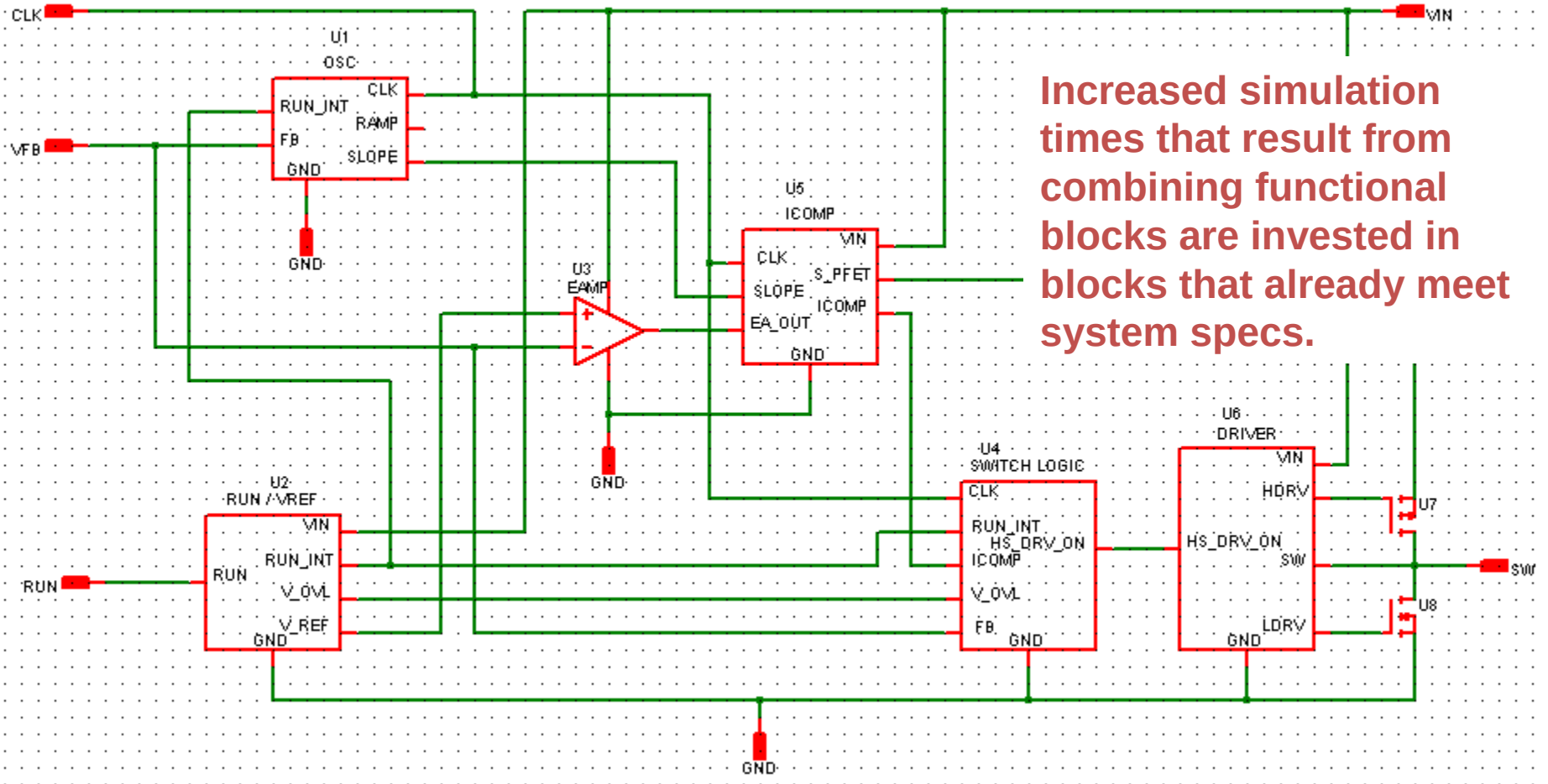
Compare Spice vs. SIMPLIS results for each Functional Block



By comparing results on a block by block basis, Design Engineer saves a lot of time because smaller Spice simulations run much faster.

SIMPLIS TECHNOLOGIES

Combine Spice Blocks once they all meet individual Block specs



Increased simulation times that result from combining functional blocks are invested in blocks that already meet system specs.

SIMPLIS TECHNOLOGIES

New Product Definition

SIMPLIS PWL Behavioral Models

- Quantitative specs on block by block basis reduces “dark interval” between spec handoff and IC design results
  - Ability to quantitatively compare Spice and SIMPLIS results on block by block basis
    - gives much more confidence that design is going in desired direction
- Very focused partnership between System Engineer and Design Engineers
    - Each concentrates on their value-added activities
    - Deviations from plan become visible to all parties very early in process
    - Allows clear delineation of responsibilities

SIMPLIS TECHNOLOGIES

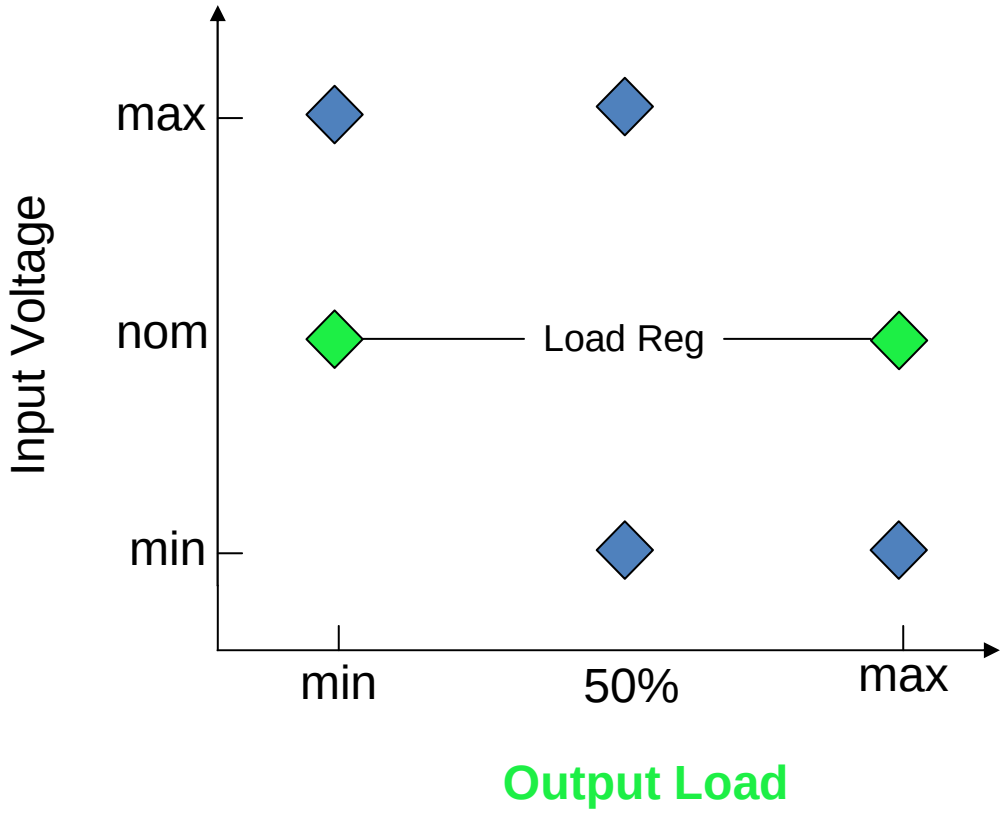
Virtual Prototyping -- some practical considerations

- To capture the full benefit of Virtual Prototyping, need to quickly verify New Product Definition performance over entire application space
- Example: Single Phase Synchronous Buck
  - What would a comprehensive Test Plan look like?*
  - How many tests per line and load range scenario?
  - How long would it take to complete?
  - What kind of results would be available?

SIMPLIS TECHNOLOGIES

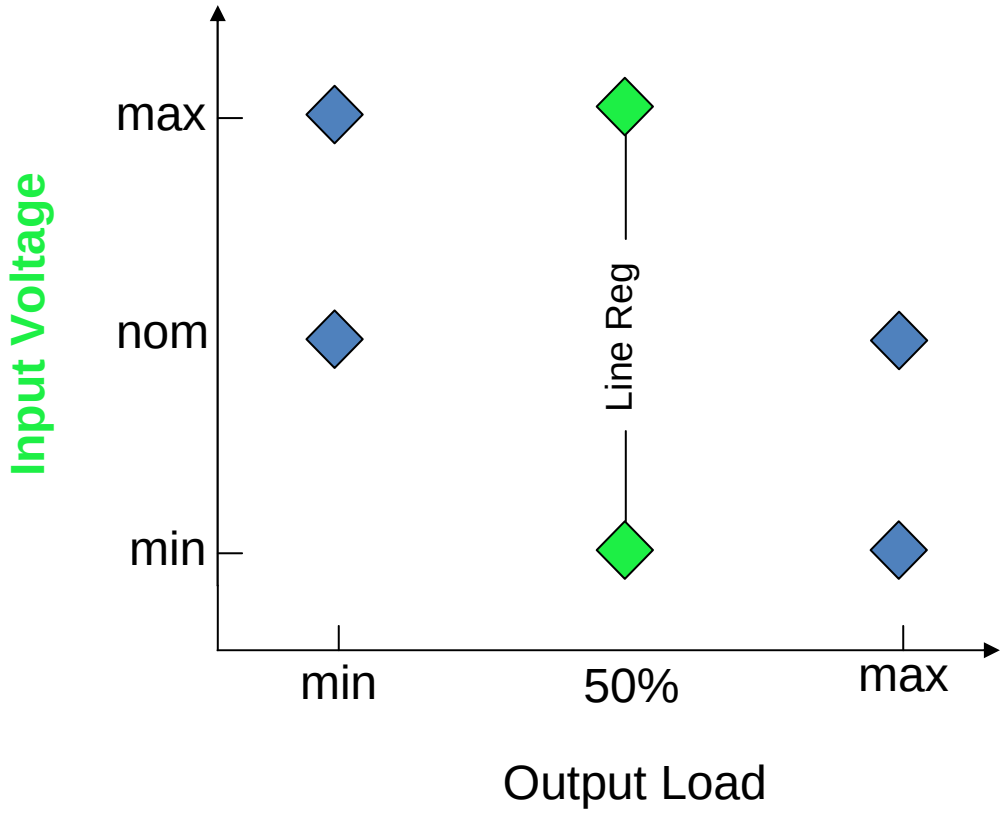
D.94.1

Load Regulation



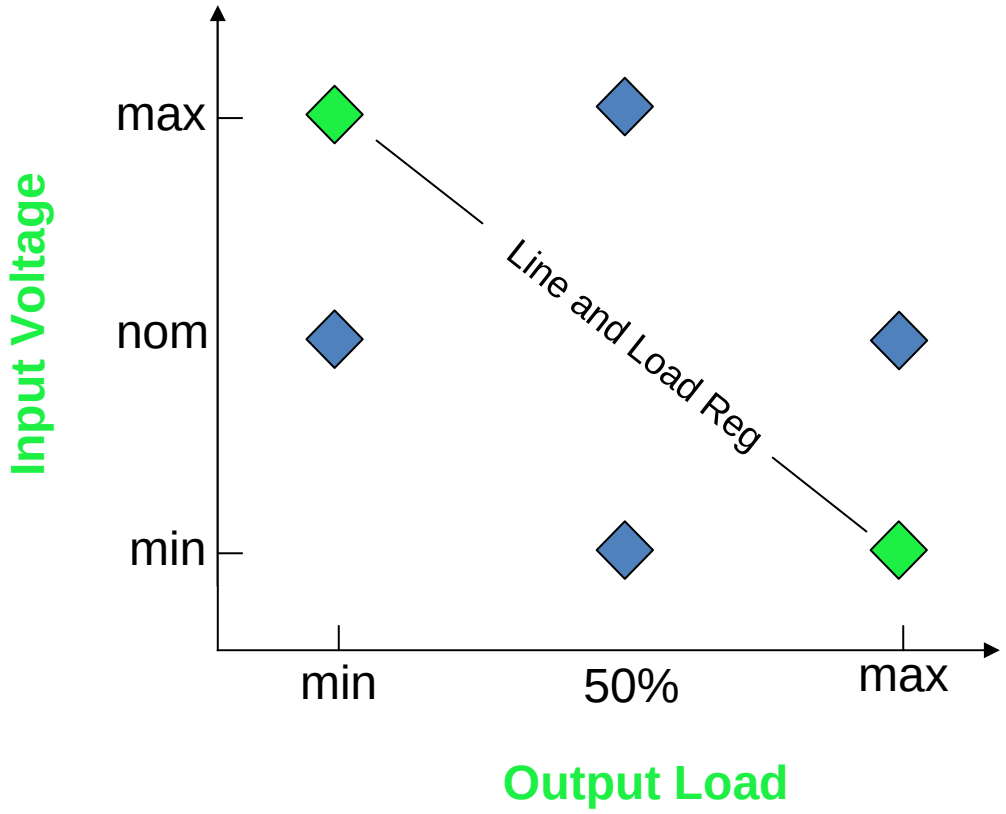
SIMPLIS TECHNOLOGIES

Line Regulation



SIMPLIS TECHNOLOGIES

Line & Load Regulation



SIMPLIS TECHNOLOGIES

Virtual Prototyping -- some practical considerations

- To capture the full benefit of Virtual Prototyping, need to quickly verify New Product Definition performance over entire application space
- Example: Single Phase Synchronous Buck
  - What would a comprehensive Test Plan look like?
  - How many tests per line and load range scenario?
    - Our Sync Buck Test Plan has ~ 130 individual simulations
  - How long would it take to complete?
    - ~ 10 min
  - What kind of results would be available?

SIMPLIS TECHNOLOGIES

D.99.1

Virtual Prototyping -- some practical considerations

- By applying PWL analysis, Multi-level modeling, and clearly focused simulation objectives
  - Now able to obtain accurate performance results over full application space in reasonable time
- Each test still requires
  - Configuration & execution
  - Results analysis & comparison with specs
  - Summary Report with links to detailed results
- When test mechanics > simulation time, automation can add value

SIMPLIS TECHNOLOGIES

Challenges for Virtual Prototyping

- Testing for all “known” design issues generates mountains of sim results
  - Need help organizing and sifting through test results
  - Drinking from this fire hose is not an exercise for the faint of heart
- Making results visible to entire design team reduces chances that important test results are overlooked

SIMPLIS TECHNOLOGIES

Virtual Prototyping -- some practical considerations

- Example: Single Phase Synchronous Buck
  - How approach Sensitivity & Worst Case analysis?
    - How many simulations to complete?
    - How much time?
    - How does this compare with Monte Carlo?

SIMPLIS TECHNOLOGIES

D.94.1

ISL70001

- Designers have indentified approximately 58 circuit parameters that should be included in a comprehensive Worst Case analysis
- Sensitivity Analysis => (58 + 1) sims per Objective Function
- Worst Case Analysis => (2 + 1) sims per Objective Function

With ~10 Objective functions => 620 sims

SIMPLIS TECHNOLOGIES

Design Verification Testing

- As Virtual Prototypes become more central to development efforts
  - there will be a need for tools to support the engineer in finding the important information amid large volume of data that will be generated
    - Automated comparison of results with requirements
    - Top-down reports with results viewable by entire design team

SIMPLIS TECHNOLOGIES

Design Verification Testing for Digital Control

- Design Definition
  - Discrete time, but infinite resolution
- Design Verification
  - Discrete time and include quantizing effects

SIMPLIS TECHNOLOGIES

D.105.1

Virtual Prototyping of Power Supply Designs

- Virtual Prototyping Process
  - From 3 Perspectives:
    - Power Supply Designer
    - Power Management IC Architect
    - **Power System Designer**

SIMPLIS TECHNOLOGIES

Virtual Prototyping for System Engineers

- Approximately 50% of system engineers are involved with designing on-board synchronous buck regulators
  - Same issues as all power supply designers
- Another big effort is working with vendors who supply critical power system functions like AC-DC Front Ends, Adapters, DC-DC Modules, etc.
  - Design Verification is big part of this responsibility
  - Virtual Prototyping is playing an increasingly important role in Vendor relationship

SIMPLIS TECHNOLOGIES

Virtual Prototyping and Power Supply Vendor Relationships

- Increasingly, Virtual Prototyping is being used to verify Vendor designs earlier and earlier in the process
- Some Systems Houses are beginning to require Virtual Prototype results as part of the RFQ response
- Virtual Prototypes are assuming a more important role in the Vendor relationship

SIMPLIS TECHNOLOGIES

Virtual Prototyping for System Engineers

- More Systems Houses are using Virtual Prototypes to resolve Power System level issues
  - Currently, detailed switching models work well for one or two power stages
  - Simulators are not able to handle simulation of many power stages with full detailed models
  - Power System simulation (with full detailed models) is coming, but not here yet

SIMPLIS TECHNOLOGIES

Summary (1)

- Virtual Prototyping
  - is becoming an increasingly important part of new product development process
    - Power Supply Designers
    - IC Controller Architects
    - Power System Engineers
  - represents the biggest design process improvement opportunity for many organizations

SIMPLIS TECHNOLOGIES

Summary (2)

- Maximizing Virtual Prototyping effectiveness requires
  - a clear and focused simulation strategy
    - an explicit simulation objective for every simulation
    - a corresponding understanding of the appropriate modeling level required to achieve simulation objective in reasonable simulation time
  - a comprehensive Test Plan that explicitly looks for known potential design faults
  - an effective way to communicate simulation strategy and test plans to the entire design organization

SIMPLIS TECHNOLOGIES

Summary (3)

- Virtual Prototypes are very effective in capturing closed loop system behavior
- We are getting smarter about how to use Virtual Prototypes to address device stresses and losses
- New tools needed to help manage the bookkeeping challenges posed by comprehensive Virtual Prototyping

SIMPLIS TECHNOLOGIES

Thank you!

Download Circuits and Materials:

http://simplistechnologies.com/downloads/apec2010

SIMPLIS TECHNOLOGIES