LEADING TECHNOLOGY
Semiconductor

L3400

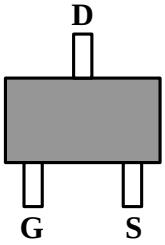
30V N-CHANNEL TRENCH FET

FEATURES

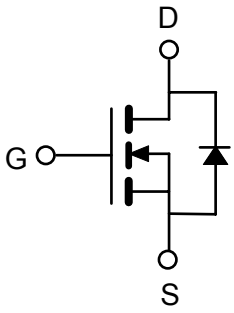
- BV_{DSS}=30V
- V_{gsth} =1.2V
- $R_{DS(ON)}$= 19.7mΩ @ V_{GS}=10V I_D=6A
- $R_{DS(ON)}$= 22.8mΩ @ V_{GS}=4.5V I_D=5A
- Q_g=20nC @ V_{GS}=10V

APPICATION

- Load Switch
- PWM application



SOT-23 Top View



ABSOLUTE MAXIMUM RATING

(T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Rating**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current[A]	T_A=25°C	I_D	5.6	A
	T_A=70°C		4.5	
Pulsed Drain Current[C]	Pulse	I_{DM}	32	
Single Pulse Avalanche Current[B]	T_A=25 °C	I_{AS}	14	A
Power Dissipation[A]	T_A=25°C	P_D	1.1	W
	T_A=70°C		0.7	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Single Avalanche Energy[B]	L=1mH	E_{AS}	100	mJ

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[A]	$R_{\theta JA}$	117	°C/W
Maximum Junction-to-Case[A]	$R_{\theta JC}$	47	°C/W

TRENCH FET ELECTRICAL CHARACTERISTICS

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250uA	30			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.7	1.2	1.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =24V, V_{GS} = 0 V			100	nA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D =6A		19.7	23.6	mΩ
		V_{GS} = 4.5 V, I_D =5A		22.8	27.4	
		V_{GS}=10V, I_D=6A, T_J=125°C		30		
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D =6A		16		S
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}=15V, V_{GS}=0V, f=1.0Mhz		894		pF
Output Capacitance	C_{OSS}			84		
Reverse Transfer Capacitance	C_{RSS}			67		
Total Gate Charge(V_{GS}=10V)	Q_g	V_{DS} =15V, I_D =6A		20		nC
Total Gate Charge(V_{GS}=4.5V)				9.3		
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			3		
Switching Characteristics[D]						
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=15V, R_{GEN}=3Ω, I_D =6A, V_{GS} =10V		4		nS
Rise Time	t_r			3		
Turn-Off Delay Time	$t_{d(off)}$			38		
Fall-Time	t_f			11		
Gate Resistance	R_g	f=1MHz		2.3		Ω
Body Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=1A		0.7	1	V
Reverse Recovery Time[D]	t_{rr}	V_{GS}=0V, I_F=8A, dI_F/dt=100A/us		15		ns
Diode Reverse Charge[D]	Q_{rr}			6		nC

Notes:

A, The value of $R_{\theta JA}$ and $R_{\theta JC}$ were measured with device mounted on tested board based on JESD51-7 requirement, and in still air environment with T_A=25° C in according to JESD51-2.

B, Single pulse UIS energy, inductor=1mH, V_{GS}=10V , T_{start}=25° C.

C, Pulse width limited by junction temperature $T_{j\,(mxa)}$=150° C, the pulse current value was based on T_A=25° C, repetitive rating based on duty cycles to keep initial T_j=25° C.

D, Pulse test: PW ≤ 300us duty cycle ≤ 2%.

Typical Electrical Characteristics (N-Channel)

T_A = +25ºC, unless otherwise noted

Figure 1. On-Regions Characteristics

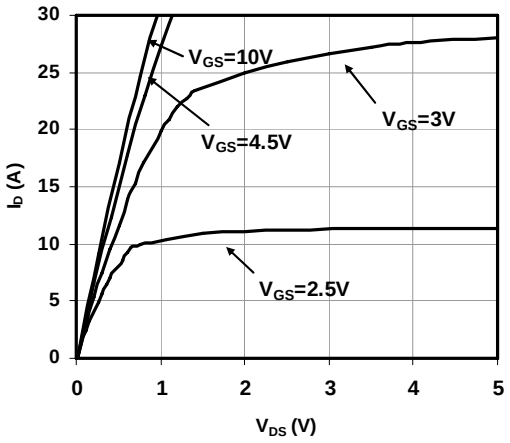


Figure 2. On-Resistance versus Drain Current

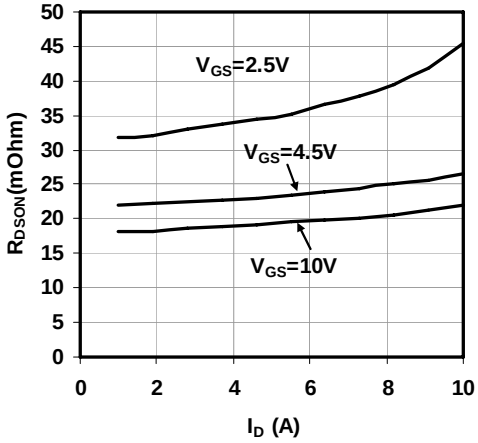


Figure3. On-Resistance Normalized versus Temperature

V_{GS}=10V, I_{DS}=6A

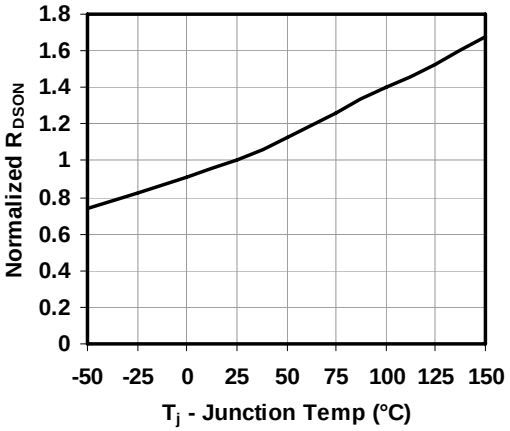


Figure 4. On-Resistance versus Gate to Source Voltage

I_{DS}=6A

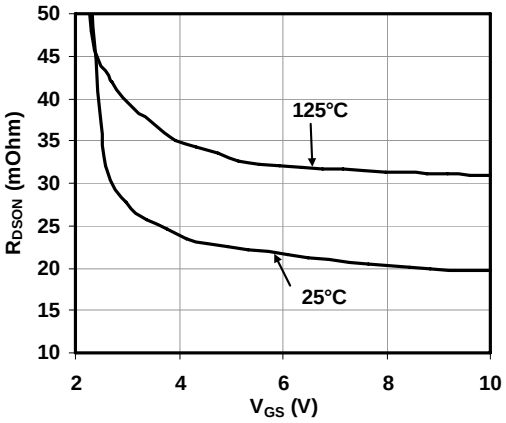


Figure 5. Transfer Characteristics

V_{DS}=5V

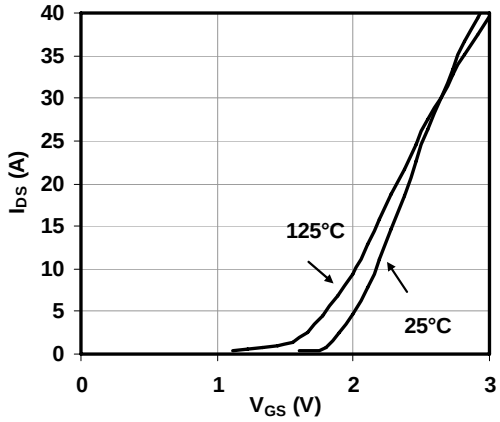
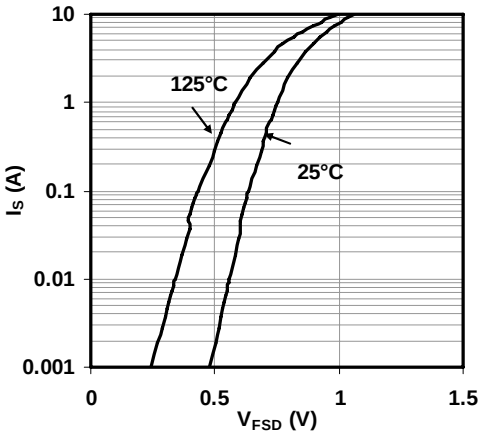


Figure 6. Body Diode Forward Voltage versus Source Current



Typical Electrical Characteristics (N-Channel)

T_A = +25ºC, unless otherwise noted

Figure 7. Threshold versus Temperature

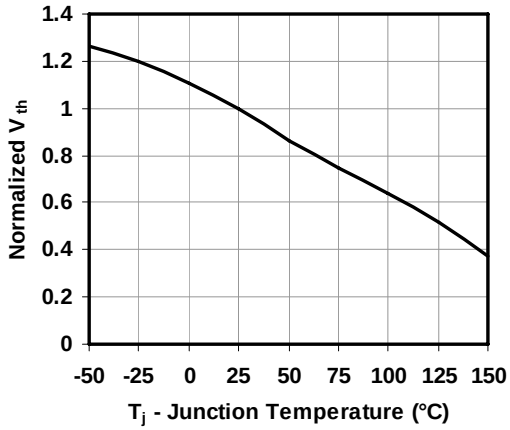


Figure 8. Body Diode Forward Voltage versus Temperature

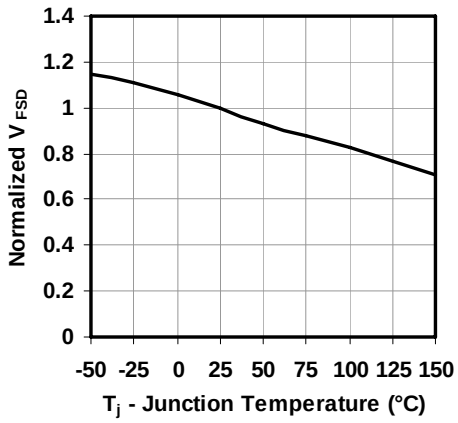


Figure 9. Gate Charge Characteristics

V_{DS}=15V I_{DS}=6A

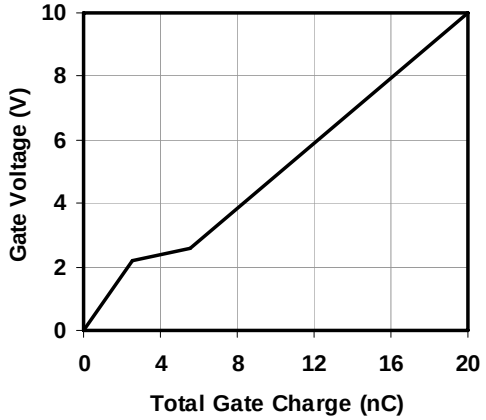
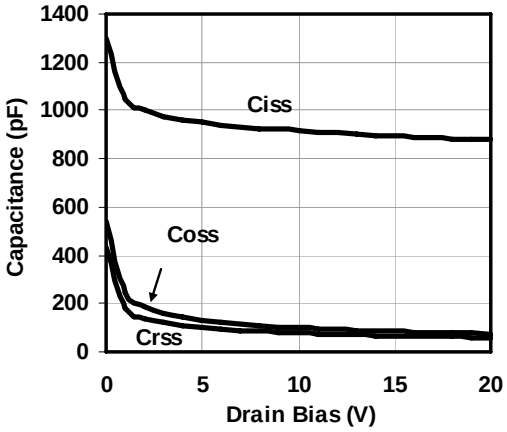
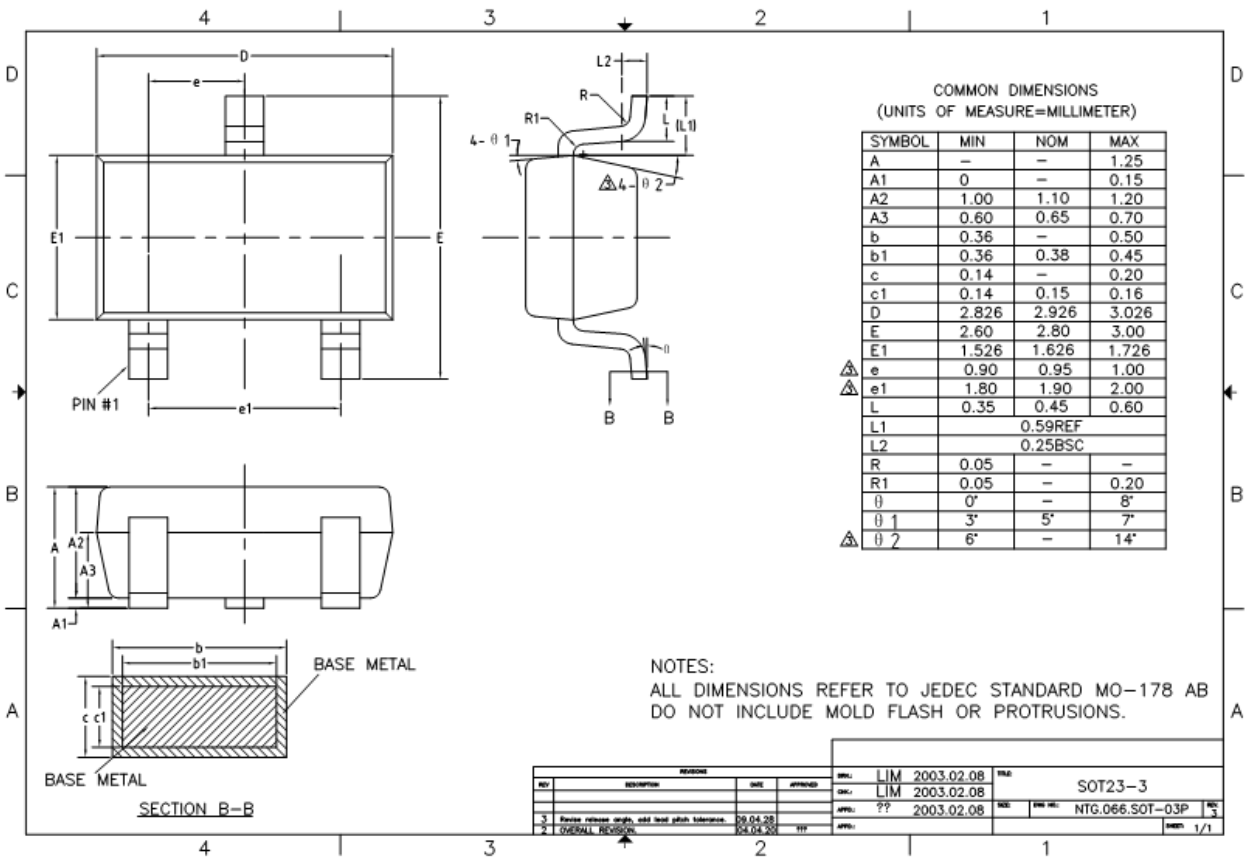


Figure 10. Capacitance Characteristics

f=1MHz



SOT23 Package Outline Drawing



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.25
A1	0	–	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	–	0.50
b1	0.36	0.38	0.45
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.05	–	–
R1	0.05	–	0.20
θ	0°	–	8°
θ 1	3°	5°	7°
θ 2	6°	–	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–178 AB
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

REV	DESCRIPTION	DATE	APPROVED
3	Revise release angle, add lead pitch tolerance.	08.04.28	
2	OVERALL REVISION.	04.04.20	???

DRN: LIM 2003.02.08
CHK: LIM 2003.02.08
APPD: ?? 2003.02.08
APPD:

TITLE: SOT23–3
SIZE: A | DWG NO: NTG.066.SOT–03P | REV: 3
SHEET 1/1