LEADING TECHNOLOGY
Semiconductor

L8822

20V COMMON-DRAIN DUAL N-CHANNEL TRENCH FET

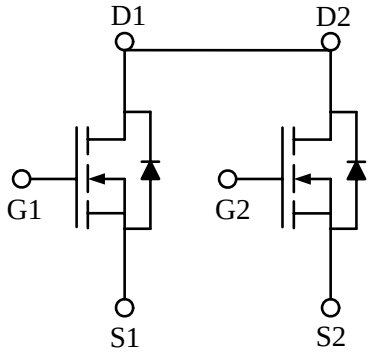
FEATURES

- BV_{DSS}=20V
- V_{gsth} =0.8V
- $R_{DS(ON)}$=14mΩ @ V_{GS}=10V I_D=7A
- $R_{DS(ON)}$=15.4mΩ @ V_{GS}=4.5V I_D=7A
- Q_g=18.7nC @ V_{GS}=4.5V

TSSOP-8 Top View

APPICATION

- Load Switch



ABSOLUTE MAXIMUM RATING

(T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Rating**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Drain Current[A]	T_A=25°C	I_D	7.9	A
	T_A=100°C		5	
	Pulse	I_{DM}	30	
Single Pulse Avalanche Current[B]	T_A=25 °C	I_{AS}	11.5	A
Power Dissipation[A]	T_A=25°C	P_D	1.3	W
	T_A=100°C		0.5	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Single Avalanche Energy[B]	L=1mH	E_{AS}	180	mJ

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[A]	$R_{\theta JA}$	94	°C/W
Maximum Junction-to-Case[A]	$R_{\theta JC}$	41	°C/W

Note:

A, The value of $R_{\theta JA}$ and $R_{\theta JC}$ were measured with device mounted on tested board based on JESD51-7 requirement, and in still air environment with TA=25° C in according to JESD51-2.

B, Single pulse UIS energy, inductor=1mH, V_{GS}=10V , T_{start}=25° C.

TRENCH FET ELECTRICAL CHARACTERISTICS

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250uA	20			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.5	0.8	1	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =18V, V_{GS} = 0V			100	nA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7A		14	16.5	mΩ
		V_{GS} = 4.5 V, I_D =7A		15.4	18.5	
		V_{GS}=10V, I_D=7A, T_J=125°C		20.4	24.5	
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D = 7A		26		S
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}=15V, V_{GS}=0V, f=1.0Mhz		1480		pF
Output Capacitance	C_{OSS}			180		
Reverse Transfer Capacitance	C_{RSS}			152		
Total Gate Charge(V_{GS}=10V)	Q_g	V_{DS} =15V, I_D = 7A		39		nC
Total Gate Charge(V_{GS}=4.5V)				18.7		
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			6.5		
Switching Characteristics[C]						
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=15V, R_{GEN}=3Ω, I_D =7A, V_{GS} =10V		5		nS
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall-Time	t_f			8		
Gate Resistance	R_g	f=1MHz		1.7		Ω
Body Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=1A		0.7	0.9	V
Reverse Recovery Time[C]	t_{rr}	V_{GS}=0V, I_F=7A, dI_F/dt=100A/us		18		ns
Diode Reverse Charge[C]	Q_{rr}			34		nC

Notes:
C, Pulse test: PW ≤ 300us duty cycle ≤ 2%.

Typical Electrical Characteristics (N-Channel)

T_A = +25ºC, unless otherwise noted

Figure 1. On-Regions Characteristics

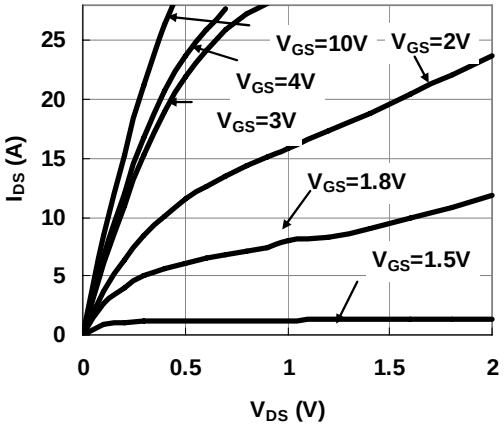


Figure 2. On-Resistance versus Drain Current

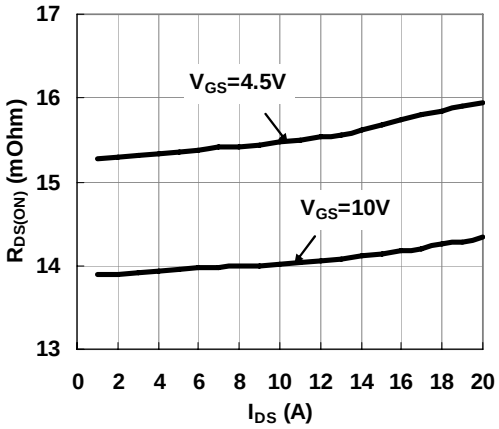


Figure3. On-Resistance versus Temperature

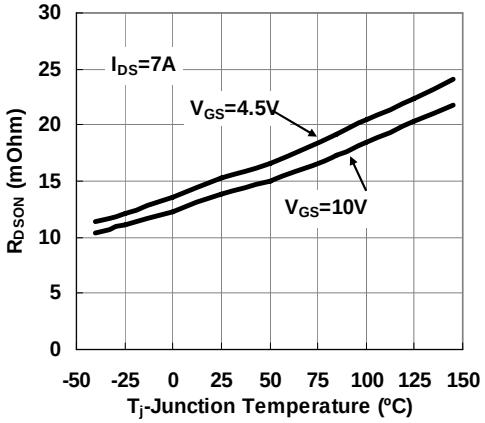


Figure 4. On-Resistance versus Gate to Source Voltage

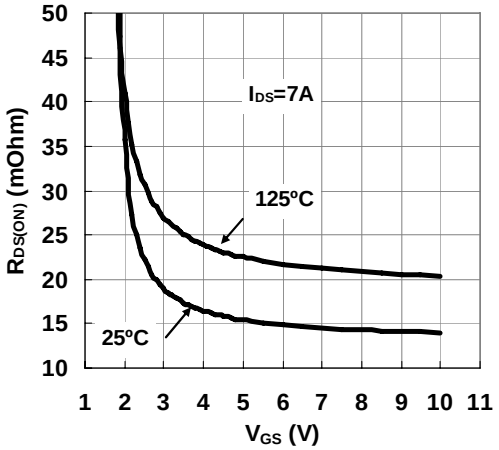


Figure 5. Transfer Characteristics

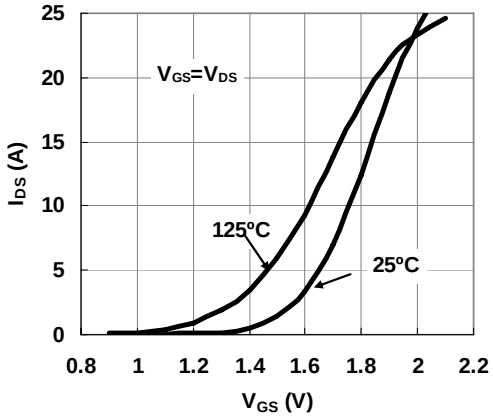
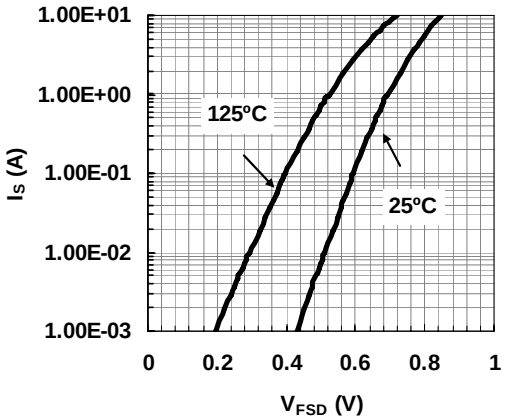


Figure 6. Body Diode Forward Voltage versus Source Current



Typical Electrical Characteristics (N-Channel)

T_A = +25ºC, unless otherwise noted

Figure 7. Normalized V_{TH} versus Temperature

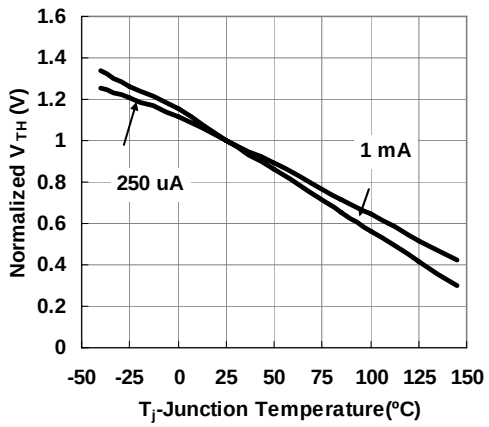


Figure 8. Normalized V_{SD} versus Temperature

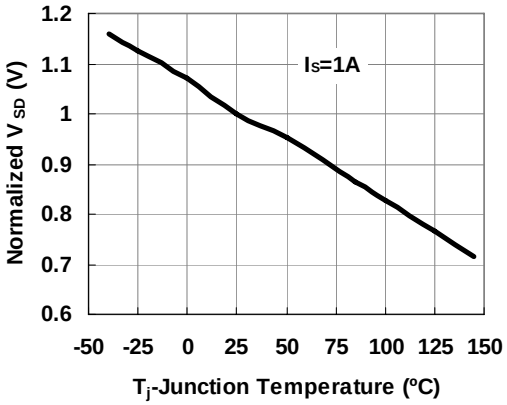


Figure 9. Gate Charge Characteristics

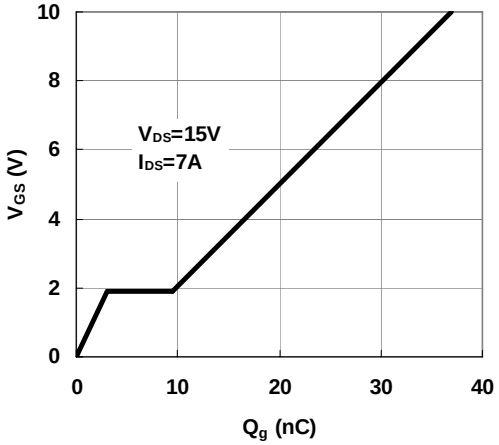
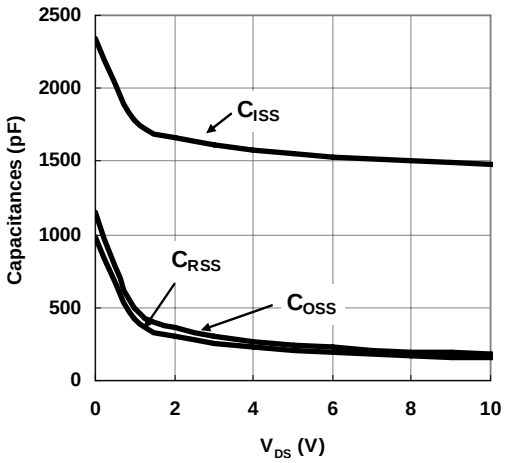
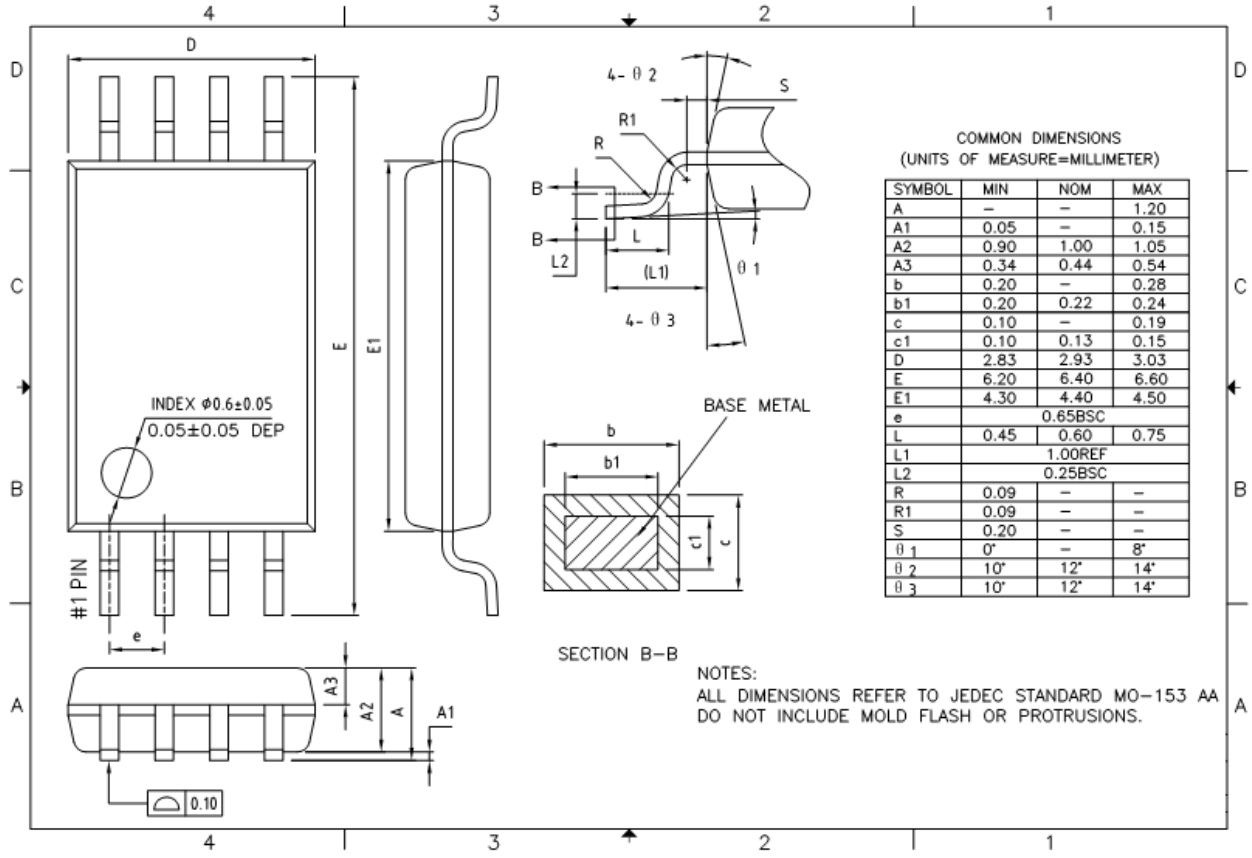


Figure 10. Capacitance Characteristics



TSSOP-8 Package Outline Drawing



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	2.83	2.93	3.03
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.