A Novel Symmetrical Rectifier Configuration With Low Voltage Stress and Ultralow Output-Current Ripple

Chen Zhao, Min Chen, Guoxing Zhang, Xinke Wu, *Member, IEEE*, and Zhaoming Qian, *Senior Member, IEEE*

***Abstract*—The dc–dc topologies with capacitive output filter are going to be widely used especially for high-output current applications because of its inherent advantages in the lower voltage stress on rectifiers and the smaller occupied printed circuit board layout area at the secondary side. However, the parasitic resonance between the equivalent leakage inductance of the power transformer and the equivalent output junction capacitance of the rectifier still practically exists in the center-tapped rectification configuration, which leads to considerable voltage ringing on the rectifier and then results in the utilization of the rectifier with much higher breakdown voltage rate and the decrease of conversion efficiency. Moreover, the relatively larger output-current ripple induces the both larger conduction loss in the secondary-side windings of the power transformer and the capacitive output filter. In this paper, a novel symmetrical rectifier configuration is proposed, which can effectively clamp the practical voltage stress on the rectifier without any parasitical voltage spike and reduce the output-current ripple due to the bypass effect of the auxiliary flying-balancing capacitors. The leakage inductance and the output filter capacitor can be treated as an inherent small *LC* filter to reduce the output voltage ripple further. Based on the theoretical analysis and the optimal design considerations, a 300-W lab-made *LLC* resonant dc–dc converter with this proposed configuration is built up to verify its advantages in high conversion efficiency.**

***Index Terms*—Capacitive filter, dc–dc converter, high efficiency, low voltage stress, synchronous rectifier.**

I. Introduction

With the rapid development in consumer electronics, the traditional ac/dc power supply adapter with relatively larger package size and lower power density would not meet the prospective market requirement anymore, especially in portability which is going to be one of the most important features of the next generation consumer electronics. Therefore, the advanced ac/dc power supply adapter with smaller package size and higher power density will definitely obtain most of the market share in the near future.

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C. Zhao was with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China. He is now with Silergy Corporation, San Jose, CA 95131, USA (e-mail: chanezhao@zju.edu.cn).

M. Chen, G. Zhang, X. Wu, and Z. Qian are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, Zhejiang Province, China (e-mail: calim@zju.edu.cn; gxzhny@zju.edu.cn; wuxinke@zju.edu.cn; qian@zju.edu.cn).

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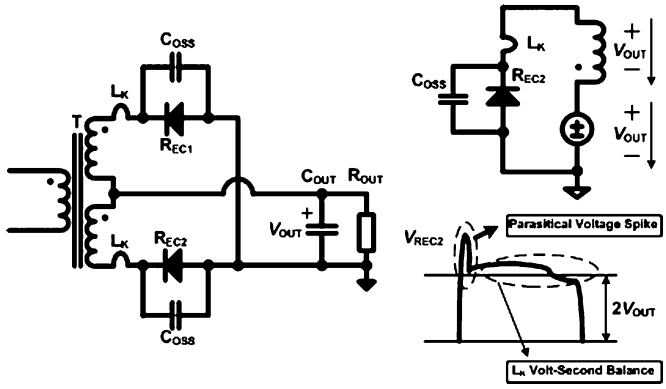


Fig. 1. Conventional center-tap rectifier configuration.

It is well-known that only the natural convection cooling is allowed for the power supply adapter. As the package size increases along with the increase of the power level, the ratio of the package surface area to the package volume will reduce, which means the reduction of the effective heat dissipating capability. Therefore, in order to upgrade the power density of the adapter, its conversion efficiency must be pushed up further to meet the rigorous thermal limitation. Otherwise, the power density has to be reduced to ensure the reliability of the heat dissipation. For this reason, the centre-tapped rectifier configuration with capacitive output filter as shown in Fig. 1 is going to be widely used in the front-end dc/dc converter of the ac/dc power supply adapter especially for the high output-current applications because of its inherent advantages in lower conduction loss and smaller occupied printed circuit board (PCB) layout area, for example in *LLC* resonant dc/dc converter [1]–[18] and in soft-switched phase-shift full-bridge dc/dc converter with primary-side energy storage inductor (PSFB-PESI) [19], [20]. Obviously, synchronous rectifier (SR) can be used instead of diode rectifier for high efficiency. However, the practical voltage stress on the secondary-side rectifiers is always higher than 2 $V_{\rm OUT}$ because of the voltage spike during the switch transition caused by parasitic resonance between the leakage inductance L_K of power transformer and the equivalent output junction capacitance ($C_{\rm OSS}$) of output rectifier, and the considerable volt-second balance across L_K when operating at high-load current condition [21].Therefore, the power supply engineer cannot utilize the output rectifiers with much lower breakdown voltage rate to reduce the conduction loss and the switching loss further. Besides, the relatively large output-current ripple would not only increase the conduction loss in the secondary-side windings of the power

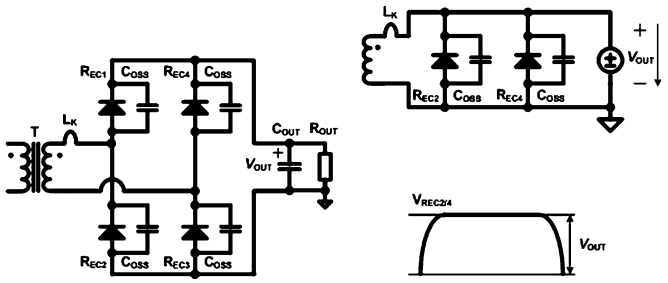


Fig. 2. Conventional full-bridge rectifier configuration.

transformer, but also would lead to large output voltage ripple, which always needs bulky electrolytic aluminum capacitors to reduce and then meet the given design specification of the ac/dc power supply adapter. A full-bridge rectifier configuration with capacitive output filter shown in Fig. 2 can effectively clamp the voltage stress on the rectifiers at $V_{\rm OUT}$ without any parasitical voltage spike even in the practical application areas, and then the output rectifiers with much lower breakdown voltage rate can be utilized, which means much lower $R_{\rm DSON}$ of the MOSFET or much lower forward voltage V_F of the schottky diode. However, the efficiency benefit obtained from the lower $R_{\rm DSON}$ or the lower V_F would always be counteracted by the increase of the utilized rectifier amount, and the total manufacture cost is going to be higher. Moreover, this rectifier configuration still suffers the considerable large output-current ripple and when the SR is employed for the high output-current applications, the driving circuit for the high-side rectifiers would be rather difficult and complex.

Based on Fig. 1, [22] and [23] present a novel low voltage stress (LVS) rectifier configuration as shown in Fig. 3(a). Zhao *et al.* [24] present the basic operation principle and the relative optimum design considerations when utilized in *LLC* resonant dc/dc converter and the PSFB-PESI dc/dc converter. The voltage stress on the output rectifiers can be effectively clamped at 2 $V_{\rm OUT}$ without any parasitical voltage spike through two equivalently series-connected capacitors, the auxiliary flying-balance capacitor $C_{\rm AUX}$ and the output filter capacitor $C_{\rm OUT}$, as shown in Fig. 3(b). Even employing the current mode driving strategy to drive the SRs, the residual energy stored in the leakage inductance of the current transformer $L_{\rm KCT}$ and the trace parasitical inductance is still too low to cause the considerable voltage spike, as shown in Fig. 3(c). Then the output rectifier with much lower breakdown voltage rate can be utilized for the practical applications. Additionally, thanks to the ac component bypass effect of $C_{\rm AUX}$, the reduced output-current ripple helps to decrease the electrolytic aluminum capacitors utilization amount at the output side and the current rms value in the secondary-side windings of the power transformer. Therefore, the conversion efficiency and the power density can be effectively improved further.

Although compared with the conventional rectifier configuration shown in Fig. 1, the LVS rectifier configuration proposed in [22] can help to reduce the voltage ripple on the capacitive output filter due to the ac component bypass effect of $C_{\rm AUX}$. According to the theoretical analysis presented in [24], the output-current ripple is always optimum designed to be about half of the entire secondary-side current ripple, and a small additional *LC* filter at the output side is still necessary sometime to meet the given requirement of the output-voltage ripple. To reduce the output-current ripple further and save the small additional *LC* filter, this paper presents a novel symmetrical rectifier configuration with capacitive output filter as shown in Fig. 4(a), which has the outstanding features in LVS and ultralow output-current ripple. It has the voltage stress clamping cell and energy transfer cell similar to the LVS rectifier configuration as shown in Fig. 4(b), and thanks to the symmetrical configuration consisting of four secondary-side windings and two auxiliary flying-balance capacitors $C_{\rm AUX1/2}$; the voltage stress on the SRs can not only be effectively clamped at 2 $V_{\rm OUT}$ without any parasitical voltage spike but also the output-current ripple can be considerably reduced. The leakage inductance of the power transformer at the secondary side can be treated as an inherent small filter inductance and help to reduce the voltage ripple on the output-capacitive filter further. The feasibility to remove the small additional *LC* output filter would bring in the lower conduction loss at the output side and the smaller occupied PCB layout area. It means the improvement of the conversion efficiency and the power density. For high-output current applications, SR is always utilized for the lower conduction loss and can be easily driven by the current mode driving strategy, which has been already presented and analyzed in [18] and [25]. Section II elaborates the basic operation principle of the proposed symmetrical rectifier configuration when it is employed in *LLC* resonant dc/dc converter and PSFB-PESI dc/dc converter, respectively, and Section III focuses on several optimum design considerations. Finally, two 300-W lab-made *LLC* resonant dc/dc converter prototypes with the conventional rectifier configuration and the proposed rectifier configuration are built up, respectively, to compare and verify the presented theoretical analysis about the proposed one's outstanding advantages in LVS and ultralow output-current ripple, which would be good for high conversion efficiency.

II. Operation Principle Analysis

The proposed symmetrical SR configuration is suitable for the *LLC* resonant dc/dc converter and the PSFB-PESI dc/dc converter to obtain high conversion efficiency and high power density as shown in Fig. 5(a). For the primary-side of *LLC* resonant converter, its half-bridge consists of two power MOSFETs, $\rm Q_1$ and $\rm Q_2$, and the series resonant tank is composed of the resonant inductance L_R and the resonant capacitance C_R. L_M can be the magnetizing inductance of the power transformer or the added inductance in parallel with the power transformer. For the primary-side of PSFB-PESI converter, its full-bridge consists of four power MOSFETs, $\rm Q_1$–$\rm Q_4$. L_R is the primary-side series energy storage inductor and the series capacitor C_B blocks the dc bias for the power transformer. The transformer windings consist of w_P as its primary-side winding, and w_{S1}–w_{S4} as its four secondary-side windings. Note that the secondary-side windings' turns ratio and the configuration should be kept symmetric, which would be analyzed in Section III. $L_{\rm SK1}$–$L_{\rm SK4}$ represent

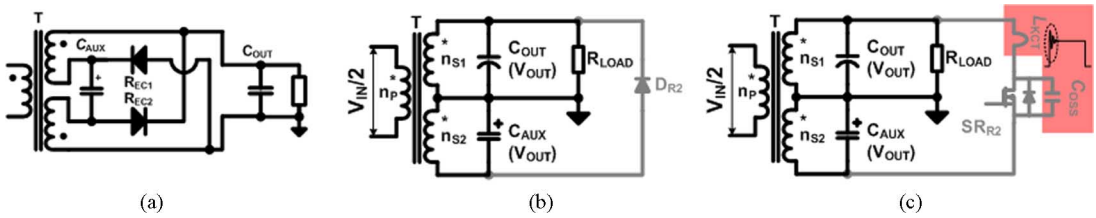


Fig. 3. (a)–(c) LVS output rectifier configurations proposed in [22] and [24].

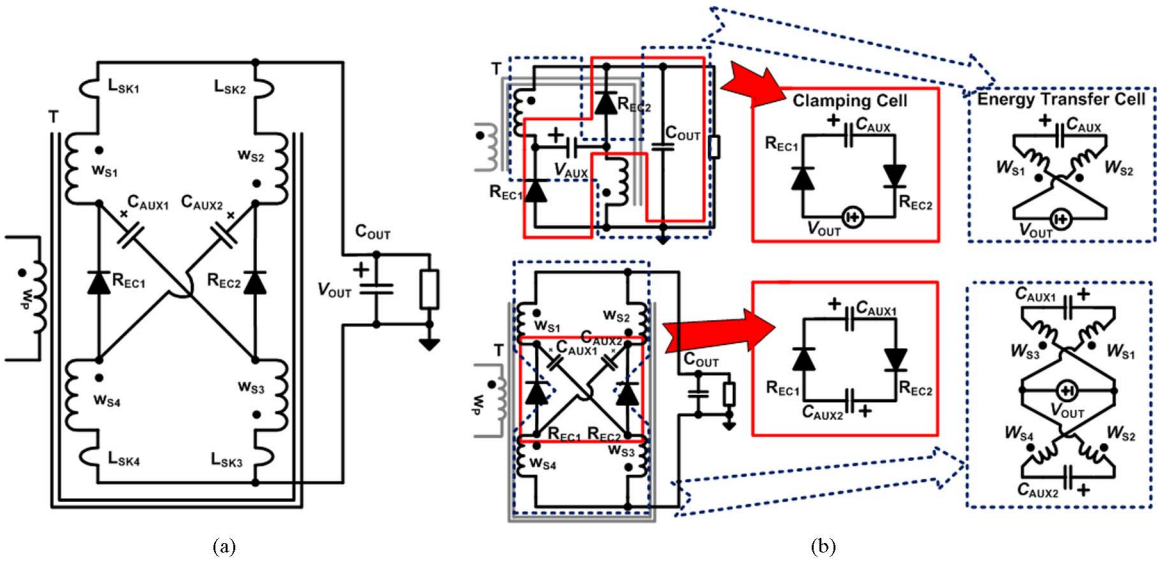


Fig. 4. (a) and (b) Proposed symmetrical rectifier configurations with low voltage stress and ultralow output-current ripple.

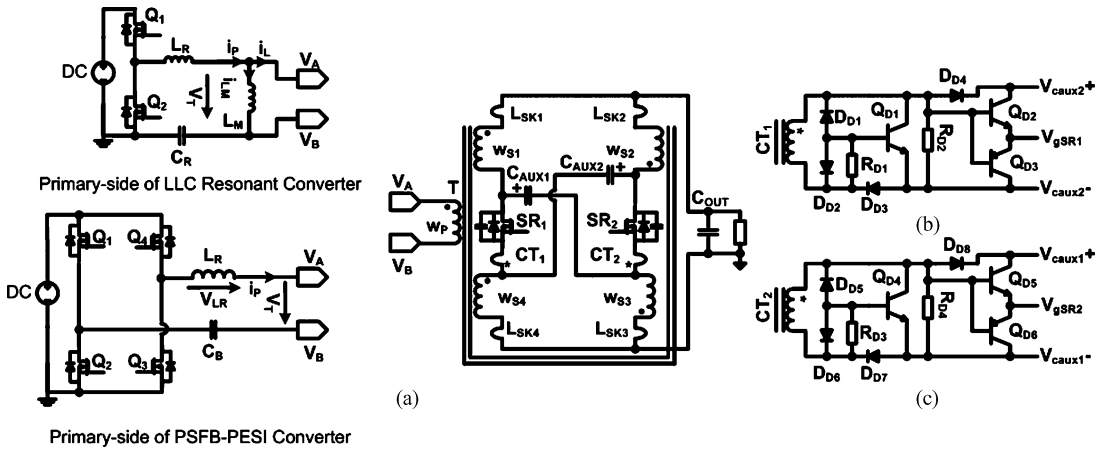


Fig. 5. (a)–(c) Proposed symmetrical SR configuration with current mode driving circuit.

the total equivalent leakage inductances of each secondary-side winding including the leakage inductances reflected from the primary-side. SR_1 and SR_2 are two synchronous rectifiers, which are driven by the same current mode driving circuit as shown in Fig. 5(b) and (c) [25]. C_{AUX1} and C_{AUX2} are two auxiliary flying-balance capacitors.

To be brief, only the discontinuous conduction mode (DCM) operation principle at the secondary side is elaborated in this section and the primary-side operation principle analysis of both the *LLC* resonant dc/dc converter and the PSFB-PESI dc/dc converter are all the foregoing work, which can be referred in detail from [1]–[20], and the continuous conduction mode operation principle could be easily deduced based on the presented DCM principle.

Some reasonable assumptions are listed below to simplify the basic operation principle analysis process: 1) neglect the forward voltage V_F of diode and the ON resistance R_{DSON} of MOSFET; 2) all the capacitors are constant and linear; 3) neglect all the parasitic components except the leakage inductance of the power transformer; 4) neglect the deadtime interval between the driving signal of the primary-side switches in the same bridge leg; 5) neglect the voltage ripple on C_{AUX1} and C_{AUX2}; and

6) the primary-side series capacitor guarantees no dc bias in the power transformer. Figs. 6 and 7 show the key operation modes and the relevant waveforms in theoretical of these two converters in DCM, respectively.

A. Topology I: LLC Resonant dc/dc Converter

Mode1 (t_0–t_1): During this mode, the secondary-side rectifier SR_1 is ON and the energy is transferred from the primary input side to the secondary output side. The voltage stress V_T on the transformer's primary-side winding is clamped at $n_T V_{\mathrm{OUT}}$ by the output voltage. SR_1 takes all the secondary-side current i_{SR1}, which equals to the reflected current of the primary-side resonant current i_P minus the power transformer's magnetizing current i_{LM} of the power transformer. They should be valid in the equations as shown in the following:

$$i_P(t) = \sqrt{2} I_{\mathrm{PRMS}} \sin(2\pi f_R t - t_\theta) \tag{1}$$

$$\begin{aligned} i_{\mathrm{LM}}(t) &= I_{\mathrm{LM}}(t_0) + \frac{n_T V_{\mathrm{OUT}}}{L_M}(t - t_0) \\ &= -\frac{n_T V_{\mathrm{OUT}}}{2L_M}(t_1 - t_0) + \frac{n_T V_{\mathrm{OUT}}}{L_M}(t - t_0) \end{aligned} \tag{2}$$

$$\begin{aligned} i_{\mathrm{SR1}}(t) &= i_p(t) - i_{\mathrm{LM}}(t) = \sqrt{2} I_{\mathrm{PRMS}} \sin(2\pi f_R t - t_\theta) \\ &\quad + \frac{n_T V_{\mathrm{OUT}}}{2L_M}(t_1 - t_0) - \frac{n_T V_{\mathrm{OUT}}}{L_M}(t - t_0) \end{aligned} \tag{3}$$

$$\frac{2\int_{t_0}^{t_1} i_{\mathrm{SR1}}(t)dt}{T_S} = I_{\mathrm{OUT}} = \frac{V_{\mathrm{OUT}}}{R_{\mathrm{OUT}}}. \tag{4}$$

where I_{PRMS} is the rms value of the primary-side current, f_R is the resonant frequency of the primary-side series resonant tank, t_θ is the leading angle of i_P, n_T is the turns ratio of the power transformer, T_S is the switching period, R_{OUT} is the output load, and I_{OUT} is the output load current.

If the auxiliary flying capacitances C_{AUX1} and C_{AUX2} are large enough, the voltage ripple across them can be neglected during the theoretical analysis, and their steady-state voltage equals to the output voltage V_{OUT}. Therefore, the voltage stress on SR_2 could be effectively clamped at 2 V_{OUT} by these two equivalently series-connected capacitors, and then the energy stored in the leakage inductance L_{SK} is too low to oscillate with them and cannot cause considerable parasitical voltage spike on the secondary-side rectifier anymore. Moreover, the entire secondary-side current ripple suffered by SR_1 would be shared by C_{AUX1} and C_{AUX2} equally, which means that there is no current ripple flowing into the output filter capacitor C_{OUT}, and then the secondary-side winding w_{S1} would also have to suffer the dc current bias supporting the output load. The peak current in SR_1 can be obtained from (7) and (8)

$$i_{\mathrm{SW1}}(t) = \frac{i_{\mathrm{SR1}}(t) + I_{\mathrm{OUT}}}{2} \tag{5}$$

$$i_{\mathrm{SW2}}(t) = \frac{i_{\mathrm{SR1}}(t) - I_{\mathrm{OUT}}}{2} \tag{6}$$

$$I_{\mathrm{SP1}} = i_{\mathrm{SR1}}(t)\big|_{\frac{di_{\mathrm{SR1}}(t)}{dt}=0} = i_{\mathrm{SR1}}(t_P) \tag{7}$$

$$t_P = \frac{\cos^{-1}\left(\sqrt{2} n_T V_{\mathrm{OUT}} / 4\pi f_R L_M I_{\mathrm{PRMS}}\right) + t_\theta}{2\pi f_R}. \tag{8}$$

where $i_{\mathrm{SW1/2}}$ and $i_{\mathrm{SR1/2}}$ are the current in the secondary-side windings and the SRs, respectively, I_{SP1} is the peak current of i_{SR1}, and t_P is the peak current time of i_{SR1}.

Mode2 (t_1–t_2): During this mode, the secondary side is going to operate in DCM because i_P equals to i_{LM}, and then SR_1 can be turned OFF with zero current switching (ZCS). The output energy is mainly supported by C_{AUX1} and C_{AUX2} transferred through all the four symmetrical secondary-side windings. If L_M's impedance Z_{LM} is designed enough larger than the primary-side resonant tank's impedance Z_R, the SRs' voltage stress is approximately around V_{OUT}.

Mode3 (t_2–t_3): Thanks to the proposed symmetrical rectifier configuration, this mode is exactly similar to mode1. The energy is transferred from the primary input side to the secondary output side through the secondary-side windings w_{S2}, w_{S3}, and SR_2.SR_2 takes the entire secondary-side current ripple, which is still equally shared by the auxiliary flying-balance capacitors. Therefore, there's no current ripple flowing into the output filter capacitor as earlier. The voltage stress on SR_1 could be effectively clamped at 2 V_{OUT} by the equivalently series-connected C_{AUX1} and C_{AUX2} and without any parasitical voltage spike.

Mode4 (t_3–t_4): This mode is similar to mode2, and SR_2 also can be turned OFF with ZCS. After the end of this mode, the converter begins next switching cycle on the same operation principle.

B. Topology II: PSFB-PESI dc/dc Converter

Being similar to the secondary-side operation principle in DCM of *LLC* resonant dc/dc converter with the proposed symmetrical SR configuration mentioned earlier, PSFB-PESI dc/dc converter just has differences in the current waveform shape as shown in Fig. 7, and the relevant expressions are described in the following.

Mode1 (t_0–t_1): During this mode, the energy is transferred from the primary input side to the secondary output side through the secondary-side windings w_{S2}, w_{S3}, and SR_1. The current in SR_1 i_{SR1} is reflected directly from the primary-side current i_P, which can be expressed in (9) and (10). The auxiliary flying-balance capacitors, C_{AUX1} and C_{AUX2}, separately share one-half of the entire secondary-side current ripple suffered by SR_1 to eliminate the current ripple flowing into C_{OUT}. The voltage stress on SR_2 could be effectively clamped at 2 V_{OUT} in a similar same way as analyzed earlier

$$i_{\mathrm{SR1}} = \begin{cases} \frac{n_T (V_{\mathrm{IN}} - n_T V_{\mathrm{OUT}})}{L_R}(t - t_0), & t_0 \le t \le t_0 + \frac{DTs}{2} \\ n_T \left[\frac{DT_S (V_{\mathrm{IN}} - n_T V_{\mathrm{OUT}})}{2L_R} - \frac{n_T V_{\mathrm{OUT}}}{L_R}\left(t - \frac{DTs}{2} - t_0\right)\right], & t_0 + \frac{DTs}{2} \le t \le t_1 \end{cases} \tag{9}$$

$$I_{\mathrm{SP1}} = \frac{DT_S (V_{\mathrm{IN}} - n_T V_{\mathrm{OUT}})}{2L_R} \tag{10}$$

where D is the operation switching duty cycle.

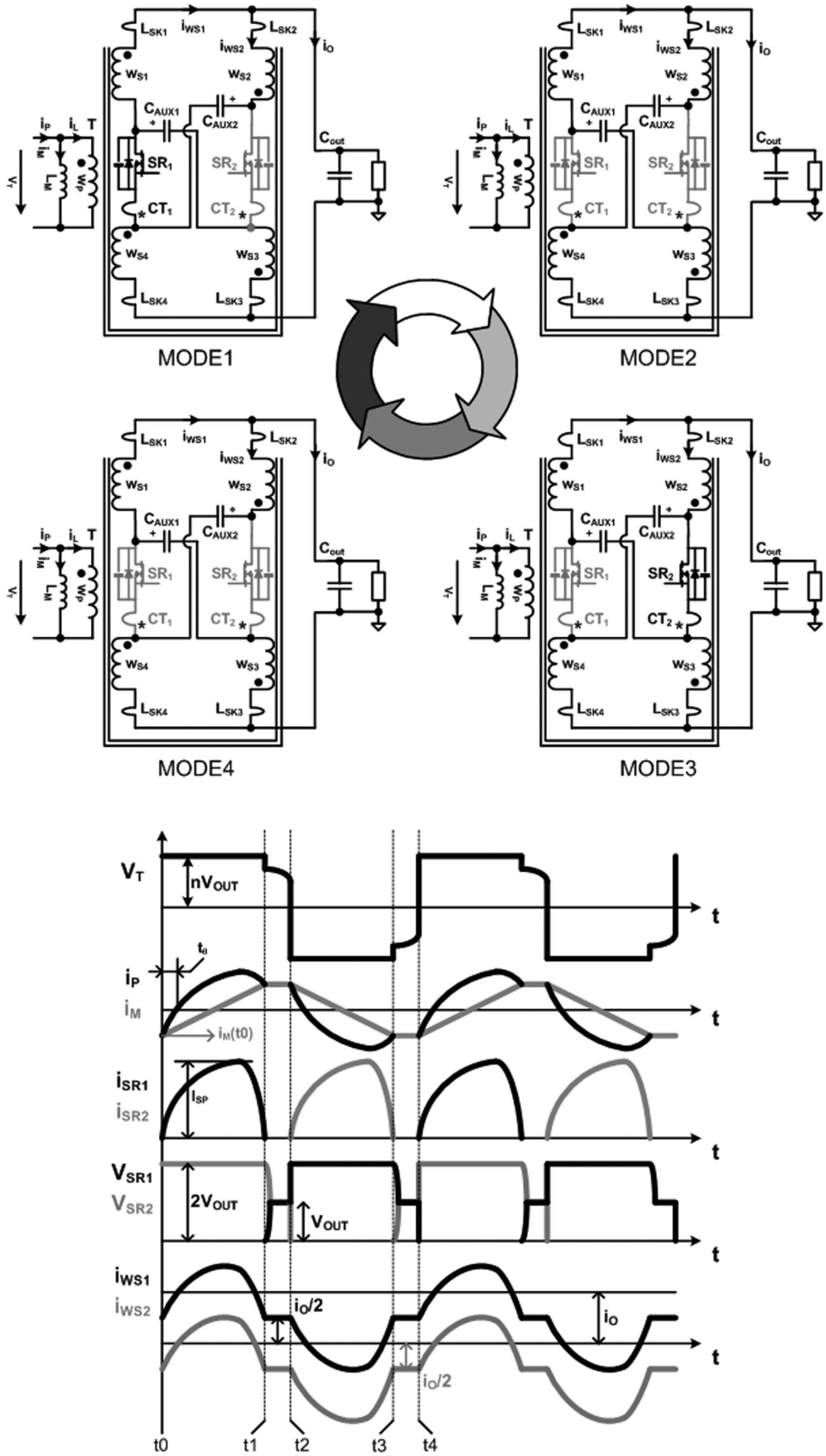


Fig. 6. Key operation modes and relevant theoretical waveforms in DCM (*LLC* resonant dc/dc converter).

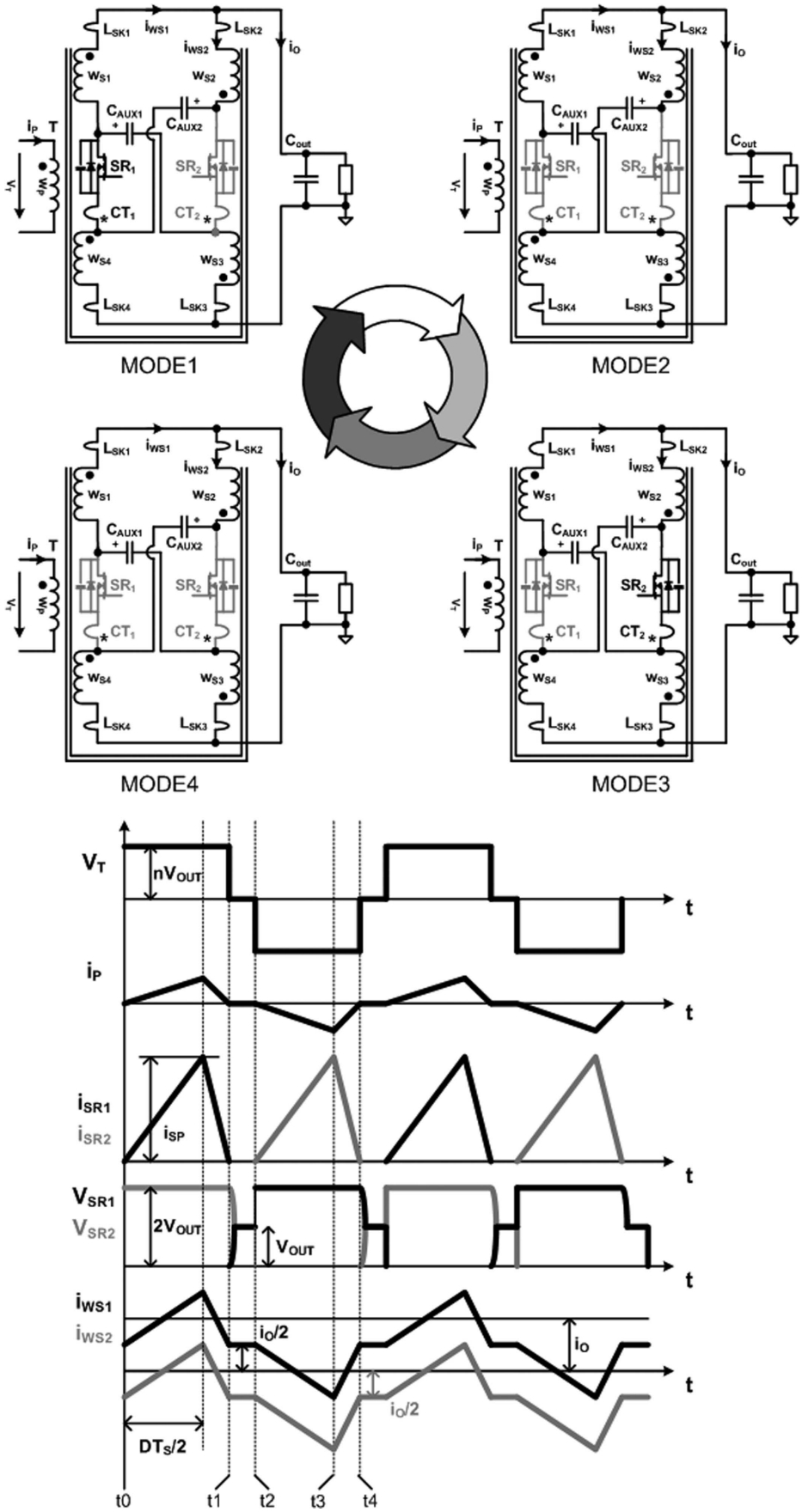


Fig. 7. Key operation modes and relevant theoretical waveforms in DCM (PSFB-PESI dc/dc converter).

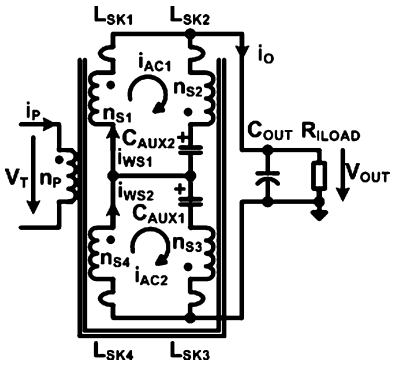


Fig. 8. Equivalent circuit of the proposed configuration in half energy transfer period.

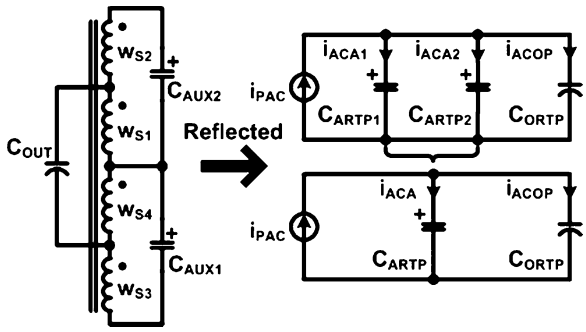


Fig. 9. Ideal equivalent circuit of the proposed configuration reflected to the primary side.

Mode2 (t_1–t_2): During this mode, i_P reaches zero as well as $i_{\rm SR1}$. $\rm SR_1$ could be turned OFF with ZCS. $C_{\rm AUX1}$ and $C_{\rm AUX2}$ support the output energy transferred through all the four symmetrical secondary-side windings. The SRs' voltage stress is approximately around $V_{\rm OUT}$.

After this mode, the proposed symmetrical rectifier configuration makes the following two modes, mode3 from t_2 to t_3 and mode4 from t_3 to t_4, to be the same as the previous two, respectively. After the end of mode4, the converter begins next switching cycle on the same operation principle.

III. Optimum Design Considerations

This section focuses mainly on several optimum design considerations for the proposed symmetrical rectifier configuration. As usual, the steady-state dc gain should be analyzed and deduced first during the whole design process, especially for the power transformer design, and then the output-current ripple eliminating principle should be anatomized, which is necessary for the power supply engineers to employ this configuration for the practical applications. The analysis of the effective voltage stress clamping for the secondary-side rectifier is presented successively. Based on these design consideration, the proposed rectifier configuration would show its obvious advantages in high conversion efficiency and high power density compared with the conventional rectifier configuration especially for the practical high-output current applications. To simplify the optimum design analysis process, the secondary-side windings w_{S1} and w_{S4} are named as $w_{\rm GA}$, winding group A, and the others w_{S2} and w_{S3} are named as $w_{\rm GB}$, winding group B.

A. Steady-State dc Gain Analysis

According to the basic operation principle presented earlier, the equivalent circuit of this rectifier configuration in the half energy transfer period can be obtained as shown in Fig. 8. It can be seen that the output load energy only flows through the winding $w_{\rm GA}$ (w_{S1} and w_{S4}) at the secondary side in this period, and the winding $w_{\rm GB}$ (w_{S2} and w_{S3}) just suffers parts of the entire secondary-side current ripple. The energy transfer process in next half period is symmetrical, similar to the previous half. Therefore, the turns ratio of the power transformer windings can be derived from (11) easily, which is valid for both *LLC* resonant dc/dc converter and PSFB-PESI dc/dc converter

$$\frac{V_T}{V_{\rm OUT}} = \frac{n_P}{n_{S1}+n_{S4}} = \frac{n_P}{n_{S2}+n_{S3}} = \frac{n_P}{n_{w_{\rm GA}}} = \frac{n_P}{n_{w_{\rm GB}}}. \quad (11)$$

where n_P is the primary-side winding turns of the power transformer and n_{S1}–n_{S4} are the secondary-side windings turns. Therefore, it can be seen that the turns of the secondary-side winding $w_{\rm GA}$ should be equal to that of the winding $w_{\rm GB}$.

B. Output-Current Ripple Elimination

Although the proposed symmetrical rectifier configuration has its inherent advantage in output-current ripple elimination which can help to reduce the voltage ripple on the capacitive output filter and save the small additional *LC* filter to meet the given requirement of the output-voltage ripple, the detailed theoretical analysis is still necessary for the power supply engineers in the practical applications. Generally, neglecting all the leakage inductances of the power transformer can effectively simplify the equivalent circuit during the energy transfer period as shown in Fig. 9, where $C_{\rm ARTP1}$ and $C_{\rm ARTP2}$ are two equivalent capacitors of $C_{\rm AUX1}$ and $C_{\rm AUX2}$ reflected from the secondary-side to the primary-side and can be combined into $C_{\rm ARTP}$ together, and $C_{\rm ORTP}$ is the equivalent reflected capacitor of the output filter $C_{\rm OUT}$. The ac current source $i_{\rm PAC}$ represents the entire primary-side ac current that can be divided into three different parts: $i_{\rm ACA1}, i_{\rm ACA2}$, and $i_{\rm ACOP}$. Current $i_{\rm ACA1}$ and $i_{\rm ACA2}$ flow in $C_{\rm ARTP1}$ and $C_{\rm ARTP2}$, respectively, and can be combined into $i_{\rm ACA}$ together, and $i_{\rm ACOP}$ flows in $C_{\rm ORTP}$. Based on this ideal equivalent circuit, the ac current source $i_{\rm PAC}$ is divided in the proportion of the impedance of $C_{\rm ARTP}$ and $C_{\rm ORTP}$ as expressed in (12). Therefore, in order to effectively achieve the output-current ripple elimination, $C_{\rm ARTP}$ should be larger than $C_{\rm ORTP}$ enough to bypass the ac current ripple as much as possible

$$i_{\rm PAC} = i_{\rm ACA} + i_{\rm ACOP} = i_{\rm ACA}\left(1+\frac{C_{\rm ORTP}}{C_{\rm ARTP}}\right) = i_{\rm ACOP}\left(1+\frac{C_{\rm ARTP}}{C_{\rm ORTP}}\right). \quad (12)$$

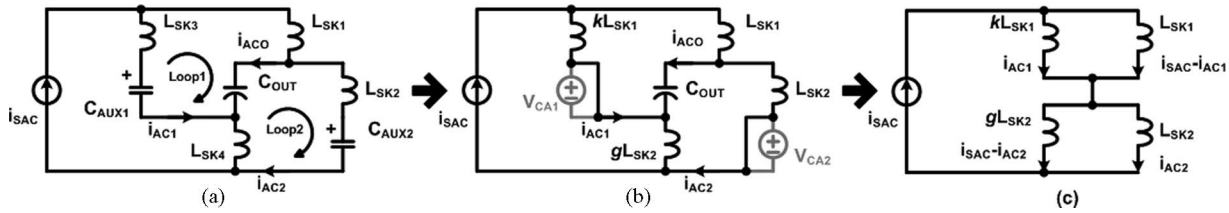


Fig. 10. (a)–(c) Improved equivalent circuits for the practical applications.

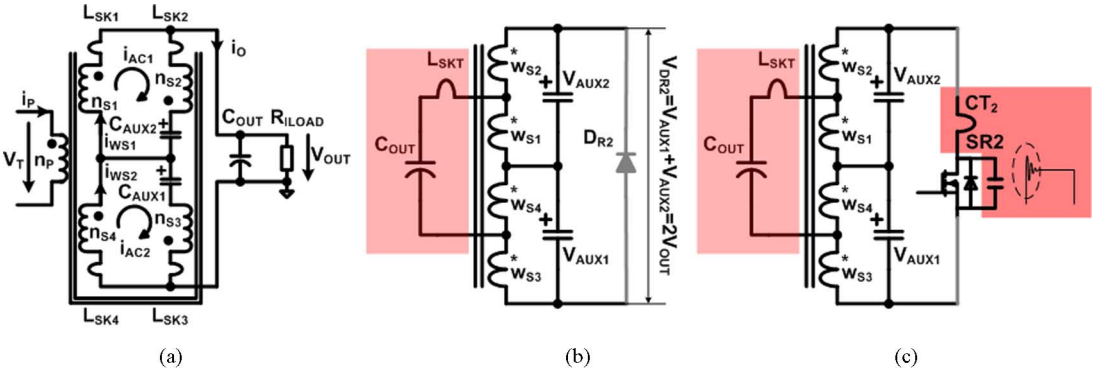


Fig. 11. (a)–(c) Equivalent circuit for the voltage stress across the rectifier.

Actually, the leakage inductance of the power transformer always exists and should be taken into account especially during the practical design process, no matter how the hand-made windings or the planar PCB windings are utilized. Then, this ideal equivalent circuit must be improved further to fit the practical application as shown in Fig. 10(a). The ac current source i_{SAC} represents the entire secondary-side ac current ripple, which can also be divided into three parts: $i_{\mathrm{AC1}}, i_{\mathrm{AC2}}$, and i_{ACO} flowing in $C_{\mathrm{AUX1}}, C_{\mathrm{AUX2}}$, and C_{OUT}, respectively. Their relationship is expressed in (13). Compared with the ac current ripple flowing in C_{AUX1} and C_{AUX2}, the voltage ripple on them is supposed to be negligible, which leads to a simpler equivalent circuit as shown in Fig. 10(b), where L_{SK3} is defined as kL_{SK1}, and L_{SK4} is defined as gL_{SK2}. Equation (14) can be derived from the simplest equivalent circuit as shown in Fig. 10(c), and then the output-current ripple elimination can be achieved effectively if the coefficient k equals to g. It shows the symmetrical characteristic of the secondary-side winding configuration. The capacitive output filter, which is much smaller in size and capacitance, can be utilized to reduce the occupied area and the complexity of the PCB layout at the secondary side.

Note that when both the coefficients k and g equal to 1, i_{AC1} equals to i_{AC2}, which means that all the four secondary-side windings equally suffer half of the entire secondary-side current ripple as shown in Figs. 6 and 7. It also reduces the conduction loss in the secondary-side windings because of the lower current rms value. On the other hand, although C_{AUX1} and C_{AUX2} are simply treated as the constant voltage sources during the aforementioned theoretical analysis, the voltage ripple still exists in the practical applications because of the finite capacitance and the equivalent series resistance, and then the increase of the voltage ripple on C_{AUX1} and C_{AUX2} can be equivalently treated as the increase of the difference between the coefficients k and g, which would increase the output-current ripple i_{ACO}. It can also be estimated by (13). Therefore, C_{AUX1} and C_{AUX2} should be designed and selected carefully to guarantee the desirable effect of the output-current ripple elimination

$$\begin{cases} i_{\mathrm{AC1}}\left(\mathrm{SL}_{\mathrm{SK3}}+\mathrm{SL}_{\mathrm{SK4}}+\frac{1}{\mathrm{SC}_{\mathrm{AUX1}}}\right)+i_{\mathrm{ACO}}\left(\mathrm{SL}_{\mathrm{SK4}}-\mathrm{SL}_{\mathrm{SK1}}\right) \\ \qquad = i_{\mathrm{AC2}}\left(\mathrm{SL}_{\mathrm{SK1}}+\mathrm{SL}_{\mathrm{SK2}}+\frac{1}{\mathrm{SC}_{\mathrm{AUX2}}}\right) \\ i_{\mathrm{AC1}}+i_{\mathrm{AC2}}+i_{\mathrm{ACO}}=i_{\mathrm{SAC}} \end{cases} \tag{13}$$

$$i_{\mathrm{ACO}}=i_{\mathrm{SAC}}-i_{\mathrm{AC1}}-i_{\mathrm{AC2}}=i_{\mathrm{SAC}}\left[\frac{k-g}{(k+1)(g+1)}\right]. \tag{14}$$

C. Voltage Stress Clamping for Rectifier

Theoretically, the secondary-side rectifiers' voltage stress can be clamped at 2 V_{OUT} when the centre-tapped transformer-winding configuration with capacitive output filter is utilized at the secondary side. However, the leakage inductance of the power transformer would always oscillate with the C_{OSS} of the rectifier in the practical applications and the caused voltage spike increases the voltage stress on the rectifier considerably. Moreover, the leakage inductance suffers visible voltage ripple because of the volt-second balance and also deteriorates the rectifiers' voltage stress especially for the high-output current applications [23].

When utilizing the proposed symmetrical rectifier configuration, the secondary-side rectifiers' voltage stress can be effectively clamped at 2 V_{OUT} by two equivalently series-connected auxiliary flying-balance capacitors, C_{AUX1} and C_{AUX2}, and then the energy stored in the leakage inductance L_{SK} of the power transformer is going to be too low to increase the voltage stress on the rectifier as well as the voltage ripple across L_{SK} caused by the volt-second balance. The equivalent circuit during the half energy transfer period is shown in Fig. 11(a).

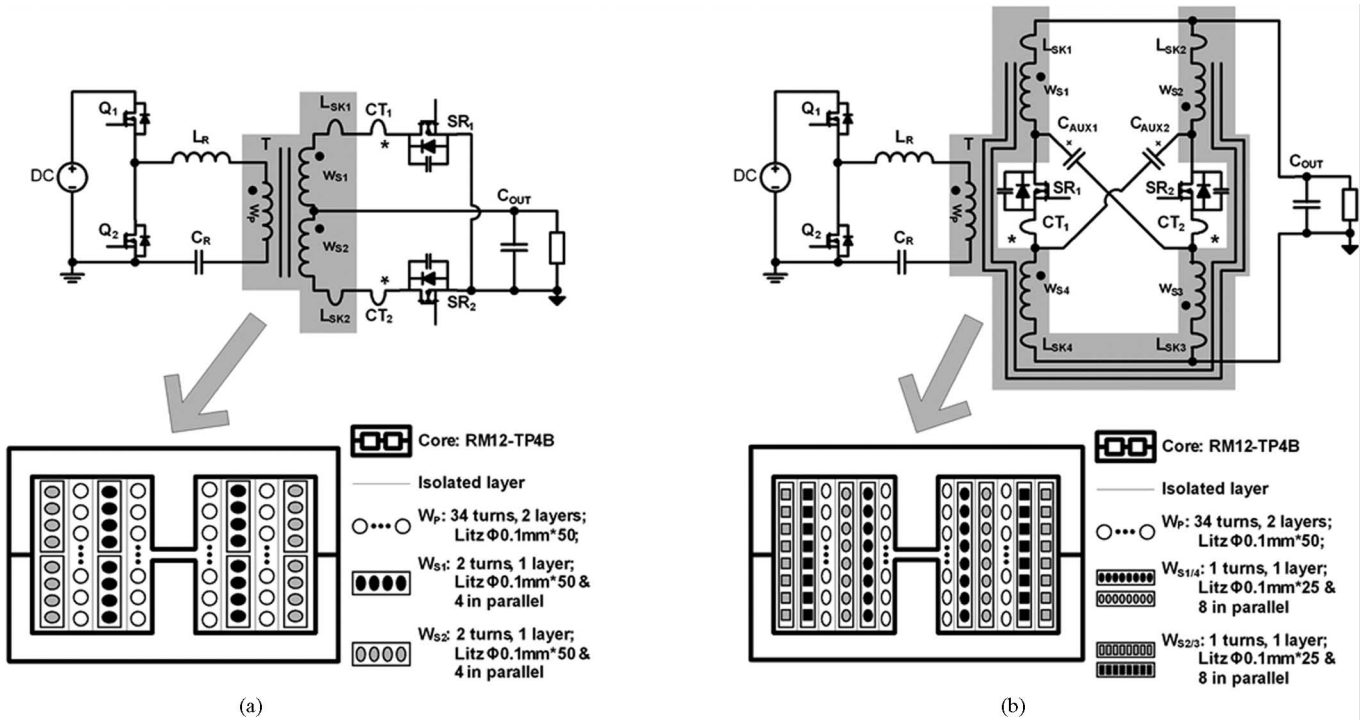


Fig. 12. Circuit diagrams of two lab-made prototypes with different secondary-side rectifier configurations. (a) *LLC* resonant converter prototype with the conventional centre-tapped rectifier configuration. (b) *LLC* resonant converter prototype with the proposed symmetrical rectifier configuration.

From Fig. 11(b) and (c), it is worthwhile to note that an inherent small *LC* output filter, which consists of the total leakage inductance at the secondary side L_{SKT}, and the output filter capacitor C_{OUT} can help to further reduce the output-voltage ripple. It brings in the feasibility to remove the small additional *LC* output filter. When employing a current sensor CT in series with SR for the current mode driving, although its very small leakage inductance and the relevant trace parasitic inductance would still oscillate with the C_{OSS} of SR, the caused voltage spike is too small to deteriorate the SRs' voltage stress. The next half energy transfer period is symmetrical and has the same benefits as presented earlier. Therefore, with this advantage in the effectively voltage stress clamping, the SRs with much lower breakdown voltage rate can be utilized to reduce both the driving loss and the conduction loss at the secondary side. It does good help in obtaining high conversion efficiency for the dc/dc converters.

IV. Experimental Results

Two lab-made prototypes of *LLC* resonant dc/dc converter with different secondary-side rectifier configurations are built up, respectively, for the experimental verification of the theoretical analysis presented earlier and the performance comparison of the improvements obtained from the proposed symmetrical rectifier configuration. Fig. 12 shows the both circuit diagrams and the transformer windings' implementation in these two lab-made prototypes. Some other relevant circuit parameters and the utilized components' characteristic are listed in Table I. Note that in order to show the improvement of the proposed rectifier configuration in low voltage stress of SR based on a relatively fair platform, it is more reasonable to employ the same SR (FDI038AN06 from Fairchild) during the comparison for these two prototypes, although the prototype shown in Fig. 12(b) has much lower SRs' voltage stress.

As the comparison results shown in Figs. 13–16, it is obvious that the proposed configuration does great help in restraining the voltage spike on the secondary-side SRs. Due to the current mode driving strategy utilized for the secondary-side SRs, although there is still some small ringing across the SRs in the practical applications, which is mainly caused by the parasitical resonance between the SRs' C_{OSS} and the leakage inductance of the current sensor CT and the parasitical trace inductance of the PCB layout, the dramatically reduced voltage stress means the feasibility to utilize the SRs with lower breakdown voltage rate to improve the conversion efficiency as shown in Fig. 21. Fig. 17 shows the benefit of substituting the 40-V_{DSS} SR (HAT2169H) with the 60-V_{DSS} SR (FDI038AN060A0) in lab-made prototype with the proposed rectifier configuration.

Figs. 18 and 19 show the remarkable effect of the output-current ripple reducing with different input voltage. Although the proposed configuration can help to eliminate the output-current ripple as the theoretical analysis presented above, when considering a little asymmetry, both in the practically handmade secondary-side windings and the primary-side complementary control signal, the smaller output-current ripple would still exist. Smaller output-current ripple leads to smaller conduction loss in the output capacitive filter and the trace of PCB layout. The size and the occupied PCB area of the output capacitive filter can also be reduced considerably.

TABLE I
CIRCUIT PARAMETERS AND COMPONENT CHARACTERISTICS OF TWO LAB-MADE PROTOTYPES

CIRCUIT PARAMETERS AND COMPONENT CHARACTERISTICS		
	(a) with the conventional rectifier configuration	(b) with the proposed rectifier configuration
Input Voltage Range	$350V_{DC}$-$400V_{DC}$	
Output Power	$12V_{DC}$: 25A	
Resonant frequency	100kHz	
Power MOSFET	Q_1, Q_2: SPI20N60C3 (Vendor: Infineon CoolMOS);	
Resonant Tank	L_R: 91uH: RM8-TP4B: Litz wire: (Φ0.1mm*50)*24turns; C_R: 22nF/1000V_{DC}: Film Cap (Vendor: WIMA);	
Transformer	Referred from Fig.14;	
SR	SR_1, SR_2: FDI038AN06 (Vendor: Fairchild): 2 in parallel for each winding;	
Auxiliary Cap	N/A	C_{AUX1}, C_{AUX2}: 47uF/16V_{DC}:5 in parallel: Ceramic Cap (Murata);
Output Cap	C_{OUT}: 1800uF/16V_{DC}: 4 in parallel: Electrolytic Aluminum Cap (Nichicon: HZ(M))	C_{OUT}: 680uF/25V_{DC}: Single: Electrolytic Aluminum Cap (NCC: KZH)

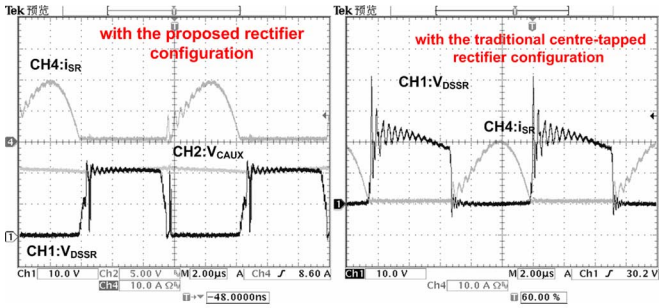


Fig. 13. Voltage stress V_{DSSR} comparison at 350 V_{IN} and 12 A (half-load). (a) With the proposed rectifier configuration. (b) With the traditional centre-tapped rectifier configuration.

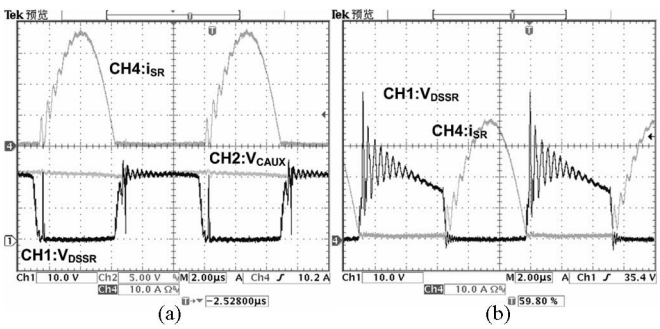


Fig. 14. Voltage stress V_{DSSR} comparison at 350 V_{IN} and 25 A (full-load). (a) With the proposed rectifier configuration. (b) With the traditional centre-tapped rectifier configuration.

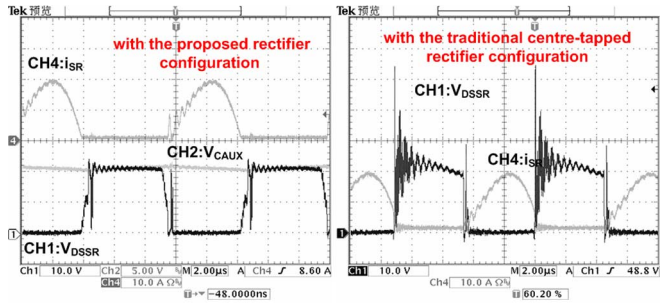


Fig. 15. Voltage stress V_{DSSR} comparison at 400 V_{IN} and 12 A (half-load). (a) With the proposed rectifier configuration. (b) With the traditional centre-tapped rectifier configuration.

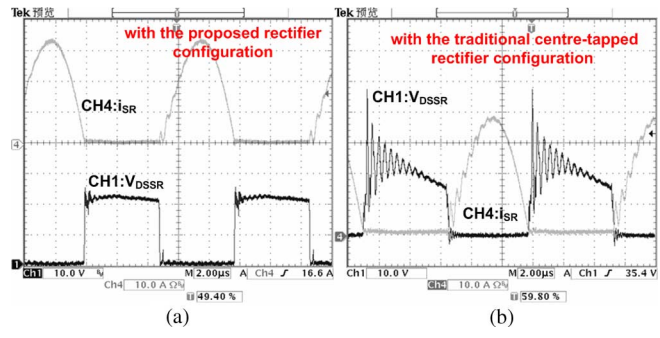


Fig. 16. Voltage stress V_{DSSR} comparison at 400 V_{IN} and 25 A (full-load). (a) With the proposed rectifier configuration. (b) With the traditional centre-tapped rectifier configuration.

Fig. 20 shows the current waveform in the secondary-side winding i_{W1} of transformer at full-load and different input voltage condition. The existing dc bias helps to reduce rms value of the current and is good for the further reduction of transformer's winding loss. Approximately, treating the current in the secondary-side winding as sinusoid to simplify the calculation, (15) shows the comparison between the current rms value in single secondary-side winding at critical continuous conduction operation mode and full-load output condition, but with different rectifier configurations

$$\begin{cases} I_{\mathrm{RMS\_SS}} = \frac{\pi}{4} I_{\mathrm{OUT}}, \\ \qquad \text{with conventional rectifier configuration} \\ I_{\mathrm{RMS\_SS}} = \frac{\sqrt{4+2\pi^2}}{8} I_{\mathrm{OUT}}, \\ \qquad \text{with proposed rectifier configuration.} \end{cases} \tag{15}$$

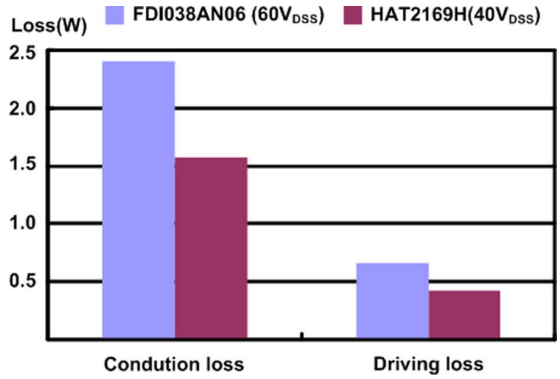
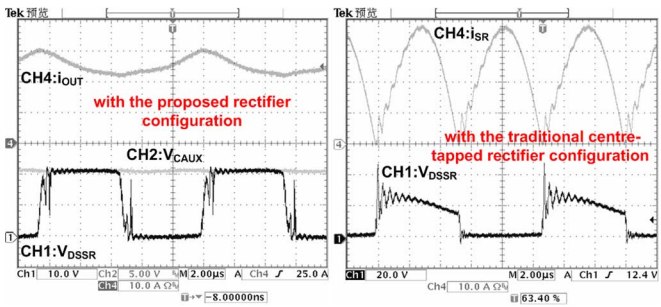
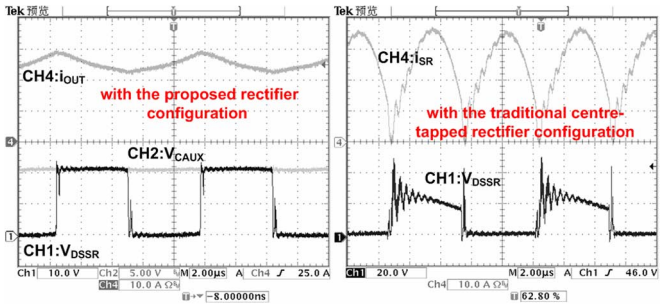


Fig. 17. Benefit from substituting 40 $V_{\rm DSS}$ SR for 60 $V_{\rm DSS}$ SR with the proposed rectifier configuration.



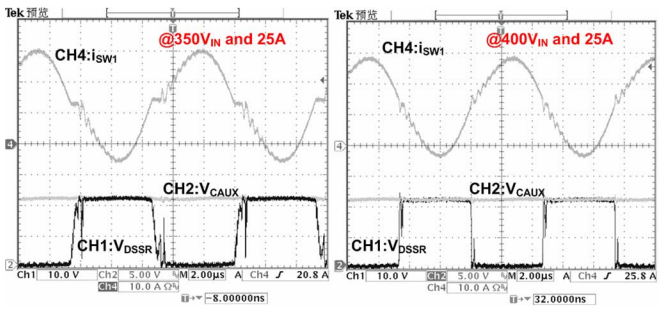
(a) (b)

Fig. 18. Output-current ripple comparison at 350 $V_{\rm IN}$ and 25 A (full-load). (a) With the proposed rectifier configuration. (b) With the traditional centre-tapped rectifier configuration.



(a) (b)

Fig. 19. Output-current ripple comparison at 400 $V_{\rm IN}$ and 25 A (full-load). (a) With the proposed rectifier configuration. (b) With the traditional centre-tapped rectifier configuration.



(a) (b)

Fig. 20. Current in the secondary-side winding at full-load and different input voltage condition: (a) at 350 $V_{\rm IN}$ and 25 A; (b) at 400 $V_{\rm IN}$ and 25 A.

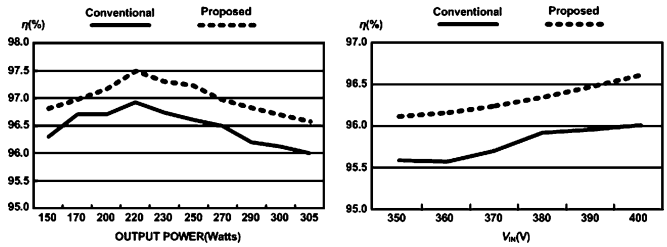


Fig. 21. Efficiency comparison between the lab-made prototypes with different rectifier configuration. (a) Output Power (Watts). (b) $V_{\rm IN}$ (V).

Finally, Fig. 21(a) shows the considerable improvement of the conversion efficiency obtained by utilizing the proposed rectifier configuration at 400-$V_{\rm IN}$ input and different power output condition and Fig. 21(b) shows the full-load efficiency comparison at different voltage input condition.

V. Conclusion

A novel symmetrical rectifier configuration with capacitive output filter is proposed in this paper. It effectively clamps the voltage stress on the secondary-side rectifier at 2 $V_{\rm OUT}$ without any parasitical voltage spike, and meanwhile reduces the output-current ripple dramatically because of the bypass effect of two auxiliary flying-balance capacitors. Therefore, the rectifier with much lower breakdown voltage rate can be utilized to reduce the conduction loss directly; the current ripple elimination effect not only reduces the loss in the secondary-side windings of power transformer, but also reduces the required capacitance, size, and the occupied PCB layout area of the capacitive output filter. Furthermore, the leakage inductance at the secondary side and the output filter capacitor can be treated as an inherent small *LC* filter to reduce the output-voltage ripple. Two 300-W lab-made *LLC* resonant dc/dc converters with different rectifier configurations are built up to verify the features of the proposed symmetrical rectifier configuration in voltage stress clamping and output-current ripple reducing. It shows considerable advantage in high conversion efficiency.

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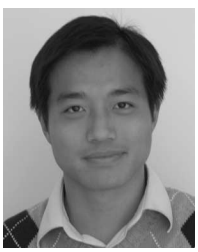
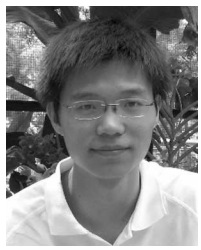


Chen Zhao was born in Zhejiang, China, in 1981. He received the B.S. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2004 and 2009, respectively.

He is currently a Senior System Engineer at Silergy Corporation, San Jose, CA. His research interests include soft-switching techniques, high-efficiency dc–dc converter and ac–dc converter, and power electronics system integration.

Min Chen received the B.S. degree in applied electronics, the Ph.D. degree in electrical engineering, both from Zhejiang University, Hangzhou, China, in 2000 and 2006, respectively.

He was a Postdoctoral Research Fellow in College of Electrical Engineering, Zhejiang University during 2007–2009, where he is currently a Lecturer. Since 2007, he has been involved with the Lighting Research and Development Laboratory, National Engineering Research Center for Applied Power Electronics. His research interests include modern lighting system for high-intensity discharge Lamps and LED, regenerative energy system, inverter system, energy storage system, and stability of modern power electronics systems. He has authored or coauthored more than 30 technical papers published in various international journals and conferences. He has applied for over 12 patents, and 8 of them are patents of inventions.



Guoxing Zhang was born in Zhejiang, China, in 1984. He received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2007, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include synchronous rectifier techniques, and dc–dc converters.

Xinke Wu (M'09) was born in Jiangsu, China, in 1978. He received the B.S. and M.S. degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2000 and 2002, respectively, and the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2006.

He is currently an Assistant Research Fellow at National Engineering Research Center (NERC) for Applied Power Electronics, Zhejiang University. His research interests include soft-switching of power conversion, power factor correction, high-efficiency dc–dc converter, and power electronics system integration.

Zhaoming Qian (SM'92) received the Graduate degree in radio engineering from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1961, and the Ph.D. degree in applied science from Catholic University of Leuven, Leuven, Belgium and the Interuniversity Microelectronics Center, Leuven, in 1989.

Since 1961, he has been involved in teaching and the research on electronics and power electronics at Zhejiang University. in 1992, he was a Professor in the College of Electrical Engineering, Zhejiang University, where he is currently the Deputy Director of National Engineering Research Center for Applied Power Electronics and the Deputy Director of Scientific Committee of National Key Laboratory of Power Electronics. His research interests include power electronics and its industrial applications, power electronic system integration, and electromagnetic compatibility (EMC) in power electronic systems, etc. He has authored or coauthored more than 200 papers published in international journals and conferences and one book on EMC design.

Dr. Qian has received the Excellent Education Awards from the China Education Commission and Zhejiang University in 1993, 1997, and 1999, respectively, and the Science and Technology Development Awards from the China Education Commission in 1999 and 2003, respectively.