FAIRCHILD SEMICONDUCTOR™

QRC (transformer) design v.1.0

Blue cell	is the input parameters
Red cell	is the output parameters

1. Define the system specifications

Minimum Line voltage (V_{line}^{min})	185	V.rms
Maximum Line voltage (V_{line}^{max})	265	V.rms
Line frequency (f_L)	50	Hz

	$V_{o(n)}$		$I_{o(n)}$		$P_{o(n)}$		$K_{L(n)}$	
1st output for feedback	5	V	1.00	A	5	W	50	%
2nd output	13	V	0.10	A	1	W	13	%
3rd output	13	V	0.10	A	1	W	13	%
4th output	24	V	0.10	A	2	W	24	%
5th output		V		A	0	W	0	%
6th output		V		A	0	W	0	%
Maximum output power (P_o) =	10.0	W						
Estimated efficiency (E_{ff})	80	%						
Maximum input power (P_{in}) =	12.5	W						

2. Determine DC link capacitor and DC link voltage range

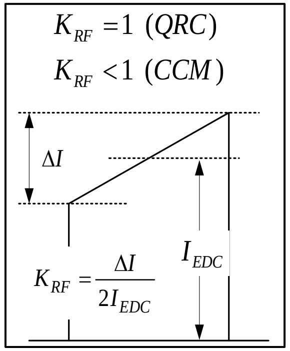
DC link capacitor (C_{DC})	22	μF
Minimum DC link voltage (V_{DC}^{min}) =	244	V
Maximum DC link voltage (V_{DC}^{max})=	375	V

3. Determine Maximum duty ratio (Dmax)

Maximum duty ratio (D_{max})	0.25	
Max nominal MOSFET voltage (V_{ds}^{nom}) =	456	V
Output voltage reflected to primary (V_{RO})=	81	V
The turn ratio (n) =	17	

4. Determine transformer primary inductance (Lm)

Minimum switching frequency of FPS (f_s^{min})	50.4	kHz
Maximum switching frequency of FPS (f_s^{max})	67	kHz
Ripple factor (K_{RF})	1	
Necessary minimum primary side inductance (L_m^{min}) =	2944	μH
The tolerance of L_m(+−)	10	%
Typical primary side inductance (L_m) =	3239	μH
Maximum primary side inductance (L_m^{max}) =	3533	μH
I_{EDC} @worst case(V_{in}^{min}) =	0.205	A
ΔI @worst case(V_{in}^{min} & L_m^{min}) =	0.410	A
Maximum peak drain current (I_{ds}^{peak}) =	0.410	A
RMS drain current (I_{ds}^{rms}) =	0.118	A
Maximum DC link voltage switch from CCM to QRC when L_m^{max}(V_{DC}^{CCM})	374	V



5. Choose the proper FPS considering the input power and minimum current limit

di/dt test condition @ datasheet	240	mA/sec			
Internal delay time for current limit (t_{CLD})	0.5	μsec			
Minimum I_{LIM} @ datasheet	0.8	A			
Actual minimum I_{LIM} when V_{DC}^{min} =	0.678	A	>	0.410	A
	−>O.K.				

6. Determine the proper core and the minimum primary turns

Saturation flux density (B_{sat})	*0.32*	T	<= Strongly recommend not to change!!!
Cross sectional area of core (A_e)	31	mm^2	
Maximum I_{LIM} @ datasheet	1.00	A	
Actual maximum I_{LIM} when V_{DC}^{max} =	1.187	A	
Minimum primary turns to avoid core saturation (N_p^{min})=	422.9	T	

7. Determine the number of turns for each output

	$V_{o(n)}$		$V_{F(n)}$				# of turns	
Vcc (Use Vcc start voltage)	14	V	1.2	V	84.1	=>	84	T
1st output for feedback	5	V	0.6	V	31	=>	31	T
2nd output	13	V	0.6	V	75.3	=>	75	T
3rd output	13	V	0.6	V	75.3	=>	75	T
4th output	24	V	0.6	V	136.2	=>	136	T
5th output	0	V	0	V	0.0	=>	0	T
6th output	0	V	0	V	0.0	=>	0	T
VF : Forward voltage drop of rectifier diode			Primary turns (N_p)=				450	T
			--->enough turns					
Ungapped AL value (AL)	1300	nH/T^2						
Gap length (G) ; center pole gap =	2.19728	mm						

8. Determine the wire diameter for each winding

	Diameter		Parallel		$I_{D(n)}^{rms}$		(A/mm^2)
Primary winding	0.2	mm	1	T	0.12	A	3.77
Vcc winding	0.2	mm	1	T	0.01	A	0.32
1st output winding (5V)	0.33	mm	2	T	1.49	A	8.70
2nd output winding (13V)	0.2	mm	1	T	0.16	A	5.07
3rd output winding (13V)	0.2	mm	1	T	0.16	A	5.07
4th output winding (24V)	0.2	mm	1	T	0.16	A	5.18
5th output winding (V)		mm		T	#####	A	#####
6th output winding (V)		mm		T	#####	A	#####
Copper area (A_c) =	31.03	mm^2					
Fill factor (K_F)	0.2						
Required window area (A_{wr})	155.17	mm^2					

9. Choose the rectifier diode in the secondary side

	$V_{D(n)}$		$I_{D(n)}^{rms}$	
Vcc diode	84	V	0.10	A
Rectifier diode for 1st output (5V)	31	V	1.49	A
Rectifier diode for 2nd output (13V)	76	V	0.16	A
Rectifier diode for 3rd output (13V)	76	V	0.16	A
Rectifier diode for 4th output (24V)	138	V	0.16	A
Rectifier diode for 5th output (V)	0	V	#####	A
Rectifier diode for 6th output (V)	0	V	#####	A

10. Determine the output capacitor

	$C_{o(n)}$		$R_{C(n)}$		$I_{cap(n)}$		$\Delta V_{o(n)}$	
Output capacitor for 1st output (5V)	470	uF	10	mΩ	1.1	A	0.04	V
Output capacitor for 2nd output (13V)	100	uF	60	mΩ	0.1	A	0.02	V
Output capacitor for 3rd output (13V)	100	uF	60	mΩ	0.1	A	0.02	V
Output capacitor for 4th output (24V)	220	uF	60	mΩ	0.1	A	0.02	V
Output capacitor for 5th output (V)		uF		mΩ	#####	A	#####	V
Output capacitor for 6th output (V)		uF		mΩ	#####	A	#####	V

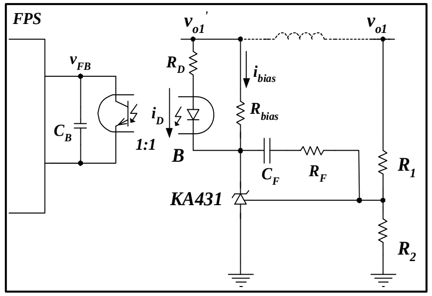
11. Design RCD snubber

Primary side leakage inductance (L_{lk})	100	uH	
Maximum Voltage of snubber capacitor (V_{sn})	400	V	
Maximum snubber capacitor voltage ripple	30	%	
Snubber resistor (R_{sn})=	225.9	kΩ	
Snubber capacitor (C_{sn})=	0.220	nF	
Power loss in snubber resistor (P_{sn})=	0.708	W	(In Normal Operation. Will decrease at standby due to burst op.)
Peak drain current at V_{DC}^{max} (I_{ds2}) =	0.19	A	
Max Voltage of Csn at V_{DC}^{max} (V_{sn2})=	209	V	
Max Voltage stress of MOSFET (V_{ds}^{max})=	583	V	

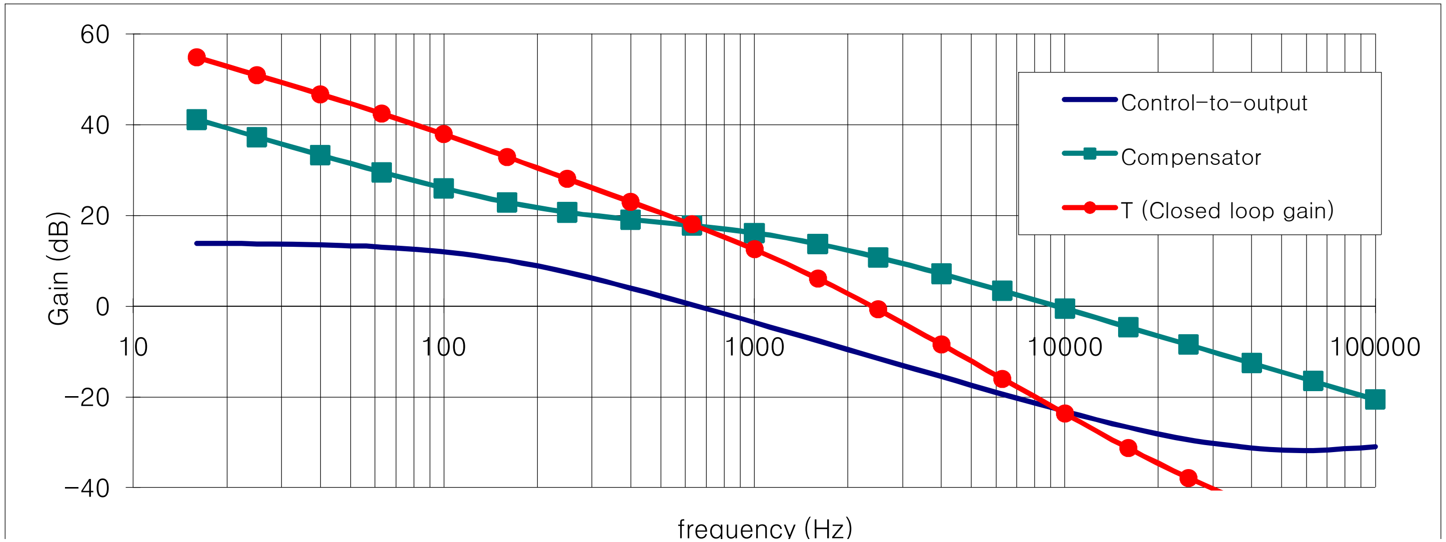
12. Design Feedback control loop

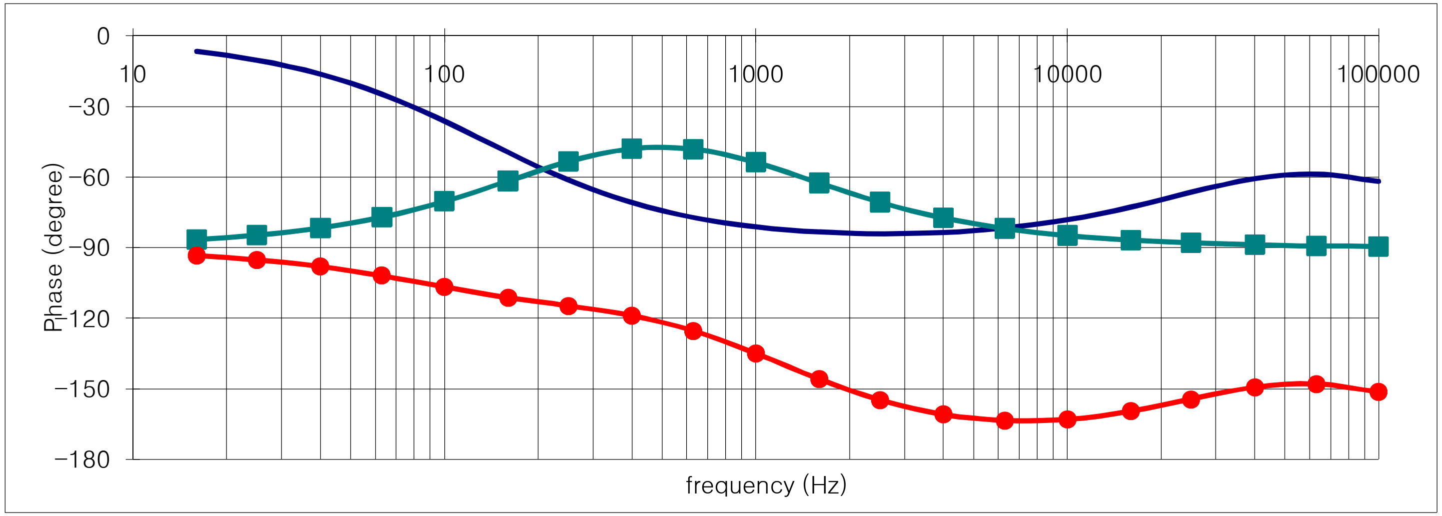
Control–to–output DC gain =	5				
Control–to–output zero (w_z) =	212766	rad/s =>	f_z=	33,880	Hz
Control–to–output RHP zero (w_{rz})=	669643	rad/s =>	f_{rz}=	106,631	Hz
Control–to–output pole (w_p)=	851	rad/s =>	f_p=	136	Hz

Voltage divider resistor (R_1)	5.6	kΩ
Voltage divider resistor (R_2)=	6	kΩ
Opto coupler diode resistor (R_D)	1	kΩ
KA431 Bias resistor (R_{bias})	1.2	kΩ
Feeback pin capacitor (C_B) =	47	nF
Feedback Capacitor (C_F) =	47	nF
Feedback resistor (R_F) =	10	kΩ



Feedback integrator gain (w_i) =	11398	rad/s =>	f_i=	1,815	Hz
Compensator zero (w_{zc})=	1364	rad/s =>	f_{zc}=	217	Hz
Compensator pole (w_{pc})=	7092	rad/s =>	f_{pc}=	1,129	Hz





0
−30
−60
−90
−120
−150
−180
Phase (degree)
10
100
1000
10000
100000
frequency (Hz)