



# FSU04N60A

## N-Channel MOSFET

**Pb** Lead Free Package and Finish

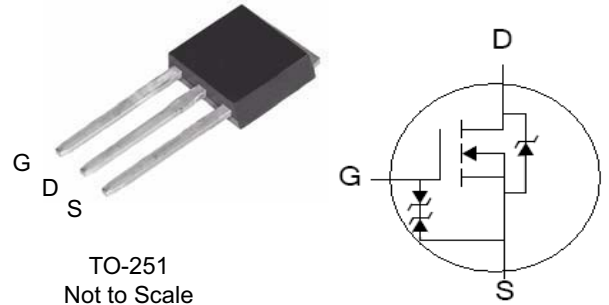
### Applications:

- Adaptor
- TV Main Power
- SMPS Power Supply
- LCD Panel Power

### Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- ESD improved Capability

$V_{DSS}$	$R_{DS(ON)}$ (Typ.)	$I_D$
600 V	1.9 $\Omega$	4 A



TO-251  
Not to Scale

### Ordering Information

PART NUMBER	PACKAGE	BRAND
FSU04N60A	TO-251	FSU04N60A

### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	FSU04N60A	Units
$V_{DSS}$	Drain-to-Source Voltage (NOTE *1)	600	V
$I_D$	Continuous Drain Current	4*	A
$I_{D@ 100^\circ\text{C}}$	Continuous Drain Current	2.9	
$I_{DM}$	Pulsed Drain Current, $V_{GS}@ 10\text{V}$ (NOTE *2)	16	
$P_D$	Power Dissipation	86	W
	Derating Factor above $25^\circ\text{C}$	0.69	$\text{W}/^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy $L=10\text{ mH}$	300	mJ
$I_{AS}$	Pulsed Avalanche Rating	Figure 16	A
$dv/dt$	Peak Diode Recovery $dv/dt$ (NOTE *3)	5.0	V/ns
$V_{ESD(G-S)}$	Gate to Source ESD (HBM-C=100pF, $R=1.5\text{K}\Omega$ )	3000	V
$T_L$ $T_{PKG}$	Maximum Temperature for Soldering Leads at 0.063 in (1.6 mm) from Case for 10 seconds	300	$^\circ\text{C}$
	Package Body for 10 seconds	260	
$T_J$ and $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

**Caution:** Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

### Thermal Resistance

Symbol	Parameter	FSU04N60A	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.45	$^\circ\text{C}/\text{W}$	Drain lead soldered to water cooled heatsink, $P_D$ adjusted for a peak junction temperature of $+150^\circ\text{C}$ . 1 cubic foot chamber, free air.
$R_{\theta JA}$	Junction-to-Ambient	62.5		

**OFF Characteristics**  $T_J=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	600	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient, Figure 11.	--	0.67	--	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	25	$\mu A$	$V_{DS}=600V, V_{GS}=0V$
		--	--	250		$V_{DS}=480V, V_{GS}=0V$ $T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	--	--	10	$\mu A$	$V_{GS}=+20V$
	Gate-to-Source Reverse Leakage	--	--	-10		$V_{GS}=-20V$

**ON Characteristics**  $T_J=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance Figure 9 and 10.	--	1.9	2.3	$\Omega$	$V_{GS}=10V, I_D=2.0A$ (NOTE *4)
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
gfs	Forward Transconductance	--	5.0	--	S	$V_{DS}=15V, I_D=2.0A$ (NOTE *4)

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$C_{iss}$	Input Capacitance	--	470	--	$\mu F$	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$
$C_{oss}$	Output Capacitance	--	58	--		
$C_{rss}$	Reverse Transfer Capacitance	--	15	--		
$Q_g$	Total Gate Charge	--	18	--	nC	$V_{DD}=300V$ $I_D=4A, V_{GS}=10V$
$Q_{gs}$	Gate-to-Source Charge	--	2.2	--		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	--	10	--		

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	12	--	ns	$V_{DD}=300V$ $I_D=4A$ $V_{GS}=10V$ $R_G=4.7\Omega$
$t_{rise}$	Rise Time	--	46	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	50	--		
$t_{fall}$	Fall Time	--	48	--		

**Source-Drain Diode Characteristics**  $T_C=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	--	--	4	A	Integral pn-diode in MOSFET
$I_{SM}$	Maximum Pulsed Current (Body Diode)	--	--	16	A	
$V_{SD}$	Diode Forward Voltage	--	--	1.5	V	$I_S=4\text{A}$ , $V_{GS}=0\text{V}$
$t_{rr}$	Reverse Recovery Time	--	328	--	ns	$V_{GS}=0\text{V}$
$Q_{rr}$	Reverse Recovery Charge	--	1.07	--	$\mu\text{C}$	$I_F=4\text{A}$ , $di/dt=100\text{A}/\mu\text{s}$

Notes:

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- \*1.  $T_J = +25^\circ\text{C}$  to  $+150^\circ\text{C}$ .
  - \*2. Repetitive rating; pulse width limited by maximum junction temperature.
  - \*3.  $I_{SD} = 4\text{A}$ ,  $di/dt < 100\text{A}/\mu\text{s}$ ,  $V_{DD} < BV_{DSS}$ ,  $T_J = +150^\circ\text{C}$ .
  - \*4. Pulse width  $\leq 380\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

### Characteristics Curve:

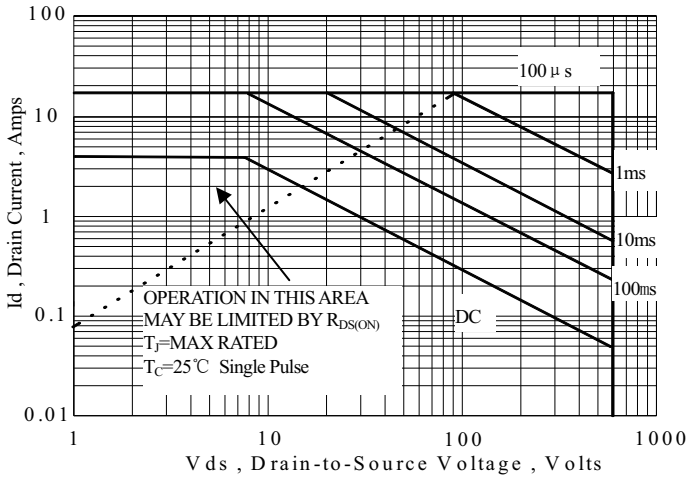


Figure 1 Maximum Forward Bias Safe Operating Area

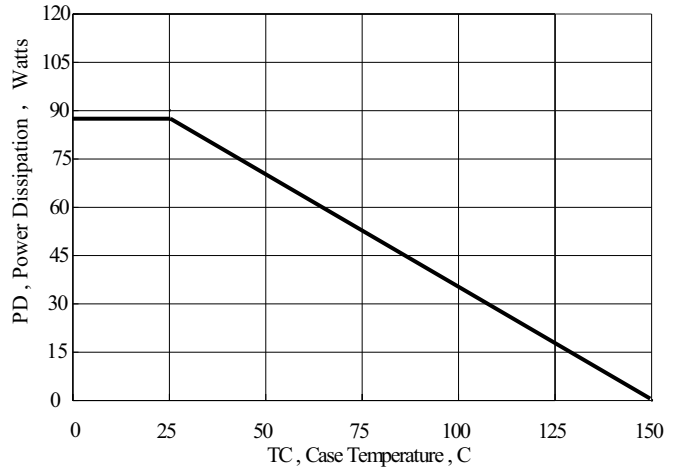


Figure 2 Maximum Power Dissipation vs Case Temperature

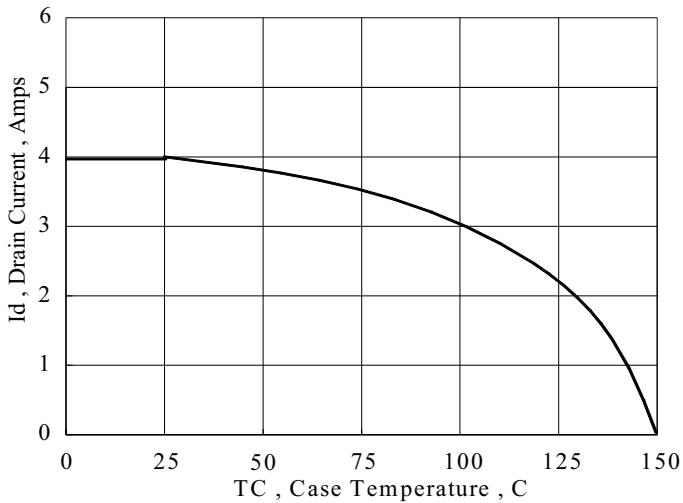


Figure 3 Maximum Continuous Drain Current vs Case Temperature

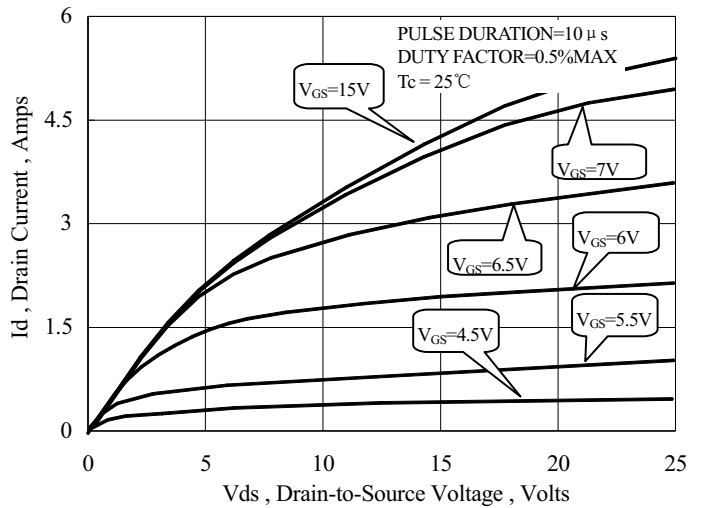


Figure 4 Typical Output Characteristics

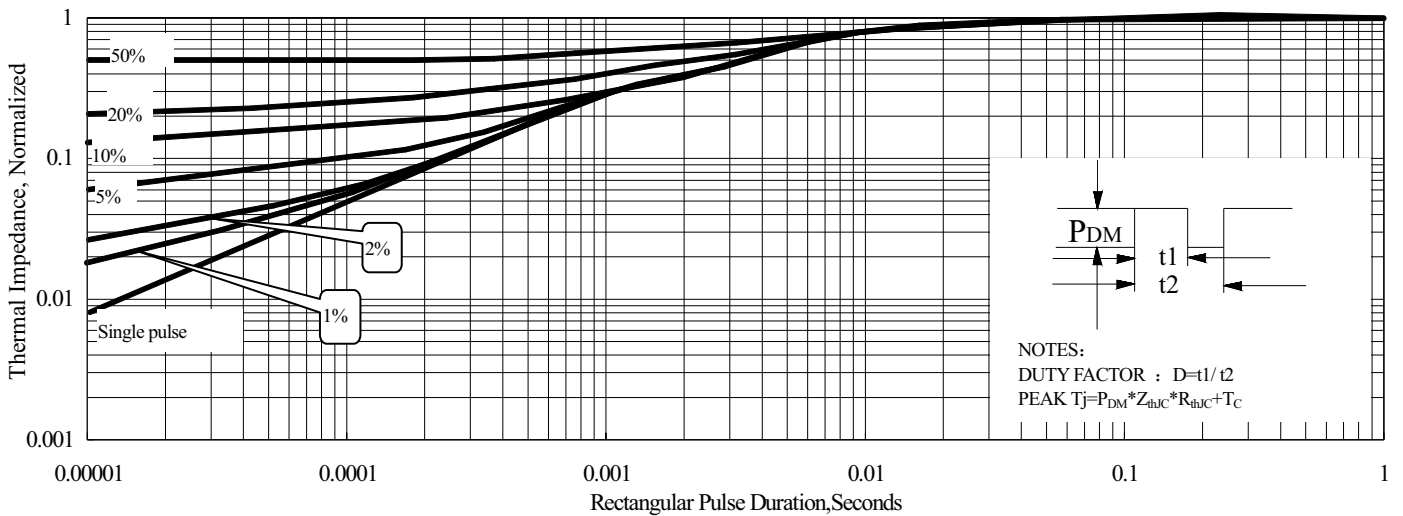


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

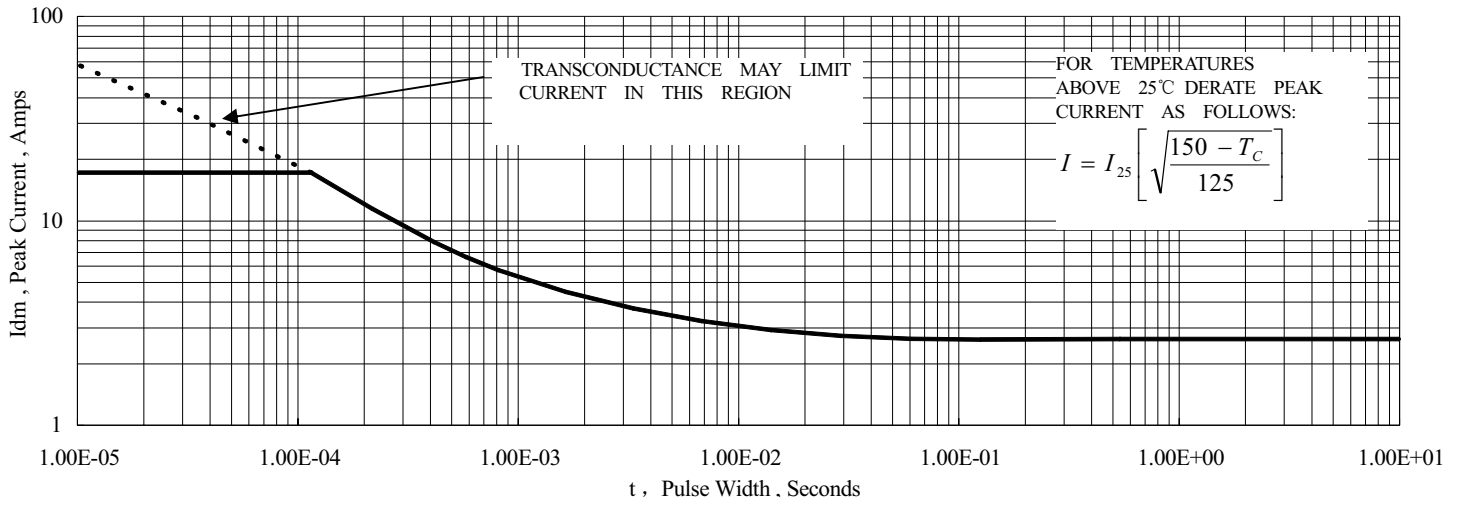


Figure 6 Maximum Peak Current Capability

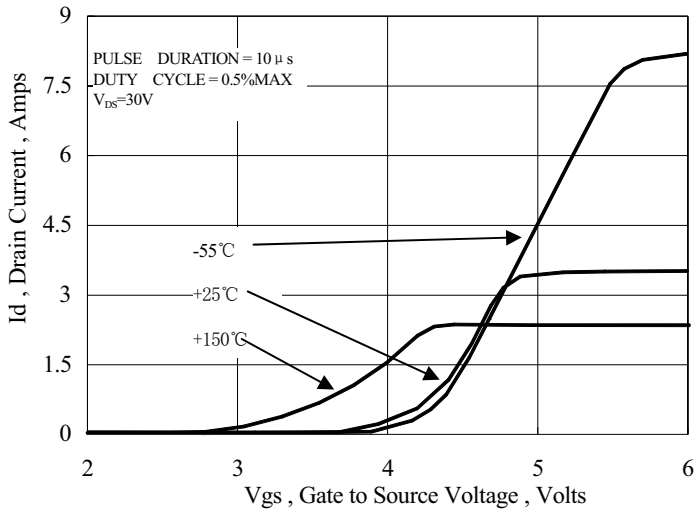


Figure 7 Typical Transfer Characteristics

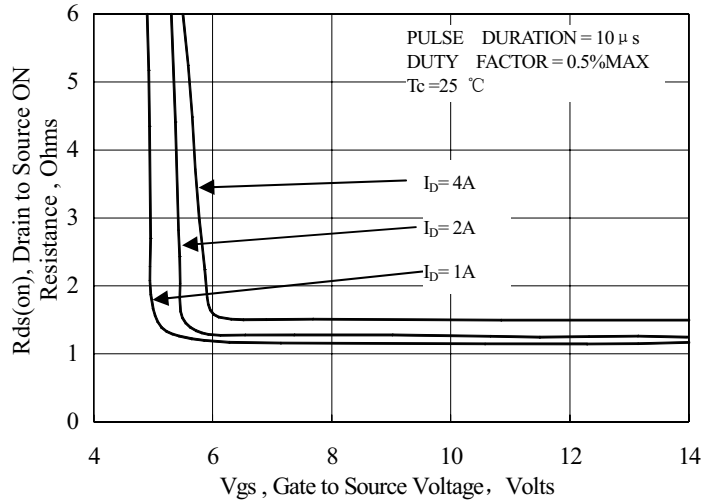


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

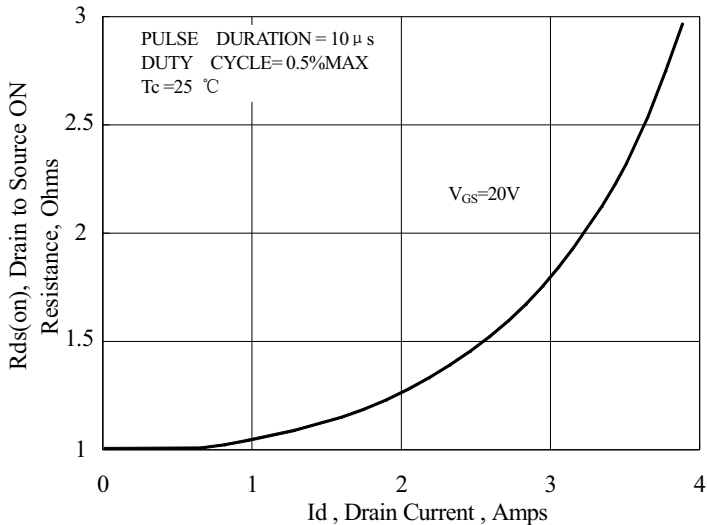


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

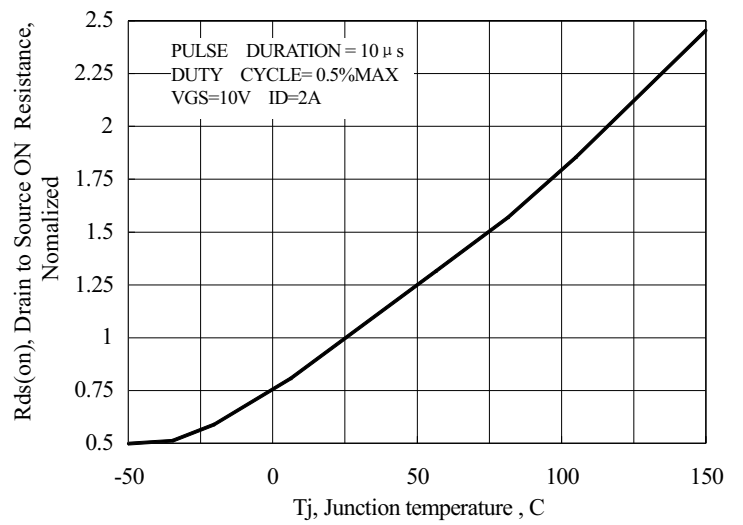


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature

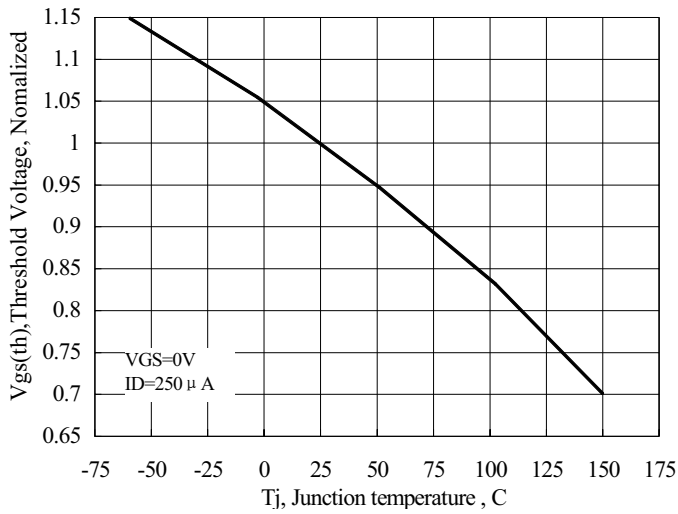


Figure 11 Typical Threshold Voltage vs Junction Temperature

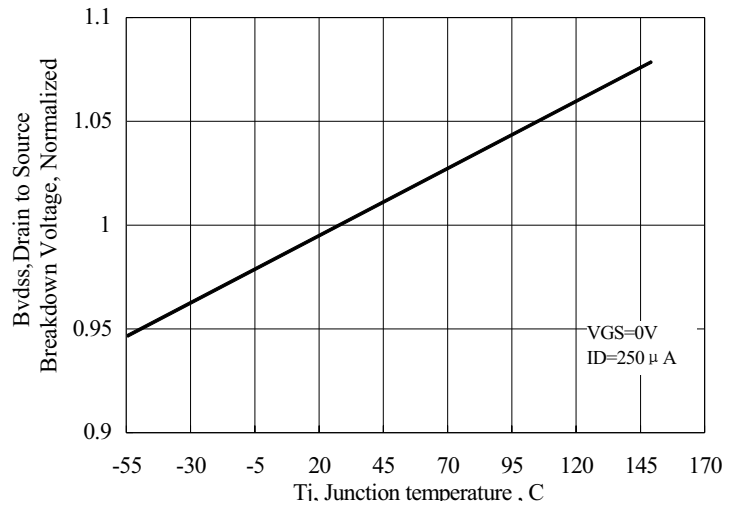


Figure 12 Typical Breakdown Voltage vs Junction Temperature

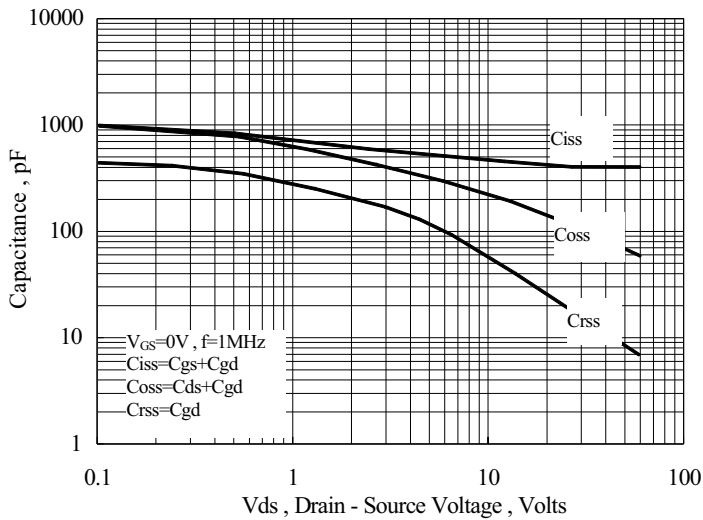


Figure 13 Typical Capacitance vs Drain to Source Voltage

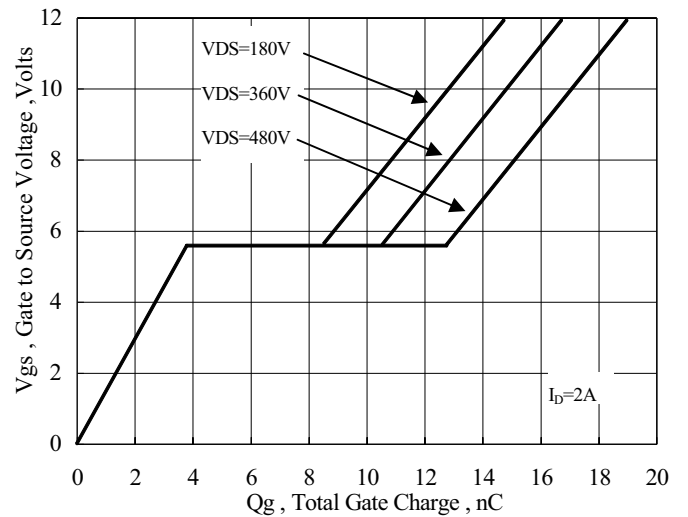


Figure 14 Typical Gate Charge vs Gate to Source Voltage

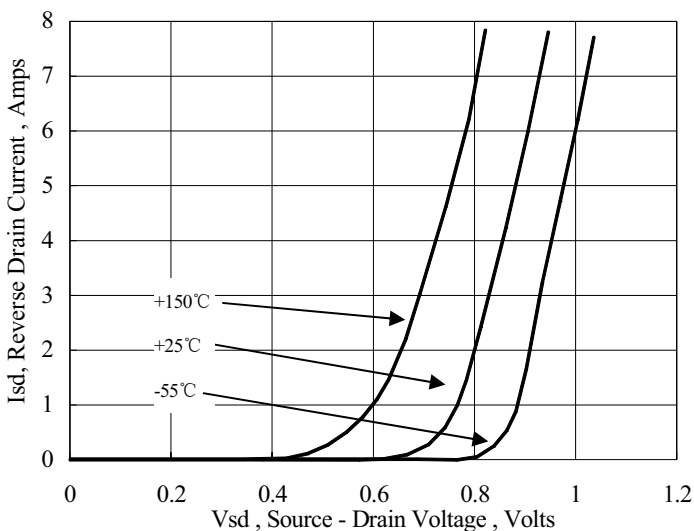


Figure 15 Typical Body Diode Transfer Characteristics

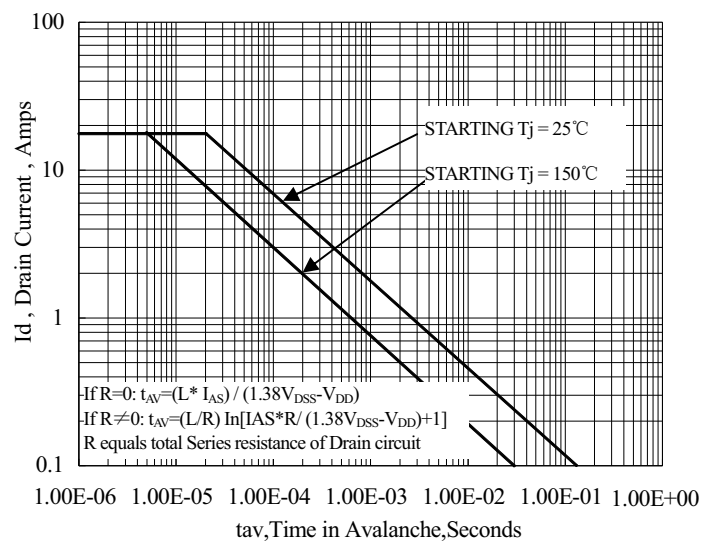


Figure 16 Unclamped Inductive Switching Capability

TEST CIRCUITS AND WAVEFORMS

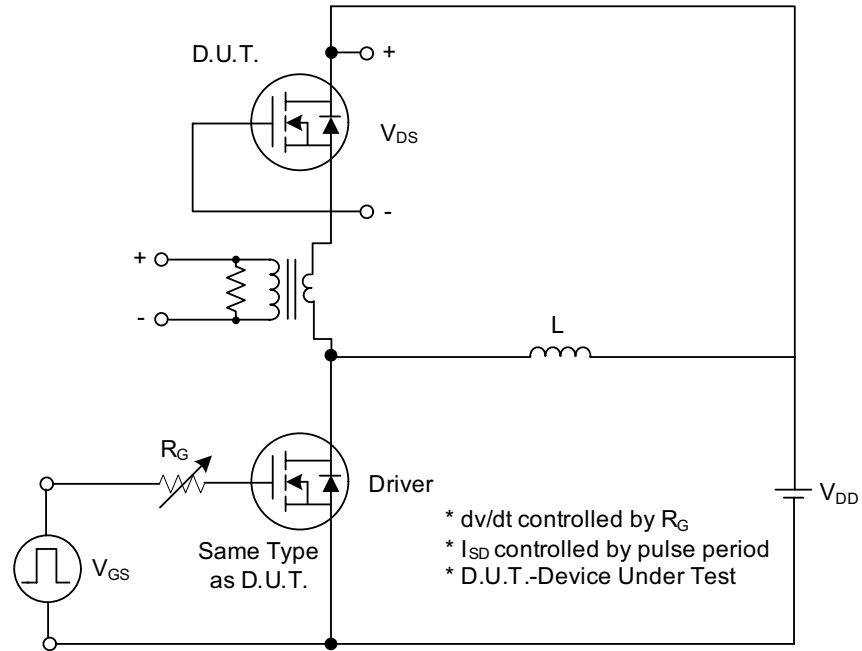


Fig. 1.1 Peak Diode Recovery  $dv/dt$  Test Circuit

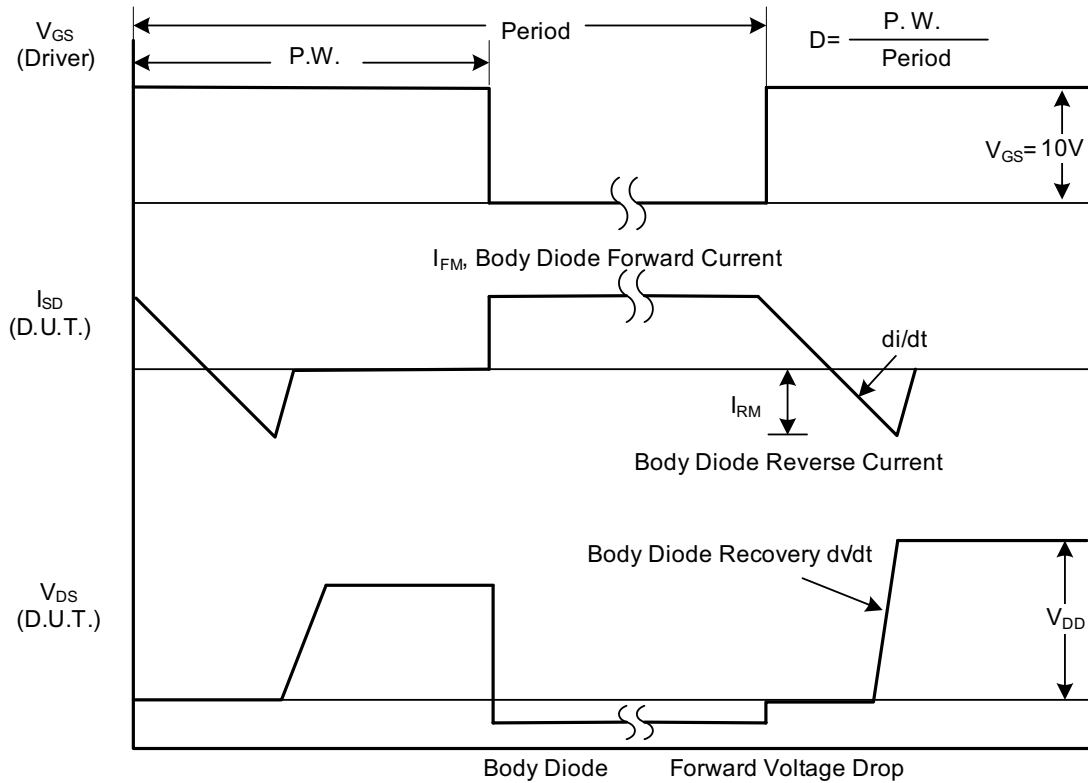


Fig. 1.2 Peak Diode Recovery  $dv/dt$  Waveforms

TEST CIRCUITS AND WAVEFORMS (Cont.)

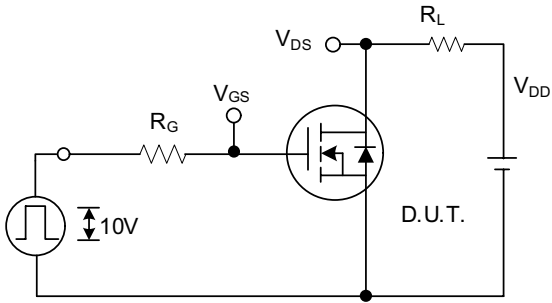


Fig. 2.1 Switching Test Circuit

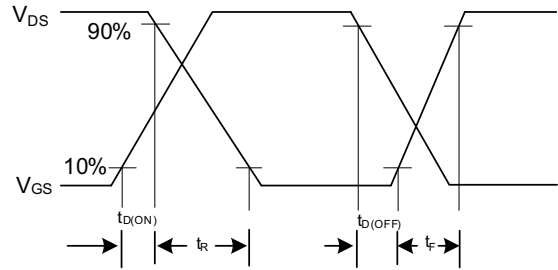


Fig. 2.2 Switching Waveforms

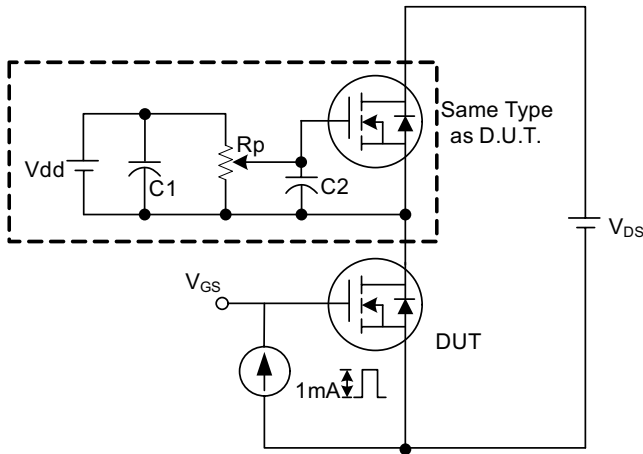


Fig. 3.1 Gate Charge Test Circuit

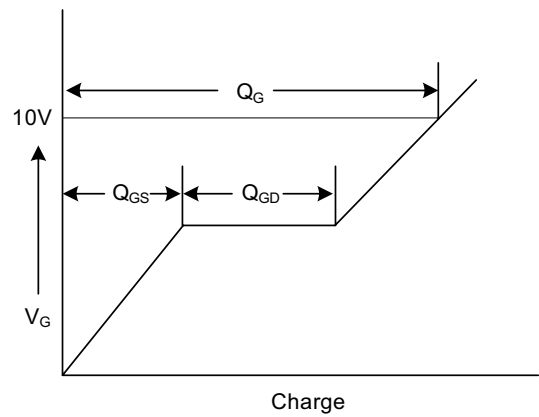


Fig. 3.2 Gate Charge Waveform

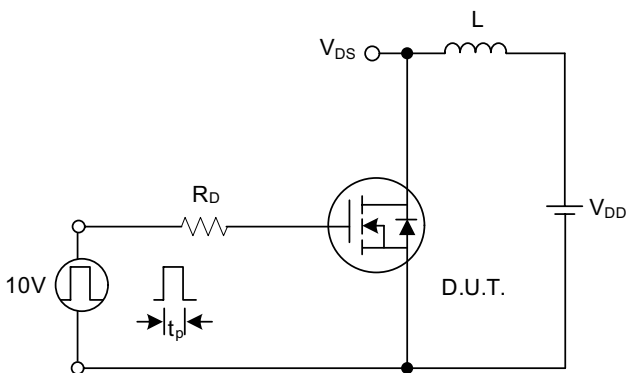


Fig. 4.1 Unclamped Inductive Switching Test Circuit

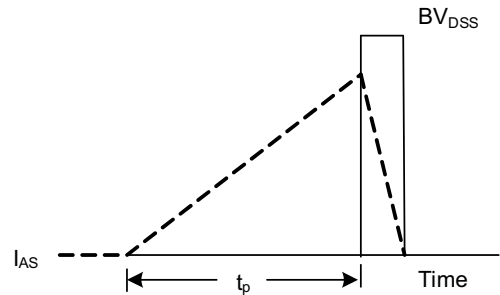


Fig. 4.2 Unclamped Inductive Switching Waveforms



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