1 Channel Synchronous PWM Controller

Halogen Free

General Description

The FP5102 / A is a DC-DC synchronous buck converter controller IC. It comprises high, low side NMOS gate drivers, boot diode, internal soft start, and over current protection circuit. With +2V to +12V V_{IN} supply voltage, it is suitable for a wide range of applications.

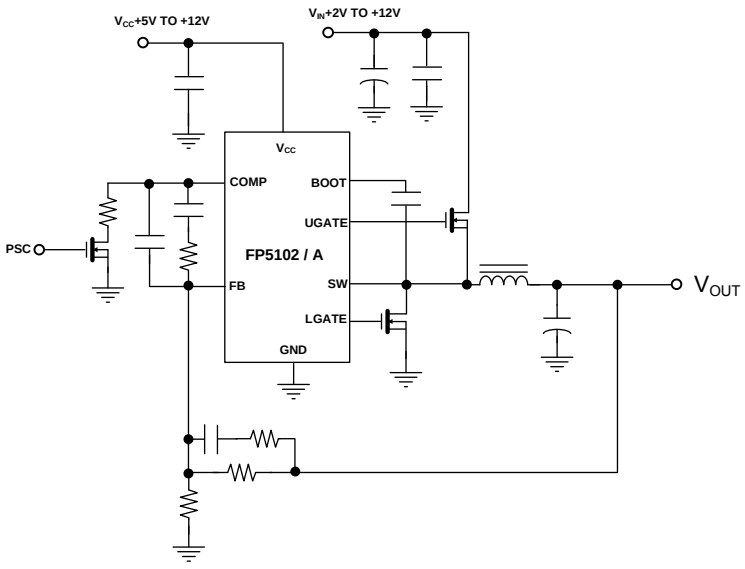
Features

- Operates from +5V to +12V Vcc Supply Voltage
- Feedback Reference Voltage: 0.8V (±2%)
- Fixed Frequency Oscillator: 300 / 600KHz
- Peak Output Driving Capability: 500mA
- Internal Soft Start Function
- High-Gain Voltage Mode PWM Control
- Over Current Protection by detecting Low-side MOS Voltage Drop
- Package: SOP8 / SOP8 (EP)

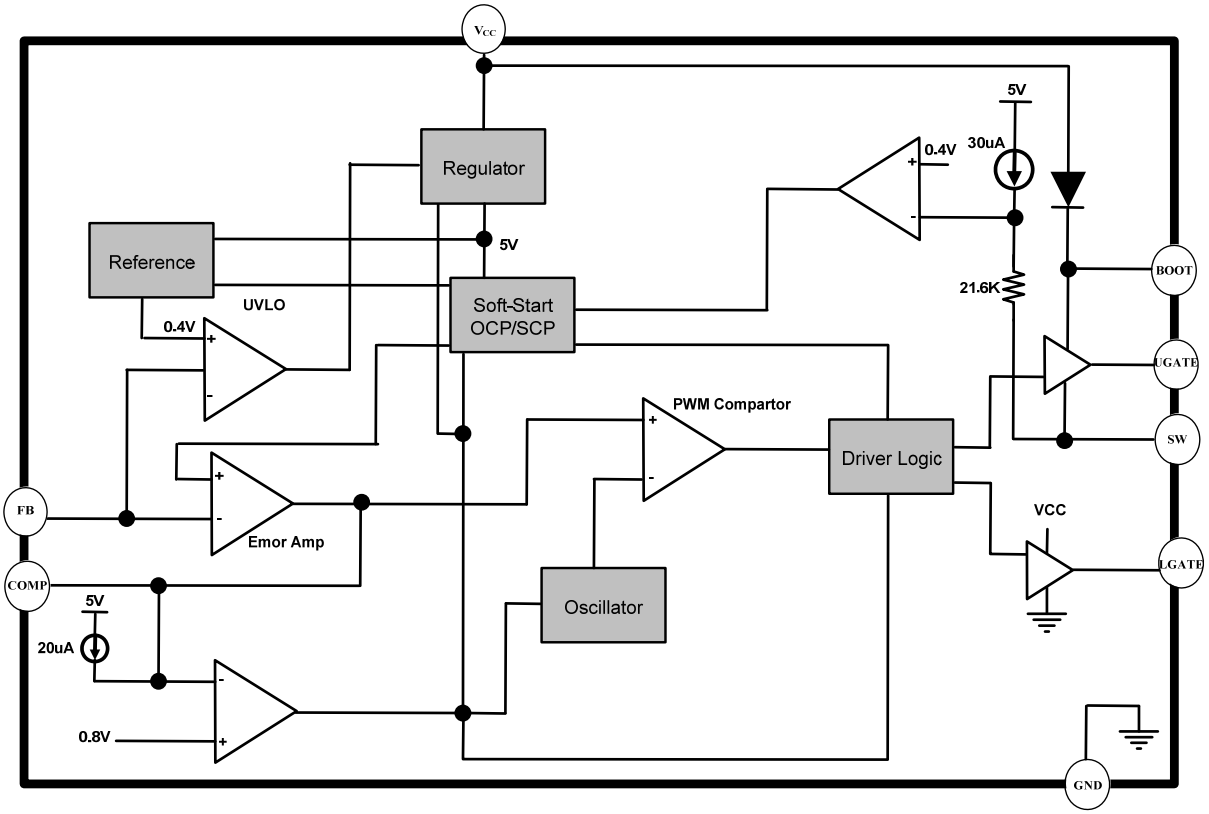
Applications

- Graphic Card
- Telecom and Datacom Applications
- High Power DC-DC Regulators

Typical Application Circuit

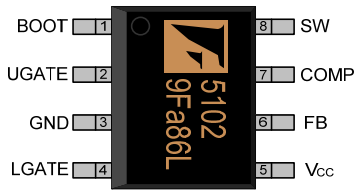


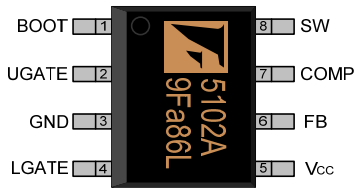
Function Block Diagram



Pin Descriptions

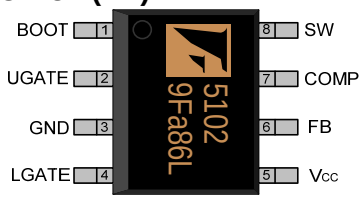
SOP-8L



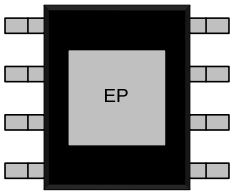


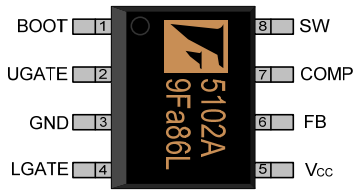
Name	No.	I/O	Description
BOOT	1	P	Boosted Power Supply Pin for High Side MOS Gate Driving
UGATE	2	O	High Side Gate Driver Output
GND	3	P	Ground
LGATE	4	O	Low Side Gate Driver Output
V_{CC}	5	P	IC Power Supply
FB	6	I	Error Amplifier Inverting Input
COMP	7	O	Error Amplifier Output
SW	8	I	Switch Signal Input

SOP-8L (EP)

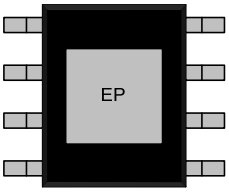


Bottom View



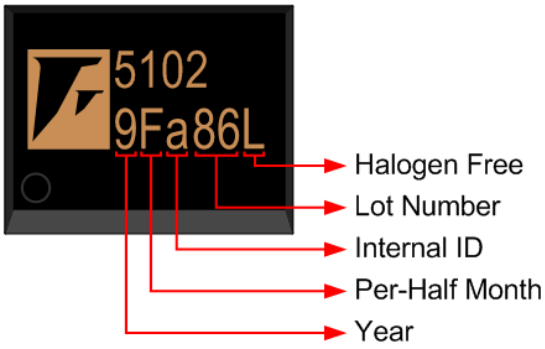


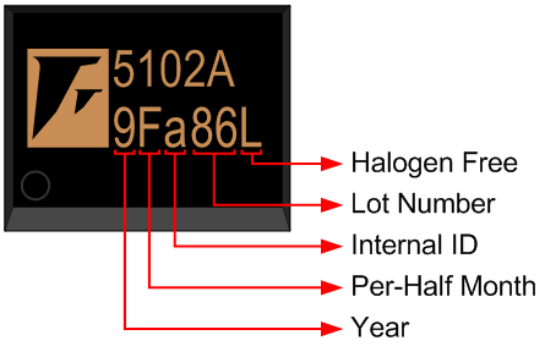
Bottom View



Marking Information

SOP-8L (EP) & SOP-8L





Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

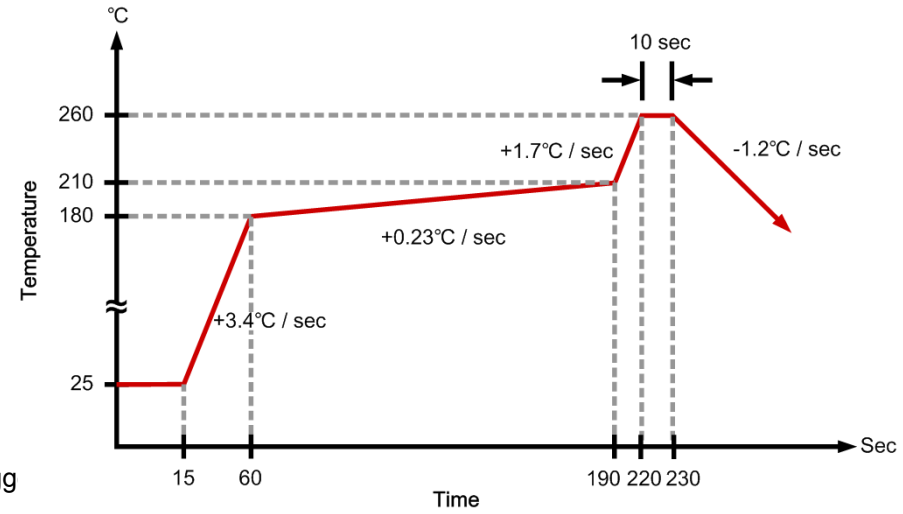
Ordering Information

Part Number	OSC Freq.	Operating Temperature	Package	MOQ	Description
FP5102DR-LF	300KHz	-40°C ~ +85 C	SOP-8L	2500EA	Tape & Reel
FP5102XR-LF			SOP-8L (EP)	2500EA	Tape & Reel
FP5102ADR-LF	600KHz	-40°C ~ +85°C	SOP-8L	2500EA	Tape & Reel
FP5102AXR-LF			SOP-8L (EP)	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}				+15	V
BOOT Supply Voltage	V_{BOOT}		-0.6		+30	V
BOOT to SW (V_{BOOT}-V_{SW})					+15	V
SW Voltage	V_{SW}		-0.6		+15	V
UGATE Voltage	V_{UGATE}		V_{SW} -0.3		V_{BOOT} + 0.3	V
LGATE Voltage	V_{LGATE}		-0.6		V_{CC} + 0.3	V
FB, COMP Voltage			-0.6		6	V
Allowable Power Dissipation		SOP-8L			0.5	W
		SOP-8L (EP)			1.3	W
Thermal Resistance (Junction to Ambient)	θ_{JA}	SOP-8L		+120		°C / W
		SOP-8L (EP)		+50		°C / W
Thermal Resistance (Junction to Case)	θ_{JC}	SOP-8L		+20		°C / W
		SOP-8L (EP)		+10		°C / W
SOP8 (EP) Lead Temperature (soldering, 10sec)					+260	°C

IR Re-flow Soldering Curve



Note:

1. Sugg

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.3	5	13.2	V
Operating Temperature			-40		+85	°C
Operating Junction Temperature			-40		+125	°C

DC Electrical Characteristics (V_{CC}= 12V, T_A=25°C, unless otherwise specified)

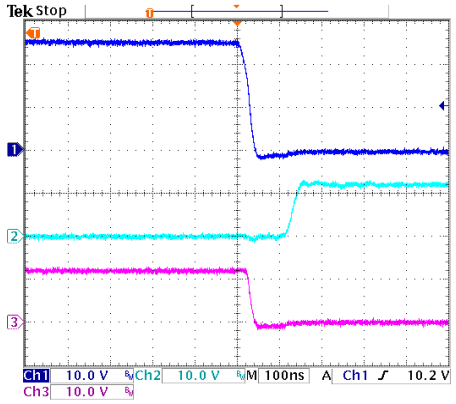
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Supply Current						
Standby Current	$I_{SHUTDOWN}$	V_{COMP}=0V		640		μA
Supply Current	I_{SUPPLY}	U_{GATE} and L_{GATE} open		5		mA
Enable / Disable						
UVLO Threshold Voltage	V_{UVLO}		3.9	4.1	4.3	V
Hysteresis Voltage	V_{HYS}		0.3	0.35	0.4	V
Oscillator						
Oscillation Frequency	f	FP5102	250	300	350	KHz
		FP5102A	500	600	700	KHz
Ramp Amplitude	ΔV_{OSC}			1.5		V_{P-P}

DC Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference						
Reference Voltage	V_{FB}		0.784	0.8	0.816	V
V_{FB} Change with Voltage	ΔV_{FB}	V_{CC}=10.8V to 13.2V		5	20	mV
V_{FB} Change with Temperature	$\Delta V_{FB} / \Delta T$	T_A = -40°C to 85°C		1		%
Error Amplifier						
Unity Gain Bandwidth Product	BW			15		MHz
Open Loop DC Gain	A_{VO}			88		dB
Gate Drivers						
Upper Gate Source Current	I_{UGASR}	V_{BOOT} - V_{SW}=12V V_{BOOT} - V_{UGATE}=6V		300		mA
Upper Gate Source Resistance	R_{UGSR}	V_{BOOT} - V_{SW}=12V V_{BOOT} - V_{UGATE}=1V		7	10	Ω
Upper Gate Sink Resistance	R_{UGSN}	V_{BOOT} - V_{SW}=12V V_{UGATE} - V_{SW}=1V		4	8	Ω
Lower Gate Source Current	I_{LGSR}	V_{CC}=12V, V_{LGATE} =6V		500		mA
Lower Gate Source Resistance	R_{LGSR}	V_{CC}=12V, V_{CC} - V_{LGATE}=1V		4	6	Ω
Lower Gate Sink Resistance	R_{LGSN}	V_{CC}=12V, V_{LGATE}=1V		2	4	Ω
Protection						
FB Under Voltage Protection	V_{FBUV}		0.3	0.4	0.5	V
Over Current Threshold	V_{OC}		-210	-250	-290	mV
Soft-Start Interval	T_{SS}		2	3.2	4.2	ms

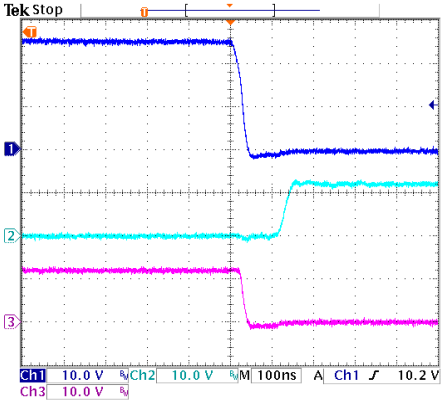
TYPICAL CHATACTERISTICS

UGATE Rising Time



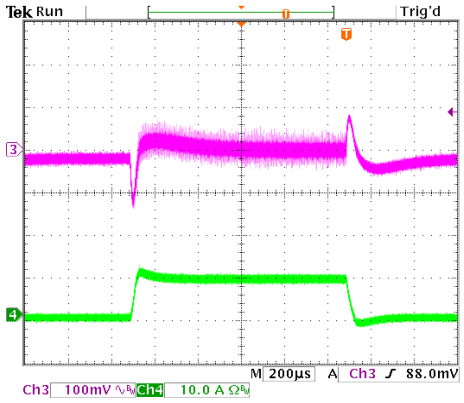
CH1:UGATE CH2:LGATE CH3:SW

UGATE Falling Time



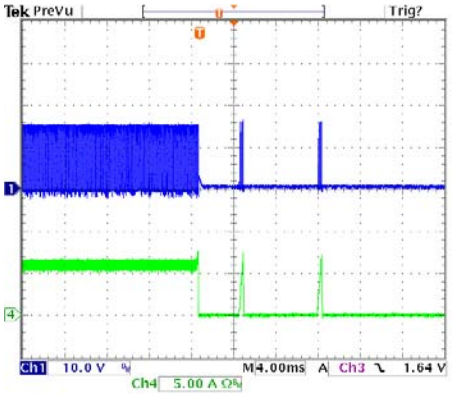
CH1:UGATE CH2:LGATE CH3:SW

Load Transient Response



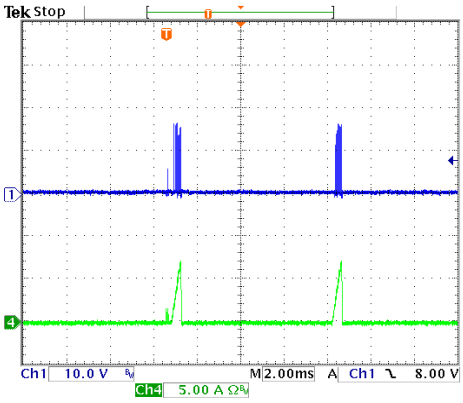
CH3:Vout CH4:I_L

Power On then Trigger OCP



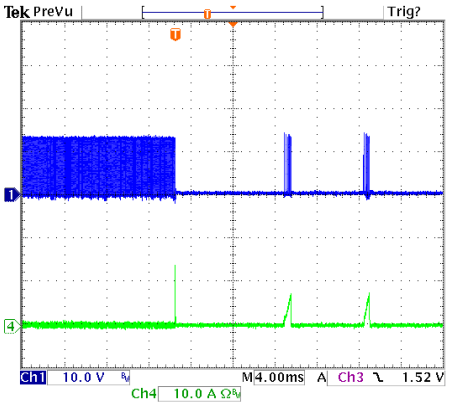
CH1:UGATE CH4:I_L

OCP then Power On



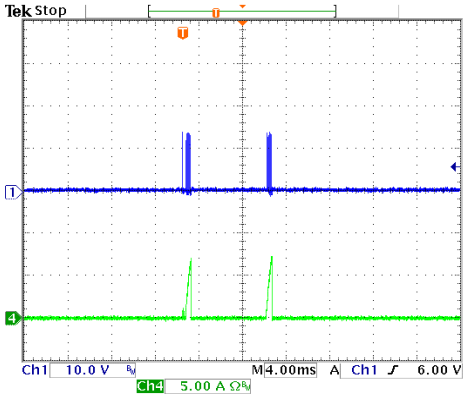
CH1:UGATE CH4:I_L

Power On then Shorted



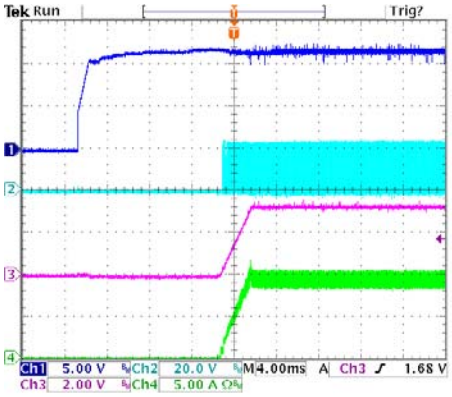
CH1:UGATE CH4:I_L

Shorted then Power On



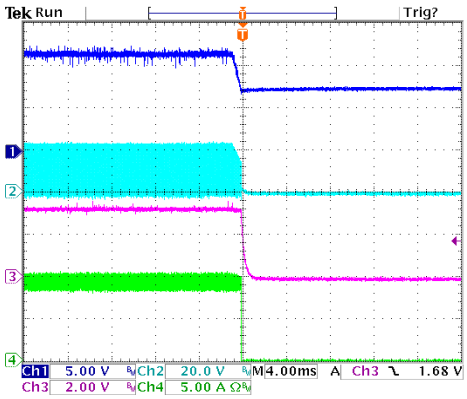
CH1:UGATE CH4:I_L

Power ON



CH1:Vin CH2:HGATE CH3:Vout CH4:I_L

Power OFF



CH1:Vin CH2:HGATE CH3:Vout CH4:I_L

Function Description

Power On Reset

The FP5102 / A automatically initializes upon input power V_{CC}. The Power-On Reset (POR) function continually monitors the bias voltage at the V_{CC} pin. The POR threshold level is typically 4.1V at V_{CC} rising.

V_{IN} Detection

After POR is outstripped, the FP5102 / A continuously generates a 10kHz pulse train with 1μs pulse width to turn on the upper MOSFET for detecting the existence of V_{IN}. FP5102 / A keeps monitoring SW pin voltage during the detection period. When the SW voltage crosses 1.5V two times, V_{IN} existence is recognized and the FP5102 / A initiates its soft start cycle as described in next section.

Soft Start

After the existence of V_{IN} is detected, the soft-start (SS) begins automatically. The feedback voltage (V_{FB}) is clamped by internal linear ramping up SS voltage during this period, causing PWM pulse width increasing slowly and thus inducing little surge current. The maximum load current is available after the soft-start cycle is completed. Soft-start completes when SS voltage exceeds internal reference voltage (0.8V), the time duration is about 3.2ms.

Over Current Protection

The FP5102 / A senses the current flowing through lower MOSFET for over current protection (OCP) by sensing the SW pin voltage as shown in the Functional Block Diagram.

A 30μA current source flows through the internal resistor 21.6kΩ to SW pin causing 0.65V voltage drop across the resistor. OCP is triggered if the voltage at SW pin (drop of lower MOSFET V_{DS}) is lower than -0.25V when low side MOSFET conducting. Accordingly inductor current threshold for OCP is a function of conducting resistance of lower MOSFET $RDS_{(ON)}$ as :

$$I_{OCSET} = \frac{-0.25V}{R_{DS(ON)}}$$

If MOSFET with $R_{DS\,(ON)}$ = 10mΩ is used, the OCP threshold current is about 25A. Once OCP is triggered, the FP5102 / A enters hiccup mode and re-soft starts again. The FP5102 / A shuts down after OCP hiccups twice.

To prevent the over current protection occurs in the normal operating load range, the drift of all

parameters in the above equation should be considered.

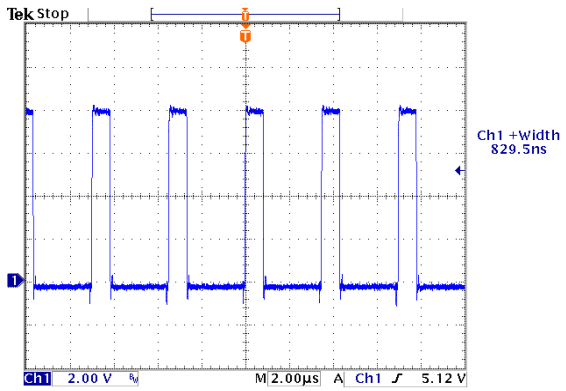
-The $R_{DS\ (ON)}$ of MOSFET varies with temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.

-The parasitic series resistance in PCB's trace must be considered and added to $R_{DS\ (ON)}$ in the above equation.

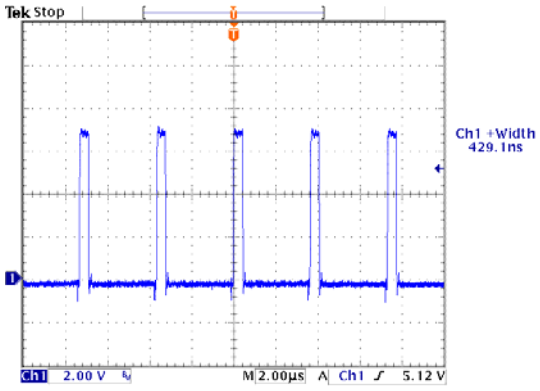
-The minimum I_{OCSET} (=-0.21V/$R_{DS\ (ON)}$) should be considered over the above equation.

Note that the I_{OCSET} is the current flow through the low side MOSFET. I_{OCSET} must be greater than maximum output current add the half of inductor ripple current. That is,

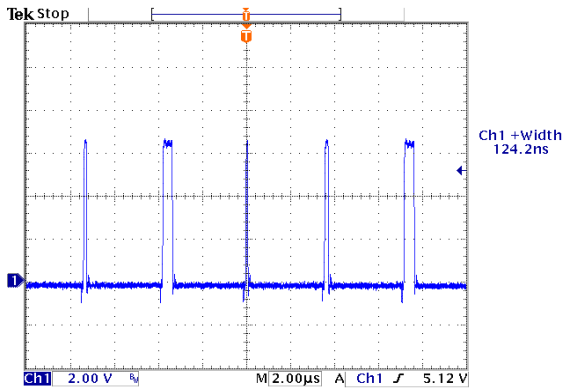
$$I_{OCSET} > I_{O(MAX)} + \frac{\Delta I_{L(MAX)}}{2}$$



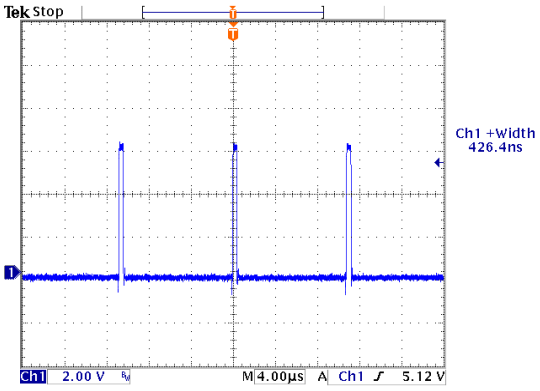
LGATE>425ns



LGATE=425ns



LGATE<425ns



LGATE<<425ns

To avoid the gate transition noise and ringing on the SW pin, the actual monitoring of the bottom-side MOSFET's on-resistance starts 200ns (nominal) after the LGATE rising edge. The

monitoring ends when the LGATE goes low. The OCP can be detected anywhere within the above window. If the regulator is running at high UGATE duty cycles (around 75% for 600kHz or 87% for 300kHz operation), then the LGATE pulse width may be not wide enough for the OCP to properly sample the V_{SW}. For those cases, if the LGATE is too narrow (or not there at all) for 3 consecutive pulses, then the third pulse will be stretched and/or inserted to the 425ns minimum width. This allows for OCP monitoring every three pulses under this kind of condition. This can introduce a small pulse-width error on the output voltage, which will be corrected on the next pulse; and the output ripple voltage will have an unusual 3-clock pattern, which may look like jitter.

Application Information

Frequency Compensation

The FP5102 / A is a voltage-mode controller for a synchronous-rectified buck converter. Figure 1 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The error amplifier (ERROR AMP) output (V_{COMP}) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the SW node. The PWM wave is smoothed by the output LC filter (L_{OUT} and C_{OUT}).

The modulator transfer function is the small-signal transfer function of V_{OUT} / V_{COMP}. This function is dominated by a DC gain and the output filter (L_{OUT} and C_{OUT}), with a double-pole break frequency at F_{LC} and a zero at F_{ESR}. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage (ΔV_{OSC}). The following equations define the modulator break frequencies as a function of the output LC filter:

$$F_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as following:

$$F_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

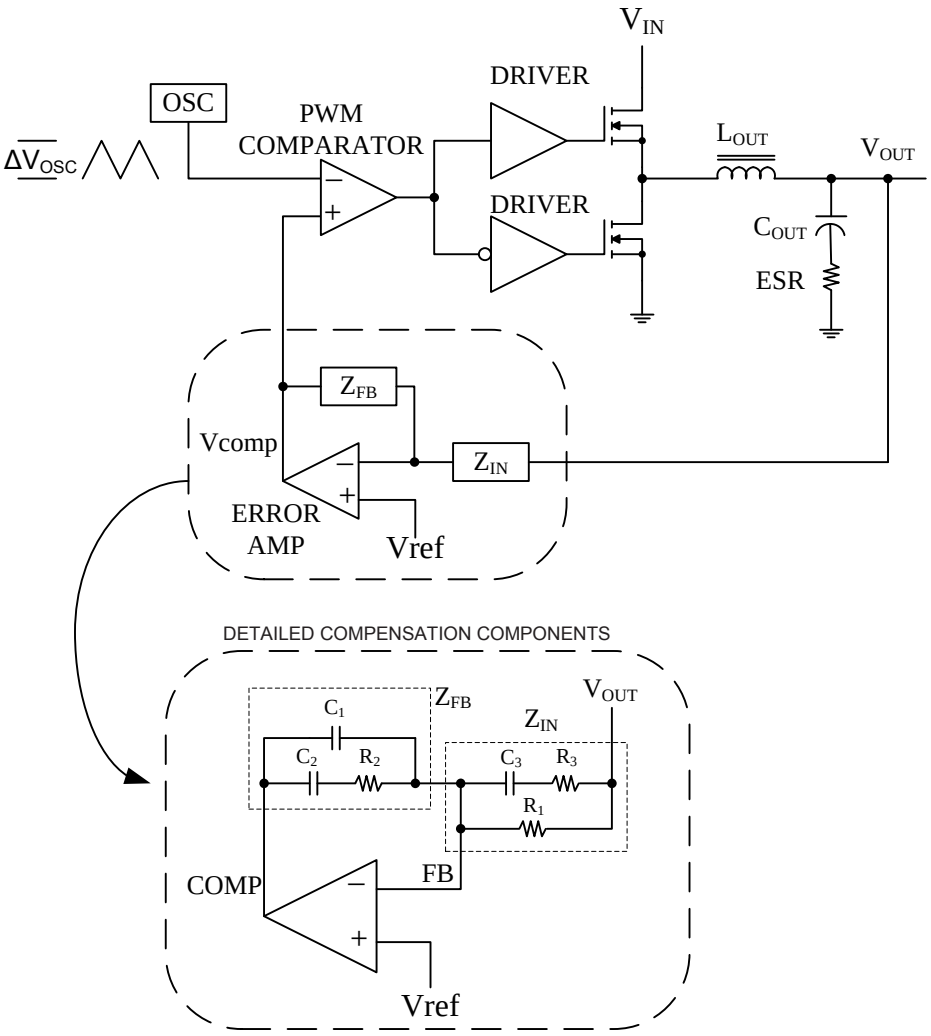


Figure 1 Voltage-mode Buck Converter Compensation Design

The compensation network consists of the error amplifier (internal to the FP5102 / A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0dB crossing frequency (F_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at F_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros, and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3), shown in Figure 1.

$$F_{Z1} = \frac{1}{2\pi R_2 C_2}$$

$$F_{P1} = \frac{1}{2\pi R_2 (\frac{C_1 C_2}{C_1 + C_2})}$$

$$F_{Z2} = \frac{1}{2\pi C_3 (R_1 + R_3)}$$

$$F_{P2} = \frac{1}{2\pi R_3 C_3}$$

Use the following steps to locate the poles and zeros of the compensation network.

1. Pick gain (R_2/R_1) for the desired converter bandwidth.

   Choose a value for R_1, usually between 1K and 10K.

   Select the desired zero crossover frequency

   $$F_O : (1/5 \sim 1/10) \times F_S > F_{ESR}$$

   Use the following equation to calculate R_2:

   $$R_2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R_1$$

2. Place the first zero below the filter's double pole (~75% F_{LC}).

   $$F_{Z1} = 0.75 \times F_{LC}$$

   Calculate the C_2 by the equation:

   $$C_2 = \frac{1}{2\pi \times R_2 \times F_{LC} \times 0.75}$$

3. Place the first pole at the ESR zero.

   $$F_{P1} = F_{ESR}$$

   Calculate the C_1 by the equation:

   $$C_1 = \frac{C_2}{2\pi \times R_2 \times C_2 \times F_{ESR} - 1}$$

4. Place the second zero at filter's double pole.

5. Place the second pole at half the switching frequency.

   $$F_{P2} = 0.5 \times F_S$$

   $$F_{Z2} = F_{LC}$$

   Combine above two equations will get the following component equations

   $$R_3 = \frac{R_1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

   $$C_3 = \frac{1}{\pi \times R_3 \times F_S}$$

6. Check the gain against the error amplifier's open loop gain.

7. Estimate phase margin. Repeat if necessary.

Figure 2 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual modulator gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 2. Using the above guidelines should give a compensation gain similar to the red curve plotted. The open-loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The closed-loop gain is constructed on the graph of Figure 2 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiply the modulator transfer function by the compensation transfer function and plotting the gain. The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable high bandwidth overall loop. A stable control loop has a gain crossing with a –20dB/decade slope and a phase margin greater than 45°. Include worst-case component variations when determining phase margin.

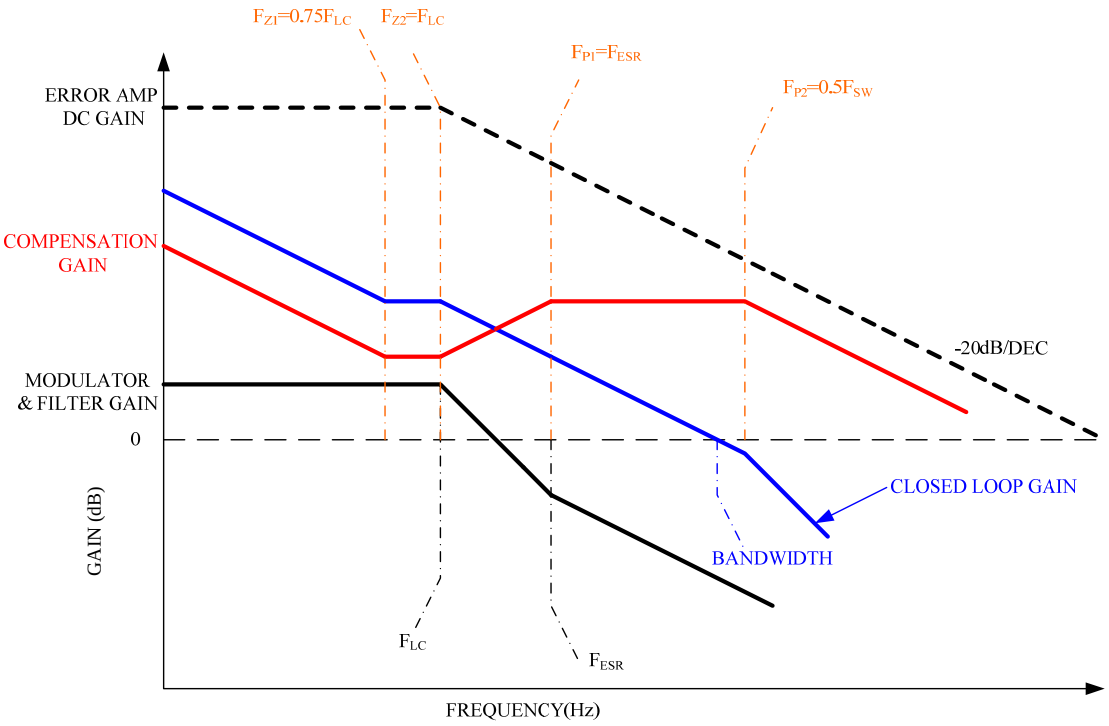


Figure 2. Asymptotic Bode Plot of Converter Gain

Component Selection

Input capacitor Selection

The voltage rating at maximum ambient temperature should be 1.25 to 1.5 times the maximum input voltage. More conservative approaches can bring the voltage rating up to 2 times the maximum input voltage. High frequency decoupling, which is highly recommended, is implemented through the use of ceramic capacitors in parallel with the bulk capacitor filtering.

In switch mode, the input current is discontinuous in a buck converter. The source current of the high-side MOSFET is a square wave. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The RMS value of input capacitor current can be calculated by:

$$I_{RMS} = I_{O\_MAX}\sqrt{\frac{V_O}{V_{IN}}\left(1-\frac{V_O}{V_{IN}}\right)}$$

It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is I_{O_MAX}/2.

Inductor Selection

The value of the inductor is selected based on the desired ripple current. Large inductance gives low inductor ripple current and small inductance result in high ripple current. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current. In experience, the value is to allow the peak-to-peak ripple current in the inductor to be 10%~20% maximum load current. The inductance value can be calculated by:

$$L = \frac{(V_{IN}-V_O)}{f\times\Delta I_L}\frac{V_O}{V_{IN}} = \frac{(V_{IN}-V_O)}{f\times[2\times(10\%\sim 20\%)I_O]}\frac{V_O}{V_{IN}}$$

The inductor ripple current can be calculated by:

$$\Delta I_L = \frac{V_O}{f\times L}\times\left(1-\frac{V_O}{V_{IN}}\right)$$

Choose an inductor that does not saturate under the worst-case load conditions even at the highest operating temperature. (The load current plus half the peak-to-peak inductor ripple current). The peak Inductor current is:

$$I_{L\_PEAK} = I_O + \frac{\Delta I_L}{2}$$

MOSFET Selection

There are three major aspects of power loss that are associated with the MOSFET. These are conduction losses, switching losses, and gate drive power losses.

$$P_{D(MOSFET)} = P_{conduction} + P_{switching} + P_{gate}$$

$$P_{D(Hligh\_MOSFET)} = I_O{}^2 \times R_{DS(ON)} \times D + \frac{1}{2} V_{IN} \times I_O \times (t_r + t_f) \times f_s + Q_{Gate} \times V_{GS} \times f_s$$

$$P_{D(Hligh\_MOSFET)} = I_O{}^2 \times R_{DS(ON)} \times (1-D) + \frac{1}{2} V_f \times I_O \times (t_r + t_f) \times f_s + Q_{Gate} \times V_{GS} \times f_s$$

V_{IN} = Input Voltage for

V_f = Lower side turn on V_{DS}

I_O = Output Current

D = Duty Cycle

t_r = MOSFET rising time

t_f = MOSFET rising time

f_s = Switching Frequency

Q_{Gate} = MOSFET gate charge

V_{GS} = MOSFET gate voltage

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. The output ripple is determined by:

$$\Delta V_O = \Delta I_L \times \left(ESR_{COUT} + \frac{1}{8 \times f \times C_{OUT}} \right)$$

Where f = operating frequency, C_{OUT}= output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

The most commonly used choice for output bulk capacitors is aluminum electrolytic capacitors because of their low cost and low ESR. Due to the capacitor ESR varies with frequency, user should consider the ESR value rated at the PWM frequency.

The output capacitance should also include a number of small capacitance value ceramic capacitors placed as close as possible to the chip; 0.1μF and 0.01μF are recommended values.

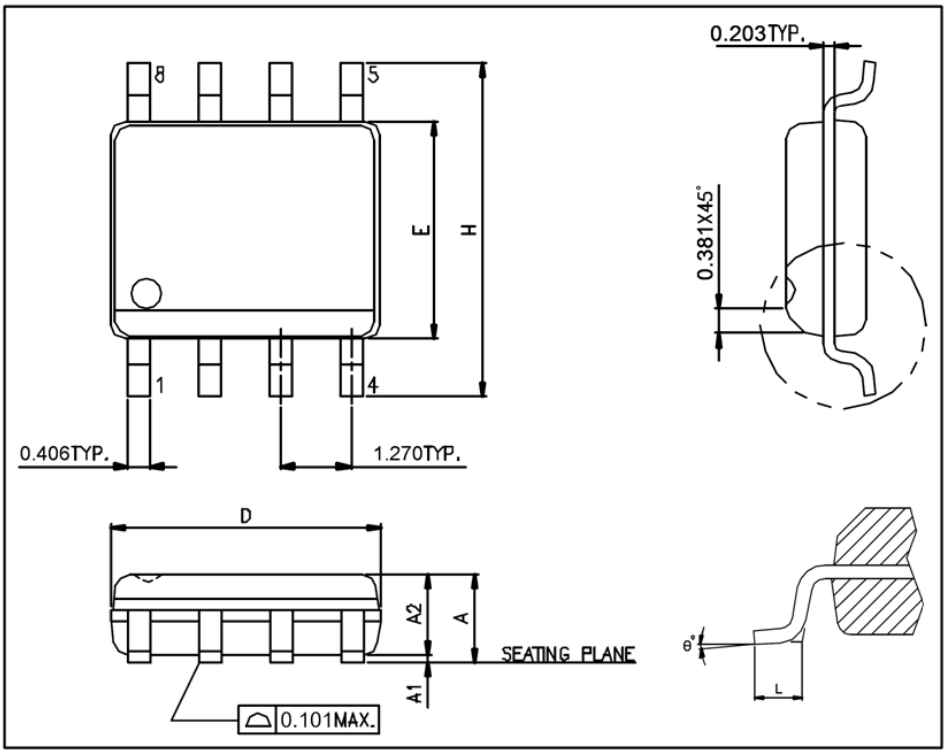
PC Board Layout Checklist

The switching power converter layout is critical to achieve low power losses, clean waveforms, and stable operation. It needs careful attention. Following are specific recommendations for good board layout:

1. Keep the high current traces and load connections as short as possible.
2. Use thick copper plated PCB whenever possible to achieve higher efficiency.
3. Keep the loop area between the SW node, low-side MOSFET, Inductor, and the output capacitor as small as possible.
4. Route high DV / Dt signals, such as SW node, away from the error amplifier input/output pins. Keep both the high DV / Dt signals and the error amplifier input/output signals as short as possible.
5. Place V_{CC} ceramic decoupling capacitors very close to V_{CC} pin.
6. All input signals are referenced with respect to GND pin. Dedicate large copper area of the PCB for a GND plane.
7. Minimize GND loops in the layout to avoid EMI-related issues.
8. Use wide traces for the lower gate drive to keep the drive impedances low.
9. Use wide land areas with appropriate thermal vias to effectively remove heat from the MOSFETs.
10. Preserve the snubber circuit to minimize high frequency ringing at SW node for EMI issues.

Package Outline

SOP-8L



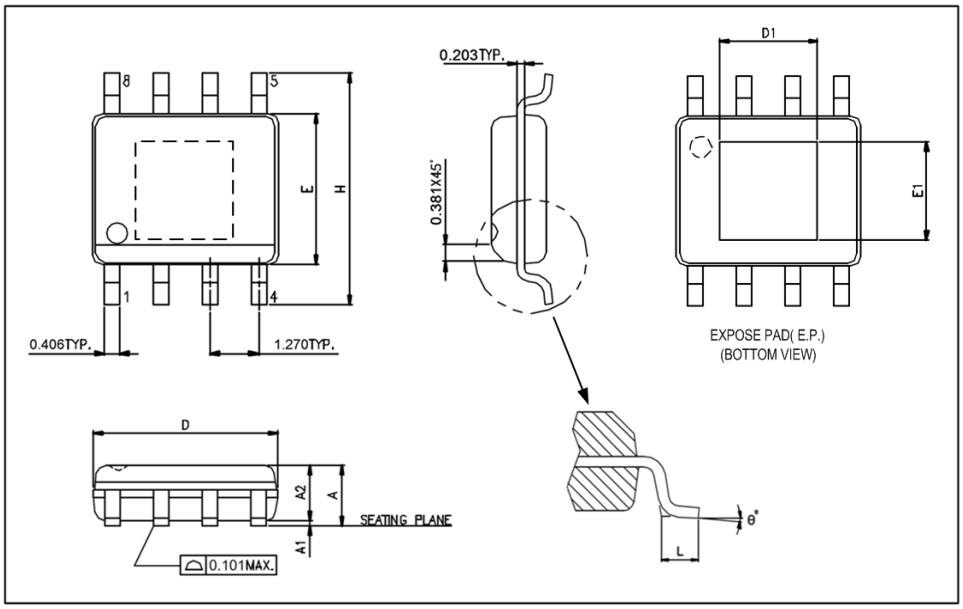
UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.

SOP-8L (EP)



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	2.184 REF	
D1	2.971 REF	

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension ”D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.