AN1279

Offline UPS Reference Design Using the dsPIC® DSC

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UPS OVERVIEW

An Uninterruptible Power Supply, or UPS, is an electronic device that provides an alternative electric power supply to connected electronic equipment when the primary power source is not available.

Unlike auxiliary power, a UPS can provide instant power to connected equipment, which can protect sensitive electronic devices by allowing them to shut down properly and preventing extensive physical damage. However, a UPS can only supply energy for a limited amount of time, typically 15 to 20 minutes. Although its use can extend to a virtually unlimited list of applications, in past years the UPS has become even more popular as a means of protecting computers and telecommunication equipment, thus preventing serious hardware damage and data loss.

Application Markets for UPS Systems

UPS systems provide for a large number of applications in a variety of industries. Their common applications range from small power rating for personal computer systems to medium power rating for medical facilities, life-support systems, data storage, and emergency equipment, and high power rating for telecommunications, industrial processing, and online management systems. Different considerations should be taken into account for these applications. As an example, a UPS for emergency systems and lighting may support the system for 90-120 minutes. For other applications like computer backup power, a UPS may typically support the system for 15-20 minutes. If power is not restored during that time, the system will be gracefully shut down.

If a longer backup period is considered, a larger battery is required. For process equipment and high power applications, some UPS systems are designed to provide enough time for the secondary power sources, such as diesel generators, to start up.

Types of UPS Systems

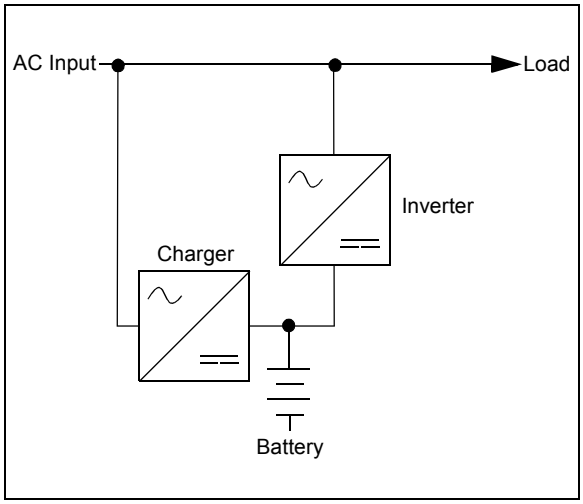
A typical UPS for computers has four basic protection roles: being able to cope with power surges, voltage shortage, complete power failure and wide variations in the electric current frequency. There are three types of UPS systems, depending on how the electric power is being stored and relayed to the electronic device connected to them:

- Offline UPS (also known as Standby UPS)
- Line-Interactive (or Continuous UPS)
- Online UPS (often called double conversion supply)

OFFLINE UPS

An Offline UPS system (see Figure 1), redirects the electric energy received from the AC input to the load and only switches to providing power from the battery when a problem is detected in the utility power. Performing this action usually takes a few milliseconds, during which time the power inverter starts supplying electric energy from the battery to the load.

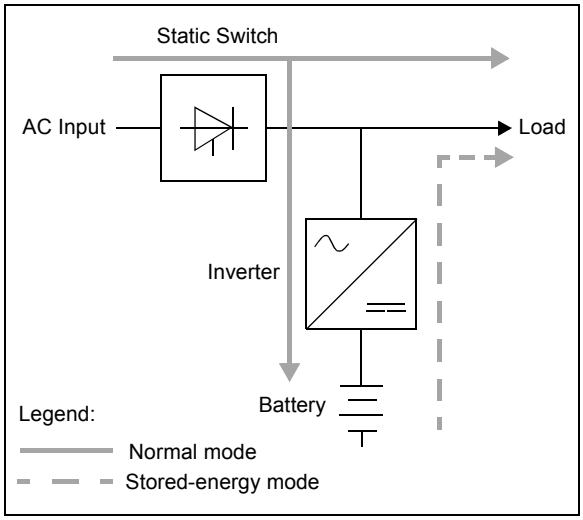
FIGURE 1: OFFLINE UPS DIAGRAM



LINE-INTERACTIVE UPS

A Line-Interactive UPS (see Figure 2), always relays electric energy through the battery to the load. When AC mains power is available, the battery is being charged continuously. At the same time, the UPS regulates the AC output voltage and the lag related to coupling the inverter is nearly zero. When a power outage occurs, the transfer switch opens and the electric energy flows from the battery to the load (Stored Energy mode). Due to these characteristics, continuous UPS systems tend to be somewhat more expensive than an offline UPS.

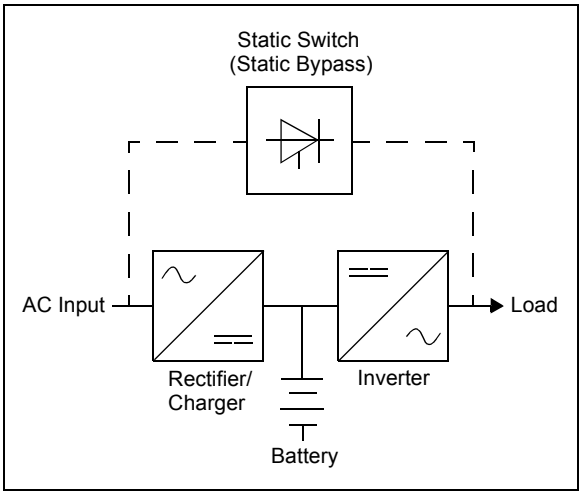
FIGURE 2: LINE-INTERACTIVE UPS DIAGRAM



ONLINE UPS

An Online UPS (see Figure 3), combines the two basic technologies of the previously described UPS models, with rectifiers and inverter systems working all of the time. As is the case with a Line-Interactive UPS, the power transfer is made instantly as an outage occurs, with the rectifier simply being turned off while the inverter draws power from the battery. As utility power is again established, the inverter continues to supply power to the connected devices, while the rectifier resumes its activity, recharging the battery. This design is sometimes fitted with an additional transfer switch for bypass during a malfunction or overload.

FIGURE 3: ONLINE UPS DIAGRAM



SYSTEM SPECIFICATIONS

The reference design in this application note describes the design of an Offline Uninterruptible Power Supply (UPS) using a Switch Mode Power Supply (SMPS) dsPIC® Digital Signal Controller (DSC).

The Offline UPS Reference Design consists of three major UPS topology blocks:

- Push-Pull Converter (steps up the DC battery voltage to a constant high-voltage DC)
- Full-Bridge Inverter (converts DC voltage to a sinusoidal AC output)
- Flyback Switch Mode Charger (current source and charges battery with constant current)

The input and output specifications are shown in Table 1.

TABLE 1: I/O SPECIFICATIONS

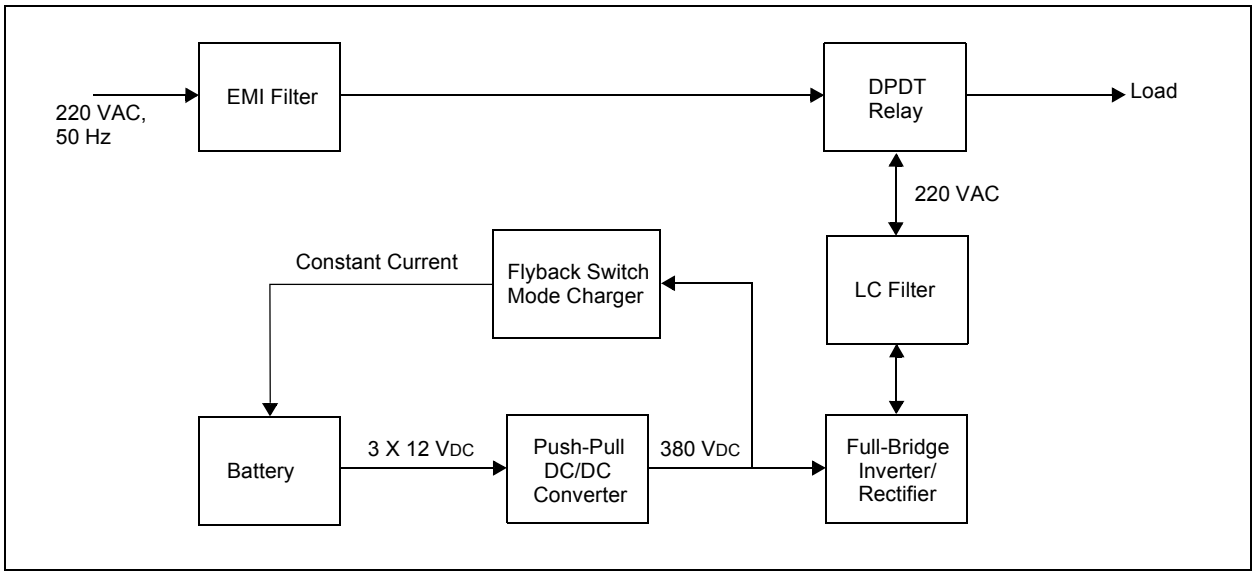
220V UPS Version Specifications	
AC Input	220 VAC ±10%, 50 Hz ±3 Hz
DC Input	3 x 12 VDC (lead acid battery)
UPS Output	220 VAC, 50 Hz ±1 Hz, sinusoidal
Rating	1000 W/1000 VA, (1300VA - 2 seconds)
Input Filtering	EMI/RFI filtering
110V UPS Specifications	
AC Input	110 VAC ±10%, 60 Hz ±3 Hz
DC Input	3 x 12 VDC (lead acid battery)
UPS Output	110 VAC, 60 Hz ±1 Hz, sinusoidal
Rating	1000 W/1000 VA, (1300VA - 2 seconds)
Input Filtering	EMI/RFI filtering

1 kVA OFFLINE UPS REFERENCE DESIGN

The Offline UPS system shown in Figure 4 operates in Standby mode and in UPS mode. When AC line voltage is present, the system is in Standby mode until a failure occurs on the AC line. During Standby mode, the battery is charged and is maintained after becoming fully charged. When the battery is charging, the inverter works as a rectifier through the IGBT's anti-parallel diodes. The flyback switch mode charger acts as a current generator and provides constant charging current to the battery.

After a power failure, the system is switched to UPS mode. In this situation, the DPDT relay is turned OFF to prevent power from being delivered to the AC line. The push-pull converter steps up the battery voltage to 380 V_{DC}. The high DC voltage is then converted with the full-bridge inverter and filtered with an LC filter to create a pure sine wave 220/110 VAC output where load is connected. This power switchover sequence is made in less than 10 ms.

FIGURE 4: OFFLINE UPS REFERENCE DESIGN



Listing of I/O Signals for Each Block, Type of Signal, and Expected Signal Levels

PUSH-PULL CONVERTER

As specified in Figure 5, measurement of DC output voltage (UDCM) is required to implement the control algorithm. The EPP signal is for enabling the driver, the temperature sensor measures heat sink temperature, and the primary current measurement (IP) protects the converter in case of transformer flux walking. The PWM outputs from the dsPIC DSC are firing pulses to the driver to control the output voltage.

FIGURE 5: PUSH-PULL CONVERTER RESOURCE DIAGRAM

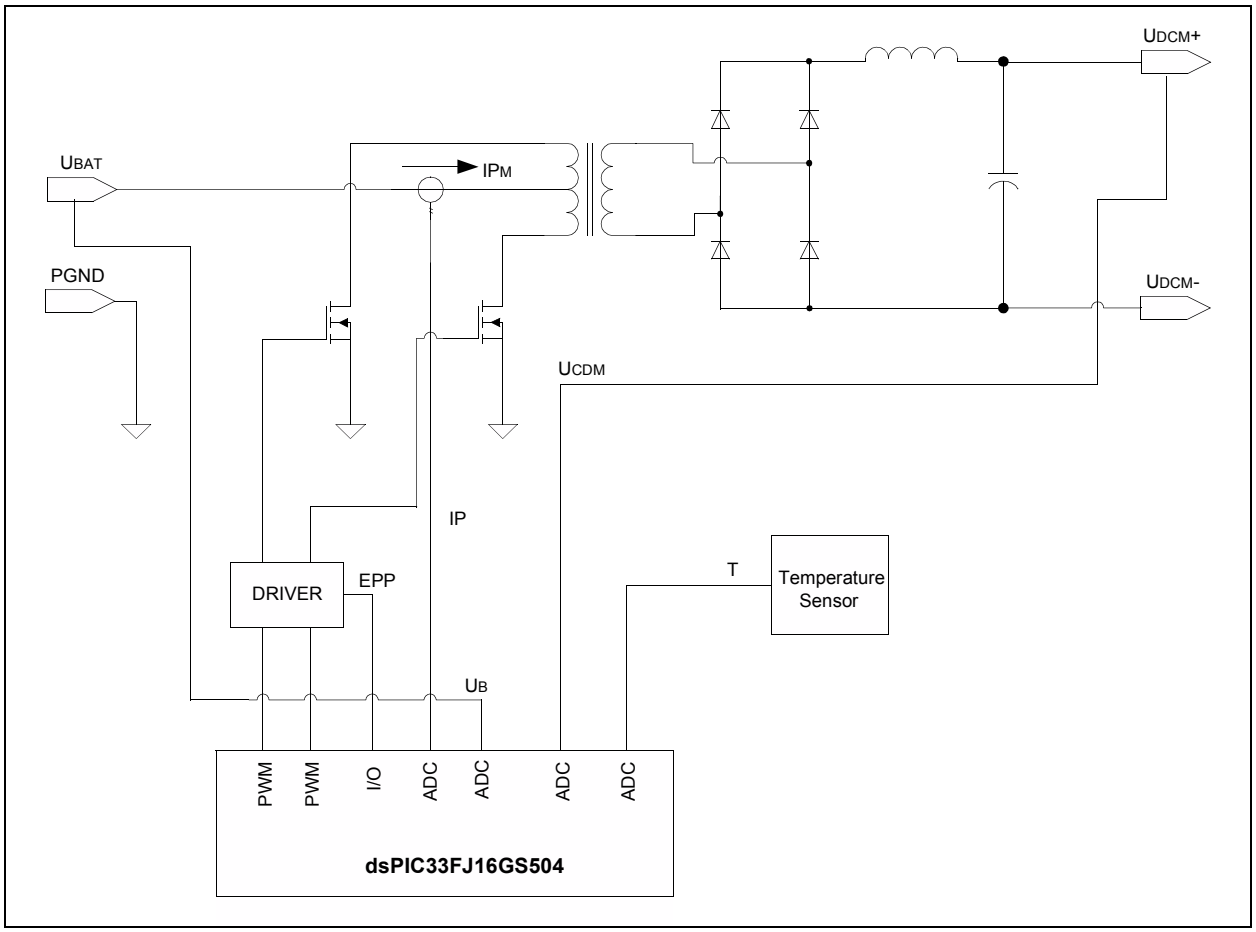


Table 2 lists the resources used by the dsPIC DSC device for a push-pull converter.

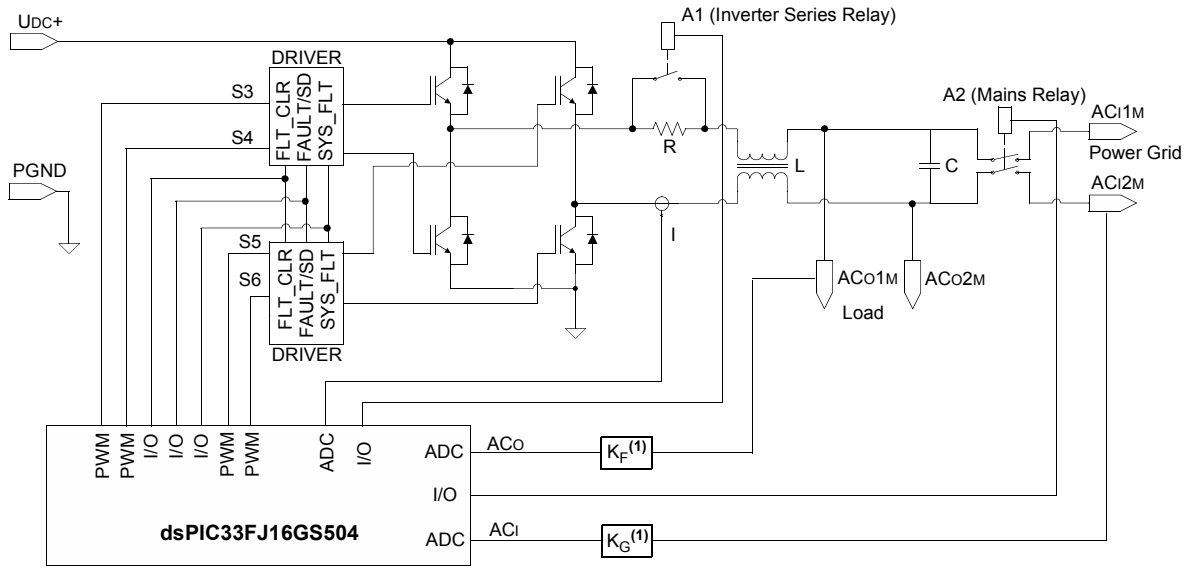
TABLE 2: RESOURCES REQUIRED FOR A DIGITAL PUSH-PULL CONVERTER

Signal Name	Type of Signal	dsPIC® DSC Resources Used	Expected Signal Level
UDCM	Analog	AN3	2.99V
IP	Analog	AN2	0V-1.65V
T (optional, not implemented in software)	Analog	AN8	0V-3.3V
UB	Analog	AN5	1.5V-1.98V
EPP	Enable driver, Digital	RB6	—
Push-Pull Gate Drive	Digital	PWM3H, PWM3L	—

FULL-BRIDGE INVERTER

The block diagram in Figure 6 illustrates that measurement of the AC output voltage (AC_O) is required to implement the control algorithm. With measurement of the output current (I), that current can be limited to prevent overloading of the converter. The presence of power grid voltage is detected with measurement of (AC_I) voltage. When power grid voltage fails, signal A2 turns off the relay K2 and prevents power flow to the line when the UPS is operational. Signal A1 controls the K1 relay, which is off when DC link voltage is low to prevent current inrush in the DC link capacitors when power grid voltage is fed to the rectifier. This happens when the UPS is operational and the battery is depleted, the UPS goes off or initial system connect to grid power. The FLT_CLR signal is used to reset the driver when a fault is detected. FAULT/SD and SYS_FLT are used to enable or disable the driver or detect driver faults. Detailed descriptions of these signals can be found in the data sheet of the drivers (IR2214). Switching of the inverter leg IGBTs is controlled by firing pulses S3, S4 and S5, S6, and is generated by the dsPIC DSC PWM modules.

FIGURE 6: DIGITAL FULL-BRIDGE INVERTER RESOURCE DIAGRAM



Note 1: KF and KG are feedback gain circuits. Refer to **Appendix D: "Schematics and Board Layout"** for details.

Table 3 shows the resources used by a dsPIC DSC device for a full-bridge inverter.

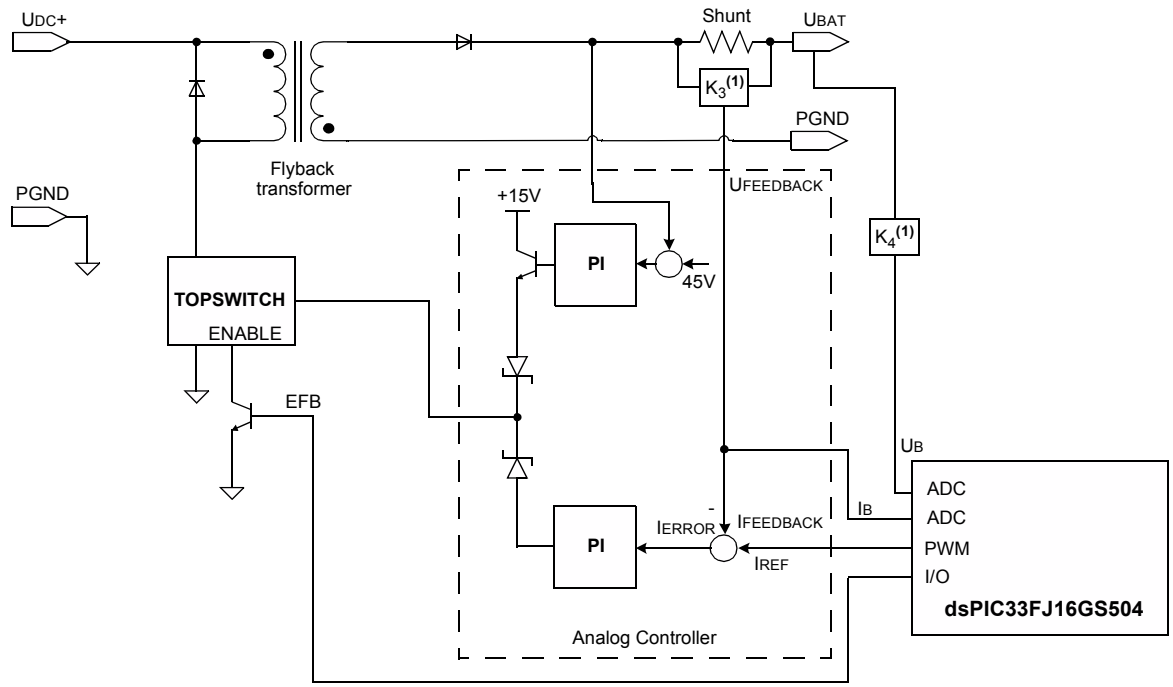
TABLE 3: RESOURCES REQUIRED FOR A DIGITAL FULL-BRIDGE INVERTER

Signal Name	Type of Signal	dsPIC® DSC Resources Used	Expected Signal Level
AC_O	Analog	AN1	0.27V-3.3V
AC_I	Analog	AN11	0.15V-3.16V
I	Analog	AN0	2.5V (nominal)
A1	Digital output	RC10	—
A2	Digital output	RC0	—
FLT_CLR	Digital output	RB7	—
FAULT/SD	Digital input (external interrupt)	RC13 (INT1)	—
SYS_FLT	Digital input	RC8	—
S3, S4 (gate drive)	PWM output	PWM1H, PWM1L	—
S5, S6 (gate drive)	PWM output	PWM2H, PWM2L	—

FLYBACK SWITCH MODE CHARGER

The block diagram in Figure 7 shows that an analog current controller is used for battery charging. Four signals are needed: EFB signal for enabling topswitch, (I_B) for measuring battery charging current, (U_B) for measuring battery voltage and I_{REF} for reference set with PWM4L output.

FIGURE 7: DIGITAL FLYBACK SWITCH MODE CHARGER RESOURCE DIAGRAM



Note 1: K1 and K2 are feedback gain circuits. Refer to **Appendix D: "Schematics and Board Layout"** for details.

Table 4 shows the resources used by the dsPIC DSC device for a flyback switch mode charger.

TABLE 4: RESOURCES REQUIRED FOR A DIGITAL FLYBACK SWITCH MODE CHARGER

Signal Name	Type of Signal	dsPIC® DSC Resources Used	Expected Signal Level
I_{BATM}	Analog	AN4	0V-1.67V
U_{BAT}	Analog	AN5	1.5V-2V
EFB	Digital output	RC7	—
I_{REF}	PWM output	PWM4L	—

DC/DC CONVERTER

Most UPS designs contain a transformer-type DC/DC converter. The transformer provides electrical isolation between the input and output of the converter. The transformer also provides the option to produce multiple voltage levels by changing the turns ratio, or provide multiple voltages by using multiple secondary windings.

Transformer-type DC/DC converters are divided into five basic topologies:

- Forward Converter
- Push-Pull Converter
- Half-Bridge Converter
- Full-Bridge Converter
- Flyback Converter

The Flyback topology operation differs slightly from other topologies in that energy is stored in magnetic material and then released. Other topologies always transfer energy directly from input to output. Another case in which topologies are distinguished from each other is transformer core utilization:

- Unidirectional core excitation – where only the positive part (quadrant 1) of the B-H loop is used (flyback and forward converters)
- Bidirectional core excitation – where both the positive (quadrant 1) and the negative (quadrant 3) parts of the B-H loop are utilized alternatively (push-pull, half-bridge, and full-bridge converters)

Selection of a topology depends on careful analysis of the design specifications, cost and size requirements of the converter.

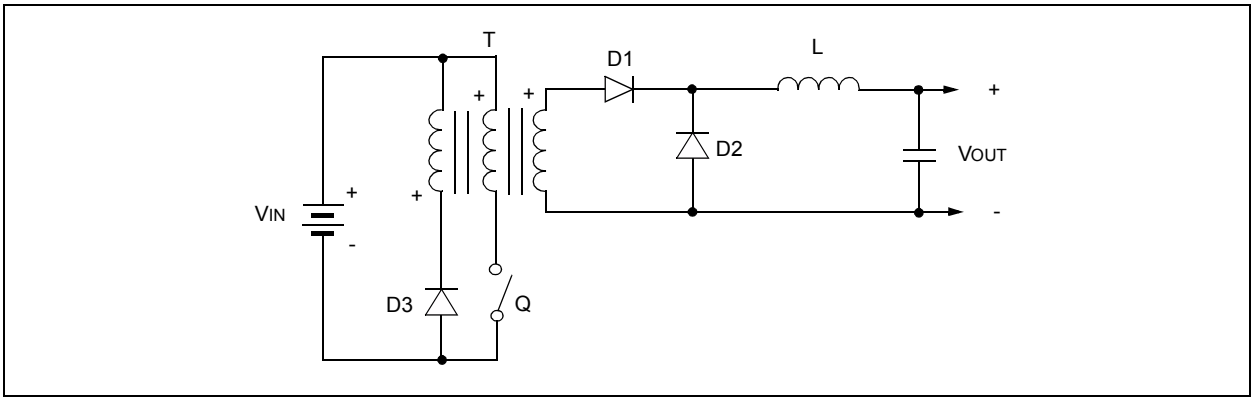
Operation of each of the above topologies is described in the following sections of this application note. Details of the topology selection and hardware design are provided in subsequent sections.

Forward Converter

A forward converter, which can be a step-up or step-down converter, is shown in Figure 8. When the transistor Q is ON, VIN appears across the primary, and then generates output voltage determined by Equation 1.

The diode D1 on the secondary ensures that only positive voltages are applied to the output circuit while D2 provides a circulating path for inductor current if the transformer voltage is zero or negative. A third winding is added to the transformer of a forward converter, also known as a “reset winding”. This winding ensures that the magnetization of the transformer core is reset to zero at the start of the switch conduction. This winding prevents saturation of the transformer.

FIGURE 8: FORWARD CONVERTER



EQUATION 1:

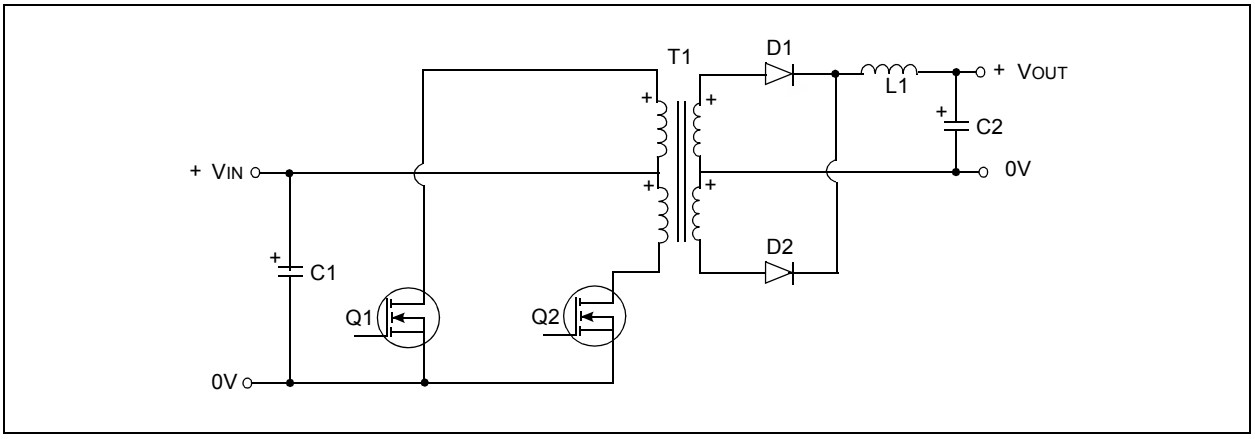
$$V_{out} = V_{in} \cdot \frac{N_2}{N_1} \cdot d$$

where d is the duty cycle of the transistor Q

Push-Pull Converter

A push-pull converter is shown in Figure 9. When Q1 switches ON, current flows through the upper half of the T1 transformer primary and the magnetic field in T1 expands. The expanding magnetic field in T1 induces a voltage across the T1 secondary; the polarity is such that D2 is forward-biased and D1 is reverse-biased. D2 conducts and charges the output capacitor C2 via L1. L1 and C2 form an LC filter network. When Q1 turns OFF, the magnetic field in T1 collapses and after a period of dead time (dependent on the duty cycle of the PWM drive signal), Q2 conducts, current flows through the lower half of T1's primary, and the magnetic field in T1 expands. At this point, the direction of the magnetic flux is opposite to that produced when Q1 conducted. The expanding magnetic field induces a voltage across the T1 secondary; the polarity is such that D1 is forward-biased and D2 is reverse-biased. D1 conducts and charges the output capacitor C2 via L1. After a period of dead time, Q1 conducts and the cycle repeats.

FIGURE 9: PUSH-PULL CONVERTER



There are two important considerations with the push-pull converter:

- Both transistors must not conduct together, as this would effectively short circuit the supply. This means that the conduction time of each transistor must not exceed half of the total period (d < 0.5) for one complete cycle, otherwise conduction will overlap.
- The magnetic behavior of the circuit must be uniform; otherwise, the transformer may saturate, and this would cause destruction of Q1 and Q2. This behavior requires that the individual conduction times of Q1 and Q2 must be exactly equal and the two halves of the center-tapped transformer primary must be magnetically identical.

These criteria must be satisfied by the control and drive circuit and the transformer. The output voltage equals that of Equation 2.

EQUATION 2:

$$V_{out} = 2 \cdot V_{in} \cdot \frac{N_2}{N_1} \cdot d$$

where:

d is the duty cycle of the transistors and $0 < d < 0.5$

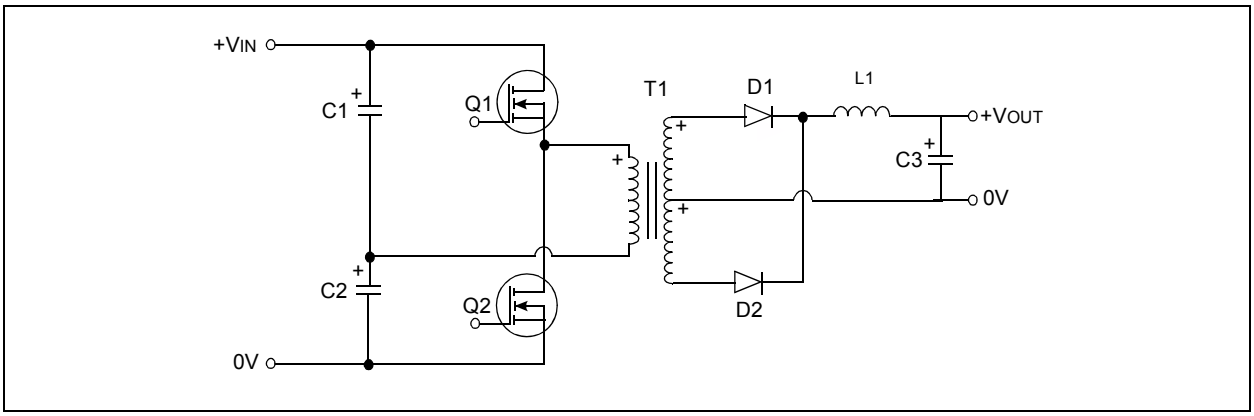
N2/N1 is the secondary-to-primary turns ratio of the transformer

Half-Bridge Converter

The half-bridge converter (see Figure 10) is similar to the push-pull converter, but a center-tapped primary is not required. The reversal of the magnetic field is achieved by reversing the direction of the primary winding current flow. In this case, two capacitors. C1 and C2, are required to form the DC input mid-point. Transistors Q1 and Q2 are turned ON alternately to avoid a supply short circuit, in which case the duty cycle, d, must be less than 0.5.

For the half-bridge converter, the output voltage VOUT equals that of Equation 3.

FIGURE 10: HALF-BRIDGE CONVERTER



EQUATION 3:

$$V_{out} = V_{in} \cdot \frac{N_2}{N_1} \cdot d$$

where:

d is the duty cycle of the transistors and $0 < d < 0.5$

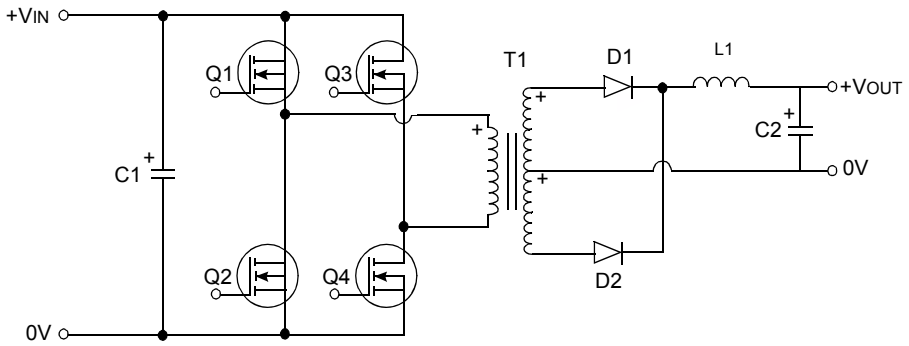
N2/N1 is the secondary-to-primary turns ratio of the transformer

Full-Bridge Converter

The full-bridge converter topology shown in Figure 11, is basically the same as the half-bridge converter, where four transistors are used.

Diagonal pairs of transistors (Q1-Q4 or Q2-Q3) conduct alternately, thus achieving current reversal in the transformer primary. Output voltage equals that of Equation 4.

FIGURE 11: FULL-BRIDGE CONVERTER



EQUATION 4:

$$V_{out} = 2 \cdot V_{in} \cdot \frac{N_2}{N_1} \cdot d$$

where:

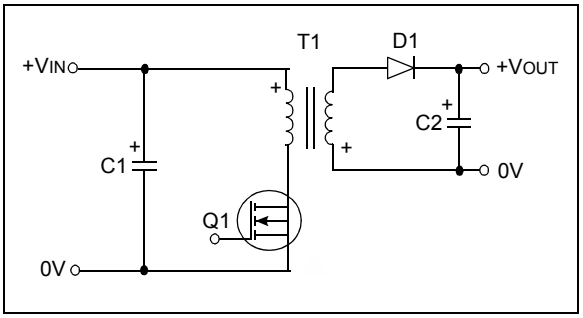
d is the duty cycle of the transistors and $0 < d < 0.5$

N2/N1 is the secondary-to-primary turns ratio of the transformer

Flyback Converter

Figure 12 shows a flyback converter circuit. When transistor Q1 is ON, due to the winding polarities, the diode D1 becomes reverse-biased. Therefore, transformer core flux increases linearly. When transistor Q1 is turned OFF, energy stored in the core causes the current to flow in the secondary winding through the diode D1 and flux decreases linearly. Output voltage is given by Equation 5.

FIGURE 12: FLYBACK CONVERTER



EQUATION 5:

$$V_{out} = V_{in} \cdot \frac{N_2}{N_1} \cdot \frac{d}{1-d}$$

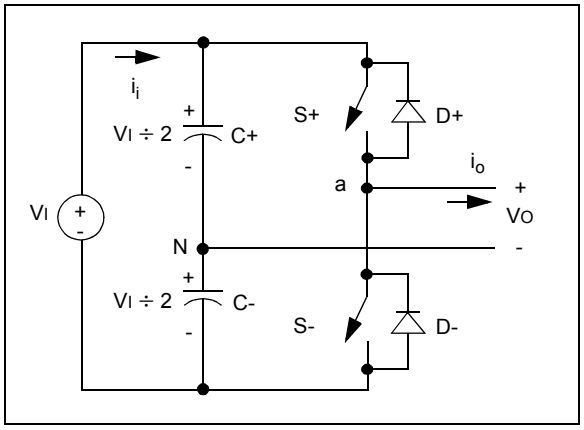
VOLTAGE SOURCE INVERTER (VSI)

A single-phase Voltage Source Inverter (VSI) can be defined as a half-bridge and a full-bridge topology. Both topologies are widely used in power supplies and single-phase UPS systems.

Half-Bridge VSI

Figure 13 shows the topology of a Half-Bridge VSI, where two large capacitors are required to provide a neutral point N, such that each capacitor maintains a constant voltage $v_i \div 2$. Because the current harmonics injected by the operation of the inverter are low-order harmonics, a set of large capacitors (C+ and C-) is required. The duty cycle of the switches is used to modulate the output voltage. The signals driving the switches must ensure some dead time to prevent shorting of the DC bus.

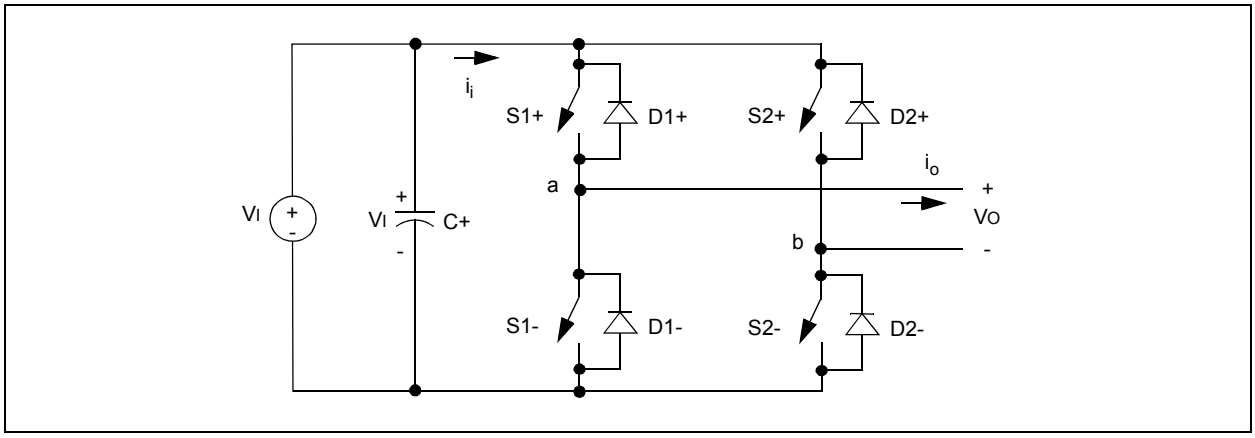
FIGURE 13: SINGLE-PHASE HALF-BRIDGE VSI



Full-Bridge VSI

Figure 14 shows the topology of a Full-Bridge VSI. This inverter is similar to the half-bridge inverter; however, a second leg provides the neutral point to the load. Both switches S1+ and S1- (or S2+ and S2-) cannot be on simultaneously because a short circuit across the DC link voltage source v_i would be produced. To avoid the short circuit across the DC bus and the undefined AC output voltage condition, the modulating technique should ensure that either the top or the bottom switch of each leg is ON at any instant. The AC output voltage can take values up to the DC link value v_i, which is twice the value obtained with half-bridge VSI topologies. Several modulating techniques have been developed that are applicable to full-bridge VSIs. Among them, the best known are bipolar and unipolar PWM techniques.

FIGURE 14: SINGLE-PHASE FULL-BRIDGE VSI



BATTERY CHARGER

When the AC mains voltage is present, the Offline UPS charges the batteries, and therefore, a battery charger circuit is implemented.

Most battery chargers can be divided into four basic design types, or topologies:

- Linear Chargers
- Switch Mode Chargers
- Ferroresonant Chargers
- SCR Chargers

Linear Chargers

Linear chargers consist of a power supply, which converts AC power to lower voltage DC power, and a linear regulating element, which limits the current that flows into the battery. The power supply typically consists of a transformer that steps down AC power from 220/110 VAC to a lower AC voltage closer to that of the battery, and a rectifier that smooths out the existing sinusoidal AC signal into a constant-voltage DC signal. The linear regulating element may be a passive component such as a resistor or an active component such as a transistor that is controlled by a reference signal. Figure 15 shows a simplified schematic of a linear charger with a linear power supply with a resistor as the current regulating element.

Switch Mode Chargers

In a switch mode charger, AC voltage is rectified, and then converted to a lower DC voltage through a DC/DC converter. This type of charger contains additional charge control circuitry to regulate current flow into the battery. The charge control regulates the way in which the power switch turns ON and OFF, and may be accomplished through a circuit, a specialized integrated chip, or some type of software control. A simplified schematic for a single piece switch mode charger is shown in Figure 16.

FIGURE 15: LINEAR CHARGER

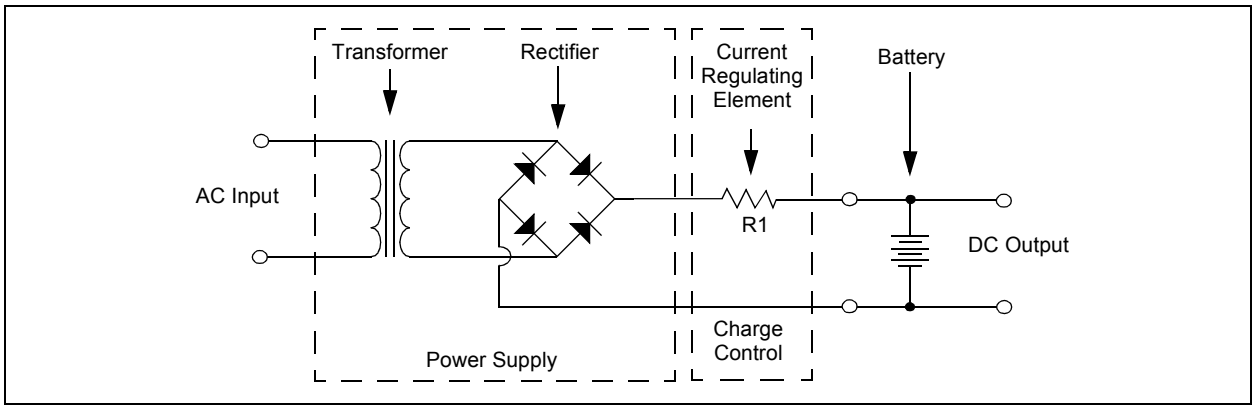
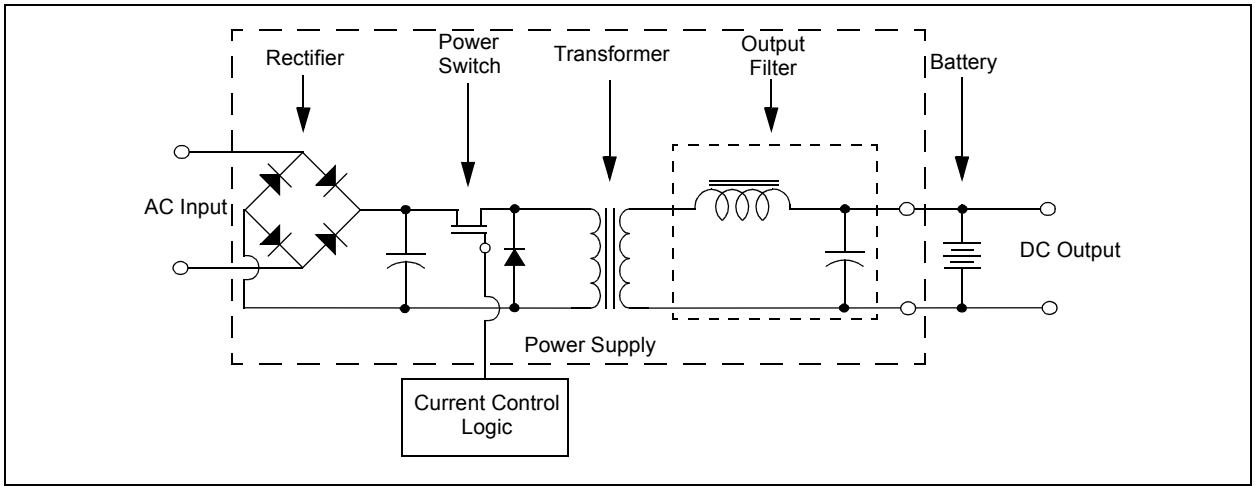


FIGURE 16: SWITCH MODE CHARGER



Ferroresonant Chargers

Ferroresonant chargers (sometimes called ferro chargers), operate by way of a special component called a ferroresonant transformer. The ferroresonant transformer reduces the AC voltage to a lower regulated voltage level while simultaneously controlling the charge current. A rectifier then converts the AC power to DC power suitable for the battery. Figure 17 shows a block diagram of a ferroresonant charger.

SCR Chargers

SCR chargers use a special component known as a Silicon-Controlled Rectifier (SCR) to control the current to the battery. The SCR is a controllable switch that can be turned ON and OFF multiple times per second. After a transformer reduces utility voltage to a value near that of the battery, the diodes rectify the current while the SCR enables the flow of charge current according to a control signal. A block diagram of an SCR charger is shown in Figure 18.

FIGURE 17: FERRORESONANT CHARGER

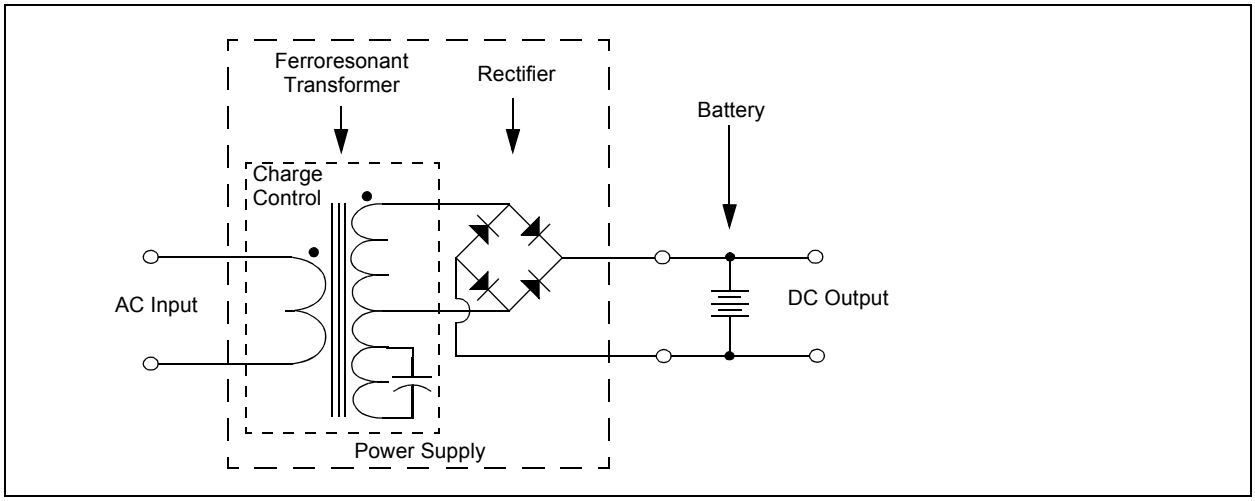
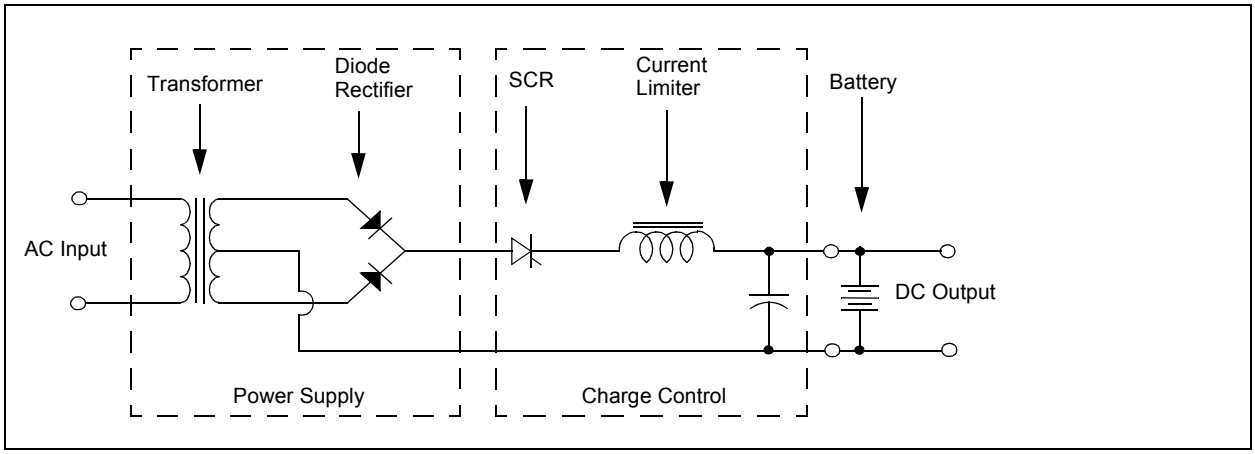


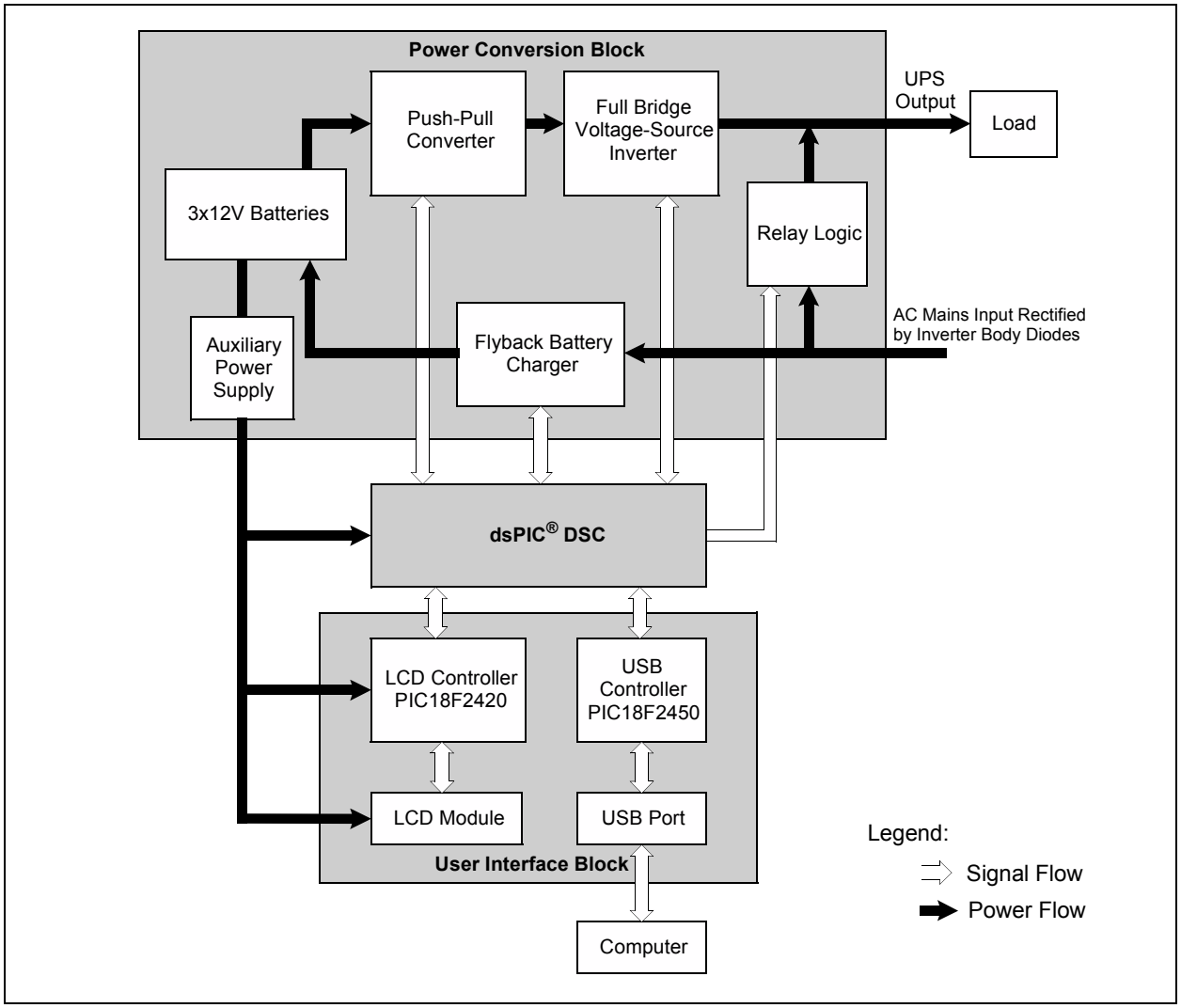
FIGURE 18: SCR CHARGER



SOFTWARE DESIGN

The Offline UPS Reference Design is controlled by a single dsPIC DSC device as shown in the system block diagram in Figure 19.

FIGURE 19: OFFLINE UPS BLOCK DIAGRAM



The dsPIC DSC device is the heart of the Offline UPS. It controls all critical operations of the system as well as the housekeeping operations. The functions of the dsPIC DSC can be broadly classified into the following categories:

- All power conversion algorithms
- UPS state machine for the different modes of operation
- Auxiliary tasks including true RMS calculations, soft start routines and user interface routines.

The dsPIC DSC device offers “intelligent power peripherals” specifically designed for power conversion applications. These intelligent power Peripherals include the High-Speed PWM, High-Speed 10-bit ADC, and High-Speed Analog Comparator modules.

These peripheral modules include features that ease the control of any switch-mode power supply with high resolution PWM, flexible ADC triggering, and comparator fault handling.

In addition to the intelligent power peripherals, the dsPIC DSC also provides built-in peripherals for digital communications including I^2C™, SPI and UART that can be used for power management and housekeeping functions.

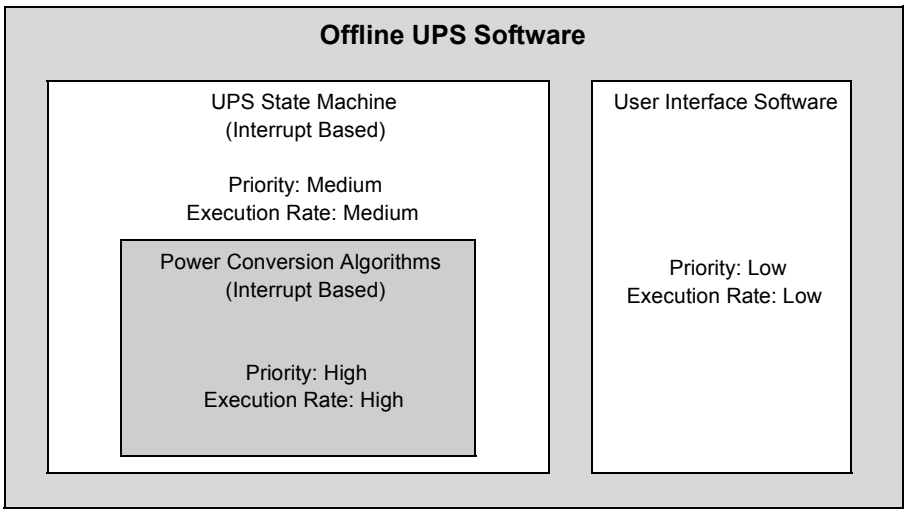
Note:	For device details, refer to the dsPIC33F “GS” series device data sheets. For more information on the peripherals, refer to the corresponding SMPS sections in the *“dsPIC33F Family Reference Manual”*.

A high-level diagram of the Offline UPS software structure is shown in Figure 20. As shown in this figure, the software is broadly partitioned into two parts:

- UPS State Machine (includes power conversion routines)
- User Interface Software

These partitions are described in more detail in subsequent sections of this document.

FIGURE 20: OFFLINE UPS SOFTWARE: HIGH-LEVEL PARTITIONS



UPS State Machine

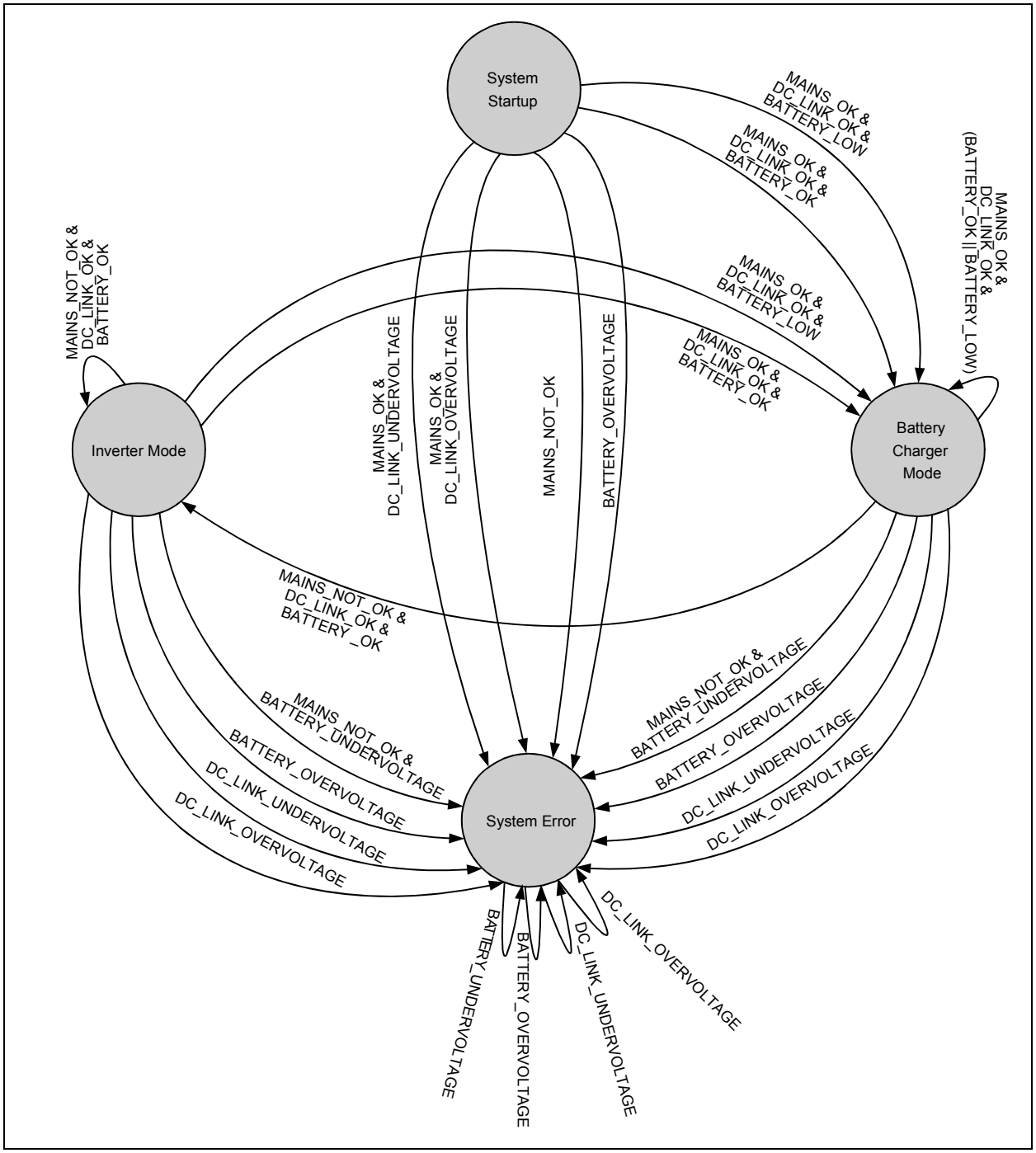
The Offline UPS software implements a state machine to determine the mode of operation for the system. The state machine is executed once every 100 µs inside a timer Interrupt Service Routine (ISR). The state machine configures the on-chip peripherals to execute the correct power conversion algorithms.

During normal operation of the offline UPS, the state machine configures the system peripherals to execute the correct power conversion algorithms as determined by the system state.

When a power failure occurs, the UPS state machine initiates a switchover sequence from Battery Charger mode to Inverter mode. When the AC mains is detected again, the state machine executes the switchover from Inverter mode to Battery Charger mode. These switchover functions must be executed in as little time as possible to ensure uninterrupted power to the load.

The Battery Charger mode and Inverter mode are the two normal operating modes of the Offline UPS. There are two other modes of operation, namely System Startup and System Error. Each mode of operation for the Offline UPS is described in the following sections. Figure 21 shows the Offline UPS state diagram.

FIGURE 21: OFFLINE UPS STATE DIAGRAM



System Startup

When the Offline UPS is turned ON, the state of the system is unknown. Therefore, the state machine first monitors all system variables and determines the starting state of the UPS.

During this time, the state machine also monitors for fault conditions and ensures that all system variables are within specification so that the UPS can switch to normal operation.

BATTERY CHARGER MODE

If the AC mains voltage is detected, the Inverter mode is disabled (if running) and the Offline UPS switches to the Battery Charger mode. The dsPIC DSC device provides the reference current level with a variable duty cycle PWM signal.

The battery voltage is measured to ascertain the state of the battery. Depending on the battery state, the value of the charging current is modified so as to achieve the fastest charging time and also to prolong the life of the batteries.

The battery charging profile has been configured for sealed lead-acid (SLA) batteries, and is summarized in Figure 22.

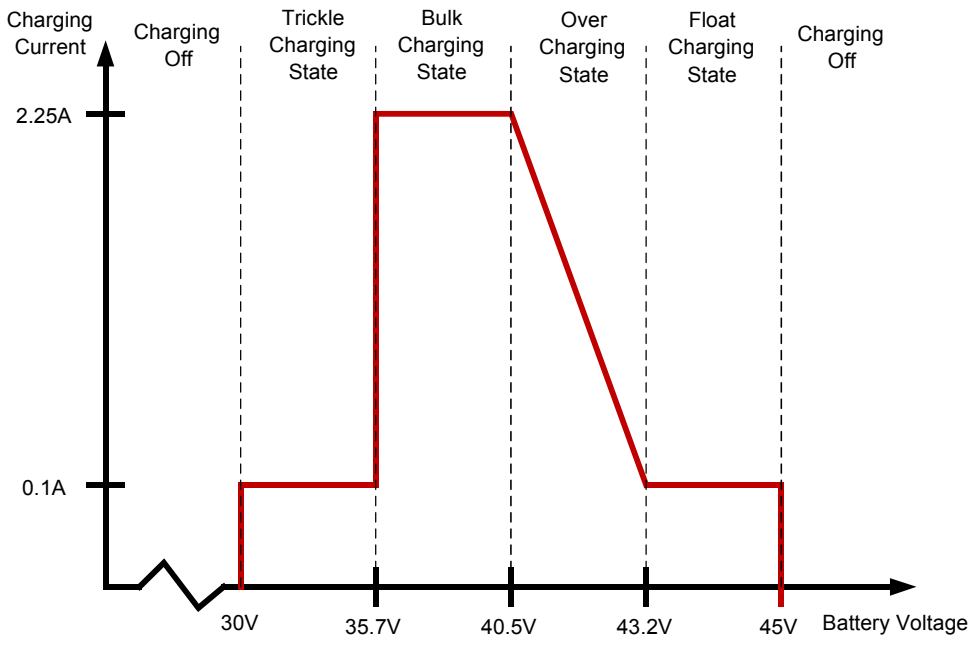
The battery charger control is implemented partly in hardware and partly in software. A flyback converter IC is used to produce a constant current source from the rectified AC mains voltage. The dsPIC DSC device provides the reference signal for the output current of the flyback converter.

This current reference signal is generated by filtering the PWM output from the dsPIC DSC. The charging current is controlled by modifying the duty cycle of the current reference PWM signal.

When the Battery Charger mode is started, the dsPIC DSC device sets up the minimum charging current. Then, the battery voltage and battery current are measured using the high-speed 10-bit ADC module. The measured battery voltage determines the charging state, and the code specifies the correct charging current from the battery charging profile shown in Figure 22.

All system variables are monitored by the state machine to initiate a switchover sequence if required. When an AC mains power failure is detected, the state machine switches the UPS operation to the Inverter mode. If a fault is detected, the system state is changed to System Error.

FIGURE 22: OFFLINE UPS BATTERY CHARGING PROFILE



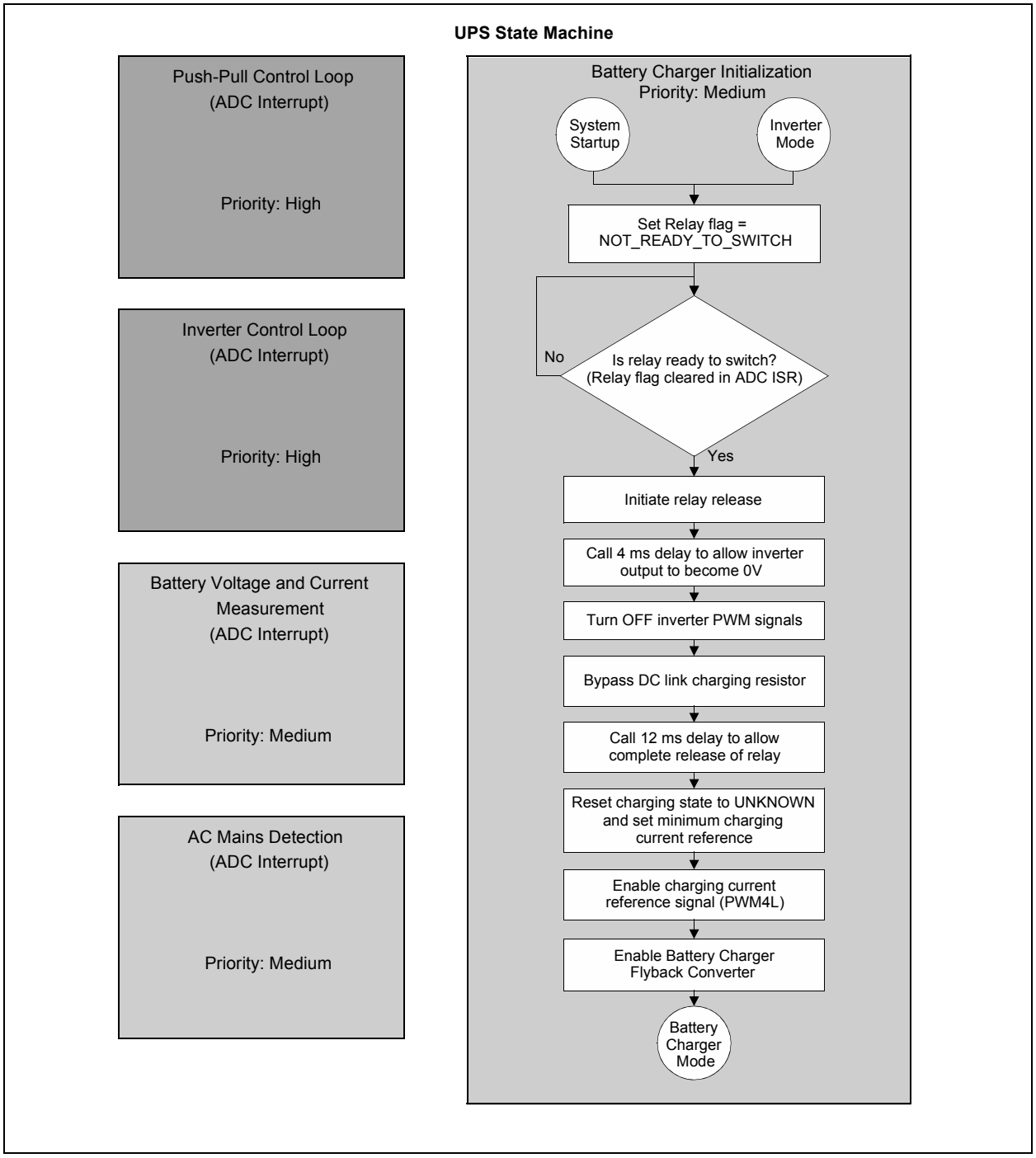
Note: Not drawn to scale

BATTERY CHARGER INITIALIZATION ROUTINE

When the offline UPS switches to the Battery Charger mode, the code must ensure that the previous mode is turned OFF. To reduce stress on the hardware components, the full-bridge inverter is turned OFF when the output reaches 0V. The flowchart for the Battery Charger mode is shown in Figure 23.

After the inverter is turned OFF, the output relay is released so that the AC mains is connected to the UPS output. The output relay must be released in the shortest possible duration so that there is no interruption of power at the UPS output. Typically, relay switching times are the limiting factor for the switchover duration.

FIGURE 23: BATTERY CHARGER INITIALIZATION FLOWCHART



The dsPIC DSC device implements a predictive technique to achieve the fastest switchover time possible. This is done by predicting the relay switching time and initiating the relay release even before the inverter output has turned OFF. The switchover operation from the inverter to the AC mains is described in subsequent sections of this application note.

BATTERY CHARGER CONTROL SCHEME

The battery charger control loop is implemented in the state machine.

If the measured charging current is less than the reference, the duty cycle is incremented by a fixed step. Conversely, if the charging current exceeds the reference, the duty cycle is reduced by the same fixed step. This process continues until the current error reduces to a negligible value.

The battery charging current control scheme is illustrated in Figure 24. The battery charger control routine is called inside the state machine under the Battery Charger mode. The battery charging control loop is therefore executed at the same rate (once every 100 µs) and also at the same priority level as the state machine. The battery current and voltage measurement is triggered using the PWM trigger feature on the dsPIC DSC device.

The measured data is scaled and stored as a variable in data memory asynchronous to the control loop execution. When the control loop is called, the data is simply read from the data memory and used for control loop calculations. The flowchart for the battery charger control loop is shown in Figure 25.

FIGURE 24: BATTERY CHARGER CONTROL SCHEME

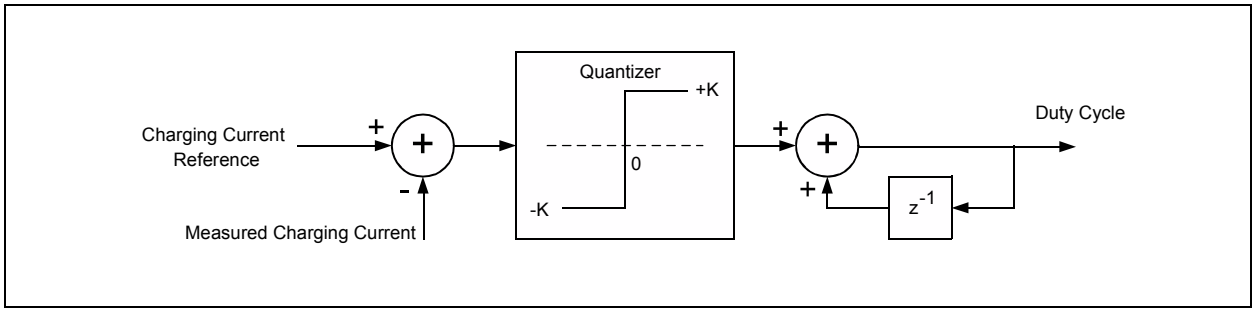
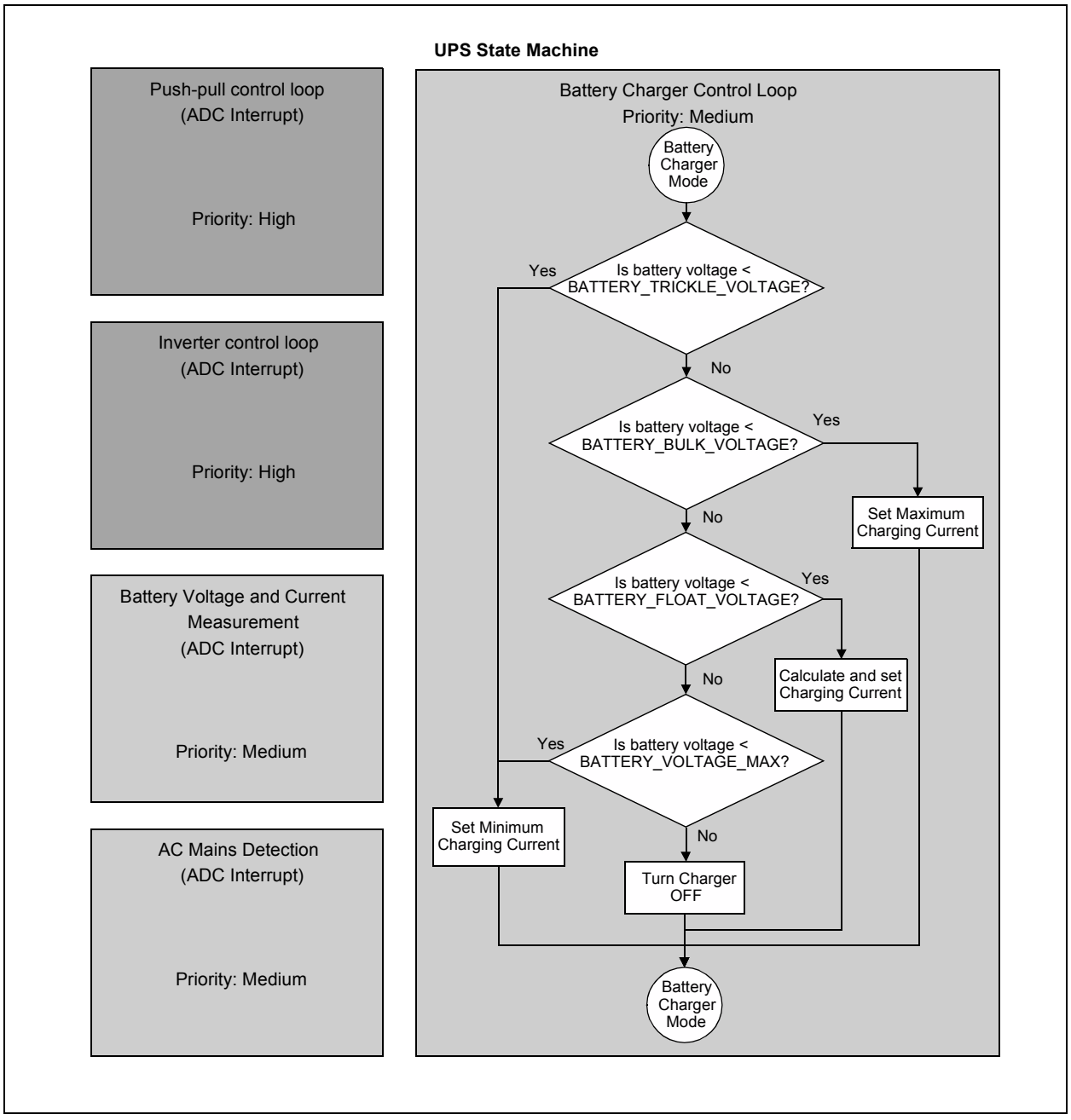
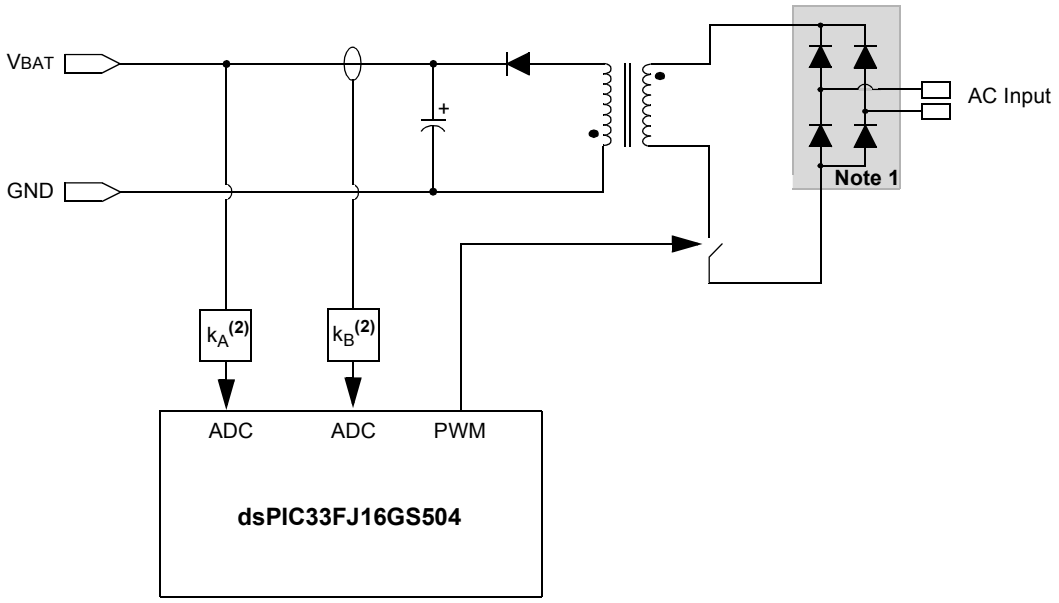


FIGURE 25: BATTERY CHARGER MODE FLOWCHART



BATTERY CHARGER RESOURCE ALLOCATION

FIGURE 26: dsPIC® DSC DEVICE RESOURCE ALLOCATION FOR BATTERY CHARGER



Note 1: The AC mains input is rectified by the body diodes of the IGBTs to provide a DC voltage to the battery charger.

2: KA and KB are feedback gain circuits. Refer to **Appendix D: "Schematics and Board Layout"** for details.

The dsPIC DSC device resources used for the battery charger are summarized in Table 5.

TABLE 5: dsPIC® DSC DEVICE RESOURCE ALLOCATION FOR BATTERY CHARGER

Signal Name	Description	Type of Signal	dsPIC® DSC Resource Used	Execution Rate/Frequency
IREF	Charging current reference	PWM output	PWM4L (remapped to pin 35)	25 kHz
IB	Charging current feedback	Analog Input	AN4	6.25 kHz
UB	Battery voltage feedback	Analog Input	AN5	6.25 kHz
EFB	Flyback converter enable	Digital Output	RC7	Activated only when the UPS switches to Battery Charger mode

Inverter Mode

If the AC mains voltage is not detected, the battery charger is disabled and the Offline UPS switches to the Inverter mode. During Inverter mode, the system is running on battery power and produces a clean sinusoidal voltage at the UPS output so that critical electronics can continue operation without interruption. The sinusoidal output waveform is generated using a sine lookup table in the data memory. This lookup table serves as the sinusoidal reference voltage for the inverter control loop.

When starting Inverter mode, the push-pull converter is ramped up to the rated DC Link voltage using a soft-start routine. The soft-start routine reduces stress on system components and also prevents voltage and current surges from the AC mains or the battery.

During normal operation of Inverter mode, the push-pull converter and the full-bridge inverter are controlled by interrupt-based power conversion algorithms, or control loops. The control loops are executed at a fast rate to achieve the best performance. The Inverter mode power conversion algorithms are the most critical routines for the dsPIC DSC device; therefore, these routines are assigned the highest user-priority level.

The state machine, which is also interrupt-based, has a lower priority than the control loops. As a result, the execution of the state machine and user interface code may be interrupted numerous times by the high-priority control loops.

This operation is possible because the dsPIC DSC device allows for nesting of interrupts. The interrupt nesting feature enables the control loops to interrupt the execution of the state machine. The state machine execution is relatively slower than the control loops. The dsPIC DSC device allows for seamless transition between the power conversion routines and the UPS state machine, with the use of multiple interrupts of differing priorities and execution rates.

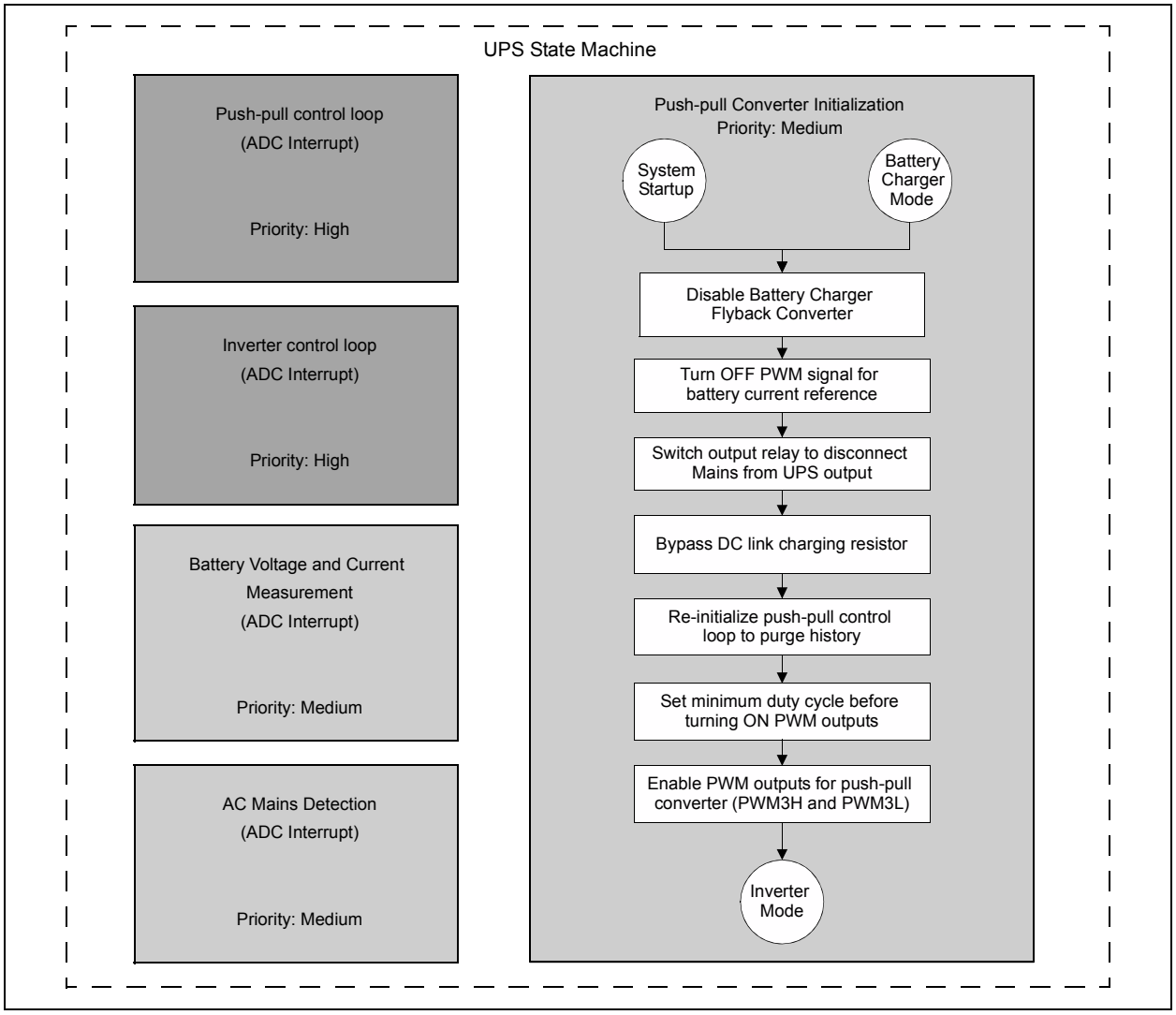
When operating in the Inverter mode, all system variables are monitored by the state machine. As soon as the AC mains voltage is detected, the switchover sequence is engaged and the system state is changed to Battery Charger mode. If any system variable is in error, the system state is changed to System Error.

PUSH-PULL CONVERTER INITIALIZATION

When the system switches to Inverter mode, any previous modes of operation must first be disabled. Therefore, the battery charger is first disabled by turning OFF the flyback converter and also by disabling the PWM output for battery current reference. The output relay is engaged to disconnect the AC mains input from the UPS output, while the inverter series resistor is bypassed by switching ON the bypass relay. Then, the push-pull converter control loop is reinitialized and all control history is purged.

The AC mains input has a wide operating voltage range; therefore, the value of the DC link voltage is unpredictable when a mains failure occurs. As a result, before turning ON the push-pull converter, the most recently measured DC Link voltage is used as the initial reference voltage for the push-pull converter. The soft-start routine enables the DC Link voltage to be ramped up at a controlled rate and thus prevents unnecessary stress on the circuit components due to current spikes.

FIGURE 27: PUSH-PULL CONVERTER INITIALIZATION FLOWCHART



SOFT-START ROUTINE

The soft-start routine is called right after enabling the push-pull converter. The soft-start routine increments the reference voltage for the push-pull converter in software in fixed steps until the reference reaches the rated DC Link voltage. At this point, the inverter is enabled by calling the inverter re-initialization routine to produce a sinusoidal voltage at the UPS output.

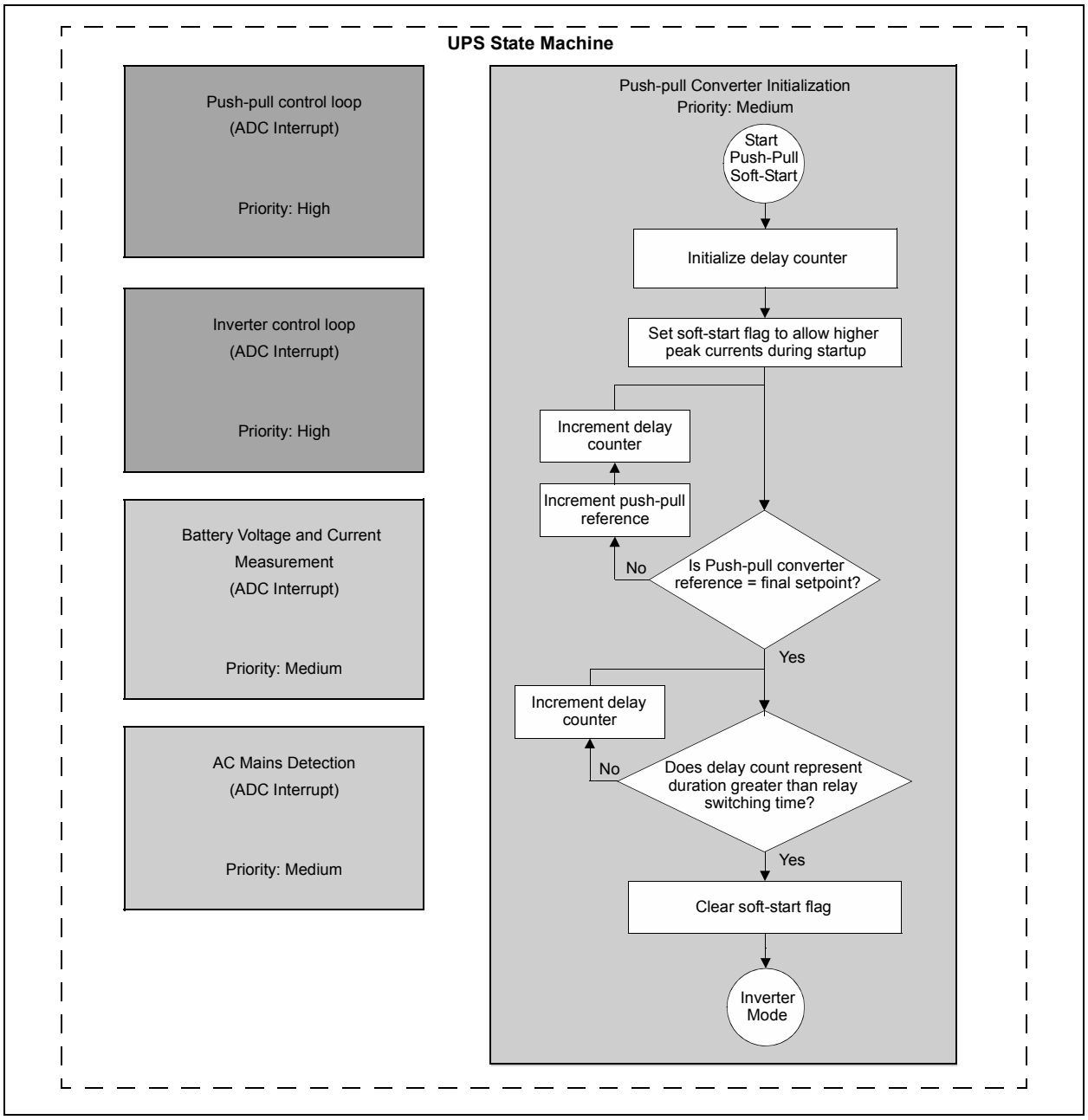
The ramp rate for the DC Link voltage is fixed and the starting voltage for the soft-start routine is variable, making the soft-start duration also variable.

The variable duration of the soft-start routine may cause uncertainty in the mains-to-inverter switchover time. The ramp rate for the soft-start routine is configured to be completed in the time required for the output relay to turn ON. This ensures that the switchover time is within the design specification of 10 ms.

However, the other situation must also be considered where the soft-start is completed in less time. In this case, the inverter output will turn ON before the relay is given enough time to switch, thereby causing the inverter output to be turned ON at the UPS output midway through the sine wave cycle. If the relay is turned ON after the completion of the soft-start, the switchover timing would be too slow.

The dsPIC DSC avoids both of these problems by initializing a delay counter at the beginning of the soft-start routine. As the soft-start routine is ramping up the DC Link voltage, the counter is incremented to reflect the soft-start duration in milliseconds. If the soft-start is completed before the minimum required time for the relay turn-on, the code continues to wait until the minimum required switching time has elapsed. Once the required relay switching time elapses, the full-bridge inverter is enabled. This technique ensures that uninterrupted power is available at the UPS output at all times.

FIGURE 28: SOFT-START ROUTINE FLOWCHART

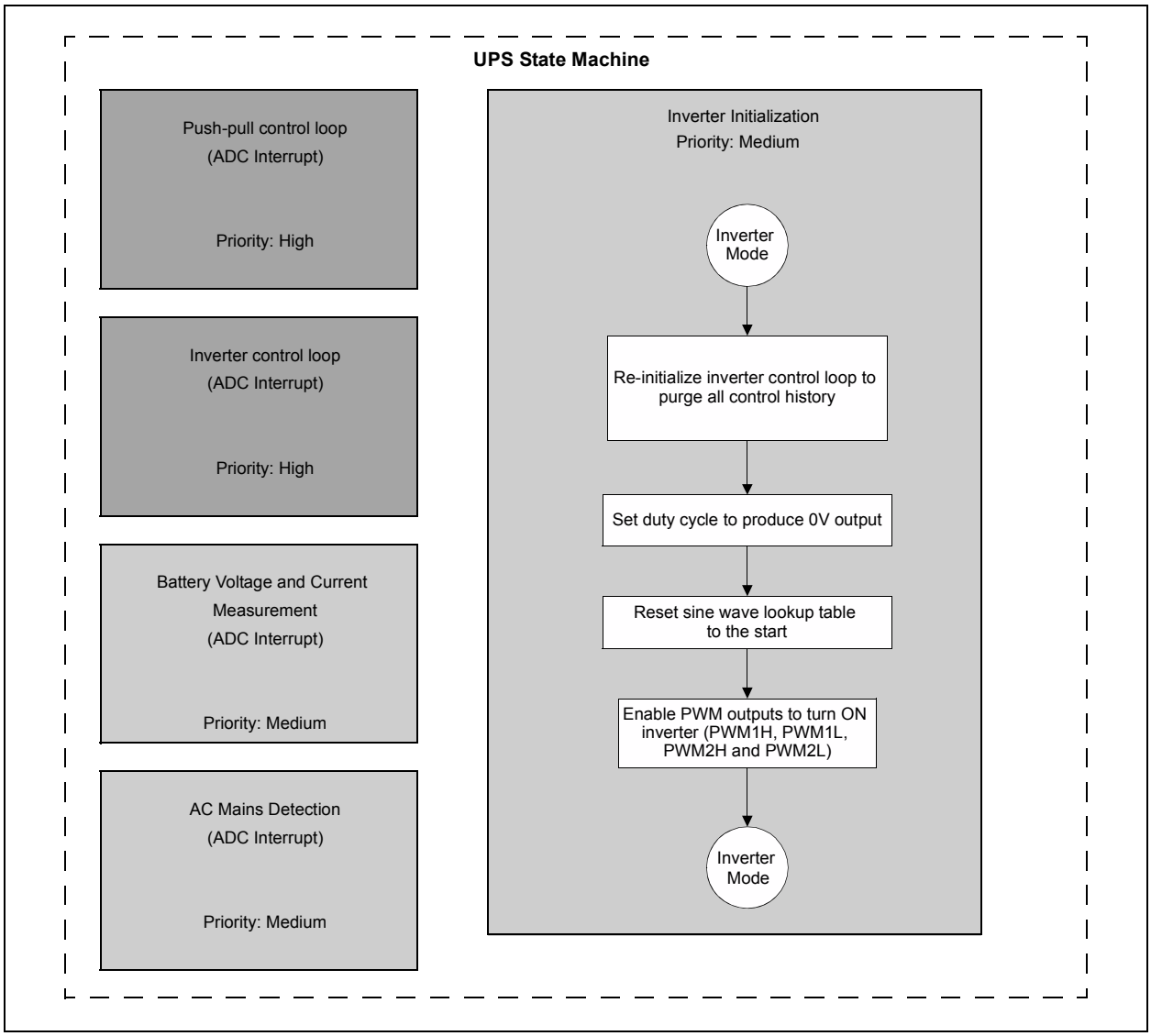


FULL BRIDGE INVERTER INITIALIZATION

The push-pull soft-start routine ensures that the DC link voltage is at the rated value and the output relay has completed the switching event. After the soft-start routine concludes, the full-bridge inverter must be enabled to produce a sinusoidal voltage at the UPS output.

The inverter control loop is reinitialized to purge all control history. The duty cycle is then configured to produce 0V output and the sine wave lookup table pointer is also reset to the start. At this point, the PWM outputs are enabled to produce the sinusoidal output voltage.

FIGURE 29: INVERTER INITIALIZATION FLOWCHART



PUSH-PULL CONTROL LOOP

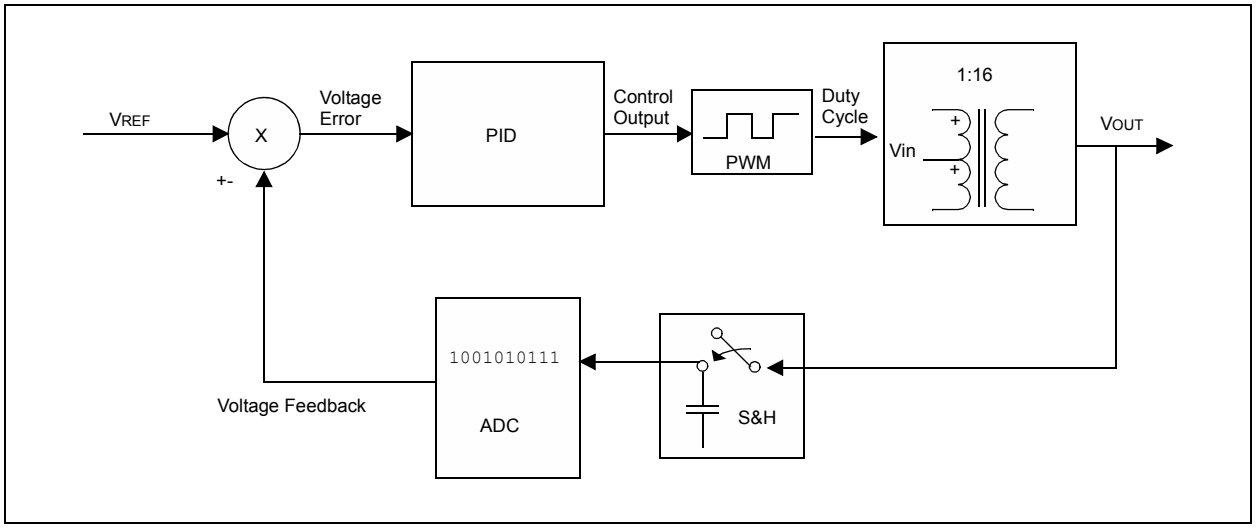
The push-pull converter is controlled with a voltage mode control scheme. The PWM module in the dsPIC DSC device is configured for Push-Pull mode with an independent time-base. The DC Link voltage is measured by the ADC and converted to a digital value. This value is subtracted from the voltage reference in software to obtain the voltage error.

The voltage error is then fed into a control algorithm that produces a duty cycle value based on the voltage error, previous error, and control history. The output of the control algorithm is also clamped to minimum and maximum duty cycle values for hardware protection.

The voltage mode control algorithm must be executed at a fast rate in order to achieve the best transient response. Therefore, the control algorithm is executed in the ADC interrupt service routine, which is also assigned the highest priority in the UPS code.

A block diagram of the push-pull converter control scheme is shown in Figure 30.

FIGURE 30: PUSH-PULL CONVERTER CONTROL SCHEME



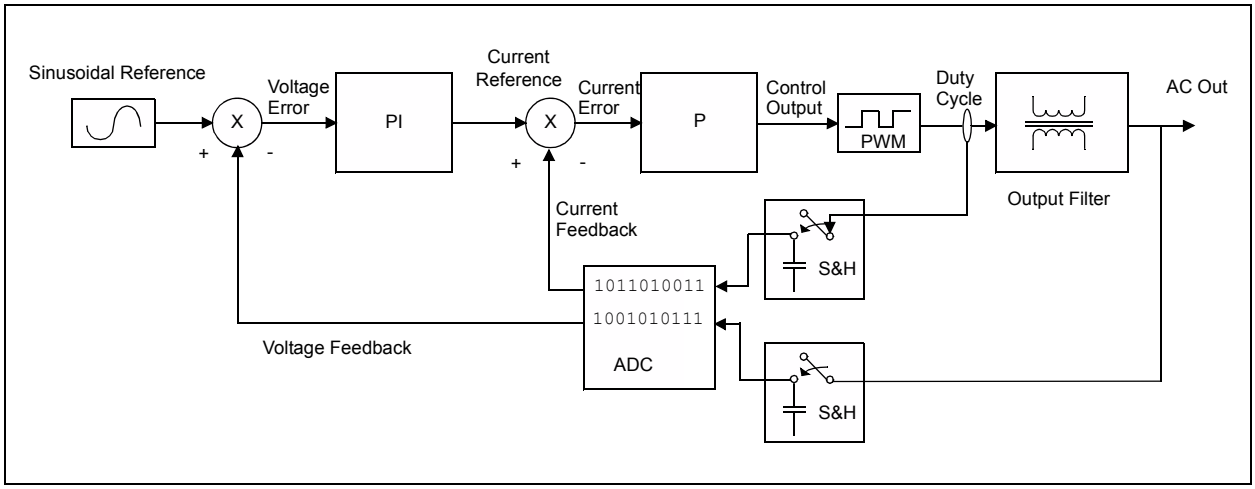
INVERTER CONTROL LOOP

The inverter output is generated by varying the voltage reference using a sinusoidal lookup table. The measured output voltage is subtracted from the present reference value and the voltage error is obtained. The voltage error is fed into the voltage error compensation algorithm within the ADC interrupt service routine. The output of the voltage error compensator produces the current reference value. The measured output current is subtracted from the current reference to obtain the current error. The current error is used as the input to the current error compensation algorithm to produce the command signal for the PWM module.

In the Offline UPS, a 3-level control is implemented for the full-bridge inverter. So the PWM module in the dsPIC DSC device is set up with a fixed duty cycle for zero output voltage. Each leg of the full-bridge inverter is operated in complementary Center-Aligned mode with dead time. The result of the control loop is added to the nominal duty cycle for one leg of the full-bridge inverter and subtracted from the nominal duty cycle for the second leg.

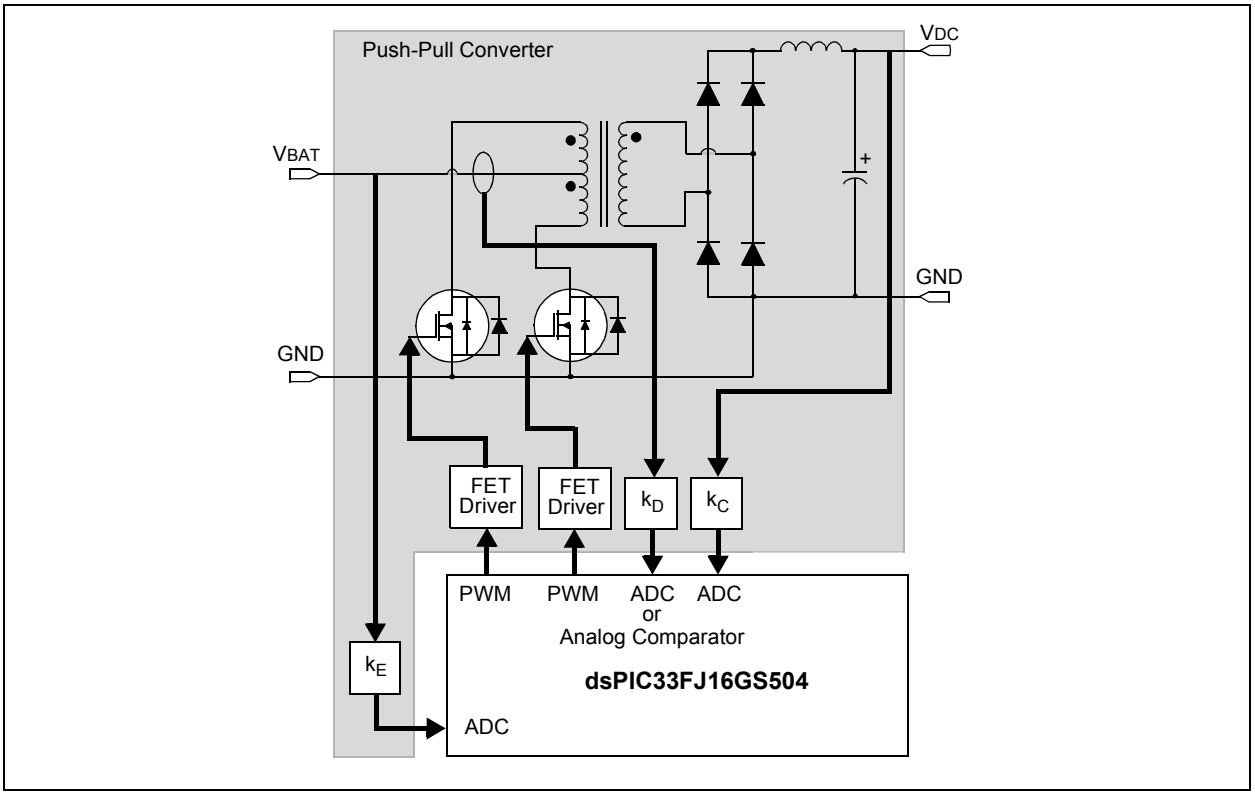
A block diagram of the full-bridge inverter control system is shown in Figure 31.

FIGURE 31: FULL-BRIDGE INVERTER CONTROL SCHEME



PUSH-PULL CONVERTER HARDWARE AND
SOFTWARE RESOURCE ALLOCATION

FIGURE 32: dsPIC® DSC DEVICE RESOURCE ALLOCATION FOR PUSH-PULL CONVERTER

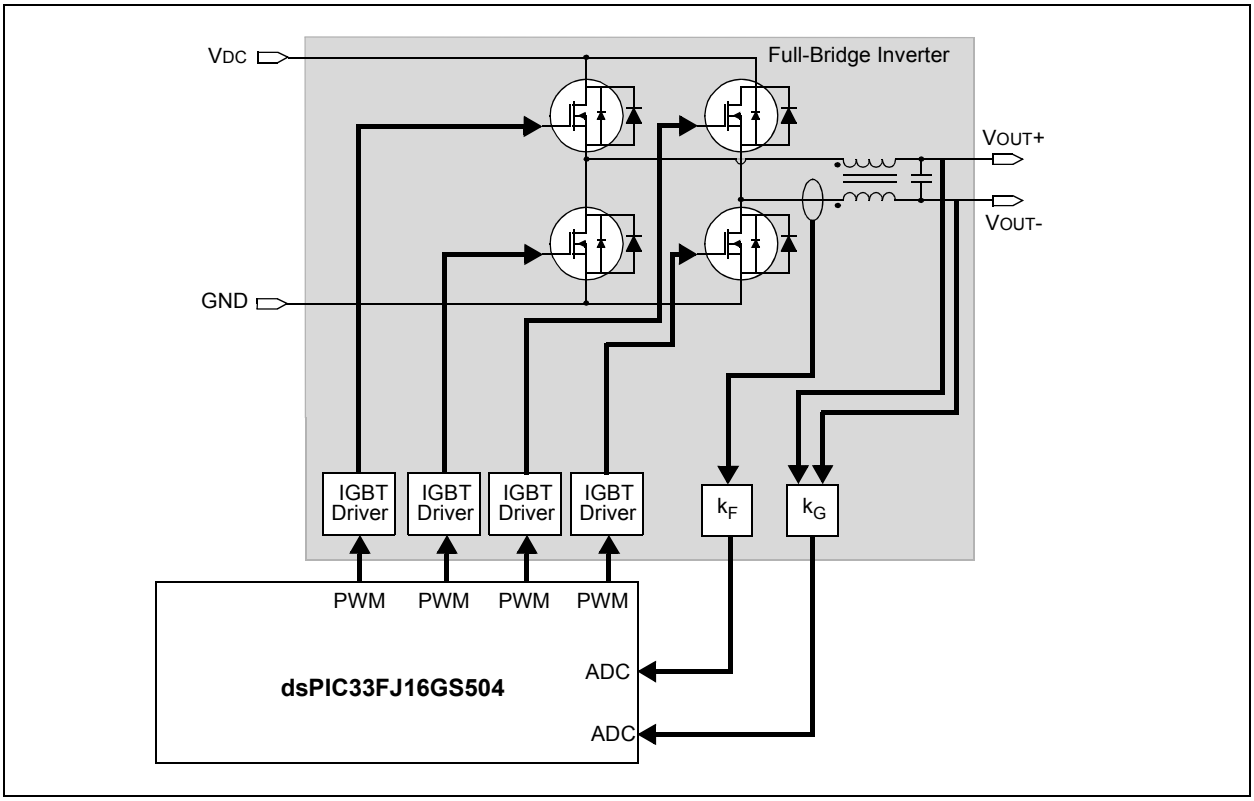


The dsPIC DSC resources used for the push-pull converter are summarized in Table 6.

TABLE 6: dsPIC® DSC DEVICE RESOURCE ALLOCATION FOR PUSH-PULL CONVERTER

Signal Name	Description	Type of Signal	dsPIC® DSC Resource Used	Sample Rate/ Frequency
S1	Push-Pull Drive Signal	PWM Output	PWM3L	100 kHz
S2	Push-Pull Drive Signal	PWM Output	PWM3H	100 kHz
IP	Push-Pull Primary Current Feedback	Analog Input	AN2	25 kHz
UDCM	DC Link Voltage Feedback	Analog Input	AN3	25 kHz

FIGURE 33: dsPIC DSC® RESOURCE ALLOCATION FOR FULL-BRIDGE INVERTER



The dsPIC DSC device resources used for the full-bridge converter are summarized in Table 7.

TABLE 7: dsPIC® DSC DEVICE RESOURCE ALLOCATION FOR FULL-BRIDGE CONVERTER

Signal Name	Description	Type of Signal	dsPIC® DSC Resource Used	Sample Rate/ Frequency
S3	Inverter Drive Signal	PWM Output	PWM1L	50 kHz
S4	Inverter Drive Signal	PWM Output	PWM1H	50 kHz
S5	Inverter Drive Signal	PWM Output	PWM2L	50 kHz
S6	Inverter Drive Signal	PWM Output	PWM2H	50 kHz
I	Inverter Output Current Feedback	Analog Input	AN0	25 kHz
ACO	Inverter Output Voltage Feedback	Analog Input	AN1	25 kHz
ACI	AC Mains Voltage Feedback	Analog Input	AN11	25 kHz
A1	Resistor Bypass Relay Drive Signal	Digital Output	RC10	Activated only at startup to charge the DC Link voltage above the minimum value.
A2	Output Relay Drive Signal	Digital Output	RC0	Activated only when the UPS switches to Inverter mode.

Inverter-to-Mains Switchover Routine

When a power failure occurs, the Offline UPS switches to the Inverter mode and operates in this mode until the mains is detected again. The system should switch from one mode to the other in the shortest possible duration in order to provide uninterrupted power to the load.

Before switching to the Battery Charger mode, the software must reliably ensure that the mains voltage detected is within the specified levels. The software must also ensure that the mains waveform is clean and has little or no distortion.

The mains detection routine is divided into the following steps:

1. **Mains High Voltage Detection:** In the Inverter mode, the UPS software first checks for the presence of high voltage on the mains. If a high voltage is detected consecutively for 5 ms, the mains detection routine proceeds to the next step.
2. **Zero-Crossing Detection:** After a high voltage has been detected, the software keeps polling the mains voltage for a zero-crossing detection. A valid zero-crossing is only detected if the previous voltage is negative and the present voltage is positive, and the difference between the previous and present measurement is above a minimum value. This ensures that spurious zero-crossings are not detected due to noise.
3. **Mains Data Collection:** Once the zero-crossing has been detected, the UPS software enters the mains data collection step. In this step, every sample of the measured mains voltage is stored in an array. Each sample of the collected data is averaged over four sine wave cycles to ensure an accurate reference. This array is later used as the mains reference to detect a mains failure.
4. **Mains Synchronization:** After collecting the mains voltage data, the mains detection routine now compares the measured voltage with the mains reference data. If the error is within ±20V consecutively for 8 ms, the software concludes that the mains is present and indicates the new state of the AC mains to the state machine.

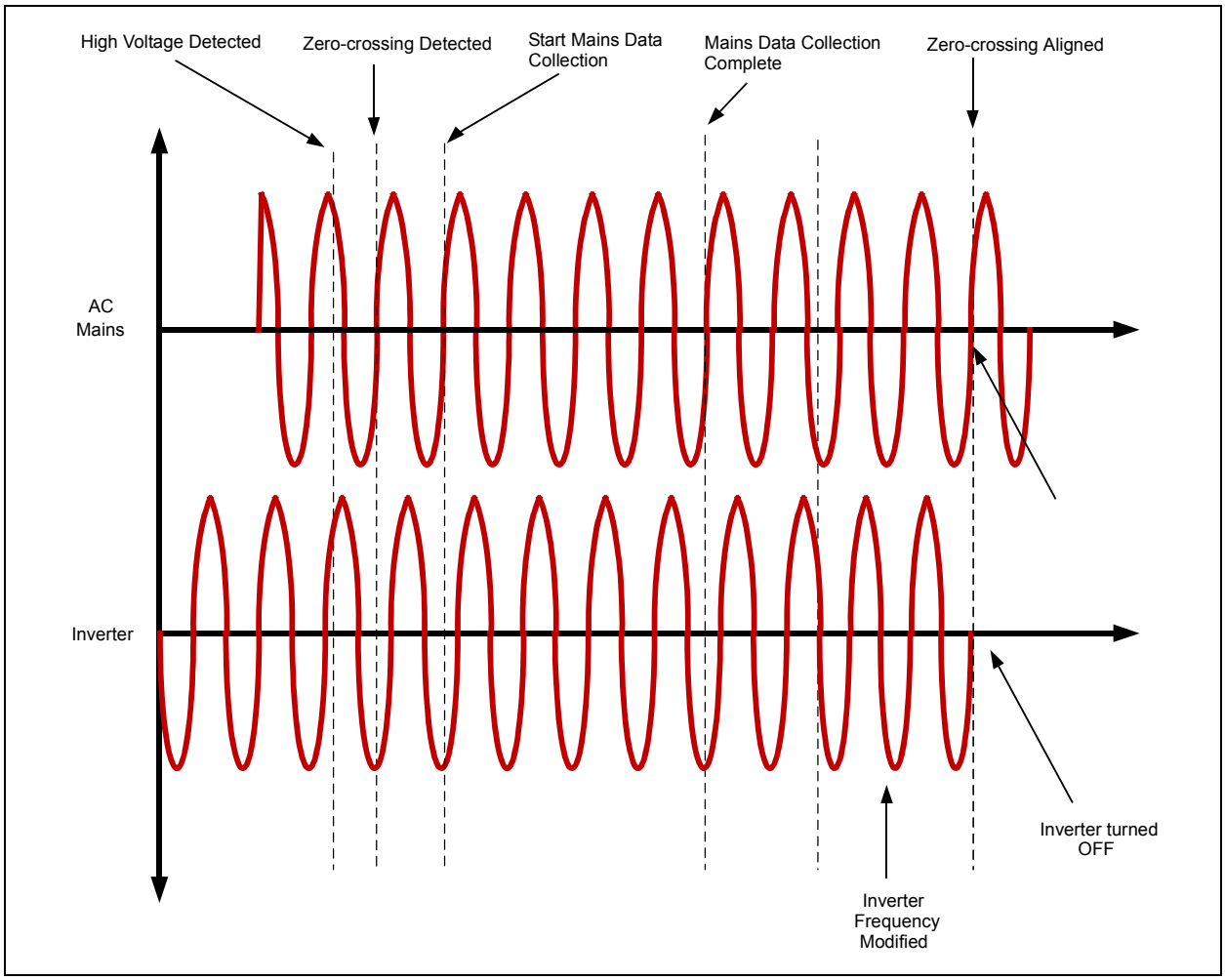
The state machine then begins the process of switching from Inverter mode to Battery Charger mode. The switchover is engaged at the zero-crossing of both the inverter and mains. This provides the smoothest transition from one mode to the other and occurs instantaneously.

It is possible that the inverter and mains are out of phase when AC mains is available again. As the frequencies of the AC mains and the inverter are nearly equal, the zero crossings of the two waveforms may never align. Therefore, the UPS software first checks whether the frequencies are very close. If there is a significant difference in frequencies, the two waveforms will eventually align at the zero crossings, which is when the UPS will engage the switchover.

If the two signals are operating at nearly the same frequency, the inverter frequency is modified slightly by discarding some of the samples from the lookup table. As a result, the zero crossings of the two signals are forced to align after a few sine wave cycles. This allows the UPS state machine to switch from the Inverter mode to the Battery Charger mode with almost zero latency. The inverter-to-mains switchover sequence is described graphically in Figure 34.

It is also important to note that the alignment of the zero crossings must be predicted using information for the relay switching time. The relay is switched a few milliseconds before the actual zero-crossing so that the relay switching delay is accounted for.

FIGURE 34: INVERTER-TO-MAINS SWITCHOVER SEQUENCE



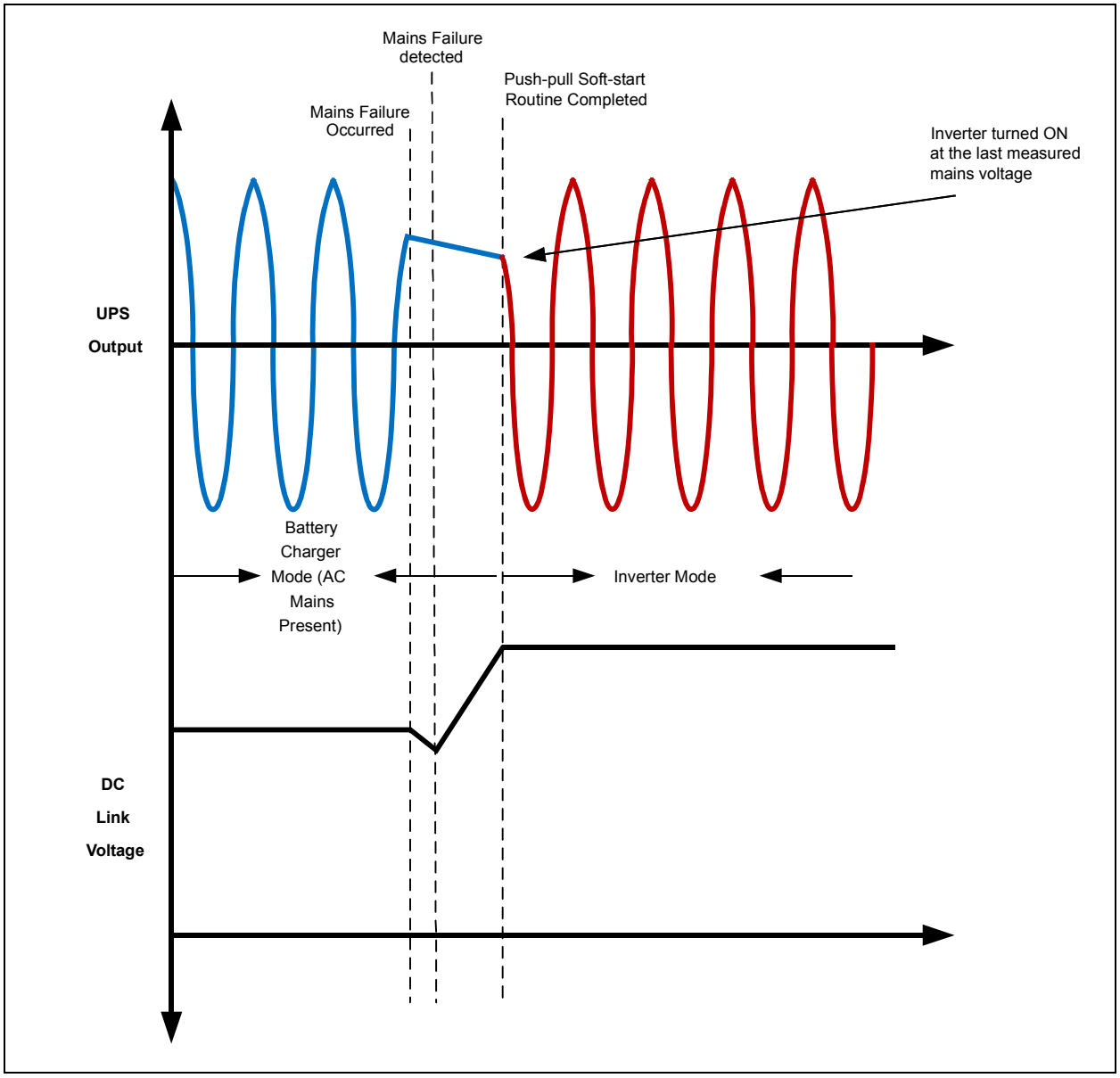
Mains-to-Inverter Switchover Routine

When mains is present, the UPS software keeps comparing the measured mains voltage with the corresponding data in the mains reference array. The quadrant information is also saved in a variable. On every sample, the error between the expected voltage and the actual voltage is calculated.

If the error is detected to be larger than ±20V, a count is incremented. If the error is detected to be outside the limit consecutively for about 1 ms, then the Offline UPS detects that a mains failure has occurred. The system state is changed to Inverter mode and the relay is switched immediately to disconnect the mains from the UPS output. The push-pull converter is then enabled and the soft-start routine is executed. After the soft-start routine is complete, the mains voltage is measured again.

Using a binary search algorithm, the appropriate sample number from the sine lookup table is selected, which is in the appropriate quadrant and has a value closest to the mains voltage. The inverter is then enabled starting at this sample number so that there is no sudden change in voltage on the UPS output. The mains-to-inverter switchover sequence is described in Figure 35.

FIGURE 35: MAINS-TO-INVERTER SWITCHOVER SEQUENCE



System Error

The UPS goes into the System Error state if a combination of the system variables is detected to be in a fault state. The state diagram in Figure 21 illustrates all conditions under which a system error is detected.

The dsPIC DSC device has built-in fault and current limit features that enable automatic shutdown of power converters with no software overhead. This feature is critical in power conversion applications and is useful in protecting the user, system hardware, and downstream electronics.

The System Error mode is designed to handle any faults after the respective power stage has been disabled. When the system enters this mode, the type of fault is displayed on the LCD module. When the UPS enters the System Error mode, the system needs to be restarted again before it can function normally.

Auxiliary Tasks

All non-critical functions of the Offline UPS are categorized as auxiliary tasks. These tasks have a relatively slow execution rate and therefore are assigned the lowest execution priority in the Offline UPS software.

The auxiliary tasks are executed in the main loop of the code. These tasks are performed only when other high-priority tasks like power conversion control loops and the UPS state machine are not active. In other words, the auxiliary tasks are performed during the “idle” time for the power conversion routines and state machine. As a result, the main loop is also referred to as the “idle loop”. The auxiliary tasks are numerously interrupted by high-priority tasks like the control loops and the state machine. Each of the auxiliary tasks is described briefly in the following sections.

OUTPUT VOLTAGE/CURRENT RMS CALCULATION

The RMS Calculation routine provides the output voltage and current information for the LCD display as well as for output overcurrent and output overvoltage/undervoltage protection.

The measured current and voltage are stored in data memory in an array of 256 points each. When the RMS calculation routine is called, the respective array is passed to the function, while the output of the function is the true RMS value of the parameter.

The DSP instructions of the dsPIC DSC device are utilized to efficiently execute the RMS calculation routines. The Q15 library includes functions for calculating sum-of-squares and square-root. Both of these operations are available in the Q15 library, and are used for implementing the RMS calculation in the offline UPS reference design.

The RMS calculation is called in the idle loop since it is executed over the AC mains cycle, and therefore, requires a relatively slow execution rate. The results are then scaled appropriately to produce a number in volts or amperes.

In order to display the result on the LCD display, each decimal digit of the RMS calculation result is stored as a character variable. The character variables are then concatenated into a string in order to display the data on the LCD module.

LCD DISPLAY

The LCD control code for the dsPIC DSC device is implemented as independent functions for writing pixels, bytes, words, or strings to the LCD module. The LCD display routines are called in the main loop.

The Offline UPS Reference Design uses a 4x20 character LCD display module controlled by a dedicated MCU (PIC18F2420). The dsPIC DSC device communicates with the LCD controller via a Serial Peripheral Interface (SPI).

The dsPIC DSC device is configured as the SPI master device and transmits all LCD commands to the LCD controller. The LCD controller converts the serial commands from the dsPIC DSC device into parallel data and also manages the timing controls for the LCD module.

Note:	Operation of the LCD controller is beyond the scope of this reference design. Visit www.microchip.com/lcd for LCD design solutions.

The LCD controller operates with a 5V supply and the dsPIC DSC operates on a 3.3V supply. However direct connections between the dsPIC DSC and LCD controller can be made because the digital-only pins of the dsPIC DSC are 5V tolerant. Also the digital outputs of the dsPIC DSC can be operated in open-drain configuration and produce logic high for the 5V LCD controller using just a pull-up resistor.

The resource allocation for LCD control is summarized in Table 8.

TABLE 8: dsPIC® DSC DEVICE RESOURCE ALLOCATION FOR LCD DISPLAY

Signal Name	Description	Type of Signal	dsPIC® DSC Resource Used	Sample Rate/Frequency
SDO	SPI Data Output	Digital Output	RP22	156.25 kHz when active
SDI	SPI Data Input	Digital Input	RP19	156.25 kHz when active
SCK	SPI Clock Output	Digital Output	RP21	156.25 kHz when active

Signal Name	Description	Type of Signal	dsPIC® DSC Resource Used	Sample Rate/Frequency
$\overline{SS}$	SPI Slave Select Output	Digital Output	RP20	Asserted only when data is transmitted to LCD controller

USB COMMUNICATION

The Offline UPS also includes a USB communication interface to enable power management for a computer or server connected to the UPS. The USB communication is performed by a separate USB controller MCU (PIC18F2450). The USB controller communicates with the dsPIC DSC device via an opto-isolated UART interface.

The resource allocation for the USB communication interface is summarized in Table 9.

TABLE 9: dsPIC® DSC DEVICE RESOURCE ALLOCATION FOR USB INTERFACE

Signal Name	Description	Type of Signal	dsPIC® DSC Resource Used	Sample Rate/Frequency
Tx	UART Transmit	Digital Output	RP27	9600 bps
RX	UART Receive	Digital Input	RP28	9600 bps

Fault States and Protection Schemes

There are a number of fault sources that can cause the system to turn off all outputs and enter the System Error mode. Any system fault can trigger the Offline UPS to enter the System Error mode. These include the following:

- Push-pull primary overcurrent
- DC Link undervoltage
- DC Link overvoltage
- Battery undervoltage
- Battery overvoltage
- Output overcurrent
- Overtemperature

The system will enter the System Error mode due to either a single fault or a combination of faults, depending on the operating modes. For example, a DC Link undervoltage condition will not cause the system to enter the System Error mode if the soft-start routine is active. Similarly, transient loads may cause the push-pull primary current to exceed the limit for a short duration. Therefore, a push-pull overcurrent fault will only be generated if the overcurrent condition persists for an extended duration.

All faults that are fast-acting and destructive to the system and user's load are handled in the high-priority control loops. The push-pull overcurrent fault is an example of a very high-speed signal that must be detected as quickly as possible. As a result, this fault is detected at the same time as the push-pull control loop. Other signals like the battery voltage are not very high-speed signals and therefore the faults are handled in the UPS state machine.

When a fault condition happens, the system enters the System Error mode and the type of fault is displayed on the LCD module.

Operation with Rectifier Loads

One of the most important applications of the Offline UPS is to provide uninterrupted power to computers and servers. Most computers and servers implement a switch-mode AC-DC power supply that implements Power Factor Correction (PFC). Such a load usually contains a front-end bridge rectifier and is therefore classified as a rectifier load.

If PFC is not implemented, the load appears as a highly capacitive load, resulting in high peak currents and a low power factor. A block diagram of the connections for such a configuration is shown in Figure 36.

The typical configuration of such a power supply contains a PFC boost converter as shown in Figure 37. The boost converter usually contains a large output capacitor. As seen from the circuit diagram, a low impedance path exists from the AC input to the output capacitor. As a result, the output capacitor draws a large inrush current when the load is first connected to the UPS output.

FIGURE 36: TYPICAL RECTIFIER LOAD FOR THE OFFLINE UPS

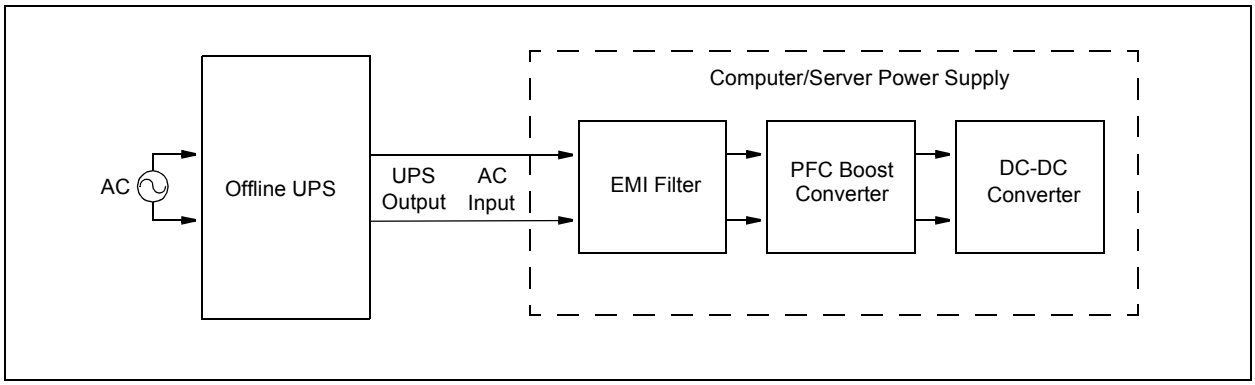
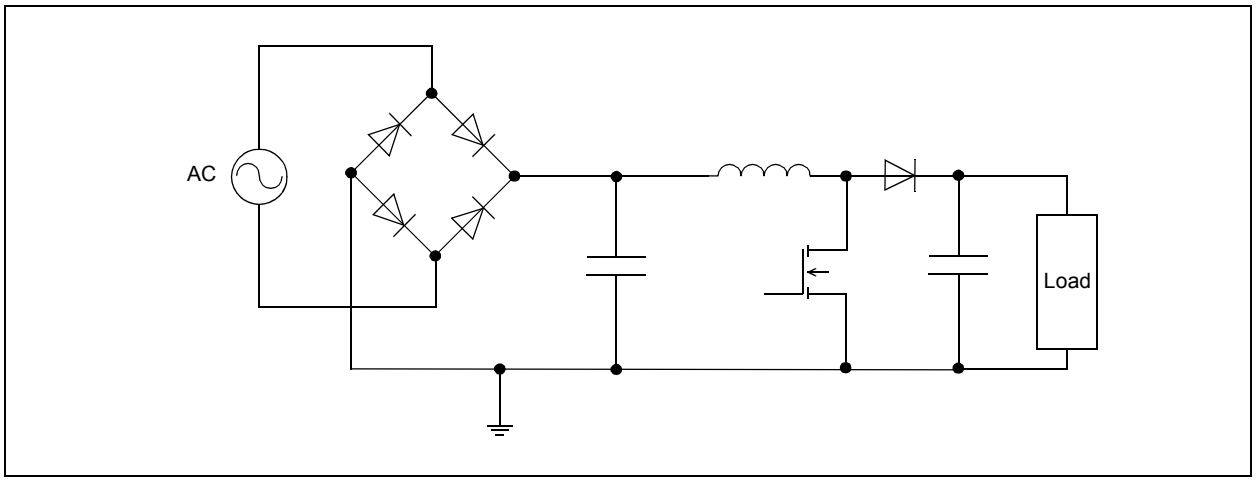
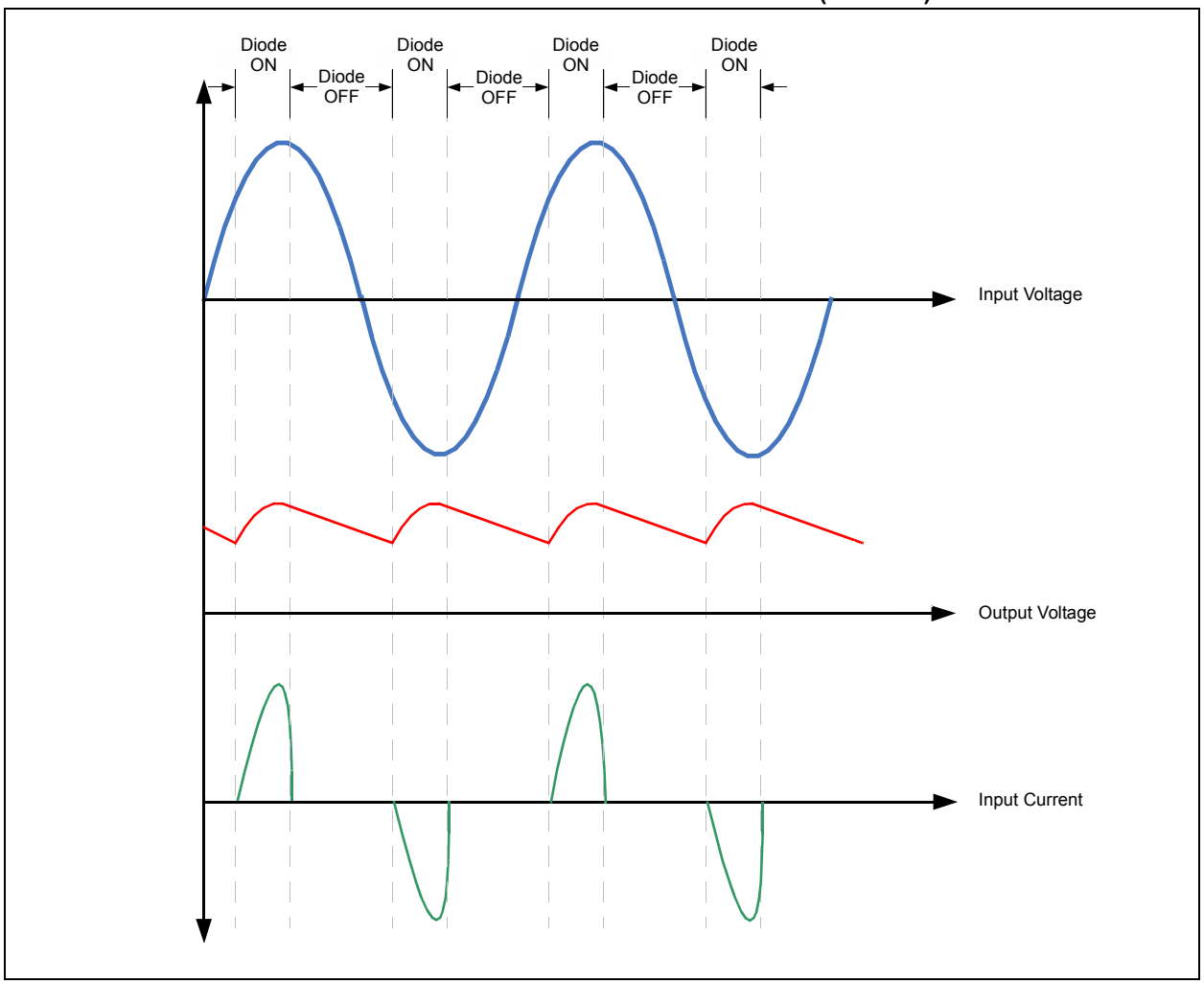


FIGURE 37: PFC BOOST CONVERTER



If PFC is not implemented, the current is drawn by the load in a very discontinuous nature with high peaks, causing the load to appear highly capacitive, as shown in Figure 38.

FIGURE 38: RECTIFIER LOAD INPUT CURRENT WAVEFORMS (NO PFC)



Due to the presence of a large capacitor on the output of the PFC boost converter, the Offline UPS needs to implement a special algorithm to handle load steps and startup conditions for rectifier loads.

The current draw during a rectifier load startup can be up to 20 times the maximum rated current. One option to support these high current surges is to design the hardware with sufficient design margin. However, this approach is usually not cost effective and may also cause a drop in performance or efficiency. The dsPIC DSC provides a number of flexible features to overcome this problem. The PWM Current-Limit feature can be used to limit the current on a cycle-by-cycle basis. This feature, along with software can help charge the output capacitor in a controlled manner so that the inrush current is limited.

In the Offline UPS Reference Design, an external interrupt is generated when an overcurrent condition occurs. This causes the PWM module to automatically shut down. Inside the Interrupt Service Routine, the PWM is configured for a very small duty cycle and then re-enabled. As the duty cycle is small, the current drawn during one PWM switching cycle is automatically limited. The duty cycle is incremented in small steps to charge the output capacitor in a controlled manner. While the current-limit fault handling routine is being executed, the inverter control loop is overridden. The inverter control loop resumes operation when the sine voltage reference of the inverter becomes equal to the actual voltage on the inverter output.

If the first current limit fault is caused by a short circuit condition on the inverter output, the current limit fault will be triggered immediately for a second time. This will cause the system to shut down with an overcurrent error. The error state is displayed on the LCD display module and is reset only when the system is turned OFF and back ON.

Peak Current Limiting Function

If the power factor of the rectifier load is too low, it will result in a high crest factor for the inverter current. The Offline UPS Reference Design is rated for a maximum crest factor of 3:1. If the crest factor of the load exceeds this value, no action is taken by the UPS if the current is within the maximum peak current rating. However, a high crest factor warning is displayed on the LCD display module.

If the peak current required by the load exceeds 15A, a current limiting function overrides the inverter control loop. This function limits the maximum current on the output by clamping the duty cycle to a maximum value.

DC Offset Elimination

A side-effect of operating with a high crest factor is that the current drawn may become asymmetric. This is caused by the presence of a small DC offset on the inverter output voltage. The DC offset occurs due to the tolerance limits of the feedback components.

A typical analog implementation requires the use of trimming resistors to eliminate the DC offset. This solution requires trimming of each UPS system during manufacturing, and therefore becomes expensive and time consuming. It may also need periodic adjustment via a servicing schedule to account for effects of long term degradation of components. The dsPIC DSC helps overcome this problem with an active algorithm to eliminate the DC offset.

The Offline UPS Reference Design implements an offset elimination routine by comparing the positive and negative peak of the measured output voltage. If an imbalance is detected, a correction factor is applied to the output voltage to cancel the DC offset. The peaks are determined by averaging the maximum and minimum recorded voltages over a number of sine wave cycles. Doing so helps to ignore the effects of load steps on the output.

HARDWARE DESIGN

Push-Pull Boost Converter

DESIGN SPECIFICATIONS

A push-pull boost converter needs to convert the wide range battery link input voltage to a stabilized high-voltage DC-Link. The design specifications used in the Offline UPS Reference Design are:

- Input voltage range: 30-45 V_{DC}
- Output voltage: 380 V_{DC}
- Continuous power: 1 kVA
- Peak power for two seconds: 1.3 kVA
- Switching frequency: 100 kHz

TOPOLOGIES CONSIDERED AND REASONS FOR CURRENT CHOICES

In Figure 39 and Figure 40 all possible push-pull boost circuits are shown. The combination of a push-pull inverter (Figure 39(C)) and a full-bridge rectifier (Figure 40(B)) was chosen, which provides the best price performance ratio. For the inverter only the low-side drive circuitry is required and simple PWM signals (see Figure 41) can drive the inverter.

FIGURE 39: PRIMARY DRIVE CIRCUITS

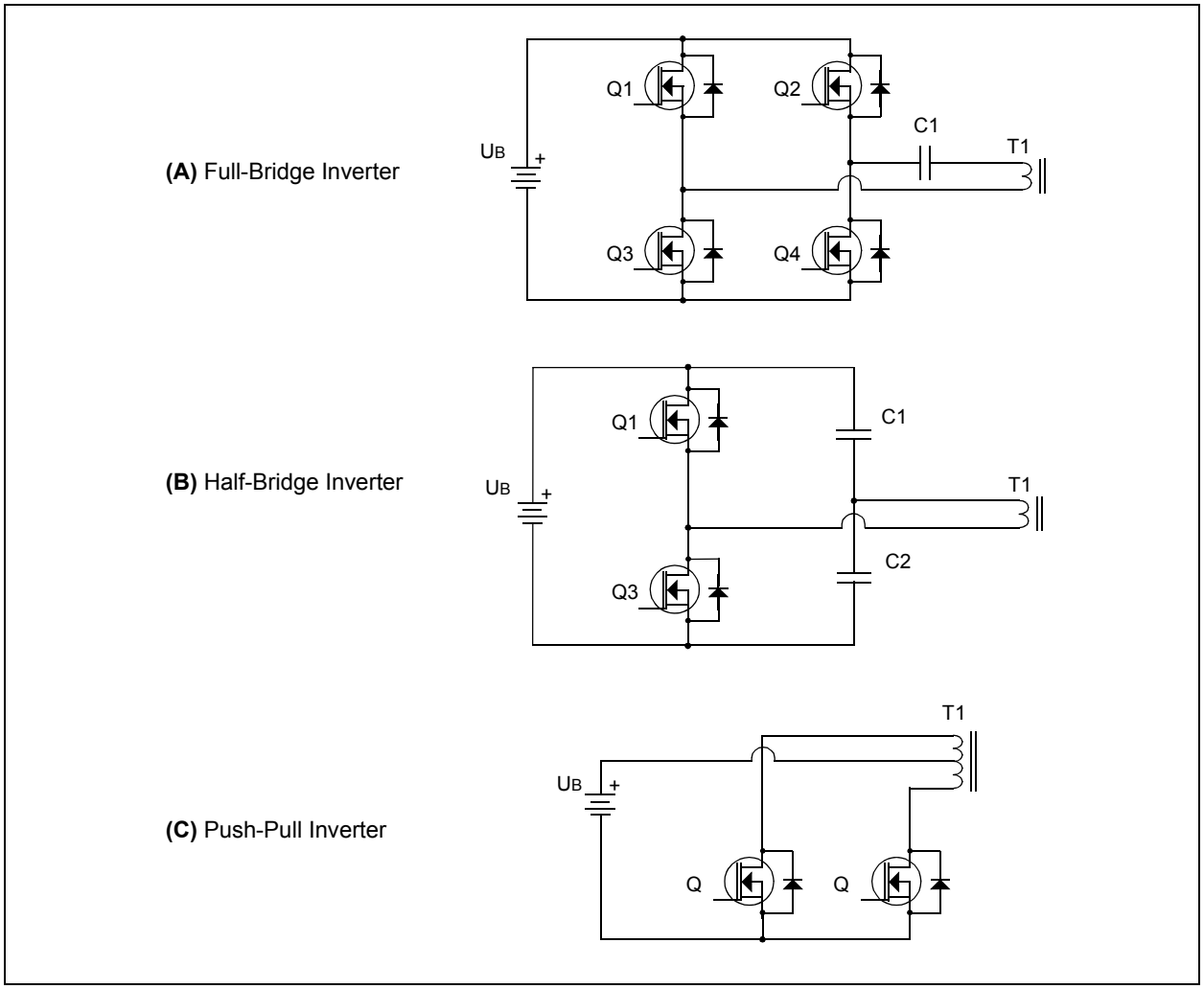


FIGURE 40: RECTIFIER CIRCUITS

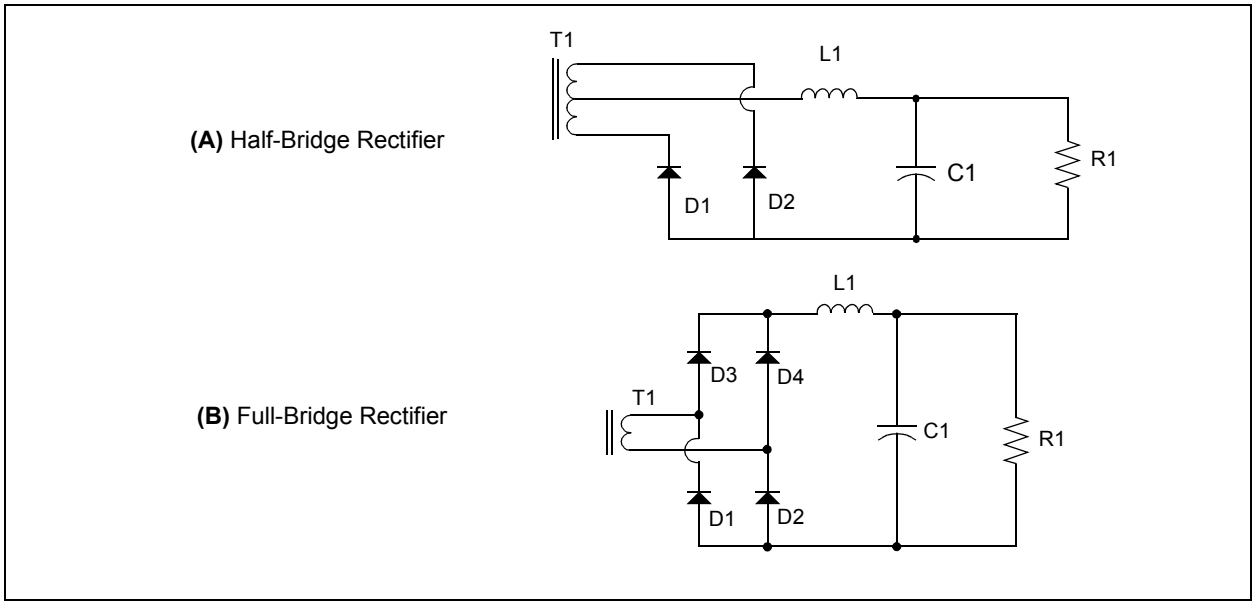
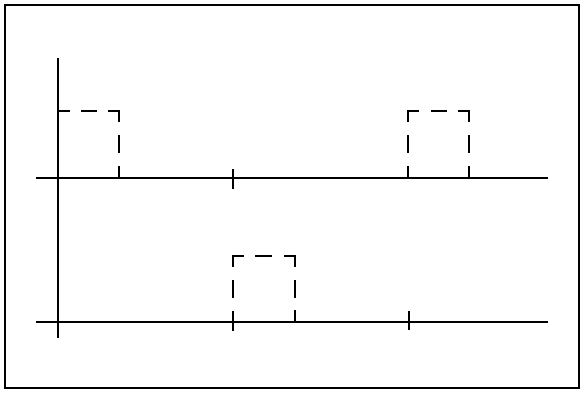


FIGURE 41: CONTROL SIGNALS FOR PUSH-PULL INVERTER



For the secondary, a full-bridge rectifier was chosen for the following reasons:

- Reducing the leakage inductance by using only one secondary winding on the transformer
- Reducing cost of transformer
- Rectifier diodes can be rated lower in reverse breakdown voltage, such diodes have better forward and switching characteristics.
- Synchronous rectification is not required due to high-voltage and low current operation.

The output voltage is calculated by Equation 6, where $N2 \div N1$ is the transformer windings ratio, and d is the duty cycle of the PWM signal. The duty cycle must be limited to the given boundary. In a real application, the duty cycle must be limited to $0.1 < d < 0.42$. This is done due to the switching behavior of the MOSFETs and transformer. Due to allowed oscillation and losses in the system, the calculation using Equation 6 is not exact. When no load is applied to the push-pull boost stage, the controller has to switch into Burst mode, and when heavy load is applied, the duty cycle must be increased to compensate for various losses.

EQUATION 6:

$$U_{DC} = U_{BAT} \cdot \frac{N_2}{N_1} \cdot 2d$$

where:

d is the duty cycle of the transistors and $0 < d < 0.5$

N2/N1 is the secondary-to-primary turns ratio of the transformer

DESIGN OF POWER-TRAIN COMPONENTS

The push-pull transformer has been designed using a ferrite magnetic core. The transformer design is based using the area product (W_aA_c) approach and is designed to meet the following conditions:

- Minimum input voltage: V_{imin} = 30V
- Maximum DC link voltage: V_o = 380V
- Maximum output power: P_{omax} = 2000W
- Primary RMS current: IP_{rms} = 30.5A
- Maximum duty cycle: D_{max} = 0.42
- Switching frequency: f = 100 kHz

The manufacturer's data sheet is used to help select the appropriate material for the desired application. For the given range of materials, frequency, core loss, and maximum flux density of the material should be considered. From the research data, 3C90 material from FERROXCUBE was selected. From core loss, maximum flux density can be calculated, as shown in Equation 7. The factors used in this equation are provided in Table 10.

EQUATION 7:

$$P_l = a \cdot f^c \cdot B_{max}^d$$

Core loss density is normally selected around 150 mW/cm^3. The calculated maximum flux density must be limited to less than half of B at saturation. This B level is chosen because the transformer core will develop excessive temperature rise at this frequency when the flux density is close to saturation. Maximum flux density can now be calculated, as shown in Equation 8.

TABLE 10: FACTORS APPLIED TO EQUATION 7 (CORE LOSS EQUATION)

Material	Frequency	a	c	d
R, 35G, N87, 3C90	f < 100 kHz	0.074	1.43	2.85
	100 kHz ≤ f < 500 kHz	0.036	1.64	2.68
	f ≥ 500 kHz	0.014	1.84	2.28
P, 45G, N72, 3C85	f < 100 kHz	0.158	1.36	2.86
	100 kHz ≤ f < 500 kHz	0.0434	1.63	2.62
	f ≥ 500 kHz	7.36e-7	3.47	2.54
F, 25G, N41, 3C81	f < 10 kHz	0.790	1.06	2.85
	10 kHz ≤ f < 100 kHz	0.0717	1.72	2.66
	100 kHz ≤ f < 500 kHz	0.0573	1.66	2.68
	f ≥ 500 kHz	0.0126	1.88	2.29

EQUATION 8:

$$B_{max} = \left(\frac{P_l}{a \cdot \left(\frac{f}{1000} \right)^c} \right)^{\frac{1000}{d}} = \left(\frac{150}{0.036 \cdot \left(\frac{100000}{1000} \right)^{1.64}} \right)^{\frac{1000}{2.68}} = 1339G$$

For selecting the right size core, the area product of the core must be calculated by Equation 9. This equation is derived from the flux linkage equation ($\psi = N * \Phi$) and represents the power handling ability of the core. Therefore, each core has a number that is a product of its window area, W_a, and the core cross-sectional area, A_c.

EQUATION 9:

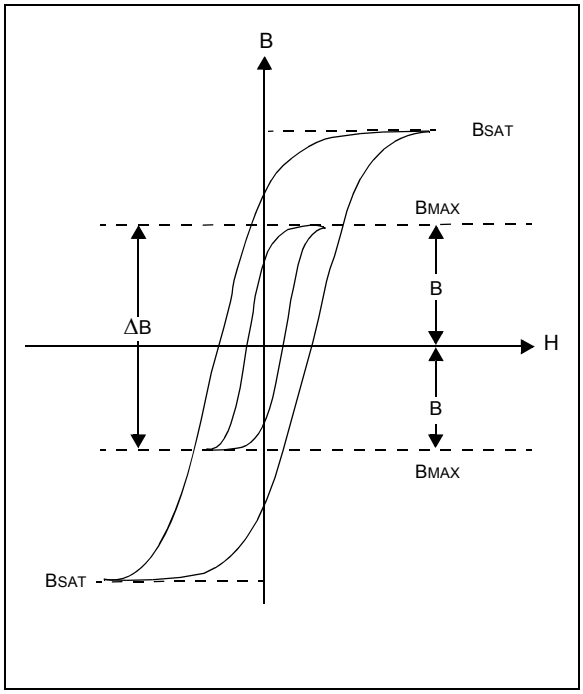
$$W_a A_c = \frac{10^8 \cdot P_{omax}}{K_t \cdot \Delta B \cdot f \cdot J}$$

ΔB in Equation 9 is equal to $2B_{max}$ due to bidirectional core excitation as seen in Figure 42. Current density of a winding is estimated to be 500A/cm^2, and maximum output power P_{omax} is 2000W. Therefore, the calculated area product is shown in Equation 10.

EQUATION 10:

$$W_a A_c = \frac{10^8 \cdot 2000}{0.254 \cdot 2678 \cdot 100000 \cdot 500} = 5.9 cm^4$$

FIGURE 42: HYSTERESIS LOOP OF MAGNETIC CORE



The selected core must have an area product larger than calculated. ETD54 shape and size of a core was selected with $W_a A_c$ = 12.6 cm^2. A larger size was selected due to the primary and secondary windings, which fit to the winding area of that core.

The primary turns are calculated by Equation 11. Given result is then rounded up or down to the integer value. In this case it is rounded to 4 turns for one-half of the primary.

EQUATION 11:

$$N_P = \frac{10^8 \cdot V_{imin} \cdot \left(\frac{2}{f}\right) \cdot D_{max}}{\Delta B \cdot A_C} = \frac{10^8 \cdot 30 \cdot \left(\frac{2}{100000}\right) \cdot 0.42}{2678 \cdot 2.8} = 3.4$$

The secondary turns are calculated by Equation 12. The result is rounded to the value 60 of secondary turns.

EQUATION 12:

$$N_s = \frac{\frac{V_o}{2D_{max}}}{V_{imin}} \cdot N_p = \frac{\frac{380}{2 \cdot 0.42}}{30} \cdot 4 = 60.3$$

The cross section of the primary and secondary windings is calculated by Equation 13. Different current densities are used (J_P = 8A/mm^2 and J_S = 5A/mm^2) to fit the windings into the transformer bobbin and because the length of one-half of the primary is very short compared to the secondary. In that case, it is allowed to use higher current density for primary as temperature of winding will not be much higher due to the short winding. Primary RMS current is I_{Prms} = 30.5A. Secondary current can be calculated by $I_{srms} = I_{Prms} * N_p \div N_s$ = 2.03A.

EQUATION 13:

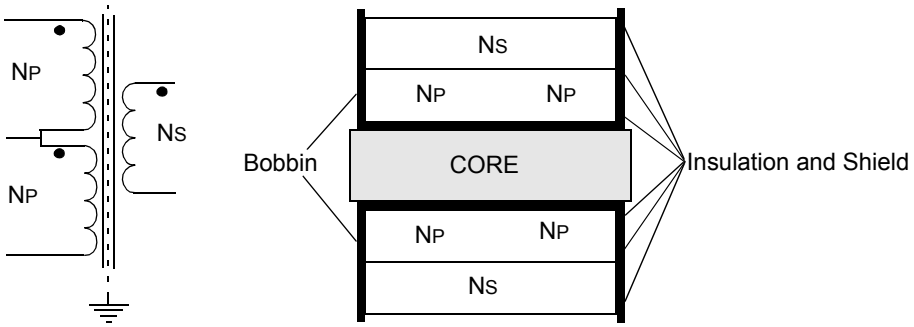
$$A_{cuP} = \frac{I_{Prms}}{J_P} = 3.81mm^2$$

$$A_{cuS} = \frac{I_{Srms}}{J_S} = 0.41mm^2$$

Because of the high switching frequency, f = 100 kHz, litz wire must be selected to reduce winding losses (losses by skin and proximity effect). Litz wire must also be designed for that frequency.

Figure 43 shows the transformer winding diagram and construction diagram.

FIGURE 43: TRANSFORMER ELECTRICAL AND MECHANICAL CONSTRUCTION



PUSH-PULL MOSFETS

When choosing the right MOSFETs the following must be considered:

- Maximum Breakdown Voltage
- Continuous Current
- Peak Current
- Package Thermal Performance

Maximum Breakdown Voltage

In the chosen configuration, a MOSFET must be able to hold more than twice the battery voltage, as expressed in Equation 14. In this calculation, a safety factor of 30% overrating was chosen. Therefore, the selected devices need to have a drain-to-source breakdown voltage higher than 117V.

EQUATION 14:

$$V_{BRDSS} > 2V_{BAT}$$
$$2 \cdot 45V \cdot 1.3 = 117V$$

Continuous Current

To calculate the current rating of the devices, peak and average currents have to be estimated. The peak and average currents can be estimated from the power ratings and input voltage. The average current is calculated using Equation 15, where P_C is the continuous power and U_{BAT} is the battery voltage.

EQUATION 15:

$$I_a = P_c / U_{bat}$$

The highest current will flow at the lowest battery voltage so the continuous current is:

$I = 1000W \div 30V = 33.34A$. And per leg, the continuous drain current is half of this: $I_D = 16.67A$.

Peak Current

The peak current must be calculated at maximum power and the form of the current waveform must also be taken into account. When we assume that the current waveform will have a sawtooth waveform with the given duty cycle (d), we can calculate the resulting peak current using Equation 16. The duty cycle (d) is calculated using Equation 17.

EQUATION 16:

$$I_{pm} = \frac{P_{\max}}{U_{bat} \cdot d}$$

EQUATION 17:

$$d = \frac{U_{DC} \cdot N_2}{2 \cdot U_{bat} \cdot N_1}$$

When we use a transformer with windings ratio of 16 the peak current is that of Equation 18:

EQUATION 18:

$$I_{pm} = \frac{2000W}{30V \cdot 0.416} = 160.3A$$

Therefore, we have to design the MOSFETs for continuous drain current of 16.67A and peak drain current of 160.3A. Because the waveform shape will not be an exact sawtooth, these calculations are only an estimate. To be on the safe side, these numbers are increased by 30%.

Package Thermal Performance

To design the thermal performance, the rms current value must be calculated. If the waveform shape and peak current are known, the rms can be calculated using Equation 19.

EQUATION 19:

$$I_{rms} = I_{pc} \sqrt{\frac{d}{3}}$$

The rms current can now be calculated and is shown in Equation 20:

EQUATION 20:

$$I_{rms} = 80.15 \cdot \sqrt{\frac{2}{3} \cdot .416} = 42.13A$$

Per leg, the current is half of this: I_{DRMS} = 21.07A . This is the most critical design consideration; therefore, an overrating of 50% should be done I_{DRMS} = 21.07A * 1.5 = 31.5A, and all current leading traces and the transformer should also be rated for this current.

The conductive losses on the MOSFETS are calculated using Equation 21.

EQUATION 21:

$$P_c = I^2_{Drms} \cdot R_{DSon}$$

For a switching frequency of 100 kHz and with the push-pull configuration also switching, losses have to be taken into account. If the current waveform is near sawtooth, turn-on losses can be neglected. Turn-off losses depend on the peak current and leakage inductance. To limit the voltage spikes at turn-off a voltage clamp circuit is used. This circuit enables the MOSFETs to operate without RC snubbers. Snubbers are only used to suppress high frequency oscillation, and not to dissipate the energy stored in the leakage inductance of the transformer. Therefore, all of the energy is dissipated on the MOSFETs. Equation 22 can be used to estimate the power dissipation at turn-off.

EQUATION 22:

$$P_{off} = f_{SW} \frac{W_L}{4}$$

In Equation 22, W_L is the energy stored in the leakage inductance at turn-off and is calculated using Equation 23.

EQUATION 23:

$$W_L = \frac{i^2 L}{2}$$

A typical transformer in this range should have not more than L = 0.5 µH of leakage inductance. Therefore, the turn off power would be that of Equation 24:

EQUATION 24:

$$P_{off} = 100e^3 \frac{1.6e^{-3}}{4} = 40W$$

Total dissipation on the MOSFETS is then $Ptot$ = $Poff$ + P_C, and it is estimated to be 55W per leg.

Now the MOSFETs can be selected. In the reference design, a TO-220 package is used for the MOSFETs. Typical junction-to-heat sink thermal resistance of these devices is RΘt = 2.5°C/W when using silicone pad insulation.

We will allow a continuous junction temperature of 110°C and a heat sink temperature of 60°C. From this and the power dissipation, we can calculate the needed thermal resistance, which provides the number of parallel MOSFETs to use.

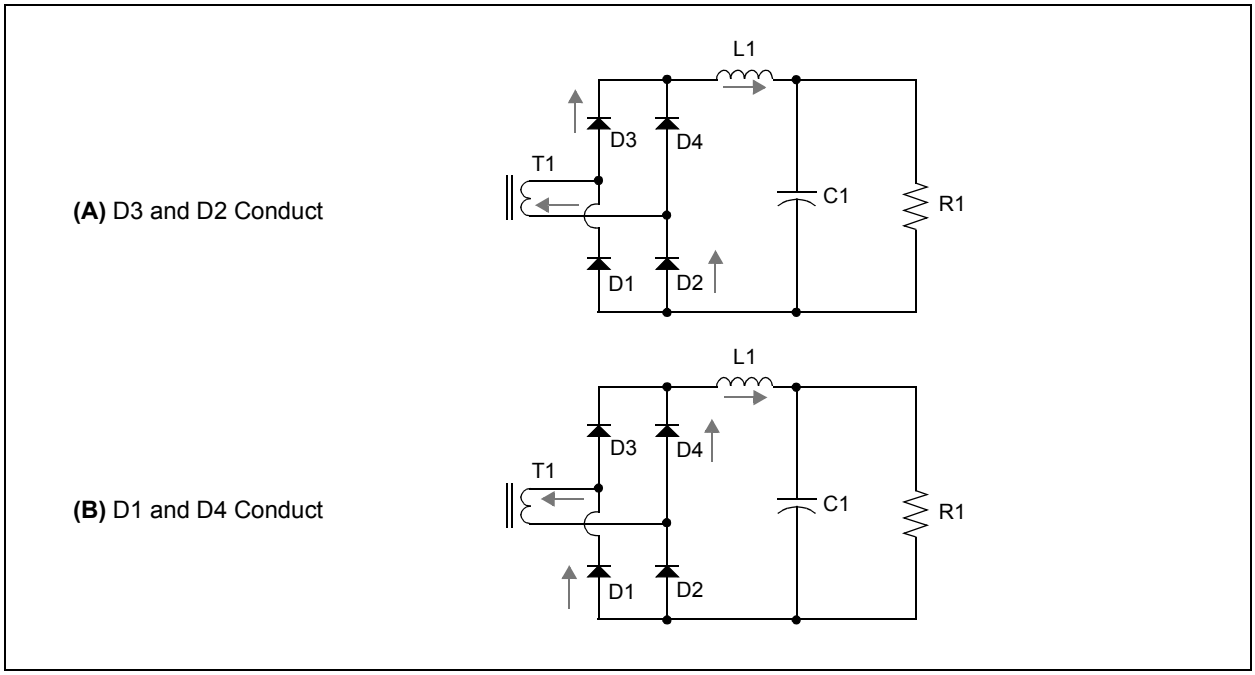
The number of necessary devices is calculated as $n = R\Theta t \div R\Theta_{JH}$ = 2.7. According to the calculation shown in Equation 25, three parallel FDP2532 devices from Fairchild Semiconductor were selected.

EQUATION 25:

$$R_{\Theta JH} = \frac{\Delta\Theta}{P_{tot}} = \frac{50}{55} = 0.91°C/W$$

FULL-WAVE RECTIFIER

FIGURE 44: RECTIFIERS WITH CURRENT FLOW



When selecting diodes, the following must be considered:

- Diode Breakdown Voltage
- Average Forward Current
- Peak Forward Current
- Switching Characteristics
- Package Thermal Performance

Diode Breakdown Voltage

The transformer secondary voltage is calculated as $VS = VBAT * N2 \div N1$. The maximum secondary voltage at the highest battery voltage is VS = 45 * 16 = 720V . Because of transformer leakage inductance, diode internal inductance, and DC link inductor inductance, voltage spikes appear on diodes when switching. Due to this, the calculated breakdown voltage is increased by 30% and should be more than 936V.

Average Forward Current

Average forward current per leg is easily calculated using Equation 26 from the desired DC link voltage and continuous output power.

EQUATION 26:

$$I_{avg} = \frac{P_c}{V_{DC}} = \frac{1000}{380} = 2.6A$$

Peak Forward Current

Peak current is calculated using the transformer current ratio and peak MOSFET current previously calculated in Equation 9.

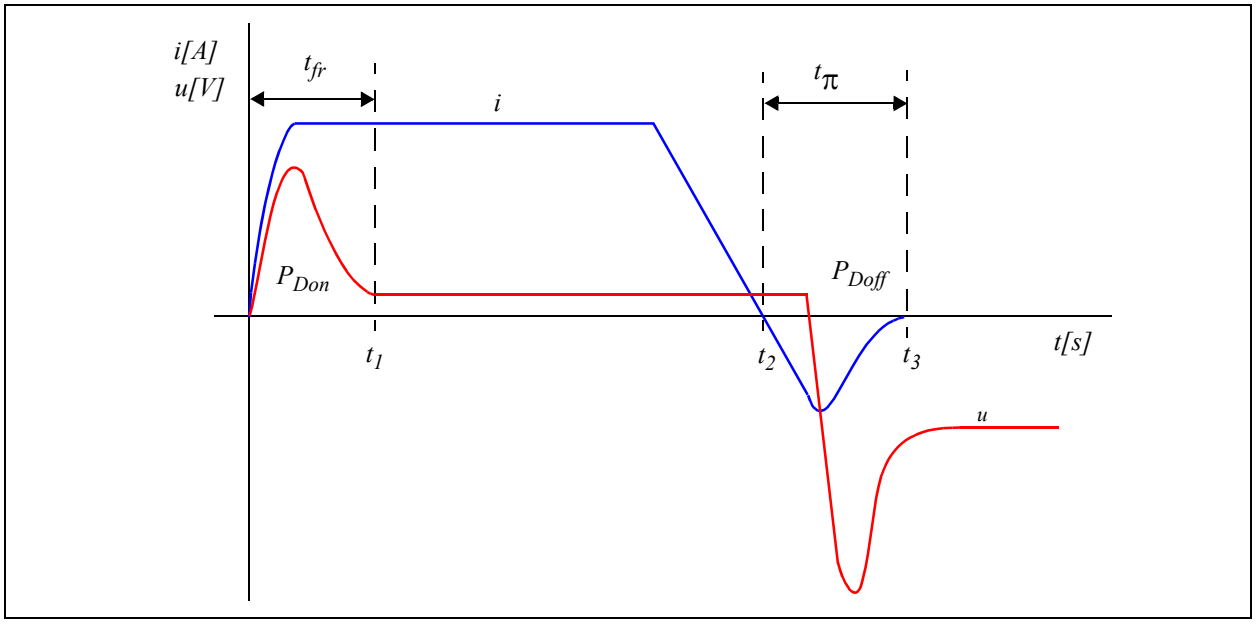
EQUATION 27:

$$I_{pD} = I_P \cdot \frac{N_1}{N_2} = 160.3 \cdot 0.625 = 10A$$

Switching Characteristics

Diode switching characteristics are determined by forward recovery time and reverse recovery time.

FIGURE 45: DIODE SWITCHING CHARACTERISTICS



Diode switching loss can be estimated using Equation 28.

EQUATION 28:

$$P_{swD} = Q_c \cdot V_{DC} \cdot f_{SW}$$

Package Thermal Performance

For diodes, an isolated TO-220-2 package is used. Continuous working junction temperature should not exceed 130°C at a heat sink temperature of 60°C. Typical thermal junction-to-heat sink resistance of the junction-isolated TO-220-2 package is $R\Theta t$ = 3.5°C/W. Therefore, the maximum allowed power dissipation per part is P_{MAX} = 70 ÷ 3.5 = 20W.

The STTH1210DI from STMicroelectronics meets the voltage and current requirements. Power loss calculation can now be done looking at the diode data sheet.

Total power loss is estimated by adding conduction losses and switching losses, as shown in Equation 29.

EQUATION 29:

$$P_{tot} = P_{swD} + P_{fD} = 10W$$

The estimation shows that the power losses are within the set criteria.

Output Inductor

This inductor is optional and is not required. Its use depends on the transformer construction and control of DC-link voltage, and the inductor value that must be used. This section describes the design of a 50 µH output inductor.

The design of the output inductor uses the area product approach with the following conditions:

- Inductance: L = 50 µH
- Peak DC current: I_p = 13A
- Operating flux density: B_m = 300 mT
- Current density: J = 500A/cm^2
- Window utilization: K_u = 0.4

First, the energy handling capability must be calculated by Equation 30.

EQUATION 30:

$$E = \frac{L \cdot I_p^2}{2} = \frac{50 \cdot 10^{-6} \cdot 13^2}{2} = 0.0043Ws$$

Then, to select the appropriate size of ferrite core, the area product calculation must be done, as shown in Equation 31.

EQUATION 31:

$$W_a A_c = \frac{2 \cdot E \cdot 10^4}{B_m \cdot J \cdot K_u} = 1.43cm^4$$

The selected core was the P36/22 pot core from FERROXCUBE due to its small size and shape, which produces less interference into surrounding components. The area product of this core is 1.46 cm^4 and can be calculated from the data in the manufacturer's data sheet.

The number of turns required to get the desired inductance of the coil is calculated by Equation 32. The Core cross section A_c = 172 mm^2 is obtained from the manufacturer's data sheet.

EQUATION 32:

$$N = \frac{L \cdot I_p}{A_c \cdot B_m} = 12.6$$

The calculated number of turns is then rounded to the nearest integer value, which is 13.

To get the desired inductance, 3C81 material with an air gap was selected to control the flux density. If an air gap is distributed into the magnetic path of the core, the effective permeability of material changes and inductance factor A_L. From the A_L value and number of turns, the inductance is calculated by Equation 33. The A_L value is obtained from the material data sheet and is 315 nH at 0.97 mm air gap.

EQUATION 33:

$$L = N^2 \cdot A_L = 53\mu H$$

The new operating flux density is verified by Equation 34 and must be lower than the saturation point of the selected material.

EQUATION 34:

$$B_{new} = \frac{L \cdot I_p}{N \cdot A_c} = 308mT$$

The 3C81 material has a saturation point at 320 mT (100°C).

If the criteria are not fulfilled, different material, air gap, number of turns, or even a bigger core must be selected.

The cross-section of a wire is calculated by Equation 35, where RMS current through the inductor is calculated from primary RMS current of push-pull transformer and turns ratio. This current is twice as large as primary because for half of a switching period, the first primary winding is conducting and in the other half, the second primary winding.

EQUATION 35:

$$A_{cu} = \frac{I_{rms}}{J} = \frac{2 \cdot I_{Prms} \cdot \frac{N_P}{N_S}}{J} = 0.82mm^2$$

The calculated value is the minimum cross-section of a wire (100 kHz litz wire must be used).

Next, the fill factor must be calculated by Equation 36. This provides an estimation of whether the winding fits into the bobbin. The fill factor must be 0.4 or less.

W_b is the bobbin winding area and is 72.4 mm^2, and can be found in the core data sheet.

EQUATION 36:

$$K_u = \frac{N \cdot A_{cu}}{W_b} = 0.15$$

Output Capacitors

When choosing DC-link capacitors, the following must be considered:

- Voltage Rating
- Ripple Current

Voltage Rating

The voltage rating is defined by the DC Link voltage: V_{DC} = 380V. Therefore, the capacitors must be above this rating.

Ripple Current

When the DC link voltage controller is working as expected, the low frequency ripple current caused by the inverter is negligible. Therefore, the capacitors need only compensate for the reactive load current, which depends on the device specifications: S = 1300VA and P = 1000W.

EQUATION 37:

$$Q = \sqrt{S^2 - P^2} = 830.7Var$$

EQUATION 38:

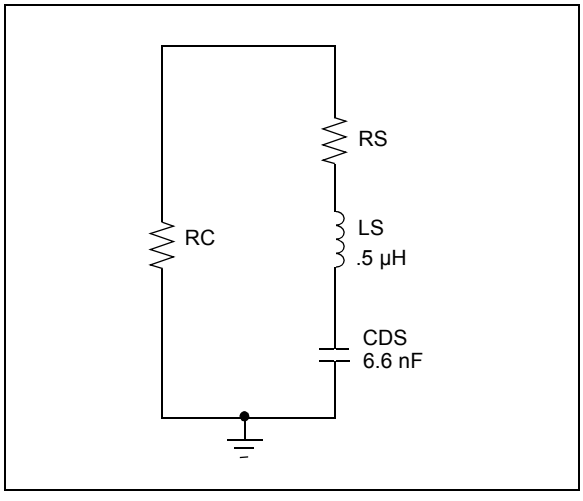
$$I_r = \frac{Q}{V_{AC}} = \frac{830.7}{230} = 3.6A$$

SNUBBERS

Snubbers are used to dampen high frequency oscillation and reduce ringing losses on diodes. Snubbers on the primary side are placed across the primary windings and are not used to handle voltage spikes at turn-off of the MOSFETs. They only reduce ringing and transformer in-rush current.

To design the snubber for the primary side, the capacitance of the MOSFETs and leakage inductance of the transformer must be known. Both parameters can be measured; however, MOSFET capacitance is voltage dependent so only an estimate can be used. In our case, the capacitance of three parallel MOSFETs is approximately C_{DS} = 7 nF, and leakage inductance of the transformer is estimated at L_S = 500 nH. A simplified high frequency circuit is shown in Figure 46.

FIGURE 46: HIGH-FREQUENCY CIRCUIT



The resonant frequency is calculated using Equation 39.

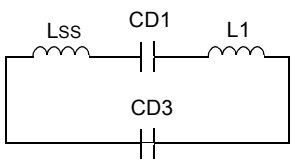
EQUATION 39:

$$f = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{DS} \cdot L_S}} = 2.7MHz$$

Damping of the system is very low because of the low primary winding resistance (RS) and the series resistance of the battery link capacitors (RC), which are both in the range of milliohms. To reduce this high frequency ringing, a series RC snubbers were added across the primary winding. The capacitance should be one to three times the capacitance of the MOSFETs, and the series resistor value should be chosen so that it grants damping and the power dissipation is within the resistor rating. To maintain high efficiency of the system we allow less than 1% of the rated power to be dissipated on the primary snubbers. The final values of the RC snubber are evaluated by experimenting and are C = 10 nF and R = 12Ω. The power rating of the resistors is 4W.

To design the snubbers for the rectifier diodes, the capacitance of the rectifier diode must be known. The simplified high frequency circuit is shown in Figure 47.

FIGURE 47: HIGH-FREQUENCY CIRCUIT



Here, the capacitor should be in the range from two to five times the capacitance of the diode. The diode capacitance can be found in the diode data sheet. For the selected diodes it is approximately C_D = 70 pF. Therefore, a good starting capacitance value for the snubber is C = 150 pF. Here we will also limit the maximum waste power to 1% of the rated converter power to keep the efficiency of the converter as high as possible. Thus, the resistor ratings will also be 4W. The resistor value should be selected so that the main switching voltage signal will produce as low as possible dissipation on the resistor. The dissipation is dependent on the RC frequency characteristics, and selecting lower resistance or lower capacitance will shift the characteristic frequency of the RC circuit higher, which result in the 100 kHz switching voltage producing less dissipation on the snubbers. However, damping of the snubbers will also decrease. A good starting value for the resistor is R = 1 kΩ.

Calculating the required snubber circuit is very complex and does not give the expected results. Therefore, the parameters have to be evaluated by experimenting. When designing the snubbers the following must be considered:

- Overall system efficiency
- Signal quality
- Device power ratings
- Device voltage ratings

Design of Drive Circuitry

To drive the MOSFETs, a driver must be used that amplifies the signal from the dsPIC DSC device and drives the gates of MOSFETs. The gate of a MOSFET behaves like a capacitor. The MOSFET drain-to-source R_{DS} depends on the gate to source voltage, V_{GS}. The higher the gate-to-source voltage, the lower the drain-to-source resistance of the MOSFET. For the selected MOSFETs:

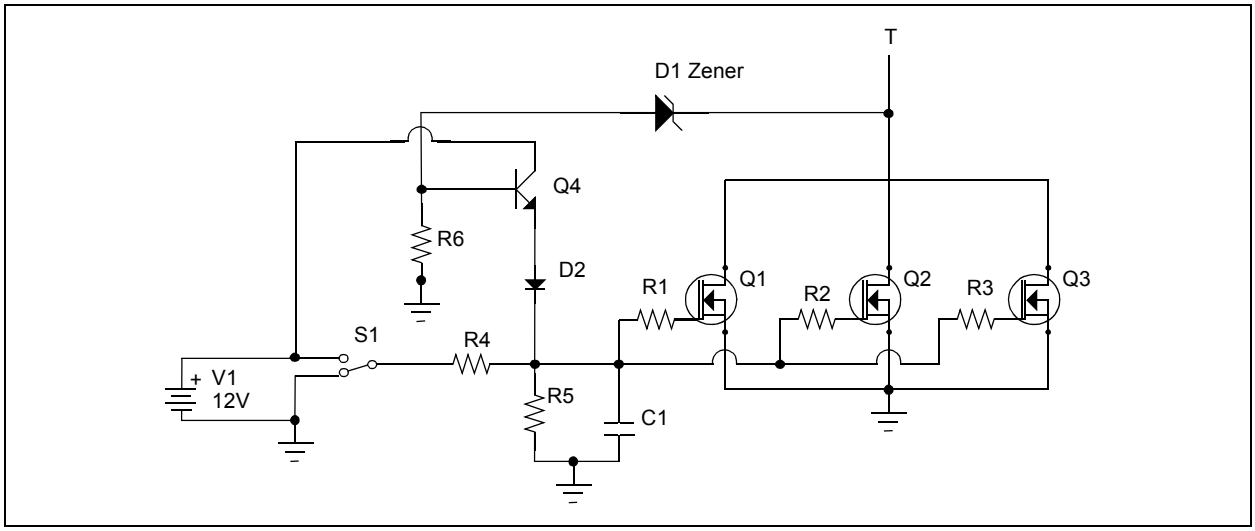
- V_{GS} = ±20V
- $V_{GS(TH)}$ = 2-4V
- $C_{G(TOT)}$ = 10.7 nF

To ensure low resistance in the ON state the gates are driven with 12V signals. The drive circuit is shown in Figure 48, which consists of the driver shown as S1, slope control elements, equalization resistors R1, R2, R3, R4, R5, and C1 turn-off voltage clamp circuit D1, D2, Q4, R6.

The elements R5 and C1 are optional. R5 is used to ensure the MOSFETs do not turn on by themselves. C1 is used to compensate for Miller capacitance and EMI control. Resistors R1, R2, and R3 are used to equalize the gate threshold voltage of the MOSFETs to ensure parallel turn-on. In combination with R4, the turn-on slope is also controlled. In addition, the turn-off slope is controlled until the drain-to-source voltage (V_{DS}) reaches the voltage clamp circuit threshold. When the voltage clamp circuit becomes active, V_{DS} stays constant and the turn-off slope is reduced. This enables part of the energy stored in the leakage inductance to be transferred to the secondary side and the other part to be dissipated in a controlled fashion by the MOSFETs. Also, overall system oscillation is reduced due to lower current slopes. However, it must be considered that the turn on time of the MOSFETs will increase and that the maximum duty cycle must be reduced.

Driver continuous supply current is calculated using Equation 40. Where n is the number of parallel MOSFETs.

FIGURE 48: MOSFET DRIVE CIRCUIT



EQUATION 40:

$$I_{Gc} = 2 \cdot n \cdot C_{G(tot)} \cdot V_{DRV} \cdot f_{SW} = 2 \cdot 3 \cdot 10.7 \cdot 10^{-9} \cdot 15 \cdot 100 \cdot 10^{3} = 96.3mA$$

Peak current estimate is calculated using Equation 41.

EQUATION 41:

$$I_{Gp} = \frac{V_{DRV} - V_{GS(TH)}}{R4 + (R1^{-1} + R2^{-1} + R3^{-1})^{-1}}$$

Driver power dissipation calculation is shown in the *"MCP14E3/MCP14E4/MCPE5 4.0A Dual High-Speed Power MOSFET Drivers With Enable"* (DS22062) data sheet. The total power dissipation is calculated to approximately $Ptot$ = 1W.

Design of Voltage and Current Feedback Circuitry

For the push-pull stage, battery link, and DC link voltage, measurements are needed. Both measurements are done differential with the MCP6022 rail-to-rail operational amplifiers. When taking high voltage differential measurements, the input resistance must be high and voltage and power rating of the resistors must not be exceeded. Because of this, 1206 resistors are used on the input dividers in the reference design. The output signal for the differential amplifiers is 5V to increase SNR. Then, a resistor divider is used near the dsPIC DSC to interface to the 3.3V, 10-bit A/D converter. In addition, a capacitor is placed near the dsPIC DSC to enable fast charge of the S&H capacitor. For measurement, 1% tolerance resistors are used. This is especially important for the differential amplifiers to guarantee the same resistance in both arms to reduce common mode noise rejection.

The MOSFET drain current and heat sink temperature are also measured. The current measurement is based on the voltage drop measurement on the drain-to-source resistance, RDS_{ON}. This type of measurement is temperature dependent so a semiconductor temperature sensor is placed which has nearly the same temperature dependency as the MOSFET, RDS_{ON}. The current feedback signal is used to prevent the transformer from saturating.

PCB Layout Considerations

For the push-pull stage, special care should be taken with traces leading the primary current. High frequency currents and high current peak values can produce a lot of noise and even losses on the PCB. Therefore, the traces should be as short as possible and they should contain no sharp edges. It is a good idea to connect the primary windings with the transformer litz wire that is used for winding the transformer (fly leads).

Care should be taken to not couple the power and signal parts with the ground planes.

Thermal Design

The heat produced by the MOSFETs and diodes must be transferred to ambient air using heat sinks. Total power loss estimation which were performed earlier are:

- For MOSFETs, P_{MOS} = 110W
- For diodes, P_{DIODE} = 40W. Forced air cooling is used to dissipate the heat

Full-Bridge Inverter

INVERTER DESIGN SPECIFICATIONS

The inverter is used to generate the UPS output voltage. The specifications are:

- Input voltage : 380 V_{DC}
- Output voltage: 230 VACrms
- Continuous power: 1 kW
- Continuous output current: 5.6 Arms
- Peak power for 2 seconds: 1300 VA
- Maximum output current: 10 Arms
- Switching frequency: 50 kHz
- Short circuit-proof

INVERTER POWER-TRAIN DESIGN

IGBT Selection

Due to the high switching frequency, IGBTs with low switching losses must be selected. Their voltage rating should be 600V with a current rating of 14A or more continuous. The STGP14NC60KD from STMicroelectronics was chosen and fulfils all of the selected criteria.

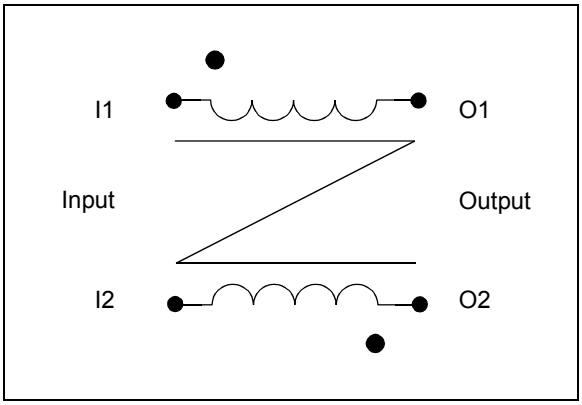
Loss estimation can be done using information in the data sheet and is estimated at P = 17W. The estimated junction-to-heat sink resistance using SilPad is: $R\Theta t$ = 3°C/W. According to these estimates, the junction temperature will raise 50°C above the heat sink temperature.

The IGBT inverter also acts as a full-wave rectifier when charging the battery from the power grid.

Output Common-mode Choke

The common mode inductor has two windings on the same core. It is called common mode because it blocks common mode interference and switching noise produced by the inverter to the output. A schematic of the inductor is shown in Figure 49. The dot on the windings indicates the start of a winding. When load is connected to the output, the flux in the core must be summed; otherwise, the inductor is connected incorrectly.

FIGURE 49: COMMON MODE INDUCTOR SCHEMATIC



Design of the output common-mode choke is the same design of that of a DC inductor, with the following conditions:

- Inductance: L = 250 µH
- Peak AC current: I_p = 17A
- Operating flux density: B_m = 380 mT
- Current density: J = 500*A/cm*^{2}
- Window utilization: K_u = 0.4
- Output power: P_o = 1000W

First, the energy handling capability must be calculated, as shown in Equation 42.

EQUATION 42:

$$E = \frac{L \cdot I_p^2}{2} = \frac{250 \cdot 10^{-6} \cdot 17^2}{2} = 0.036Ws$$

After that, to select the appropriate size of the core, the area product calculation must be done, as shown in Equation 43.

EQUATION 43:

$$W_a A_c = \frac{2 \cdot E \cdot 10^4}{B_m \cdot J \cdot K_u} = 10.3cm^4$$

The selected core is an Epcos ETD54 ferrite core. The area product of that core is 11.5 cm^4, and can be calculated from the dimension data in the manufacturer's data sheet.

The number of turns required to get the desired inductance of the coil is calculated by Equation 44. The core cross-section, A_c = 172 mm^2, is obtained from the manufacturer's data sheet.

EQUATION 44:

$$N = \frac{L \cdot I_p}{A_c \cdot B_m} = 39.9$$

The calculated number of turns is the number for both windings. The number is rounded to the value of 40, so that both winding have an equal number of turns, which is 20.

To get the desired inductance, the A_L value is calculated by Equation 45.

EQUATION 45:

$$A_L = \frac{L}{N^2} = 156nH$$

Now, from the core manufacturer's data sheet the correct air gap can be selected. For the Epcos N87 material, the air gap length is calculated with Equation 46.

EQUATION 46:

$$s = \left(\frac{A_L}{k_1} \right)^{\frac{1}{k_2}} = 3.3mm$$

The gap is chosen from the data sheet to be 3.5 mm. The new A_L value must be calculated for the new air gap by Equation 47.

EQUATION 47:

$$A_L = K_1 \cdot s^{K_2} = 148nH$$

The new inductance value is shown in Equation 48.

EQUATION 48:

$$L = N^2 \cdot A_L = 237\mu H$$

The new operating flux density is verified by Equation 49 and must be lower than the saturation point of the selected material.

EQUATION 49:

$$B_{new} = \frac{L \cdot I_p}{N \cdot A_c} = 360mT$$

N27 material has a saturation point of 410 mT (100°C).

The cross section of the wire is calculated by Equation 50, where RMS current through the inductor is calculated from the output power and the RMS value of the output voltage.

EQUATION 50:

$$A_{cu} = \frac{I_{rms}}{J} = \frac{\frac{P_o}{230V}}{J} = 0.88mm^2$$

The calculated value is the minimum cross-section of a wire (100 kHz litz wire must be used).

Next, the fill factor has to be calculated by Equation 51. This will give an estimate if the windings will fit into the bobbin. The fill factor must be 0.4 or less. W_b is the bobbin winding area and is 315.6 mm^2. This information can be found in the core data sheet.

EQUATION 51:

$$K_u = \frac{N \cdot A_{cu}}{W_b} = 0.11$$

Output Capacitor Selection

The Inverter switching transistors produce the sinusoidal pulse width modulated voltage waveform that has a fundamental frequency of 50 Hz or 60 Hz. The low-pass filter comprises an output inductor and an output capacitor to pass only the low-frequency component (50 Hz or 60 Hz) of the sinusoidal pulse width modulated voltage waveform, in order to produce a low-frequency sinusoidal output voltage.

The value of the output capacitor must be large enough to pass the fundamental frequency and low enough so that it should need high reactive current. To get a cut-off frequency of ~100 Hz, the value of the output capacitor selected is 4.7 µF. The output capacitor should be able to take the high inductor ripple current as well as suppress the switching noise. The B32924C3475M MKP series film capacitor from Epcos fulfils all of the selected criteria.

Output Relays

Two relays are used in the system. Relay K1 is used to control charging of the DC link capacitors from the power grid. During operation this relay is always on. Relay K2 is used for switchover when the power grid fails. This relay must have a fast switchover time so additional components are used to reduce the switchover time. The R||C combination of R68 and C43 is used to allow high current at turn-on, and then reduce current during the ON state to allow for faster turn-off. Resistor R72 is used to deplete the energy stored in the relay coil for faster turn-off. Transistor Q11's switching speed is increased using R-C||R combination, which allows for a higher base current at turn-on and negative voltage on the base current at turn-off.

DESIGN OF GATE DRIVE CIRCUITRY

A half-bridge driver with fault- and short-circuit protection must be used to fulfill the design specification. The selected IGBT can withstand a short circuit of 10 µs. If the driver detects a short-circuit, it will perform a soft turn-off for the IGBTs. In addition, a bootstrap with a 600V floating channel is needed to drive the high-side IGBTs. To be able to meet the EMI requirements, the turn-on and turn-off slopes should be tunable with gate resistors. The IR2214 from International Rectifier meets all of these requirements. Looking at the data sheet of the IGBTs the allowed gate voltage is V_{GMAX} = ±20V and the gate threshold voltage is $V_{G(TH)}$ = 4.5-6.5V. The driver is supplied by V_{CC} = 12V to ensure IGBT turn-on. To ensure that the IGBT does not turn on due to internal IGBT Miller capacitance when VCE rises with high slope, gate to collector capacitors are used.

DESIGN OF VOLTAGE AND CURRENT FEEDBACK CIRCUITRY

For voltage feedback, differential amplifiers are used, which are built with the MCP6022 operational amplifier. To measure power grid and output voltage, bipolar measurements are needed. To enable the differential amplifiers to measure a bipolar signal voltage, an offset of $Voff$ = 2.5V is used as the positive reference point. Therefore, the operational amplifier gives 2.5V to its output when the differential measured voltage is zero. When the differential measured voltage is negative, the output goes to 0V and conversely, the output voltage goes to 5V when the measured differential voltage is positive.

Because of the high differential input voltage, a series of 1206 resistors were used to stay within the voltage and power rating of the devices. All of the resistors used were 1% tolerance to guarantee the exact measurement and reduce common mode noise rejection.

For current measurement, a Hall effect-based sensor from LEM is used. The sensor is bipolar and signal output is 0.5V. At zero current, the output is 2.5V.

For all of the 5V signals, a resistor divider was added near the dsPIC DSC to interface with the 3.3V 10-bit A/D converter. In addition, a capacitor was added near the dsPIC DSC to fast-charge the SH capacitor.

PCB LAYOUT CONSIDERATIONS

Traces leading the output current should be held as short as possible. Special care should be taken because of high voltage. Around the IGBT driver the logical level and gate drive components should be separated, and care should be taken to not couple the parts with ground planes.

THERMAL DESIGN

IGBTs must be placed on a heat sink to dissipate the produced heat. Total power dissipation is estimated as P_{IGBT} = 68W. The devices must be mounted on the heat sink using thermal conductive and electric insulating material.

Battery Charger Design

DESIGN SPECIFICATIONS FOR BATTERY CHARGER SPECIFICATIONS

A battery charger is used to charge the batteries from the power grid. Three series lead acid batteries were used in the system. The charger design specifications are:

- Input voltage: 95-260 VAC
- Output voltage: 30-45V
- Output current: 0-2.5A
- Current control
- Voltage limit

DESIGN OF POWER-TRAIN COMPONENTS

To realize the flyback converter primary drive stage, an integrated solution TOP250Y from Power Integrations was selected. Maximum output power is calculated as PCH = UBmax * IBmax - 112.5W . The flyback works with a switching frequency of f = 132 kHz. Therefore, a fast rectifier and primary clamp diode must be used. The transformer ratio is $N2 \div N1$ = 28 ÷ 52. Based on this ratio and the maximum input voltage, the rectifier reverse voltage rating should be higher than the result of Equation 66, where $V_{F(IGBTD)}$ is the voltage drop across the IGBT anti-parallel diode, which are used for power grid voltage rectification.

The clamping elements are designed using design tools from the manufacturer of the TOP250Y.

Flyback Transformer

The flyback transformer is designed to the desired output power and output current ripple, to enable current source operation. For the flyback converter, a transformer with air gap is needed. The transformer is designed for the following conditions:

- Minimum DC link voltage: V_{imin} = 130.6 V
- Maximum DC link voltage: V_{imax} = 364 V
- Nominal DC link voltage: V_{inom} = 247.4 V
- Nominal duty cycle: d_n = 0.24
- Output current: I_{o1max} = 2.5A
- Nominal output voltage: V_o = 40V
- Secondary current ripple: ΔI_s[%] < 25 %
- Switching frequency: f = 132 kHz

The primary to secondary turns ratio is calculated with Equation 52.

EQUATION 52:

$$N_{PS} = \left(\frac{V_{inom} - V_{DSon}}{V_O + V_{Df}}\right) \cdot \frac{d_n}{1 - d_n} = 1.9$$

To limit the current ripple, the inductance of primary and secondary windings must be calculated with Equation 53.

EQUATION 53:

$$L_S = \frac{(V_o + V_{Df}) \cdot (T - T_{ON\max})}{\Delta Is} = 196\mu H$$

$$L_P = L_S \cdot N_{PS}{}^2 = 684\mu H$$

Now, the primary current can be calculated with Equation 54, where transformer efficiency is estimated at 90%, and for secondary current with Equation 55.

EQUATION 54:

$$\Delta I_S = \frac{(V_O)\cdot(T - T_{on\max})}{L_S} = I_O \cdot \Delta I_S[\%] = 1A$$

$$I_{Sc} = \frac{I_O}{(1 - d_{\max})} = 4A$$

$$I_{Speek} = I_{Sc} + \frac{\Delta I_S}{2} = 4.5A$$

$$I_{S\,rms} = \sqrt{(1 - d_{\max})(I_{Speek}(I_{Sc} - \frac{\Delta I_S}{2}) + \frac{1}{3}(I_{Speek} - (I_{Sc} - \frac{\Delta I_S}{2}))^2} = 3.2A$$

EQUATION 55:

$$\Delta I_P = \frac{(V_{i\min})\cdot T_{on\max}}{L_P} = 0.55A$$

$$I_{Pc} = \frac{V_O \cdot I_O}{(V_{i\min})\cdot 0.9 \cdot d_{\max}} = 2.4A$$

$$I_{Ppeek} = I_{Pc} + \frac{\Delta I_P}{2} = 2.7A$$

$$I_{P\,rms} = \sqrt{d_{\max}(I_{Ppeek}(I_{Pc} - \frac{\Delta I_P}{2}) + \frac{1}{3}(I_{Ppeek} - (I_{Pc} - \frac{\Delta I_P}{2}))^2} = 1.5A$$

Now, the required wires for primary and secondary can be selected. We will design the flyback transformer to run a current density of J = 4 A/mm^2. Therefore, the required copper area for the primary and secondary can be calculated with Equation 56 (litz wire for 132 kHz must be used).

EQUATION 56:

$$A_{CuP} = \frac{I_{Prms}}{J} = 0.375mm^2$$

$$A_{CuS} = \frac{I_{Srms}}{J} = 0.8mm^2$$

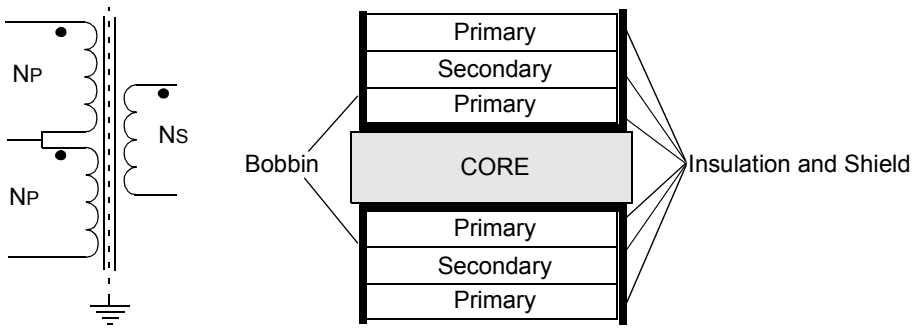
A winding factor of K = 0.2 is selected for the transformer and N87 material for the core. The maximum core flux density is set to B = 130 mT. To select the core, the area product has to be calculated with Equation 55.

EQUATION 57:

$$W_a A_c = \frac{100 \cdot P_{O\max}}{K_t \cdot 2B \cdot f \cdot J} = 0.65cm^4$$

The selected core needs to have a higher area product than what has been calculated. From the magnetics side, ETD34 and above will be sufficient; however, there needs to be enough space to fit the windings. For this in iterations for different cores, the number of turns and from this the window utilization and fill factor has to be calculated. If the window utilization is higher than 90% or a fill factor higher than 0.4, the windings will not fit. The transformer construction winding diagram and mechanical diagram are shown in Figure 50.

FIGURE 50: TRANSFORMER ELECTRICAL AND MECHANICAL CONSTRUCTION



For the windings, litz wire is used to grant low copper losses at high frequency. For switching frequency *f* = 132 kHz, a litz wire made of AWG38 wires is used to eliminate skin and proximity effect. The required number of parallel wires is calculated with Equation 58.

EQUATION 58:

$$n_{wP} = \frac{A_{CuP}}{A_{Cuw}} = 47.7$$

$$n_{wS} = \frac{A_{CuP}}{A_{Cuw}} = 101.8$$

For both, we have to select standard litz wires. So, for the primary, 45xAWG38 is selected and for the secondary, 105xAWG38 is selected. The diameter of selected wires with silk isolation is D_P = 1 mm and D_S = 1.5 mm.

For the used ETD39 core with an air gap, the required number of turns can now be calculated from the required primary inductance, turns ratio, and core data.

Primary turns are calculated with Equation 59.

EQUATION 59:

$$N_P = \frac{10^4 \cdot L_P \cdot I_{Ppeek}}{2B \cdot A_e} = 58.1 \rightarrow 58$$

$$N_S = \frac{N_P}{N_{PS}} = 30.5 \rightarrow 30$$

Now, the window utilization and fill factor can be calculated for the selected core and wires. The bobbin window is 25x7 mm. From this we can calculated how many turns for the primary and secondary (Equation 60) and the number of required layers (Equation 61).

EQUATION 60:

$$N_{tP} = \frac{25}{D_P} = 25 \rightarrow 25$$

$$N_{tS} = \frac{25}{D_S} = 16.7 \rightarrow 16$$

EQUATION 61:

$$N_{lP} = \frac{N_P}{N_{tP}} = 2.32 \rightarrow 3$$

$$N_{lS} = \frac{N_S}{N_{tS}} = \rightarrow 1.875 \rightarrow 2$$

The window utilization is shown in Equation 62 and fill factor in Equation 63.

EQUATION 62:

$$W_u = (D_P N_{lP} + D_S N_{lS}) / W_a = 86\%$$

EQUATION 63:

$$K_u = \left(A_{CuP} \cdot N_P + A_{CuS} \cdot N_S\right) / W_a = 0.25$$

According to this the windings fit to the selected core.

The required air gap can be calculated from the core data sheet. To calculate the required air gap the A_L value of the core has to be calculated. The A_L value is air gap dependent. From knowing the primary inductance and number of winding turns, the required A_L value can be calculated with Equation 64.

EQUATION 64:

$$A_L = \frac{L}{N^2} = 203.3nH$$

Now, from the core manufacturer data sheet, the correct air gap can be selected. For the used EPCOS ETD39 N87 core, the correct air gap is calculated with Equation 65.

EQUATION 65:

$$s = \left(\frac{A_L}{k_1} \right)^{\frac{1}{k_2}} = 0.95mm$$

The nearest standard air gap values are 0.7 mm and 1 mm. Our calculated value is close to 1 mm so we select an air gap of 1 mm and do not need to change the windings. If an air gap of 0.7 mm is selected, the number of winding turns must be corrected.

Battery Selection

The battery selection will depend on the DC voltage and the required backup time of the Offline UPS system. The Offline UPS Reference Design has been designed for 36V input DC voltage, being able to produce one hour of backup time with a 35 AH battery.

VOLTAGE, CURRENT AND TEMPERATURE SENSE CIRCUITRY

The battery charger works as a current source delivering the requested charge current to the battery, independent of battery voltage. For current measurement and control, a resistor and a high-side current shunt monitor (INA168 from Texas Instruments) were used. For current control, a discrete analog PI controller was built that controls the duty cycle of the TOP250Y. In addition, the measured current is fed through a differential amplifier stage to the dsPIC DSC device. Parallel to the current feedback loop, a voltage feedback loop is used to limit the output voltage in case the battery is not connected. In addition, a header is placed on the PCB to interface with a temperature sensor to monitor the battery temperature and allow battery management software to know the state of the batteries.

PCB LAYOUT CONSIDERATIONS

Precaution must be taken due to high voltage signals. Also the primary clamp components should be placed as near as possible to the transformer and the TOP250Y to reduce stress of the switching components. Care should also be taken to not couple the power, control, and measurement parts with ground planes.

THERMAL DESIGN

The top switch and rectifier diode must be mounted on a heat sink. Assuming efficiency of the battery charger to be 70%, nearly 50W of loss will be dissipated. Those losses consist of clamp losses, transformer losses, primary switch (TOP250Y), and rectifier losses. Therefore, we can estimate that near 30W of losses need to be dissipated on the heat sink. Both elements TOP250Y and the rectifier diode must be mounted on the heat sink using thermal conductive electrical insulating material.

EQUATION 66:

$$V_{BR(rect)} = V_{in} \cdot \sqrt{2} \cdot \frac{N_2}{N_1} + V_{bat} - 2 \cdot V_{F(IGBTD)} = 260 \cdot \sqrt{2} \cdot \frac{28}{52} + 45 - 2 \cdot 1.3 = 240.4V$$

Design of Auxiliary Power Supply

DESIGN SPECIFICATIONS

The auxiliary power supply provides power, which is taken from the battery link, to all of the on-board electronics. The design specifications are:

- Input voltage: 30V-45V
- Output: 150 mA @ 3.3V, 300 mA @ 5V, 500 mA @ 12V

CHOICE OF COMPONENTS

Because of a wide range of input voltage and power losses, a buck converter was used to generate 12V from the battery voltage. For 3.3V and 5V, linear regulators are used because of simplicity and price. All the voltage regulators are connected in series so the 12V buck converter needs to deliver 1A of current. For the buck converter, an LM5575 from National Semiconductor was used with the switching frequency set at f = 500 kHz. Components were selected according to the LM5575 data sheet. For the linear voltage regulators, power dissipation must be calculated to select the right package in the PCB layout. For the 5V regulator, maximum power dissipation is calculated to P_{5V} = (V_{IN} - V_{OUT}) * I_{OUT} = 3.15 mW and for 3.3V to P_{5V} = (V_{IN} - V_{OUT}) * I_{OUT} = 255 mW. For the 5V regulator, a (KE7805ER) TO-263 package with a PCB mount heat sink was selected, and for the 3.3V regulator, a (TC1262) SOT223 package was selected. For the analog circuits, additional chip inductors and capacitors were added to separate digital and analog supply voltages.

The auxiliary power supply will start when DC link voltage is present or when the button is pressed.

PCB LAYOUT CONSIDERATIONS

For the buck converter, due to very high frequency current, care should be taken when designing the output traces. The inductor, Schottky diode, and low-ESR output capacitors should be as close as possible to the IC. Also input capacitors should be placed close to the IC to block the noise produced by the buck converter.

For linear regulators, adequate PCB and copper area must be provided to keep the devices cool.

CONCLUSION

The Microchip dsPIC DSC device provides all of the necessary power peripherals used for power conversion applications. It's highly flexible Intelligent Power Peripheral (IPP), ADC, Comparator, and PWM modules simplify the hardware schematic and reduces the number of components in the design of a high-performance UPS system. The built-in DSP engine and IPP help in optimizing control loop design, being able to produce a clean sine wave output (THD less than 3%) even with a rectifier load and a crest factor of 3:1.

With the help of optimized instruction sets, like MAC, there is enough time left to perform all of the auxiliary tasks, fault protection, housekeeping, and communication with the external world. The dsPIC33F enables power conversion design with all advance features within the target price.

REFERENCES

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- *"TC1262 500mA Fixed Output CMOS LDO"* (DS21372), Microchip Technology Inc.
- *"Power Electronics Converter, Applications and Design"* by N.Mohan, T.M. Undeland, and W.P. Robbins
- *"Control Topology Options for Single-Phase UPS Inverter"* by M.J Ryan, W.E. Brumsickle, and R.D. Lorenz, IEEE transaction on industry application, Vol. 33, No. 2, March/April 1997.
- *"A Current Mode Control Technique with Instantaneous Inductor Current Feedback for UPS Inverter"* by H.Wu, D.Lin, D. Zhang, K. Yao, J.Zhang, IEEE transaction, 1999.
- *"A High Performance Sine Wave Inverter Controller with Capacitor Current Feedback and Back-EMF coupling"* by M.J Ryan and R.D. Lorenz, IEEE transaction, 1995.

NOTES:

APPENDIX A: SOURCE CODE

Software License Agreement

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All of the software covered in this application note is available as a single WinZip archive file. This archive can be downloaded from the Microchip corporate Web site at:

www.microchip.com

APPENDIX B: CONTROL SYSTEM DESIGN

The Offline UPS Reference Design implements full digital control of the push-pull converter and full-bridge inverter. MATLAB® was used to design the compensators based on the hardware and to generate optimal coefficients to be used in the software.

MATLAB SIMULINK

The simulation files contain the models for various subsystems. Some subsystems are presented as nested blocks to simplify the main diagram. Simulink® provides mathematical blocks for the time domain simulations.

There are typically two models in each file.

- Analog implementation
- Digital implementation

Each SIM file analog implementation typically consists of the following sections:

- Reference Block
- Feedback System Block
- Power System Block
- Control System Block
- Modulation Inverse Block
- Modulation Block
- Load System Block
- Special Blocks

The Simulink blocks will vary based on the converter topology and control scheme implemented (i.e., current mode, voltage mode). The following sections describe each block used within the models.

REFERENCE BLOCK

This system provides the input for the control system. Typically, it is only a DC constant for DC-DC converters or a sine wave generator for UPS-type models. The control system is required to track the reference waveform. This block may or may not be labeled as such in the actual models.

FEEDBACK SYSTEM BLOCK

Various signals are typically measured in a system. These include the voltages and currents for performing the control operations.

In digital implementation, additional blocks may be needed to account for quantization due to the presence of an ADC and zero order holds for sampling the signal at a constant frequency.

POWER SYSTEM BLOCK

This is the actual physical system. This system represents energy states and is what actually gives the output to be controlled. Typically, it will consist of an L-C circuit. The system implementation of L and C is based on integrators and saturations. The input is typically voltage given by the modulation block (conversion of duty ratio to actual excitation voltage). Depending on the topology, the power system block will change. Parasitic components such as capacitor ESR and inductor DCR are included in the system here. In addition, loading of the system will be accounted here.

CONTROL SYSTEM BLOCK

This block generates the duty ratio that drives the power section block. The feedback signals from the feedback block is the input and the output as a number between 0 and 1, which represents the duty cycle ratio.

This block may consist of various cascaded PID loops based on the control scheme (voltage mode or current mode control). In digital implementation integrators and differentiators are replaced by their digital equivalents.

MODULATION INVERSE BLOCK

This block may be part of the control system block as it converts the output of the PID loops from voltage and current quantities to duty ratio quantities between 0 and 1. Different topologies have different implementations. Typically, it involves division with a voltage quantity (e.g., input voltage for buck converter and output voltage for boost converter). It is just the inverse operation of modulation performed by the physical system in converting duty ratio into voltage.

These models typically have a division with a voltage quantity (divisor) with little variation. Sometimes in software these routines are not implemented, but in an actual system, the quantity is assumed to be constant and gains are prescaled appropriately.

MODULATION BLOCK

This block represents the average model of the switching system. This block converts the duty applied to physical system to voltage quantity. Its input is the duty cycle ratio /parameter (0 to 1) that gets converted to voltage quantity. It usually takes the system input voltage and duty cycle as input and generates an output voltage.

LOAD SYSTEM BLOCK

This block is used to generate different types of load current. For example, a step load with DC offset can be created, which is useful for step loading. Sinusoidal loads for UPS-type systems with variable phase (inductive, resistive, etc.), amplitude, and frequency can also be used depending on the choice of test conditions.

SPECIAL BLOCKS

Second order effects like saturation of inductor and dead-time are modeled for systems where these become important like UPS. These are indicated by saturation and dead-time blocks.

MATLAB .m File

The .m file is used to generate the coefficients that are used in the MATLAB model (.mdl). It also generates the scaled values to be used in the software. The generated values are in fractional format. In software they must be represented as Q15(x), where x is a fractional value.

The following parameters are typically used:

- The input voltage
- L (equivalent inductor value)
- C (equivalent capacitor value)
- ESR (capacitor ESR)
- LSR (lumped series resistance includes tracks + switch + cable resistance, etc.)

Based on the topology used, these parameters can vary from the actual values. For example, if three converters are in parallel, then simulation is performed for a single converter (instead of (3x) the capacitor value, only a single capacitor is modeled and the inductor value will remain the same).

The input voltage may vary especially when transformers are involved. Typically, all quantities are then referenced to primary or secondary based on convenience. In either case, the input voltage will vary.

Depending on implementation, input voltage may be assumed constant and lumped together with some of the gains.

Bode plots are generated by the .m file for a graphical representation. The following are typical plots:

- Loop gain plot (A x β) – this is used to determine phase and gain margin
- Closed loop plot (A x β) / (1 + A x β) or Vo / Vo* – used to determine the closed loop response and bandwidth of the system
- Disturbance rejection plot Io(s) / Vo(s) – used to determine the stiffness of the system and expected amount of voltage ripple when a load is applied as a function of frequency

Push-Pull Compensator

For the push-pull converter, a PID control algorithm has been implemented using voltage mode control. This means that the output voltage is measured and compared to a reference set point. The difference is then passed through the PID compensator. The PID control algorithm will look at the error, the previous error, and the control history to determine the output value. The output of the PID will determine the ON time for the PWM duty cycle. Figure B-1 provides a push-pull converter control scheme.

FIGURE B-1: PUSH-PULL CONTROL SCHEME

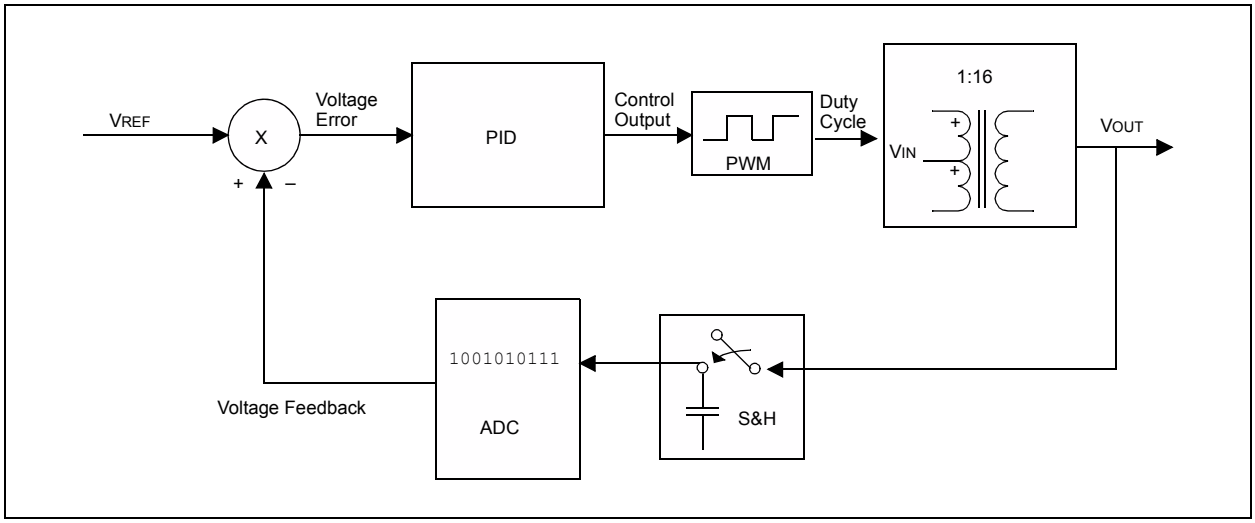
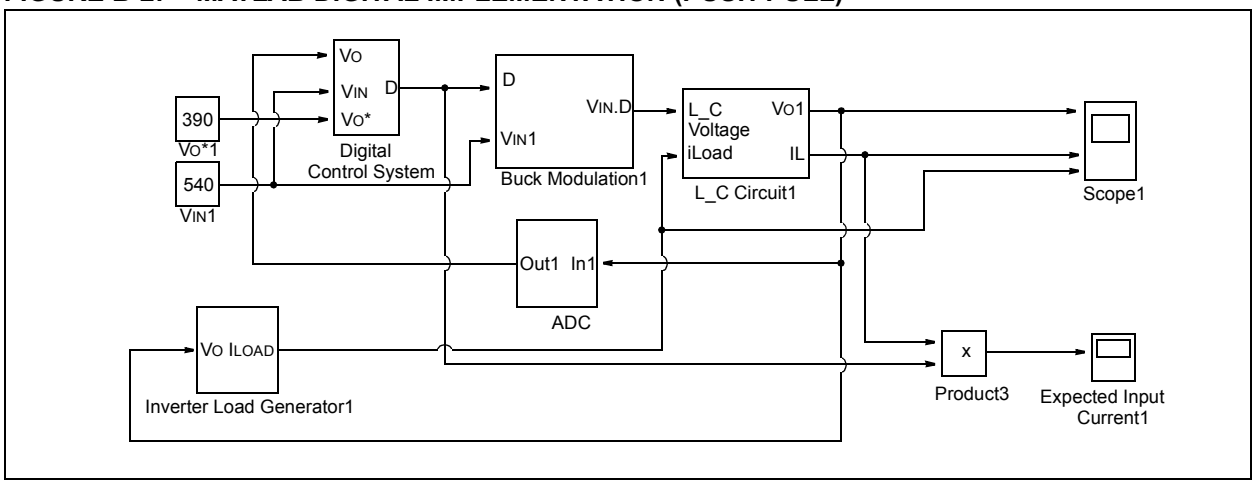


Figure B-2 shows the MATLAB Simulink block diagram. For further details of each block refer to the MATLAB (`.mdl`) file.

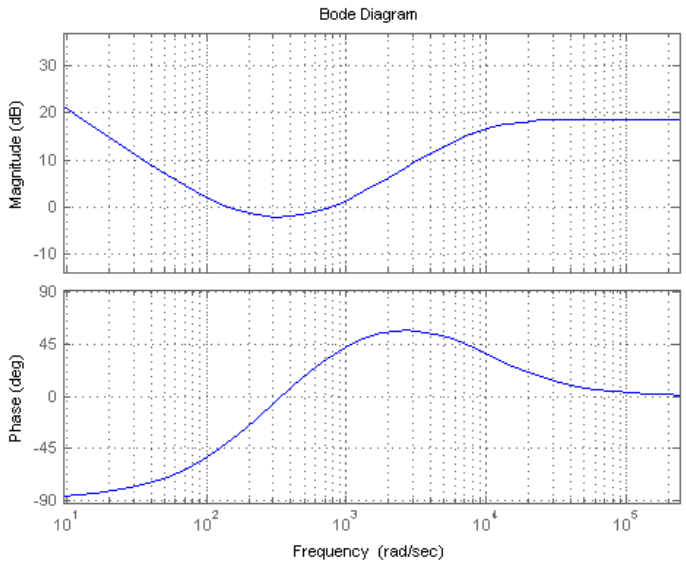
FIGURE B-2: MATLAB DIGITAL IMPLEMENTATION (PUSH-PULL)



The following bode plots are generated from the MATLAB (`.m`) file. Each plot is used to describe the behavior of the system. The disturbance rejection plot is defined as: I(s) / VO(s).

Figure B-3 describes the amount of load current amplitude needed to be applied to generate one unit voltage sag as a function of frequency. The higher this absolute figure of merit, the stiffer (better) the power supply will be. The minimum is -4 db, which will correlate to a 1A load producing 1.5V dip on the output.

FIGURE B-3: DISTURBANCE REJECTION PLOT (PUSH-PULL)



The loop gain voltage plot shown in Figure B-4 is used to find phase and gain margin. From the plot it can be seen that the phase margin (difference between 180 degrees and the phase angle where the gain curve crosses 0 db) is 90 degrees.

To prevent the system from being conditionally unstable, it is imperative that the gain plot drops below 0 db when the phase hits 180 degrees.

The blue curve is for the analog implementation and the green curve is for the digital implementation. It is generally recommended to have a phase margin of at least 40 degrees to allow for parameter variations.

The gain margin is the difference between gain curve at 0 db and where the phase curve hits 180 degrees. The gain margin (where the green line on the phase plot hits 180 degrees) is -20 db.

FIGURE B-4: LOOP GAIN VOLTAGE PLOT (PUSH-PULL)

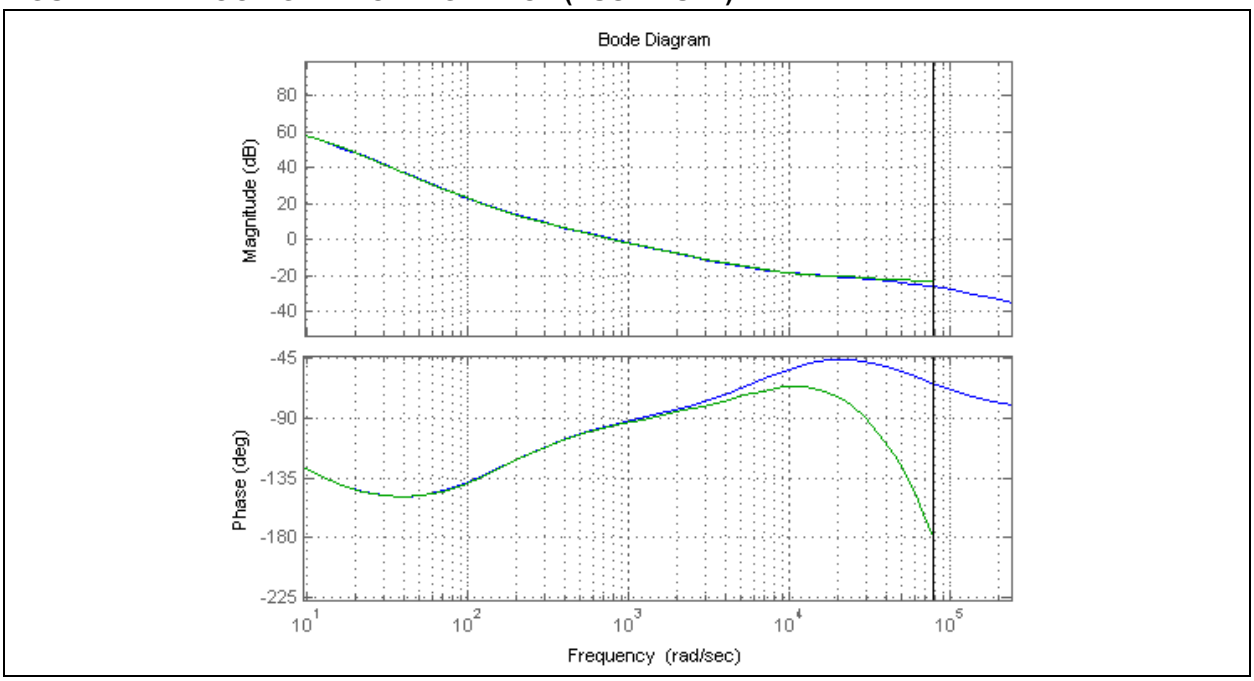
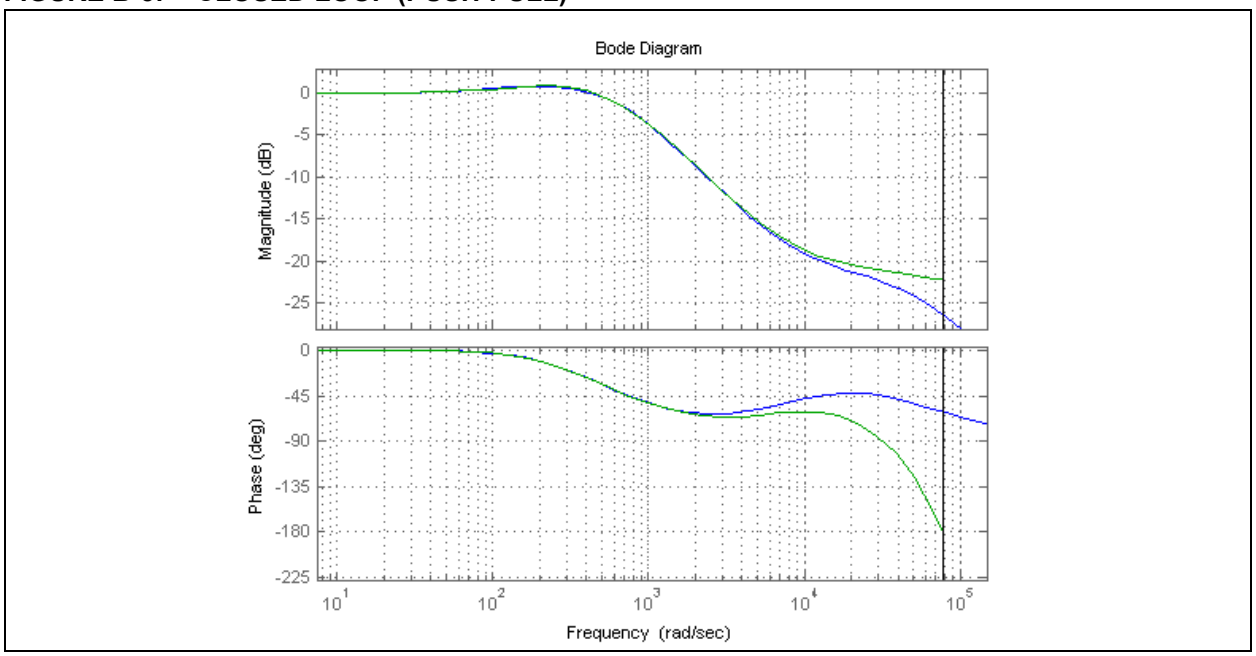


Figure B-5 shows the closed loop bode plot. The point where the gain crosses -3 db or -45 degrees in phase is usually denoted as the bandwidth. In this system, the bandwidth of the voltage loop is approximately 1250 Hz (8000 rad/s), which is closely matched by the bode plot.

FIGURE B-5: CLOSED LOOP (PUSH-PULL)



Full-Bridge Inverter Compensator

Current mode control has been implemented for the Inverter using two control algorithms: PI and P.

In current mode control, the current as well as the voltage is measured. The inverter output is generated by varying the input voltage reference using a sinusoidal lookup table. The difference is passed through the voltage error compensator (PI) and the output is the current reference value. The measured current value is subtracted from the reference and the difference is passed to the current error compensator (P). The output of the compensator is used to control the PWM outputs. Current mode control is the preferred method as it has better transient response and stability of the output. However, current mode control is usually harder to implement as there are two control algorithms instead of just one as in voltage mode control.

FIGURE B-6: FULL-BRIDGE INVERTER CONTROL SCHEME

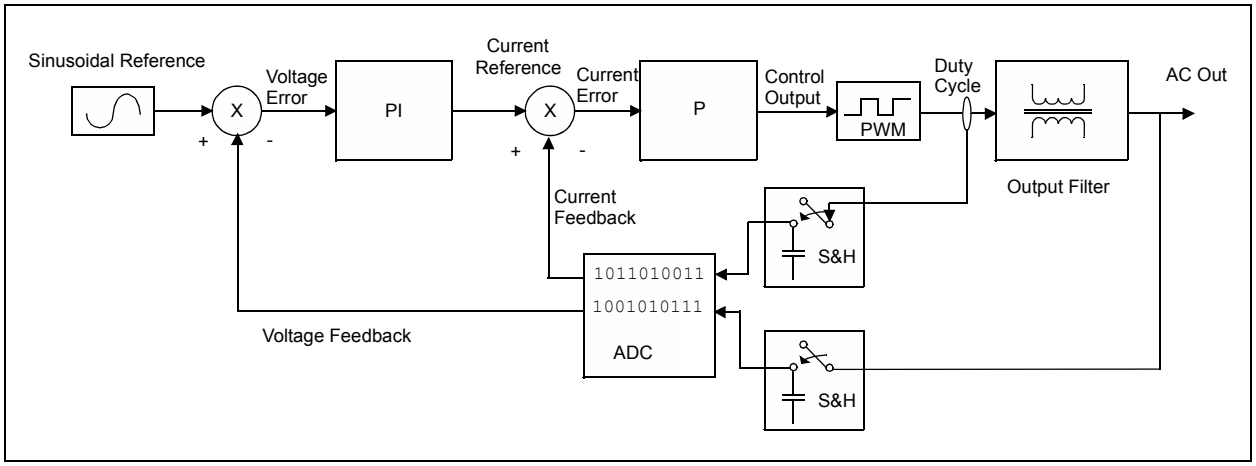
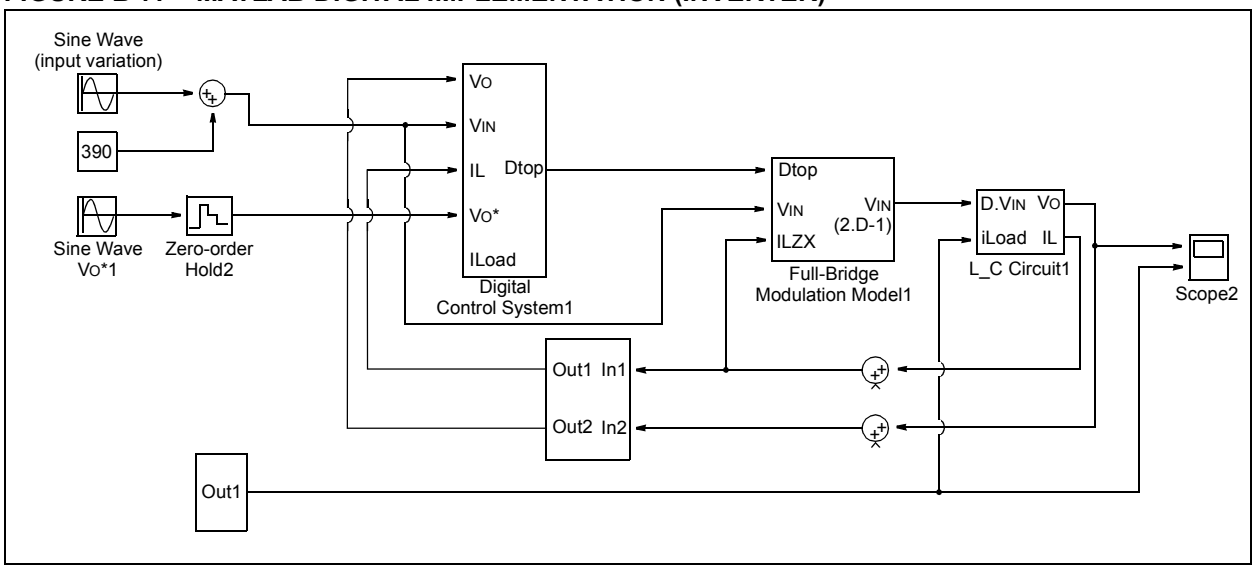


Figure B-7 shows the MATLAB Simulink block diagram for the inverter. For further details of each block, refer to the MATLAB (`.mdl`) file.

FIGURE B-7: MATLAB DIGITAL IMPLEMENTATION (INVERTER)



The disturbance rejection plot as previously described in the Push-Pull section is defined as: I(s) / Vo(s).

For the inverter, the minimum is -30 db, which implies that for 1A load amplitude @ 1000 Hz (6280 rad/s), the output voltage will exhibit a sinusoidal variation of 31V.

FIGURE B-8: DISTURBANCE REJECTION PLOT (INVERTER)

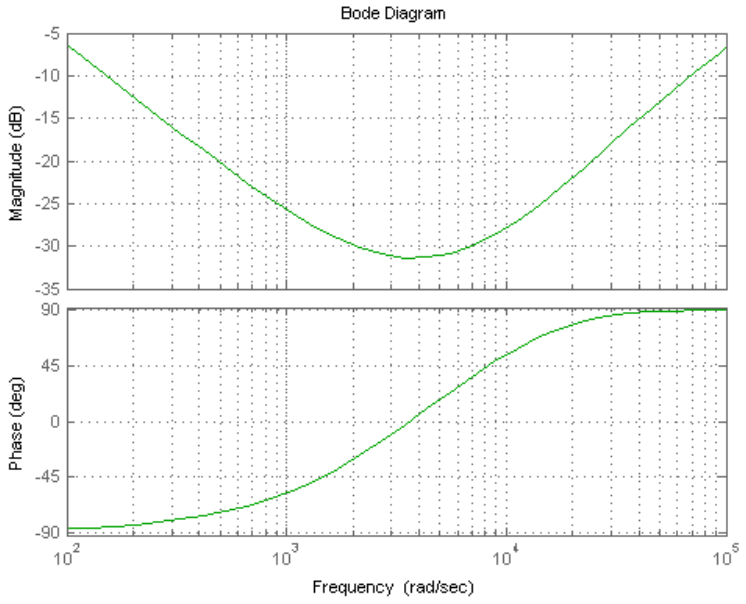


Figure B-9 shows the loop gain bode plot for the inverter. From the plot, it can be seen that the phase margin (difference between 180 degrees and the phase angle where the gain curve crosses 0 db) is 47 degrees.

The gain margin is the difference between the gain curve at 0 db, and where the phase curve hits 180 degrees. In the plots below, the gain margin (where the green line on the phase plot hits 180 degrees) is -10 db.

Figure B-10 shows the closed loop bode plot for the inverter. The point where the gain crosses -3 db or -45 degrees in phase is usually denoted as the bandwidth. In this system, the bandwidth of voltage loop is 1250 Hz (8000 rad/s), which is closely matched by the bode plots.

FIGURE B-9: FIGURE: LOOP GAIN VOLTAGE PLOT (INVERTER)

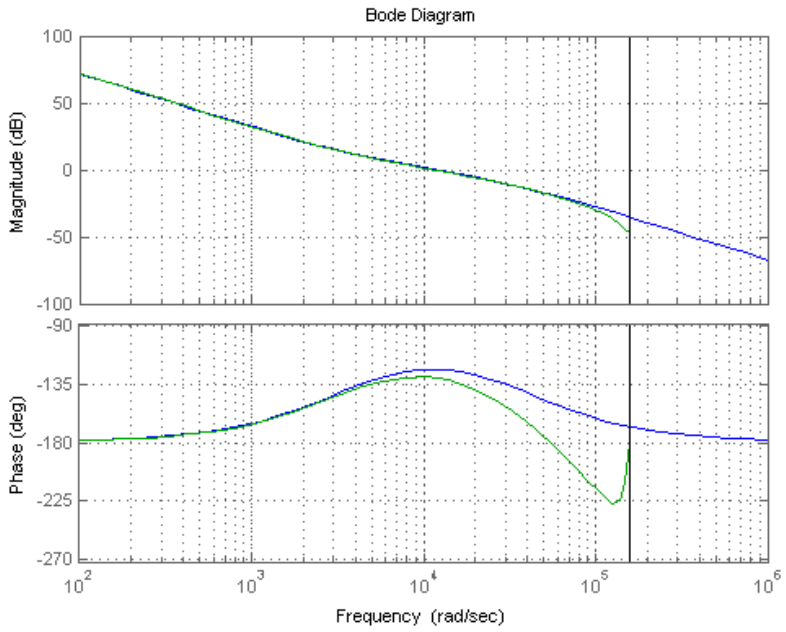
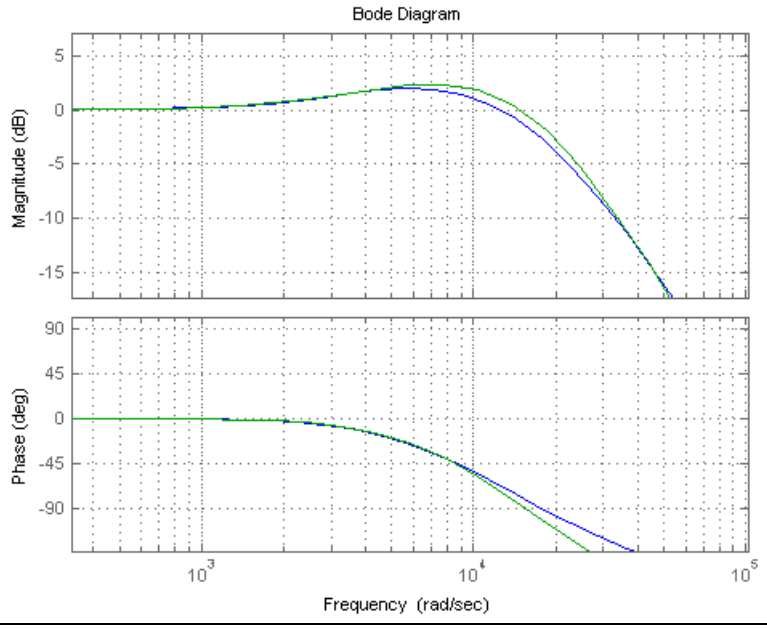


FIGURE B-10: FIGURE: CLOSED LOOP (INVERTER)



Scaling

The gains calculated from MATLAB are based on real units (volts, amps, etc.). The dsPIC DSC has a fixed point processor and the values in the processor have a linear relationship with the actual physical quantities they represent.

The gains generated by MATLAB being in real units, cannot be directly applied to these scaled values (representation of physical quantities). Therefore, for consistency, these gains themselves need to be scaled. The following sections present general concepts behind proper scaling.

The basic idea behind scaling is quantities that need to be added or subtracted should be of the same scale.

Scaling does not affect the structure of the control system block diagram in any way. Scaling only effects the software representation of various quantities.

SCALING FEEDBACK

To properly scale the PID gains, it is imperative to understand the feedback gain calculation. The feedback can be represented in various formats. Fractional format (Q15) is a very convenient representation.

Fractional format allows easy migration of code from one design to another with completely different ratings with most changes only in the coefficients defined in the header file.

To completely use the 16 bits available in the processor, the Q15 format is most convenient as it allows signed operations and full utilization of the available bits (maximum resolution). Other formats are also possible, but resolution is lost in the process. Q15 allows us to use the fractional multiply MAC operation of the dsPIC DSC effectively.

The feedback signal (typically voltage or current) is usually from a 10-bit ADC. Based on the potential divider/amplifier in the feedback circuitry, actual voltage and currents are scaled.

Typically, the feedback 10-bit value (0 -1023) is brought to +/- 32767 range by multiplying by 32. This format is also known as Q15 format: Q15(m) where -1 < m < 1 and is defined as (int) (m * 32767).

These formulas will have some error as we need 2^15 = 32768, but due to finite resolution of 15 bits we use only +/- 32767. From a control perspective, for most systems these hardly introduce any significant error.

In this format, +32767 corresponds to +3.3V and 0 corresponds to 0V.

The feedback circuitry and the left shift by 5 (x32) is effectively taking the physical quantity and dividing it by a larger base quantity. The fractional value is then represented as Q15 in software. Our goal is to find that larger base quantity.

As an example, we are trying to measure 100V. We have a potential divider such that 100V would give 1.65V on the analog pin. Then, the value read in Q15 format is 16383 or Q15(0.5), which is equivalent to Q15(100 / 200). Therefore, 200 becomes the base voltage.

The base (or normalizer) is denoted as VN. In other words, VN is the voltage that will produce 3.3V or full-range voltage on the analog ADC pin.

At this point, voltage has been scaled as a fraction (V / VN) in software.

Similarly, other physical quantities that are read via ADC feedback are also represented in Q15 format.

GAIN SCALING

In simulation the control gains are calculated in real units. For example, in current mode control, the output of voltage loop is the current reference (in amps). Therefore, the gain is Amps/Volts or in units of 1/ohms: V → Gain → I_{REF}

The goal is to obtain I_{REF} in an appropriate format like Q15(I/IN) to enable implementation of the current loop in software.

In theory, the Q15 voltage V/VN is first multiplied by VN, and then gain (G), and then the I_{REF} that is obtained is divided by IN to get current in the correct format. Since VN and IN are constants, the gain G is scaled as: G * VN / IN. This value can be used in software to act on voltage quantity and give out a current quantity.

The input quantity should be in fractional format (this has to be ensured in code). Then, the output current quantity will automatically be in the correct fractional quantity. This essentially solves the objective of scaling. The same logic applies to any control block.

By considering the input and output units and scale of each block to be implemented in software, the proper scaled values can be arrived at.

SAMPLING TIME

In calculation of the derivative and integral term in the discrete time domain, T_S (sampling time) factors show up. Since sampling time is usually constant, it can also be lumped together with the gains. For example, if G_S is the integral gain in real units, G_S * T_S * VN / IN is the scaled value.

PRESCALER

As most physical quantities are represented as Q15 format for easy multiplication with gains, the gains also need to be in fractional format. If the value of gain (G * VN / IN) is between -1 and +1, it can be easily represented as fractional format.

Multiplications can then be performed using fractional multiply functions like MAC or using `builtin_mul` functions and shifting appropriately. For example, z = (`__builtin_mulss`(x,y) >> 15) results in z = Q15(fx,fy), where all x, y, and z are in Q15 format (fx and fy are the fractions that are represented by x and y).

In many instances, the gain terms are greater than unity. Since 16-bit fixed point is a limitation, a prescaler may be used to bring the gain term within the +/- range. For example, if the value that needs to be used is 2.5, it is predivided by 4 to bring it within ±1 range.

If a prescaler is used for P term in a control block, it also must be used for the I and D term in the control block as all of the terms get added together.

To prevent number overflows, PID output and I output individually have to be properly saturated to ±32767. The saturation limits for the PID output must be set at one-fourth of the original ±32767 to account for the prescaler. Therefore, they are set at ±8192.

Finally after saturation, the output has to be postscaled by 4 to bring it to proper scale again.

Modulation and Duty Generation

The output of a control system after saturation is brought to 0-32767. Based on the topology, this can be interpreted as a duty ratio/modulation index representing 0-1. This can then be used to convert to a duty cycle value by multiplying it with the PWM period. This varies with topology, but the idea behind scaling is the same.

Again, the following equation can be used where PERIOD corresponds to 100% duty :

Duty = (`__builtin_mulss`(m, PERIOD) >> 15)

Division By VIN

The output of the controller in the MATLAB model is usually a voltage quantity. This needs to be converted to a duty/modulation quantity. To do this, the control output needs to be divided by the input voltage VIN. To avoid division, VIN can be assumed to be constant and 1/VIN can be used as a constant multiplier and bundled along with the gains in the previous blocks.

APPENDIX C: ELECTRICAL SPECIFICATIONS

This Appendix provides an overview of the UPS electrical specifications as well as scope plots from initial test results.

TABLE C-1: OFFLINE UPS REFERENCE DESIGN ELECTRICAL SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Comments
V_{IN}	Input Voltage	210	220	242	V	
f_{IN}	Input Frequency	47	50	53	Hz	
V_{OUT}	Output Voltage		220		V	
f_{OUT}	Output Frequency	49	50	51	Hz	
$V_{BATTERY}$	Battery Input Voltage	34	36	45	V	
P_{OUT}	Continuous Output Power	—	—	1000	VA	
OLP	Over Load Protection	>100	—	135	%	1350 VA for 2 seconds
THD	Output Voltage THD	—	—	3	%	Full load (resistive)
η	Battery Charger Mode System Efficiency	—	84	—	%	
	Inverter Mode System Efficiency	—	—	84	%	>50% load
$t_{TRANSFER}$	Mains to Inverter Transfer Time	—	—	10	ms	
	Inverter to Mains Transfer Time	—	0	—	ms	
I_{CHARGE}	Battery Charge Current	—	2	2.5	A	
$I\_{BATTERY}$	Battery Input Current (note 1)	—	—	40	A	@ 100% load
T	Operating Temperature	—	25	—	°C	
CF	Crest Factor	—	—	3:1	—	
PF	Power Factor (Inductive Load)	.65	—	—	—	Only tested at .8 PF
	Power Factor (Rectifier Load)	.65	—	—	—	

Note 1: UPS run time will vary with output load current and the batteries discharge rate. Refer to the battery data sheet for specific discharge times.

FIGURE C-1: EFFICIENCY CHART ACROSS LOAD SPECTRUM

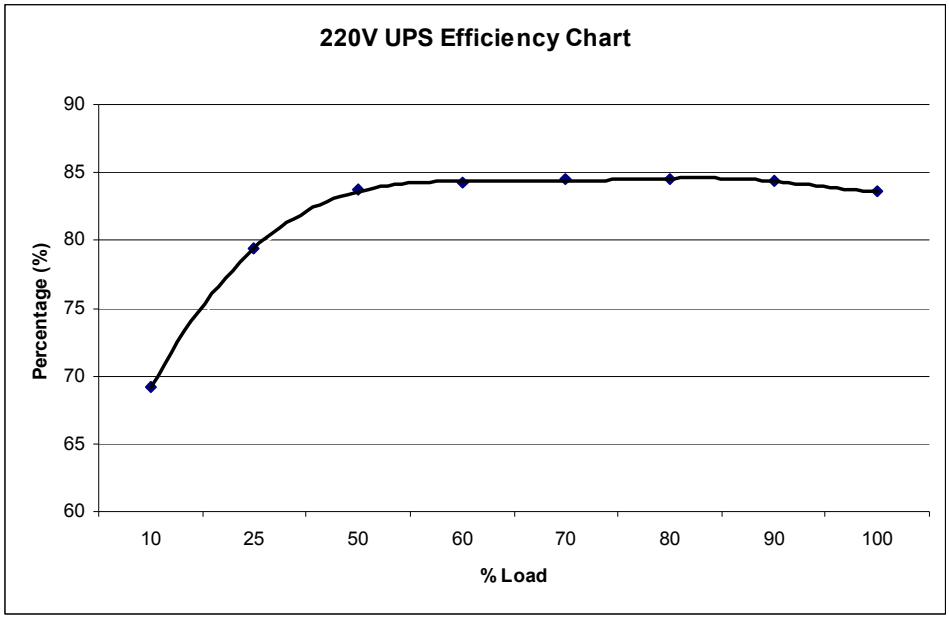


FIGURE C-2: OUTPUT VOLTAGE WAVEFORM – NO LOAD

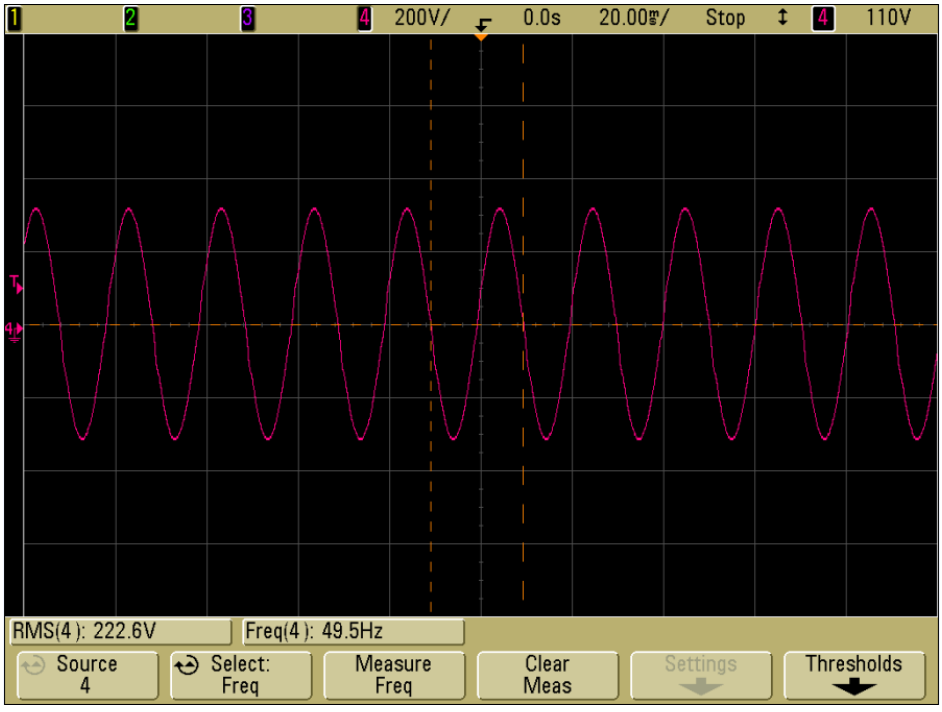


FIGURE C-3: OUTPUT VOLTAGE AND OUTPUT CURRENT – FULL LOAD

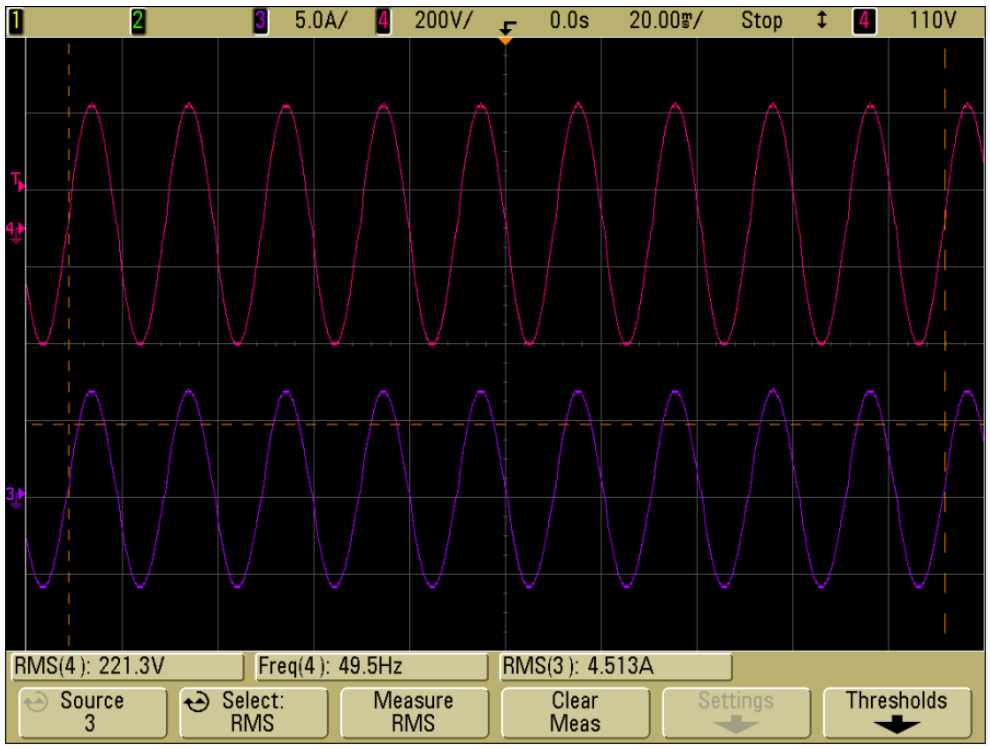


FIGURE C-4: OUTPUT VOLTAGE AND OUTPUT CURRENT – 500 VA REACTIVE LOAD

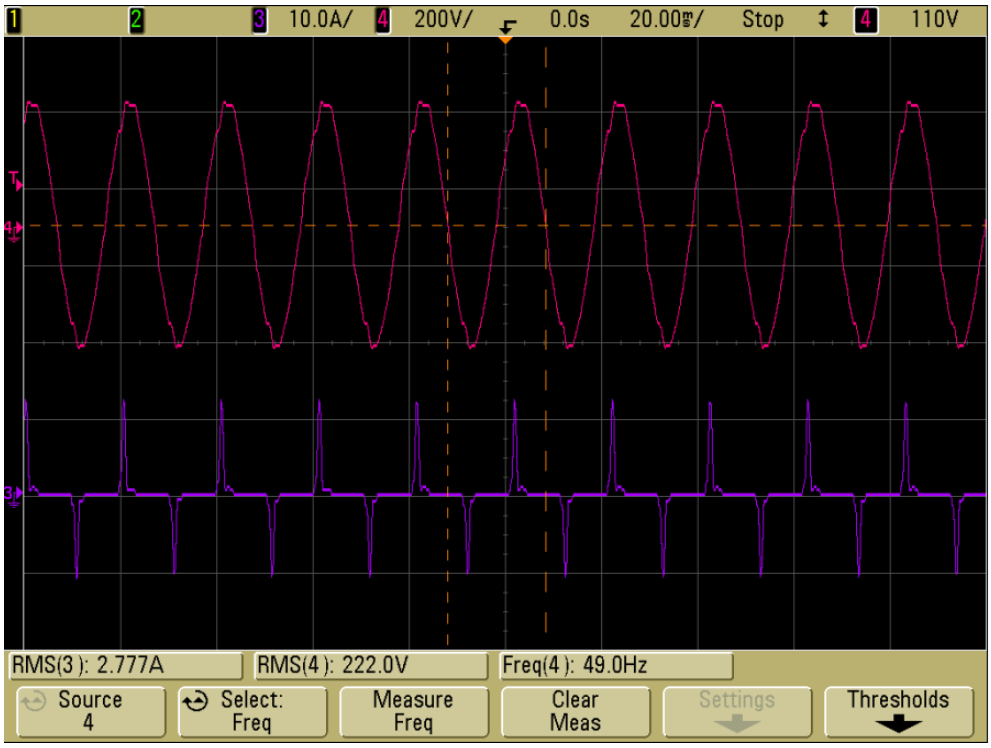


FIGURE C-5: MAINS TO INVERTER SWITCH OVER – 400W LOAD

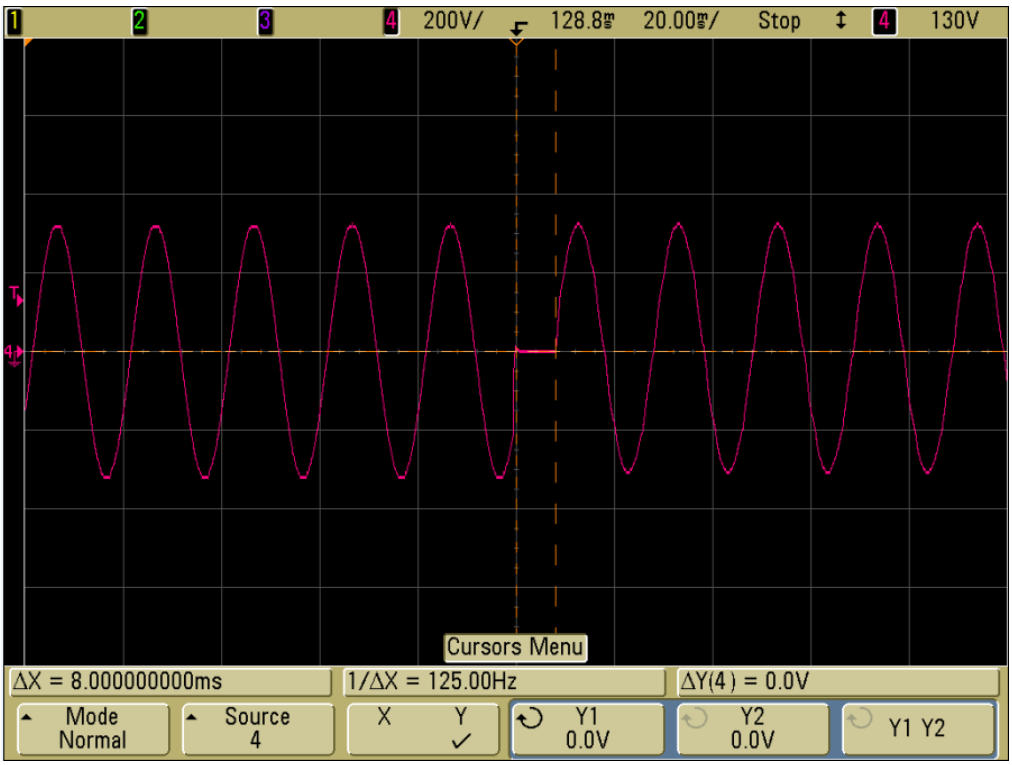


FIGURE C-6: INVERTER TO MAINS SWITCH OVER – 400W LOAD

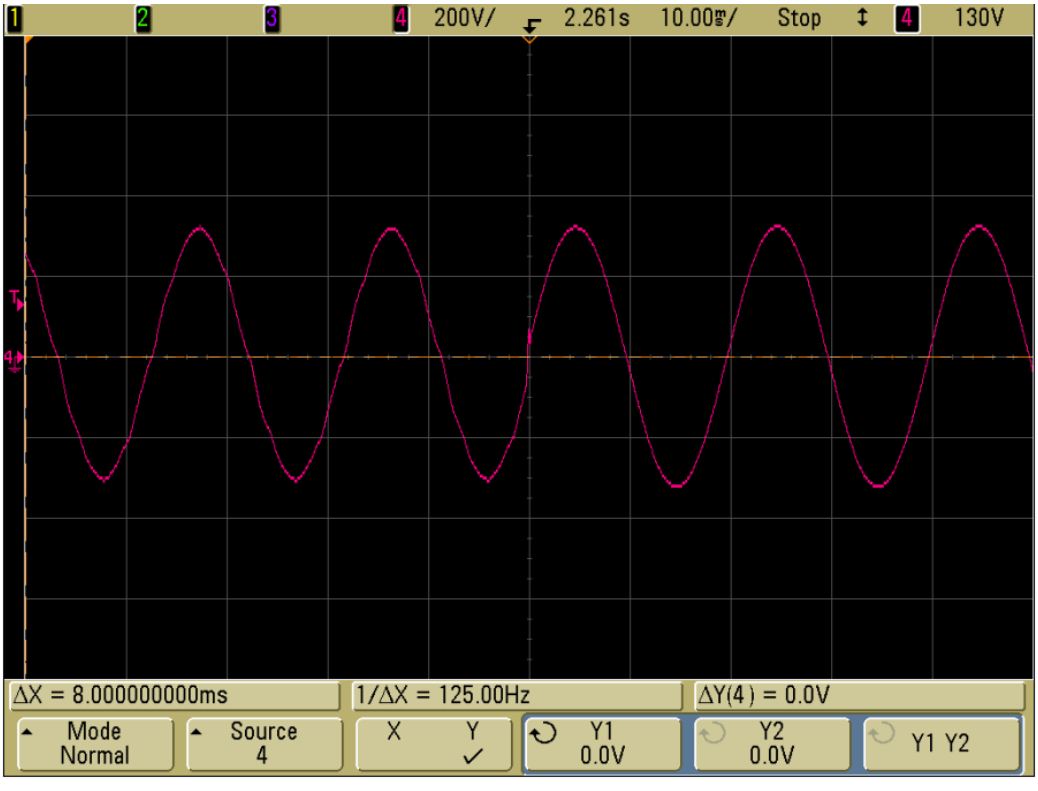


FIGURE C-7: DYNAMIC LOAD RESPONSE – 400W UNLOAD

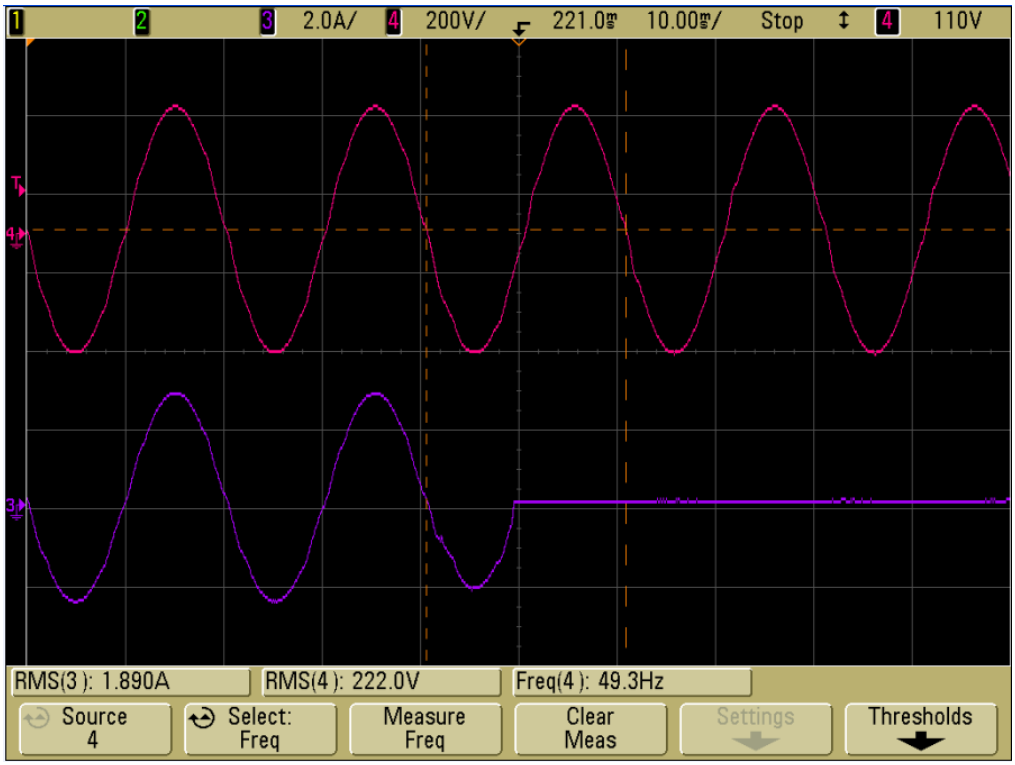
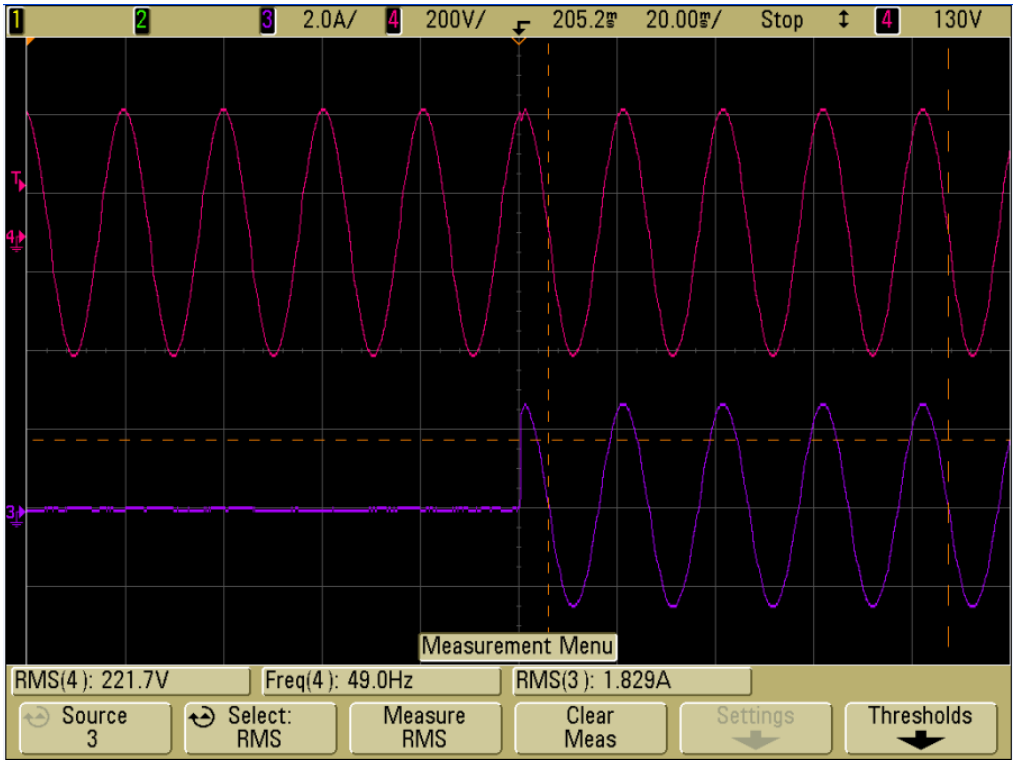


FIGURE C-8: DYNAMIC LOAD RESPONSE – 400W LOAD STEP



APPENDIX D: SCHEMATICS AND BOARD LAYOUT

FIGURE D-1: OFFLINE UPS REFERENCE DESIGN BOARD LAYOUT (TOP)

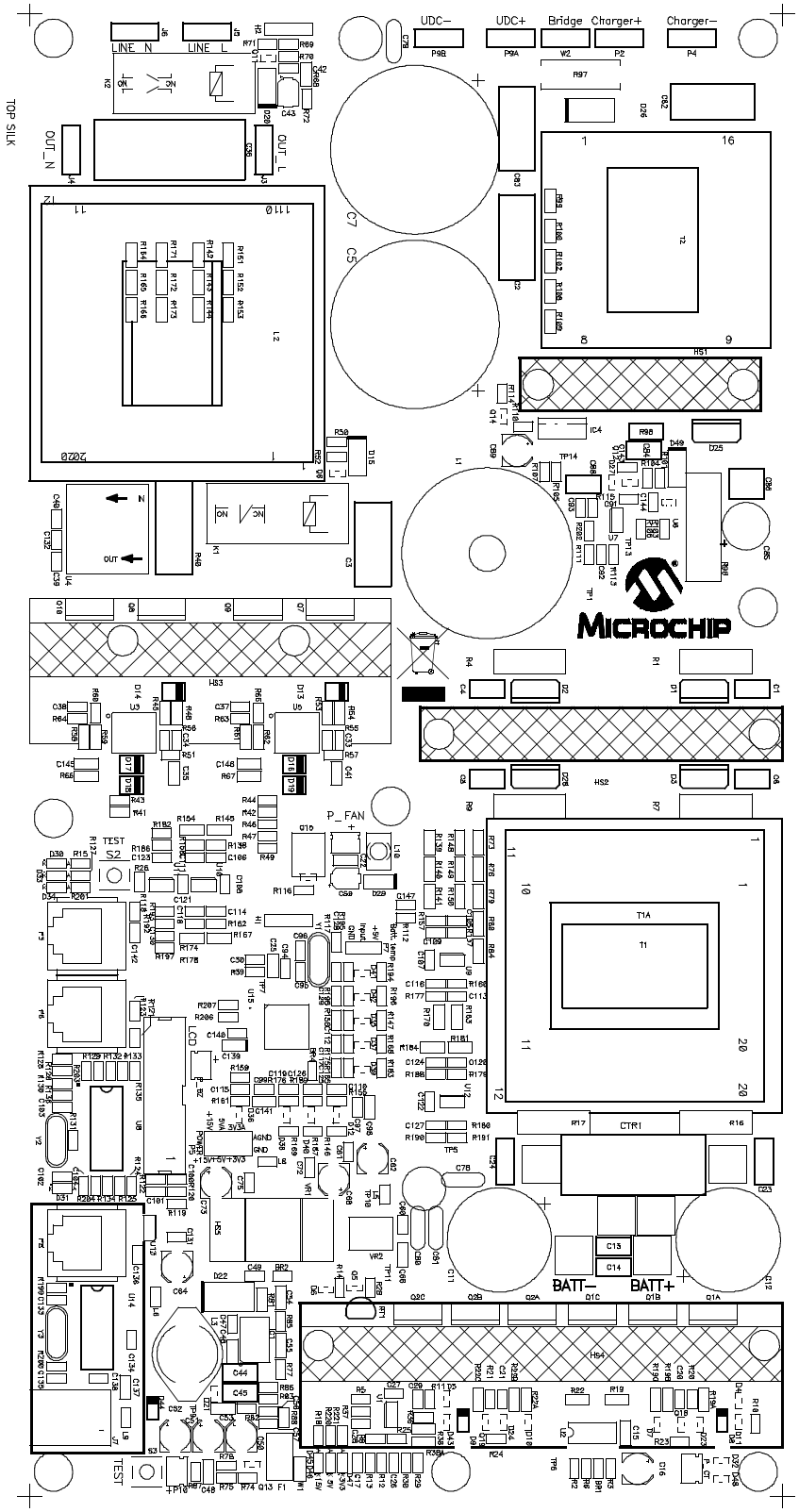


FIGURE D-2: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 1 OF 8)

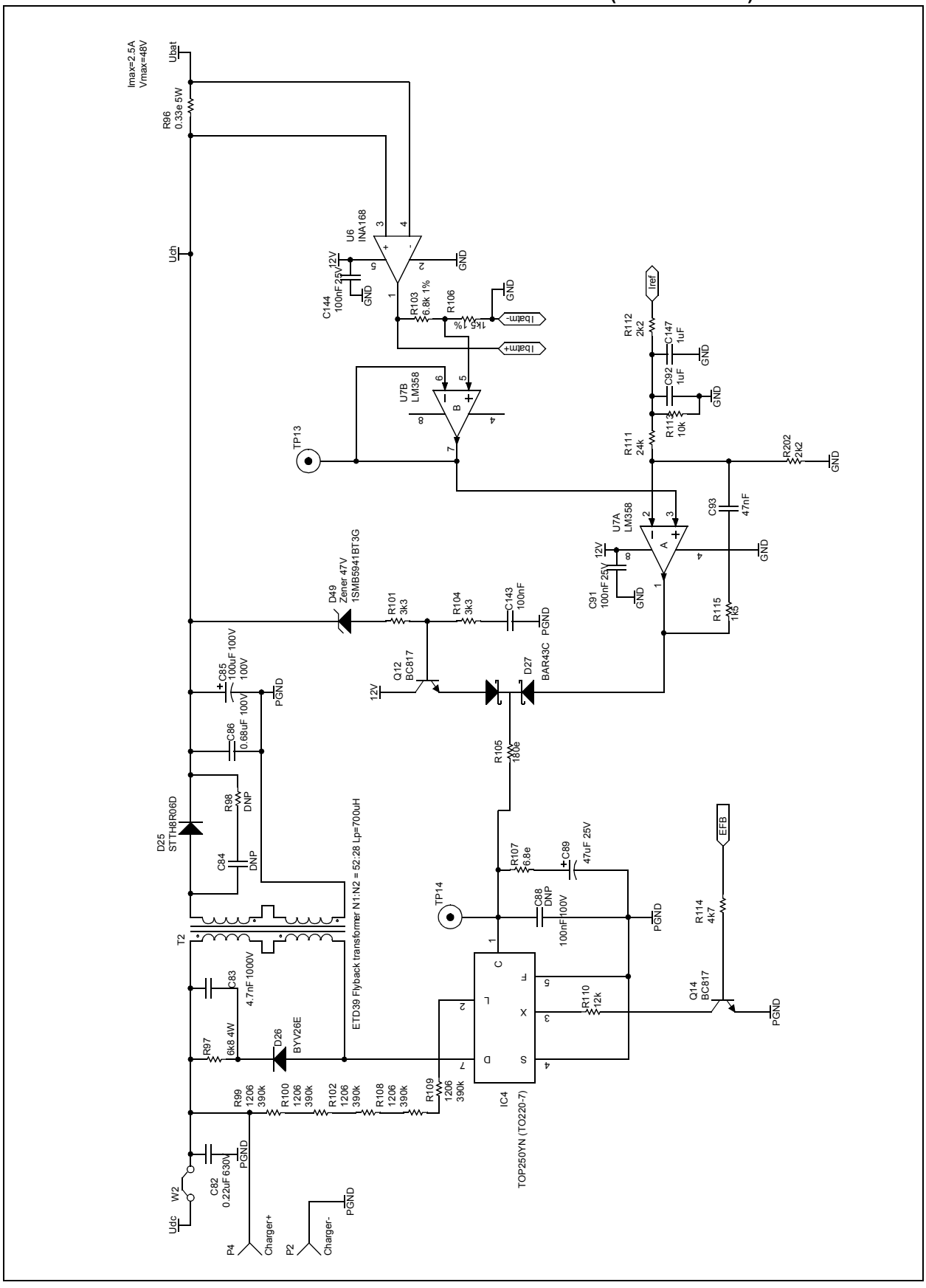


FIGURE D-3: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 2 OF 8)

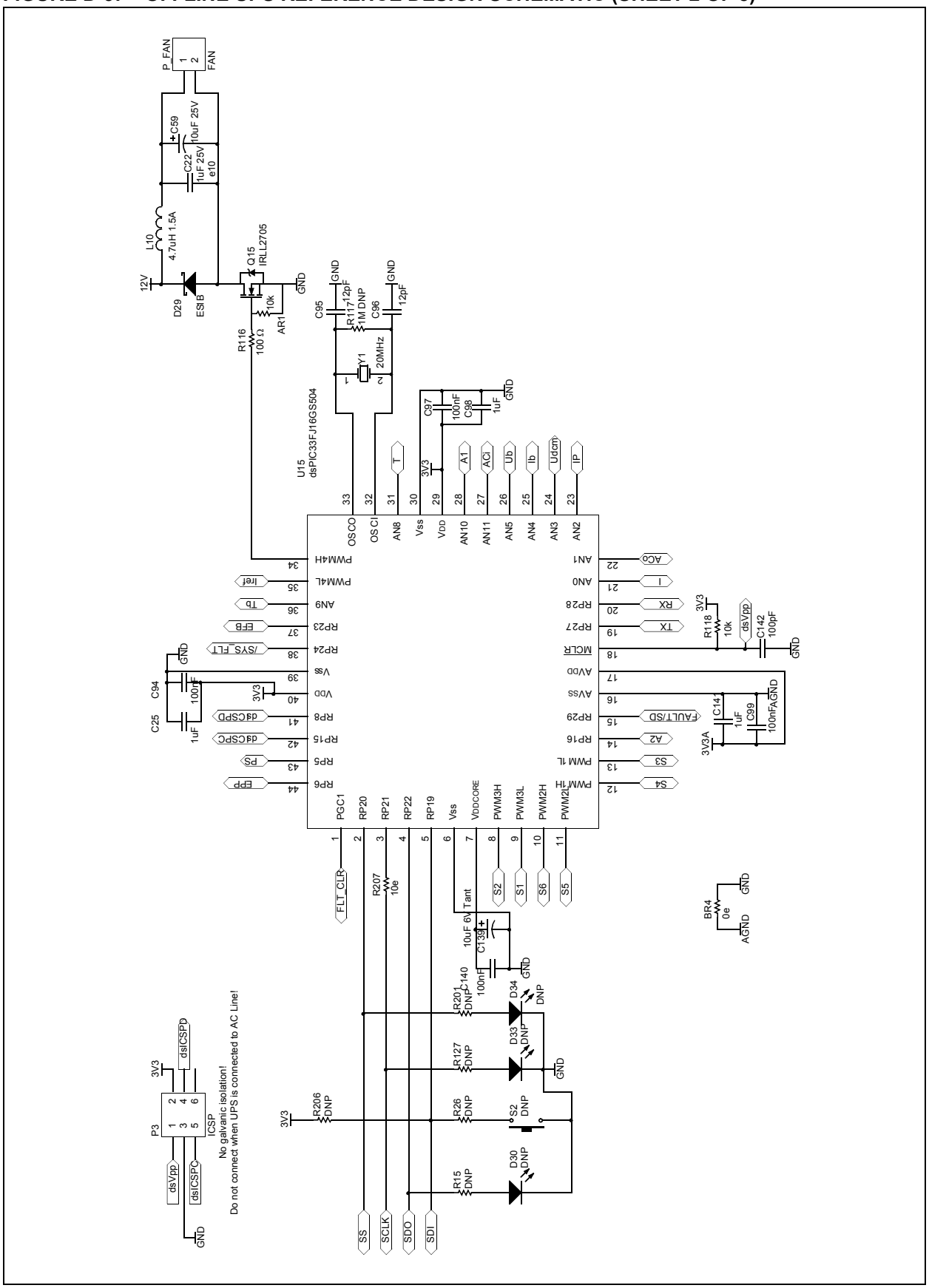


FIGURE D-4: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 3 OF 8)

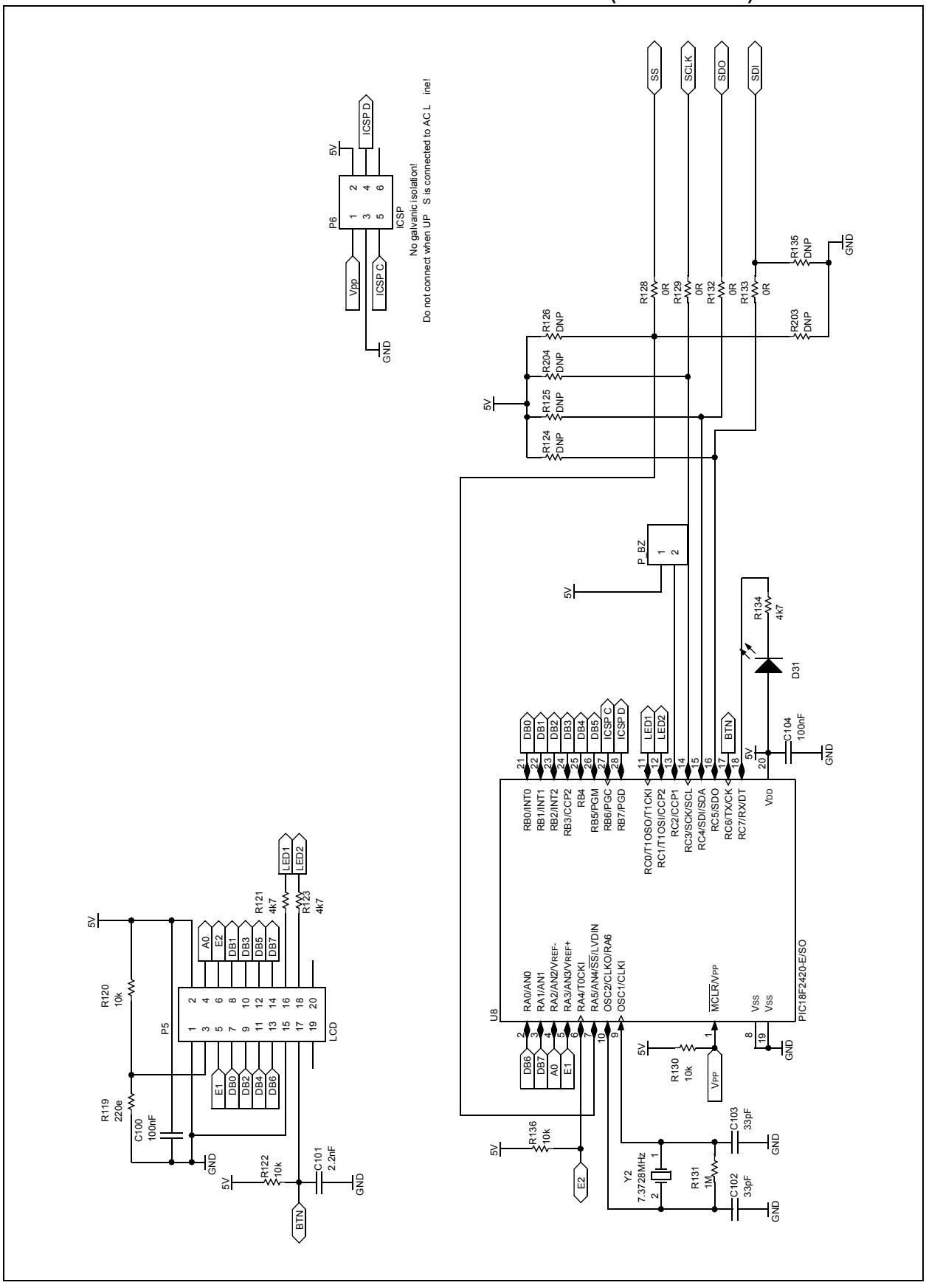


FIGURE D-5: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 4 OF 8)

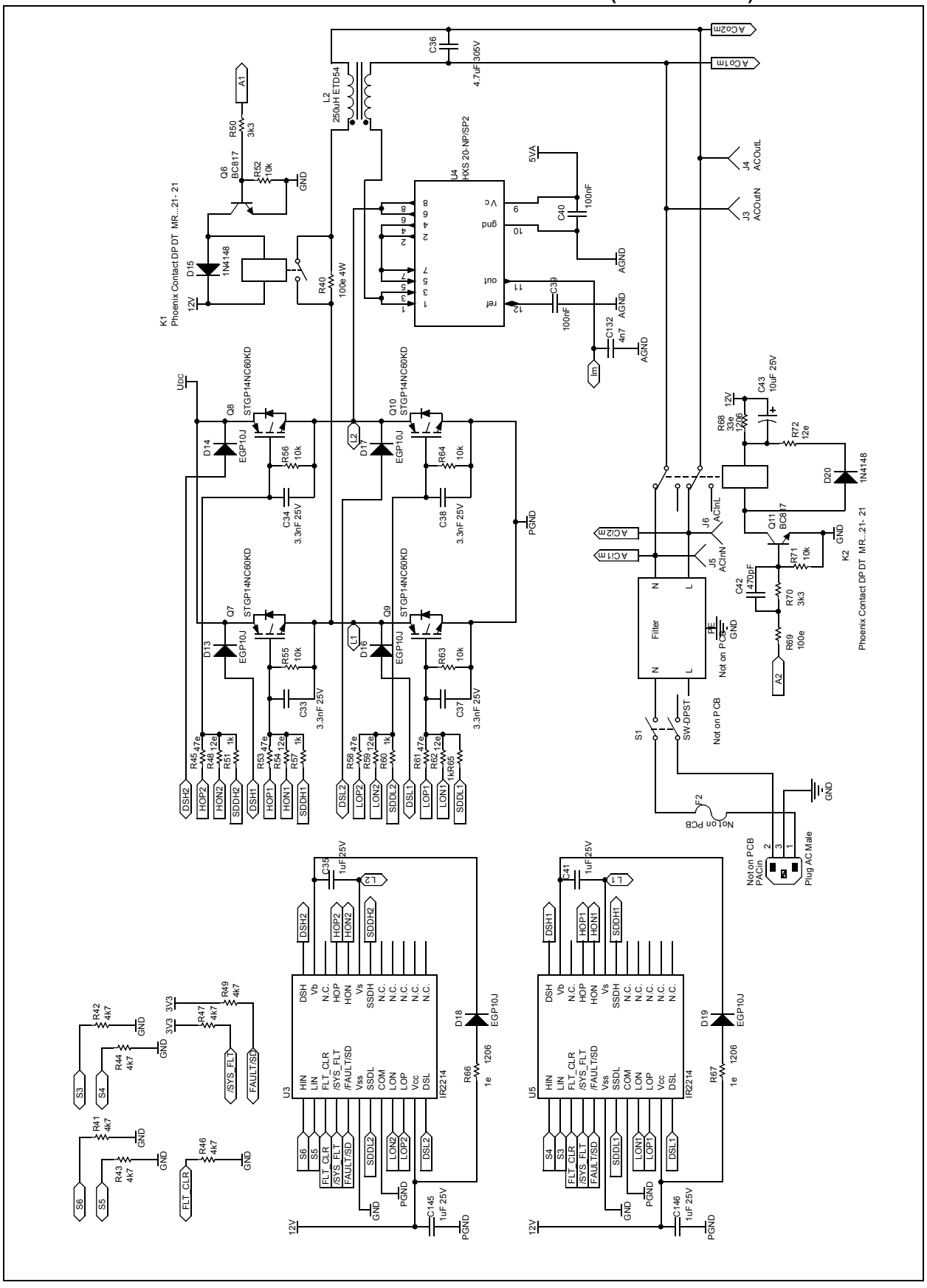


FIGURE D-6: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 5 OF 8)

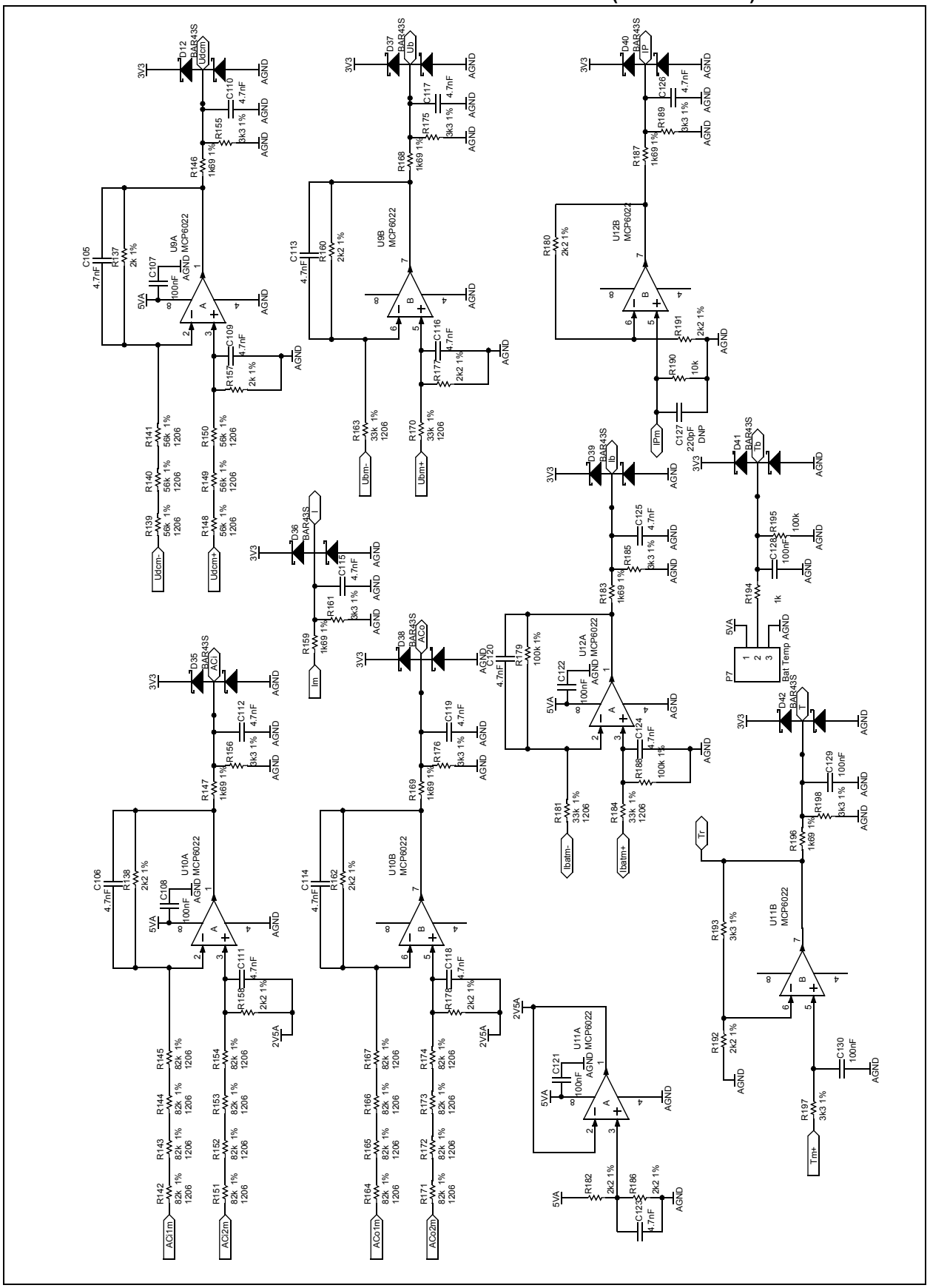


FIGURE D-7: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 6 OF 8)

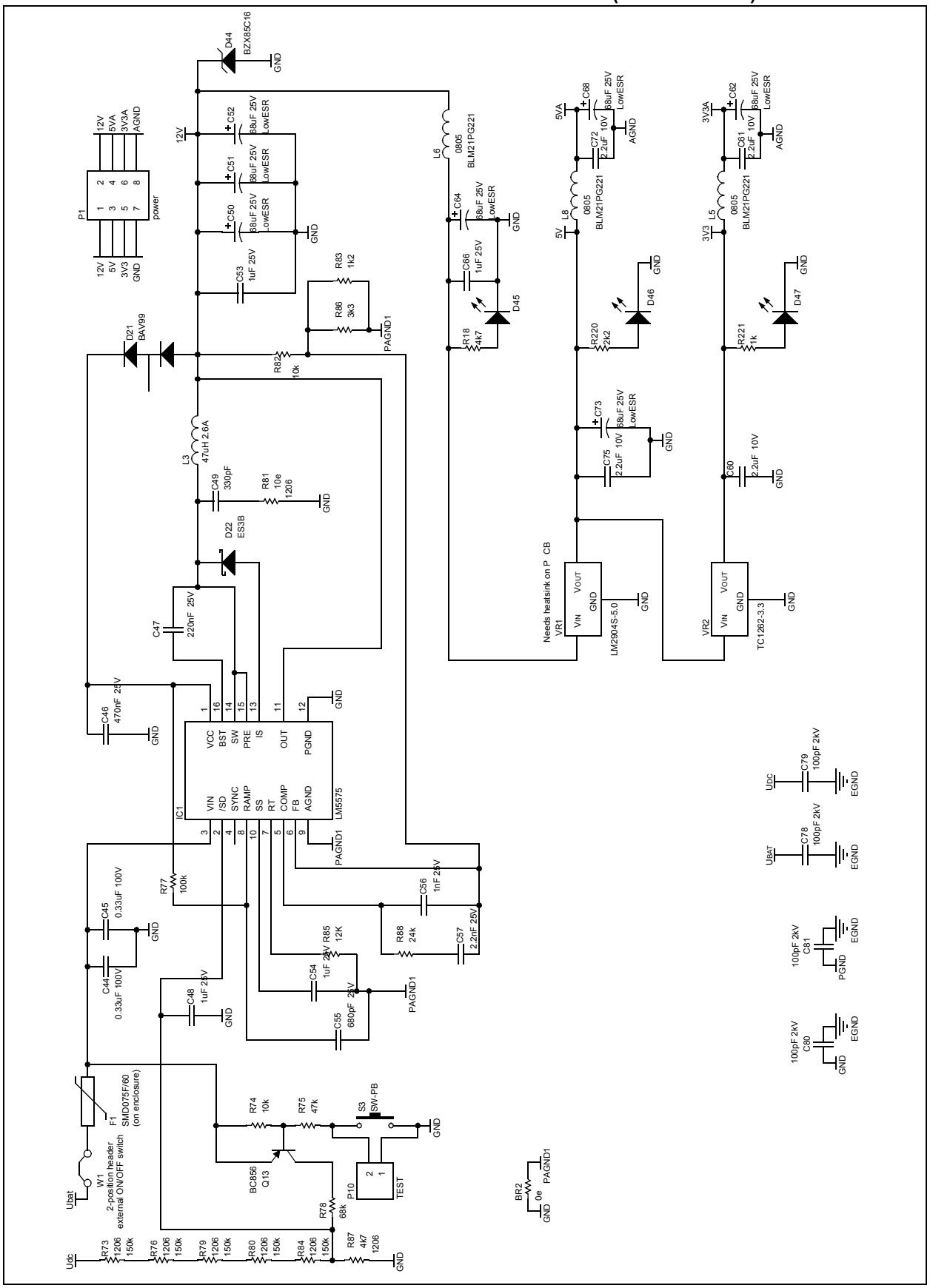


FIGURE D-8: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 7 OF 8)

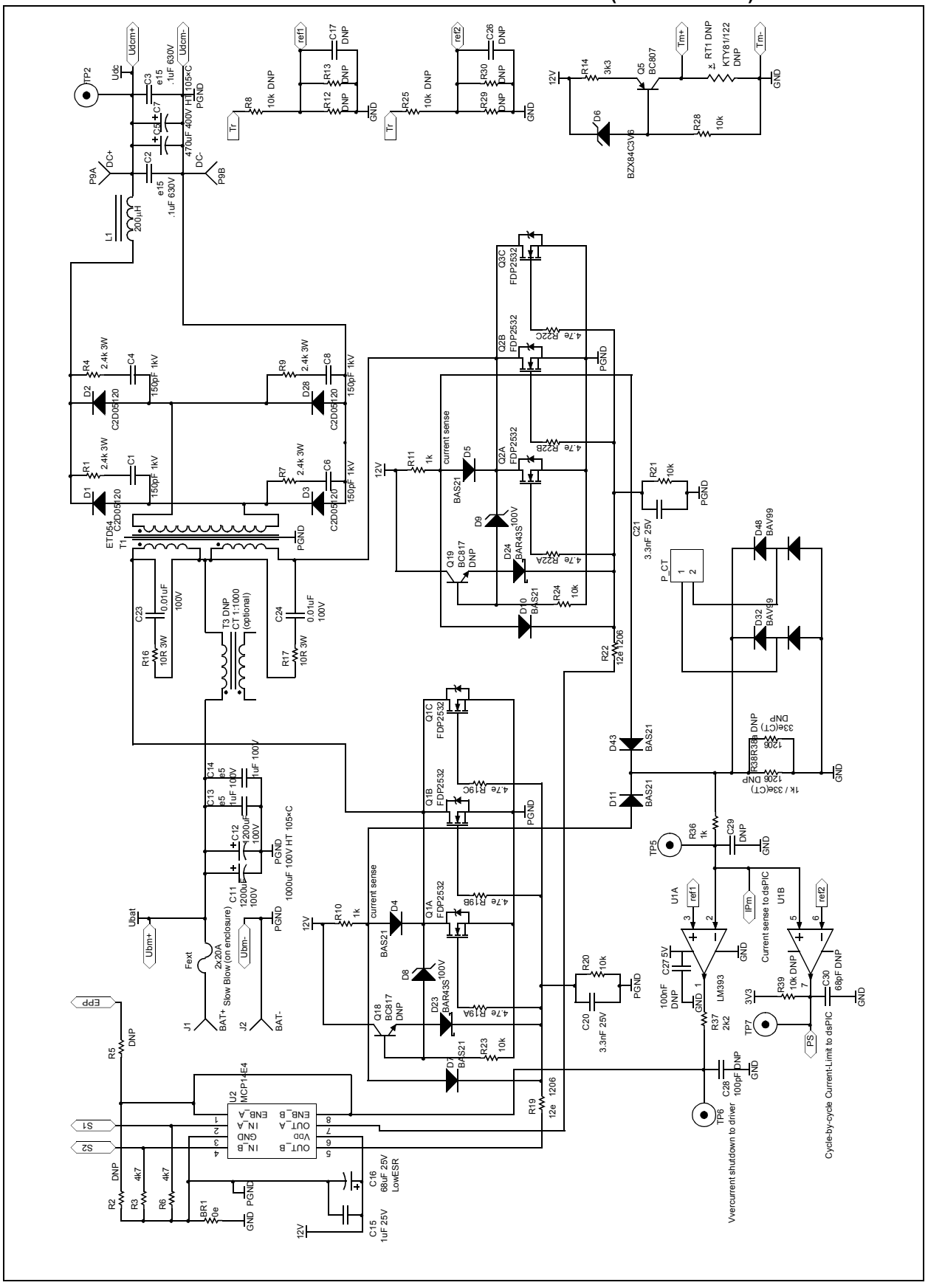
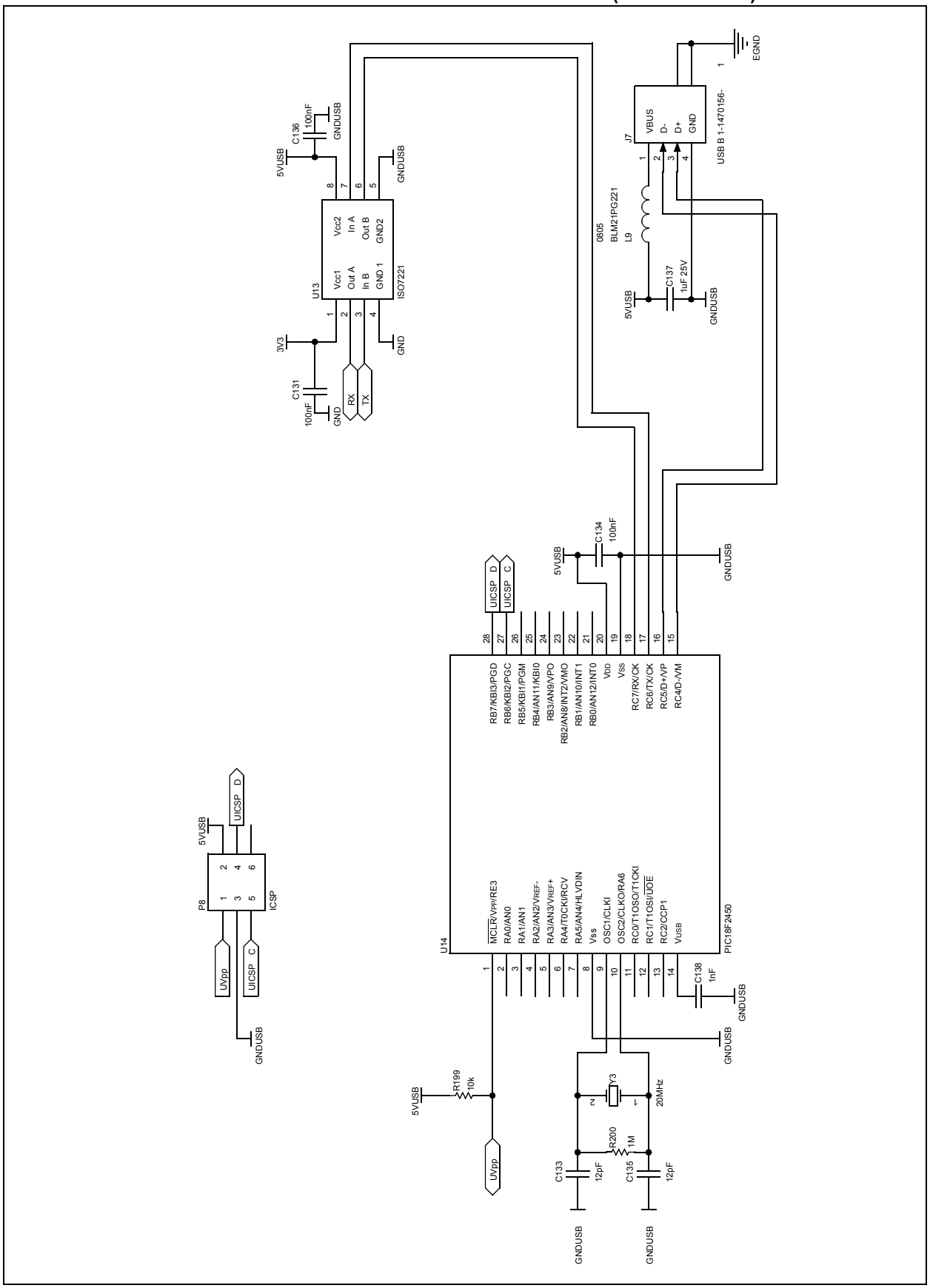


FIGURE D-9: OFFLINE UPS REFERENCE DESIGN SCHEMATIC (SHEET 8 OF 8)



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