AN1792
APPLICATION NOTE

DESIGN OF FIXED-OFF-TIME-CONTROLLED PFC PRE-REGULATORS WITH THE L6562

by C. Adragna

Beside Transition Mode (TM) and fixed-Frequency Continuous Conduction Mode (FF-CCM) operation of PFC pre-regulators a third approach is proposed that couples the simplicity and affordability of TM operation with the high current capability of FF-CCM operation: it is a peak current-mode control with fixed-OFF-time. After showing advantages and limits of this technique, in both its basic and advanced implementation, design equations will be given and a practical design will be illustrated and evaluated.

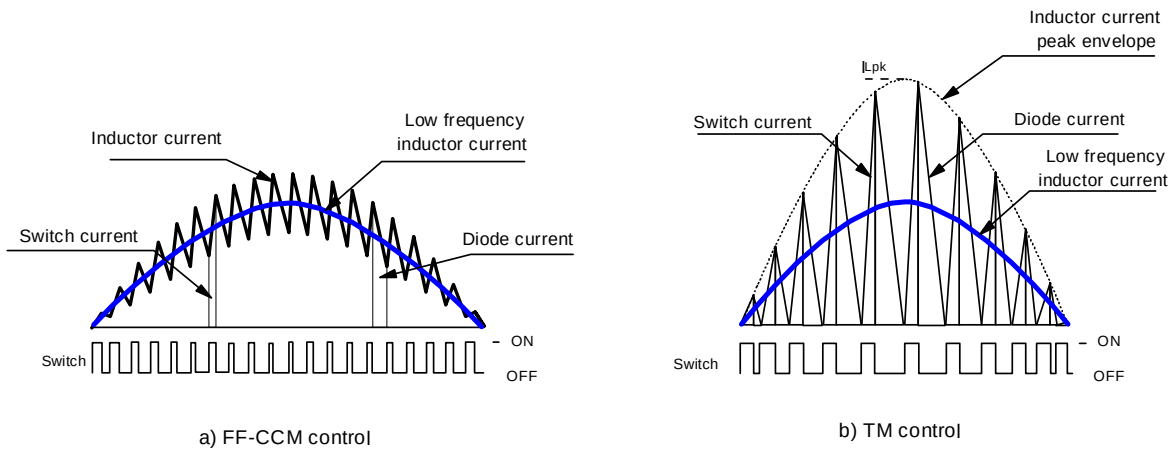
Introduction

Two methods of controlling Power Factor Corrector (PFC) pre-regulators based on boost topology are currently in use: the Fixed-Frequency (FF) PWM and the Transition Mode (TM) PWM (fixed ON-time, variable frequency). The first method employs average current-mode control, a relatively complex technique requiring sophisticated controller IC's (e.g. STMicroelectronics' L4981A/B) and a considerable component count. The second one uses the simpler peak current-mode control, which is implemented with cheaper controller IC's (e.g. STMicroelectronics' L6561, L6562), much fewer external parts and is therefore much less expensive.

With the first method the boost inductor works in Continuous Conduction Mode (CCM), while TM makes the inductor work on the boundary between continuous and discontinuous mode, by definition. For a given power throughput, TM operation then involves higher peak currents as compared to FF-CCM (see figure 1). This, also consistently with the above mentioned cost considerations, suggests the use of TM in a lower power range, while FF-CCM is recommended for higher power levels.

This criterion, though always true, is sometimes difficult to apply, especially for a midrange power level, say around 150-300W. The assessment of which approach gives the better cost/performance trade-off needs to be done on a case-by-case basis, considering the cost and the stress of not only power semiconductors and magnetics but also of the EMI filter: at the same power level, the switching frequency component to be filtered out in a TM system is twice the line current, whereas it is typically 1/3 or 1/4 in a CCM system.

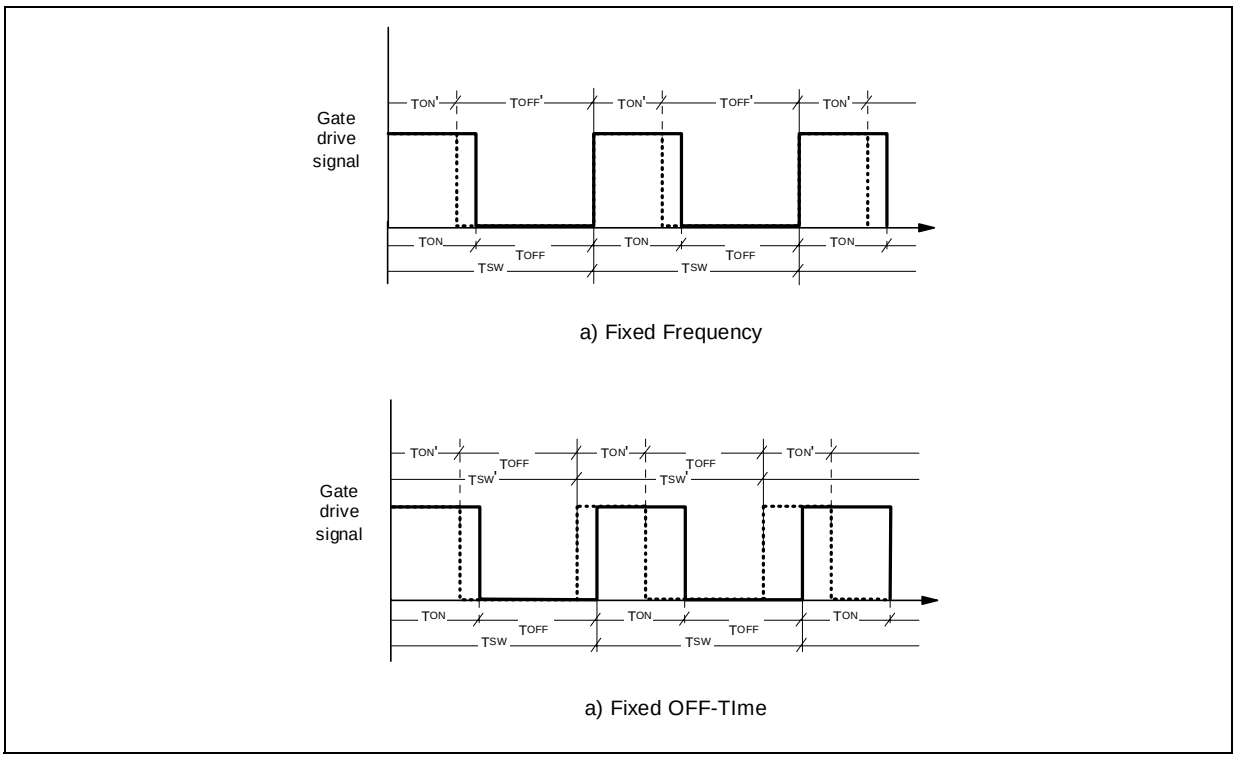
Figure 1. Line, inductor, switch and diode currents in: a) FF-CCM PFC, b)TM PFC.



In this area where the TM/CCM usability boundary is uncertain, a third approach that couples the simplicity and affordability of TM operation with the high current capability of CCM operation can be a solution to the dilemma.

Generally speaking, FF PWM is not the only alternative when CCM operation is desired. FF PWM modulates both switch ON and OFF times (their sum is constant by definition), and a given converter will operate in either CCM or DCM depending on the input voltage and the loading conditions. Exactly the same result can be achieved if the ON-time only is modulated and the OFF-time is kept constant, in which case, however, the switching frequency will not be fixed anymore (see figure 2). This is referred to as "Fixed-OFF-Time" (FOT) control. Peak-current-mode control can still be used.

Figure 2. Basic waveforms for Fixed-frequency PWM (a) and Fixed-OFF-Time PWM (b)

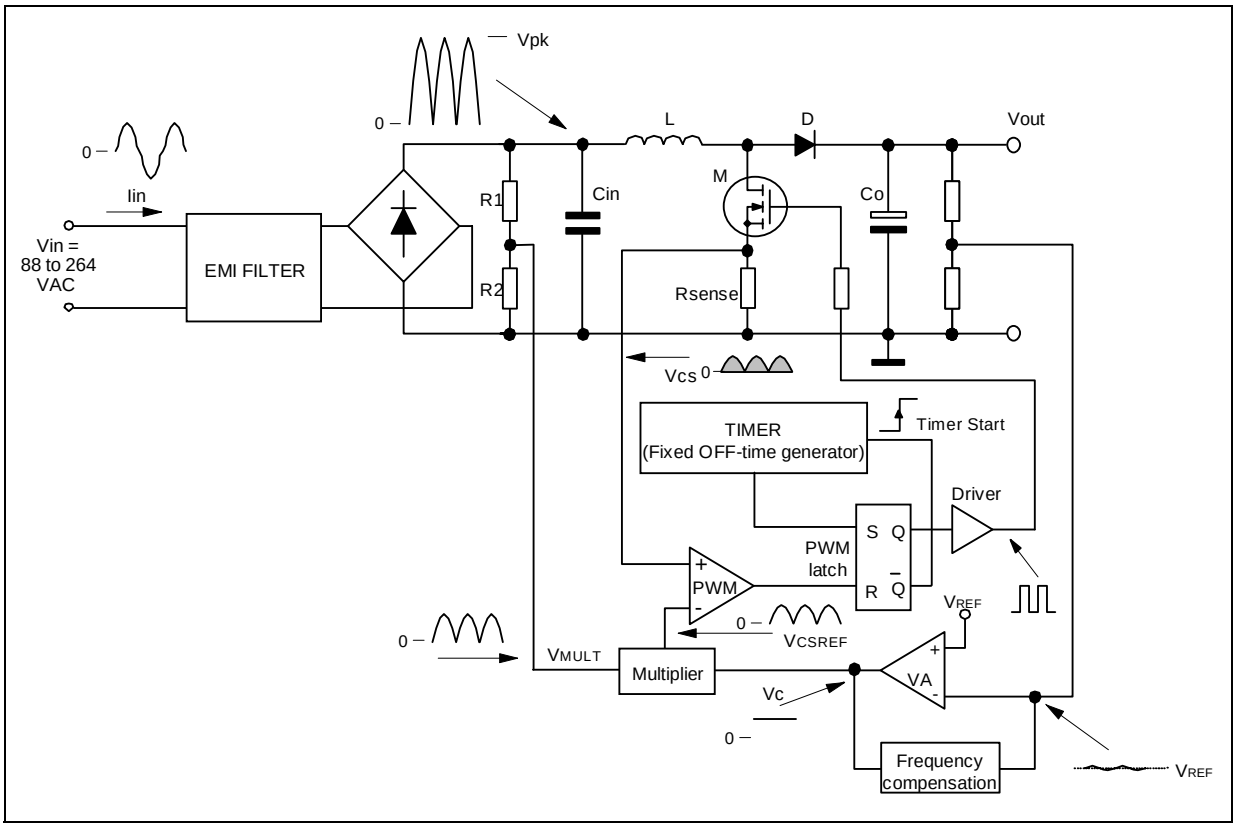


The concept of FOT control is not new [1], [2] but, to the author's knowledge, it has never been applied to PFC pre-regulators to allow CCM operation. In addition to the many advantages and the few drawbacks that this control technique brings to PFC pre-regulators and that will be highlighted in the following sections, an important point is that FOT control does not need a specialized control IC. A simple modification of a standard TM PFC controller operation, requiring just few additional passive parts and no significant extra cost, is all that is needed.

Operation of a FOT-controlled PFC pre-regulator and its practical implementation

Figure 3 shows a block diagram of a FOT-controlled PFC pre-regulator. An error amplifier (VA) compares a portion of the pre-regulator's output voltage Vout with a reference V_{REF} and generates an error signal V_C proportional to their difference. V_C, a DC voltage by hypothesis, is fed into an input of the multiplier block and there multiplied by a portion of the rectified input voltage V_{MULT}. At the output of the multiplier, there will be a rectified sinusoid, V_{CSREF}, whose amplitude is proportional to that of V_{MULT} and to V_C, which represents the sinusoidal reference for PWM modulation. V_{CSREF} is fed into the inverting input of a comparator that, on the non-inverting input, receives the voltage V_{CS} on the sense resistor Rsense, proportional to the current flowing through the switch M (typically a MOSFET) and the inductor L during the ON-time of M. When the two voltages are equal, the comparator resets the PWM latch and M, supposed already ON, will be switched off.

Figure 3. Block diagram of an FOT-controlled PFC pre-regulator.



As a result, V_{CSREF} determines the peak current through M and the inductor L. As V_{CSREF} is a rectified sinusoid, the inductor peak current will be enveloped by a rectified sinusoid as well. The line current Iin will be the average inductor current, that is the low frequency component of the inductor current resulting from the low-pass filtering operated by the EMI filter.

The PWM latch output $\overline{Q}$ going high activates the Timer that, after a predetermined time T_{OFF} has elapsed, sets the PWM latch, thus turning M on and starting another switching cycle. If T_{OFF} is such that the inductor current does not fall to zero, the system will operate in CCM.

It is apparent that FOT control requires nearly the same architecture as TM control, just the way the OFF-time of M is determined changes. It is not a difficult task to modify externally the operation of standard TM PFC controller so that the OFF-time of M is fixed. As a controller we will refer to the L6562 [4], which is suitable for a few hundred watts power applications because of its gate drive capability and its high noise immunity.

The circuit that implements FOT control with the L6562 is shown in figure 4 along with some relevant waveforms. During the ON-time of M the gate voltage VGD is high, the diode D is forward-biased and the voltage at the ZCD pin is internally clamped at $V_{ZCDclamp} \approx 5.7V$. During the OFF-time of M V_{GD} is low, the diode D is reverse-biased and the voltage at the pin decays with an exponential law:

$$V_{ZCD} = V_{ZCDclamp} e^{\frac{-t}{RC}},$$

until it reaches the triggering threshold ($V_{ZCDtrigger} \approx 1.4V$) that causes the switch to turn on. The time needed for the ZCD voltage to go from $V_{ZCDclamp}$ to $V_{ZCDtrigger}$ will define the duration of the OFF-time T_{OFF}:

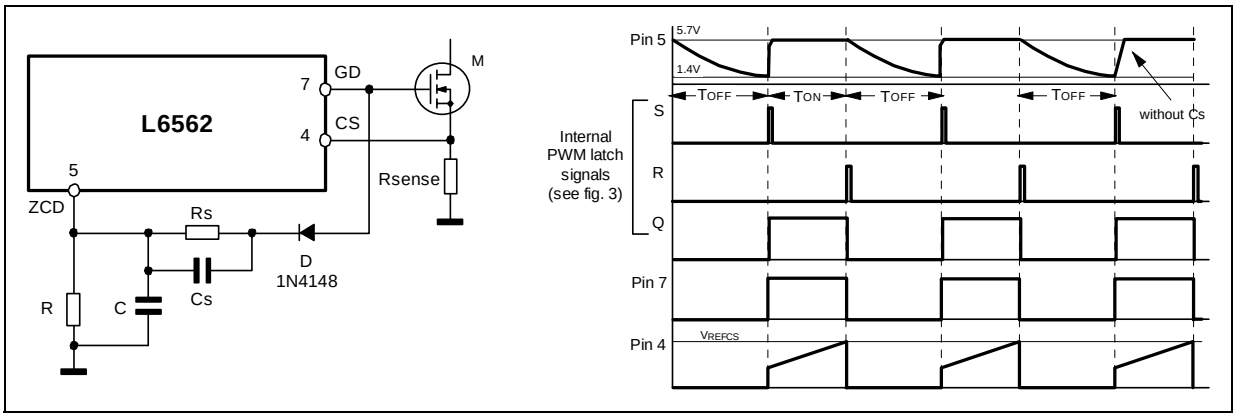
$$T_{OFF} = RC \ln \frac{V_{ZCDclamp}}{V_{ZCDtrigger}} \approx 1.4 \cdot RC \,. (\alpha)$$

As a practical rule, it is convenient to select a capacitor first and then to calculate the resistor needed to achieve the desired T_{OFF}. As the gate voltage V_{GD} goes high the resistor Rs charges the timing capacitor C as quickly as possible up to $V_{ZCDclamp}$, without exceeding clamp rating (I_{ZCDx} =10 mA). Then it must fulfill the following inequalities:

$$\frac{V_{GDx} - V_{ZCDclamp} - V_F}{I_{ZCDx} + \frac{V_{ZCDclamp}}{R}} < Rs < R\frac{V_{GD} - V_{ZCDclamp} - V_F}{V_{ZCDclamp}}, (\beta)$$

where V_{GD} (assume V_{GD} = 10V) is the voltage delivered by the gate driver, V_{GDx} = 15V its maximum value, and V_F the forward drop on D.

Figure 4. Circuit implementing FOT control with the L6562 and relevant timing waveforms.



When working at high line/light load the ON-time of the power switch becomes very short and the resistor Rs alone is no more able to charge C up to $V_{ZCDclamp}$. The speed-up capacitor Cs is then used in parallel to Rs. This capacitor will cause an almost instantaneous charge of C up to a level, after that Rs will complete the charge up to $V_{ZCDclamp}$. It is important that the steep edge caused by Cs does not reach the clamp level, otherwise the internal clamp of the L6562 would undergo uncontrolled current spikes (limited only by the dynamic resistance of the 1N4148 and the ESR of Cs) that could overstress the IC. Cs must then be:

$$Cs < C\frac{V_{ZCDclamp}}{V_{GDx} - V_{ZCDclamp} - V_F}, (\gamma)$$

Implications of FOT control for CCM-operated PFC pre-regulators

Essentially, the aim of FOT control in PFC pre-regulators is to allow CCM operation, and hence high power capability, but with the same complexity level of a TM-operated PFC stage. This goal can be achieved since the properties of FOT control enable the use of the simpler "peak current-mode" control rather than the more complex "average current-mode" needed by the FF-CCM approach.

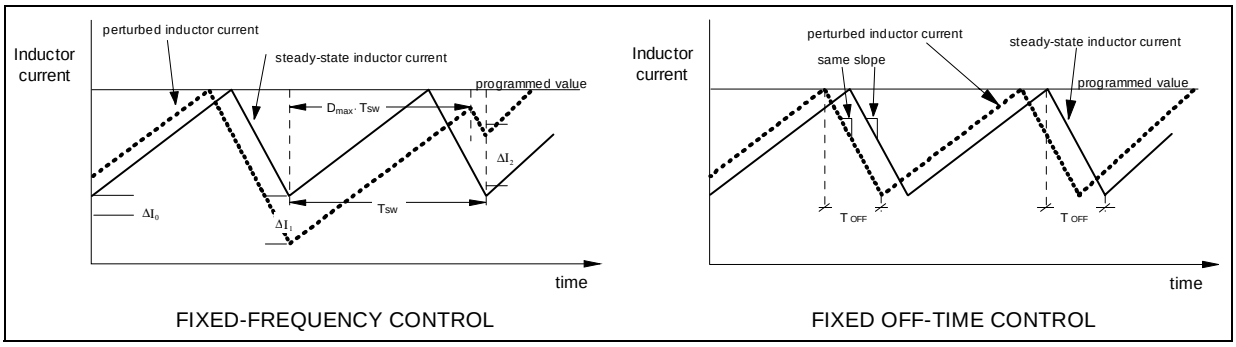
In short, peak current-mode FOT control provides an unconditionally stable inner current loop with no gain peaking and shows "dead-beat control" characteristics. Referring to reference [1] for a detailed explanation of these properties, it is useful to see how they affect the characteristics of FOT-CCM PFC pre-regulators.

1) *Simple control, low part count.* The absence of the sub-harmonic instability typical of FF-systems at duty cycles greater than 50% (see figure 5), makes FOT control very convenient in a PFC boost stage, where the duty cycle can theoretically reach 100%. FF-CCM using peak-current-mode results in an unstable system as long as the instantaneous line voltage is below half the regulated output voltage (condition for duty cycle >50%) with no slope compensation, unless the system is designed to run in DCM (Discontinuous

Conduction Mode) under these conditions. This is quite a limitation. This is why average-current-mode is usually preferred for FF-CCM operation, despite the penalty of an increased circuit complexity. Additionally, FOT control does not require the use of an auxiliary winding on the boost inductor as does the TM approach. If the control IC can be powered by an external source (e.g. the transformer of a cascaded DC-DC converter) the inductor can be made with a single winding with some saving in its cost.

2) *Dynamic behavior improvement.* The optimum response of the inner current loop tends to limit inductor current ringing resulting from load changes. However, it has little impact on the performance of the outer voltage control loop, still largely dominated by the low bandwidth needed to achieve a high PF.

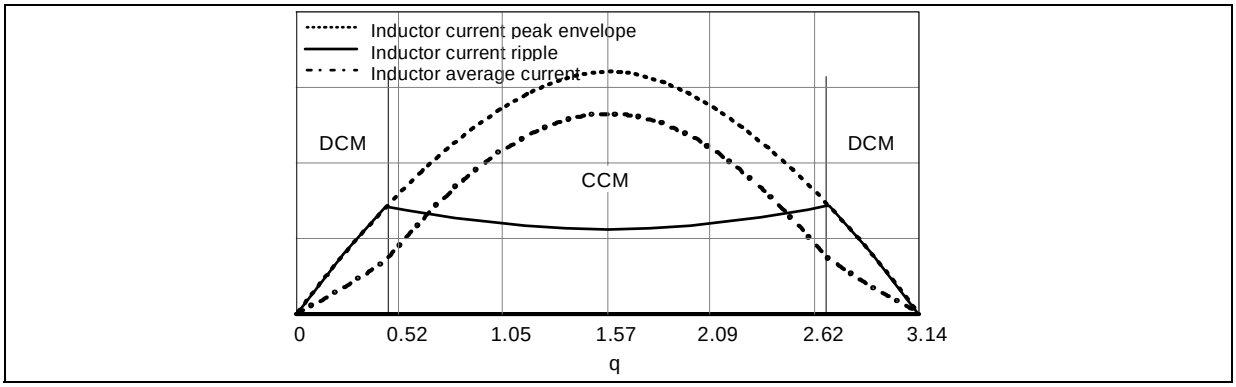
Figure 5. FF vs. FOT control at D>50%: instability (FF) and stability with critical damping (FOT).



3) *Reduced EMI emissions.* Variable frequency operation is inherent in FOT concept: any variation of load current or input voltage is compensated by the feedback control with a variation of the switch ON-time. Thus, the switching frequency of a PFC pre-regulator is modulated, at a modulation rate twice the mains frequency, by the input voltage swinging all the way from zero to the peak. The result is a spread-spectrum action that reduces the peak energy of the noise generated and simplifies the ability to comply with EMI regulations.

4) *DCM and CCM always live together, at least at nominal load.* Figure 6 shows typical current waveforms: at two points along the sinusoid the inductor current ripple during one switching cycle equals the peak value in that cycle. This is the boundary between CCM and DCM operation: there will be DCM around the line voltage zero-crossings and CCM around the top of the sinusoid. As the power is reduced, the region of DCM operation will get larger until it takes up the entire line cycle.

Figure 6. Typical current waveforms along a line voltage half-cycle of a FOT-controlled PFC stage.



5) *Stress due to boost diode's reverse recovery and MOSFET's capacitive loss is alleviated.* CCM operation requires the use of ultra-fast recovery diodes. In the DCM portion, however, (typically, about 30% of the line cycle) the recovery of the boost diode is not invoked, hence the related losses in the diode itself and those induced in the MOSFET are reduced. Additionally, because of the DCM portion, the capacitive losses at MOSFET turn-on due to the discharge of the drain capacitance are decreased as well. Actually, during a small part of the DCM portion the MOSFET is soft-switched.

6) *Line current distortion is not negligible.* It will be shown that as long as the system operates in CCM the line current waveform is a portion of a sinusoid but, as it enters DCM around the line voltage zero crossings, the shape changes, causing a distortion of the line current (see the dash-dot line in figure 6). However, it will be shown that its harmonic contents is still comfortably compliant with EN61000-3-2 standards on harmonic current emissions. Thus the practical impact of this drawback is very limited.

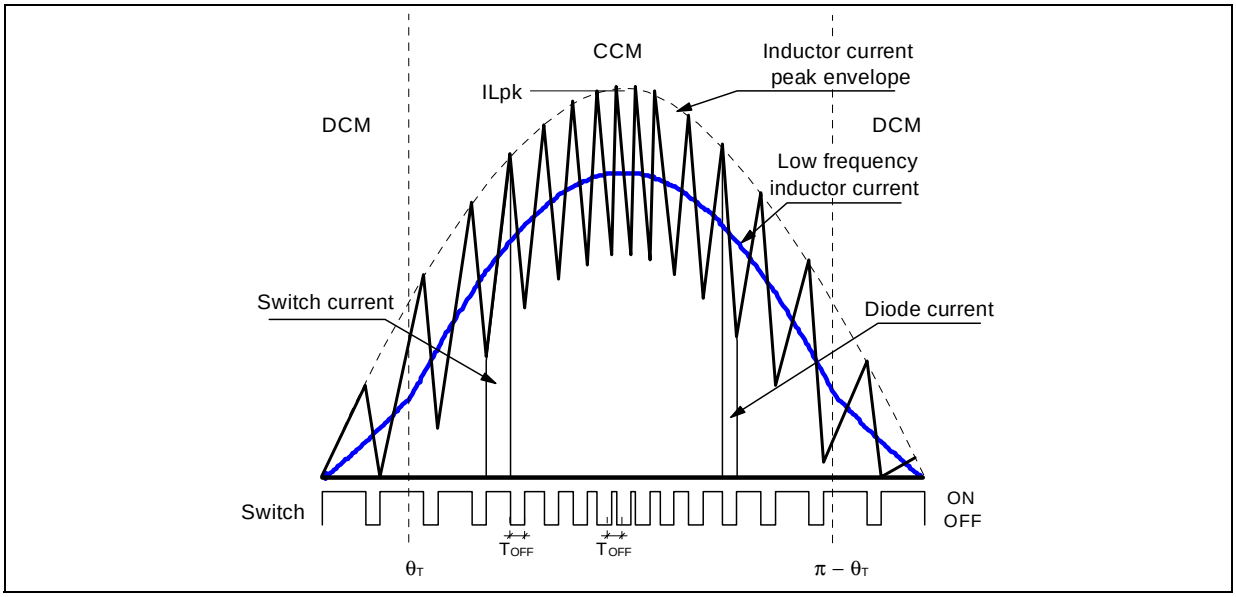
7) *Trade-off between operating frequency and line current distortion.* It will be shown that, in order to limit line current distortion at high line, the OFF-time must be selected greater than a minimum value. This could prevent the use of a switching frequency high enough to have a relatively small inductor size. However, a variant of the basic FOT control will be presented that allows the designer to overcome this issue.

FOT-CCM PFC: large-signal characteristics.

The large-signal characteristics of a FOT-CCM PFC boost pre-regulator will be now discussed from the qualitative point of view. For details on the FOT-CCM PFC large signal model derivation, please refer to [3]. The quantitative results of the approximate analysis described in [3], provided in tables 2, 3 and 4, are the basis for a design procedure that will be outlined in another section.

It is well-known that in a boost converter, during the MOSFET's OFF-time TOFF (which is a given design parameter), the inductor demagnetizes and releases the energy stored during the ON-time. If in a switching cycle T_{OFF} is long enough to completely discharge the inductor within that cycle, there will be DCM operation, otherwise there will be CCM operation. As previously said, if the PFC boost is operated with FOT, DCM and CCM operation alternate in a line half-cycle. The phase angle $\theta_T \in [0, \pi/2]$ where the operation changes from DCM to CCM will be referred to as the "transition angle". Considering waveform symmetry, operation will change from CCM back to DCM at the supplementary phase angle $\pi - \theta_T$. In each line half-cycle there will be CCM operation for $\theta_T < \theta < \pi - \theta_T$ and DCM operation for $\theta < \theta_T$ and $\theta > \pi - \theta_T$. In a given converter (i.e. for given Vout, L and T_{OFF}), the transition angle θ_T depends on the operating conditions (line voltage and output load). Figure 7 shows schematically the inductor current, also pointing out how it is split between the MOSFET M and the diode D. The low-frequency component, that is the line current Iin(θ), is shown too.

Figure 7. Inductor, switch and diode currents in a CCM-FOT-controlled PFC stage.



During the DCM portion of the line half-cycle MOSFET's ON-time T_{ON} is constant and, as T_{OFF} is constant by definition, the switching frequency and MOSFET duty cycle will be constant as well. Their value depend on the peak input voltage and the output load. During the CCM portion they change with both the peak and the instantaneous line voltage but not with the load. The switching frequency is maximum on the top of the sinusoid, reaches the minimum at the DCM/CCM boundary and does not change any more in the DCM portion.

Table 1. List of basic symbols used in tables 2 to 4

Symbol	Parameter
T_{OFF}	Fixed MOSFET OFF-time
L	Boost inductor's inductance
Vpk	Peak line voltage ($\sqrt{2}$ times the RMS value Vac)
Vout	Pre-regulator's output regulated voltage
Pout	Pre-regulator's output power
Pin	Pre-regulator's input power (= Pout / η , η = efficiency)
I_{Lpk}	Peak of inductor current sinusoidal envelope
k	Vpk/Vout ratio
Γ	Conventional zero-voltage-input inductor current ripple: Vout·T_{OFF}/L

Table 2. Timing quantities of FOT-controlled boost PFC pre-regulators

Symbol	Parameter	DCM	CCM
θ_T	Transition angle (DCM⇒CCM boundary)	$\sin^{-1}\frac{\Gamma}{I_{Lpk}+k\Gamma}$	
$T_{ON}(\theta)$	MOSFET ON-time	$\frac{LI_{Lpk}}{kV_{out}}$	$\left(\frac{1}{k\sin\theta}-1\right)T_{OFF}$
$D(\theta)$	MOSFET duty cycle	$1 - k\sin\theta_T$	$1 - k\sin\theta$
$f_{sw}(\theta)$	Switching frequency	$\frac{k}{T_{OFF}}\sin\theta_T$	$\frac{k}{T_{OFF}}\sin\theta$
$\delta f_{sw}(\theta)$	Switching frequency modulation depth	$2\frac{1-\sin\theta_T}{1+\sin\theta_T}$	
$T_{FW}(\theta)$	Inductor demagnetization time	$\frac{k\sin\theta}{1-k\sin\theta}T_{ON}$	T_{OFF}
$D_L(\theta)$	Inductor current circulation duty cycle	$\frac{1-k\sin\theta_T}{1-k\sin\theta}$	1

Table 3. Inductor and line input current in FOT-controlled boost PFC pre-regulators

Symbol	Parameter	DCM	CCM
$\Delta I_L(\theta)$	Inductor current ripple	$I_{Lpk}\sin\theta$	$\Gamma(1 - k\sin\theta)$
$I_{L(av)}(\theta)$	Inductor average current	$\frac{1}{2}\frac{I_{Lpk}^2}{I_{Lpk}+k\Gamma}\frac{\sin\theta}{1-k\sin\theta}$	$\left(I_{Lpk}+\frac{\Gamma}{2}k\right)\sin\theta-\frac{\Gamma}{2}$
$I_{in}(\theta)$	Line input current	$\frac{1}{2}\frac{I_{Lpk}^2}{I_{Lpk}+k\Gamma}\frac{\sin\theta}{1-k\lvert\sin\theta\rvert}$	$\left(I_{Lpk}+\frac{\Gamma}{2}k\right)\sin\theta-\frac{\Gamma}{2}\mathrm{sgn}(\sin\theta)$

As shown in figure 7, the inductor current will be a series of rising (during T_{ON}) and falling (during T_{OFF}) ramps whose peaks are enveloped by $I_{Lpk}\sin\theta$. In a single switching cycle, the current will always be triangular: in the DCM portion the triangles start from zero and touch zero before the end of the cycle, in CCM the triangles are superimposed on top of a current pedestal. The inductor current ripple is minimum on the top of the sinusoid and maximum at the transition DCM⇔CCM. Note that this property gives a practical meaning to the transition phase angle θ_T; its sine provides the ratio of the maximum current ripple amplitude to the inductor peak current, the so-called "ripple factor" Kr, a parameter typically used in the

design phase to specify how deep in CCM the system is required to operate:

$$Kr = \sin\theta_T = \frac{\Delta I_{Lpk(max)}}{I_{Lpk}} \quad (1)$$

Line current is made by a sinusoidal portion (during CCM, $\theta_T < \theta < \pi - \theta_T$), shifted downwards during positive half-cycles and upwards during negative half-cycles by $\Gamma/2$, in-phase with the line voltage, that is joined to line voltage zero-crossings through non-sinusoidal segments corresponding to the DCM portion. These non-sinusoidal segments result in a distortion of the line current, thus it is not possible to achieve unity power factor even ideally, unlike as with TM and FF-CCM techniques.

Table 4. Approximate energetic relationships in FOT-controlled boost PFC pre-regulators

Symbol	Parameter	Approximate value
I_{Lpk}	Inductor peak current	$\approx \frac{2Pin}{kVout} + \frac{4-k\pi}{2\pi}\Gamma$
Ipk	Line peak current	$\approx \frac{2Pin}{kVout} + \frac{4-\pi}{2\pi}\Gamma$
$Iin_{(rms)}(\theta)$	Line RMS current	$\approx \frac{\sqrt{2}Pin}{kVout}$
$I_{Q(rms)}$	MOSFET RMS current	$\approx \frac{Pin}{kVout}\sqrt{2-\frac{16k}{3\pi}}$
$I_{D(rms)}$	Diode RMS current	$\approx \frac{Pin}{kVout}\sqrt{\frac{16k}{3\pi}}$
$I_{Co(rms)}$	Output capacitor total RMS current	$\approx \frac{Pin}{kVout}\sqrt{\frac{16k}{3\pi k}-1}$
$I_{Co,H2}$	Peak-to-peak low-frequency current ripple	$\approx \frac{Pin}{Vout} + \frac{k\Gamma}{3\pi}$

It is worth reminding that the accuracy of the approximate energetic relationships of table 4 is quite good at maximum load for low values of the parameter k, that is at low line voltage, but worsens at high line and as the power throughput is reduced. Since in the design phase current stress is calculated at maximum load and minimum line voltage, their accuracy is acceptable for design purpose. An exact description, accurate under all operating conditions, requires the use of the exact model [3], which is quite difficult to treat without using an automatic calculation tool, such as MathCad®.

To give the reader a better idea on how the various quantities change within a half-line cycle as well as how peak and RMS current values change under different operating conditions, a series of 3-D plots generated with MathCad® are provided (figures 8 to 14).

All of these plots refer to a pre-regulator designed for Vout=400V and a maximum inductor current ripple equal to 40% of the maximum inductor peak current (Kr=0.4) when supplied with 88Vac (k=0.311, θ_T=24°) at rated load $Pout_0$ ($\Rightarrow$ Pin = Pin_0). Frequency values are normalized to that on the top of the sinusoid @88Vac. T_{ON} is normalized to T_{OFF}. Currents within a line half-cycle are normalized to the peak inductor envelope I_{Lpk} @88Vac. Peak or RMS values are normalized to their respective maximum values @88Vac.

Figure 8. Normalized switching frequency vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

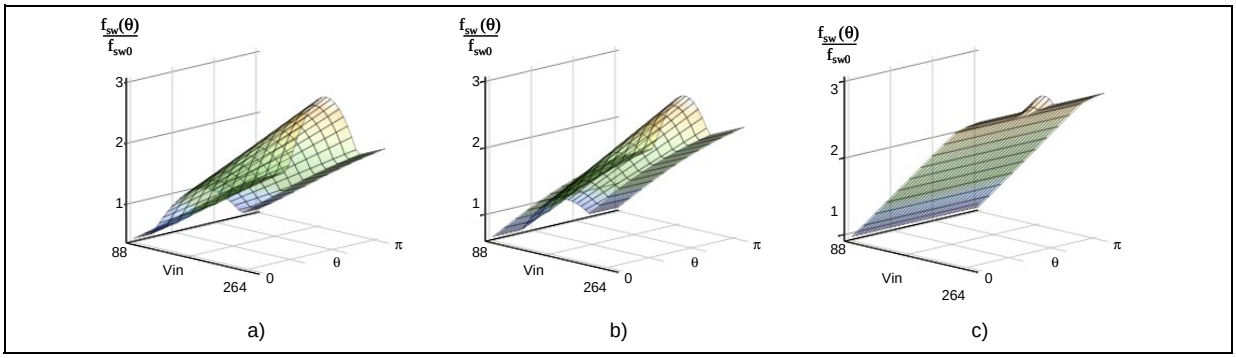


Figure 9. Normalized MOSFET's ON-time vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

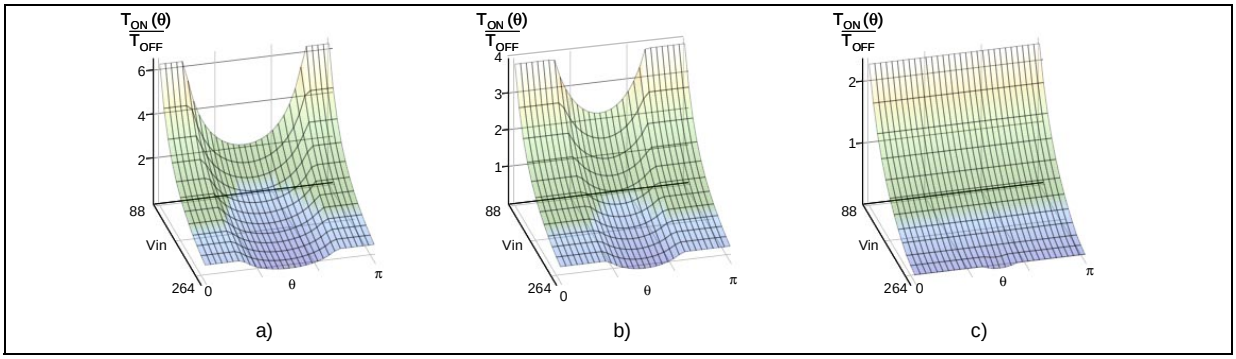


Figure 10. Inductor current conduction angle vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

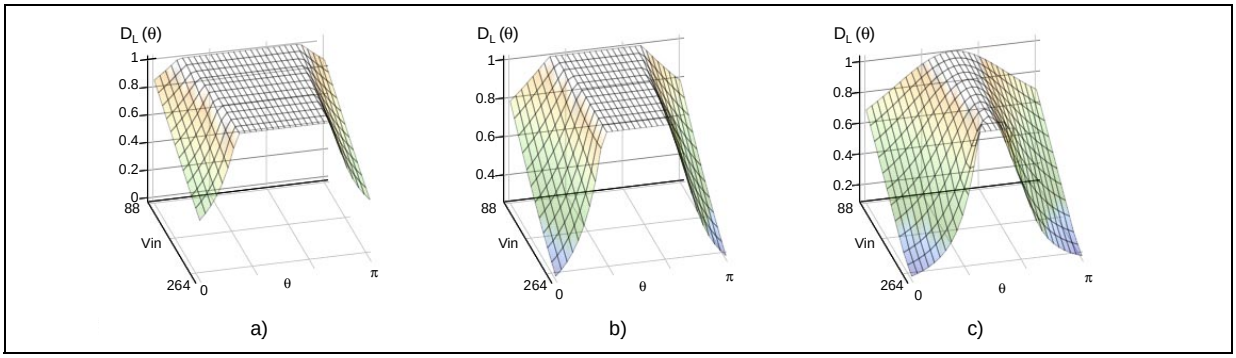


Figure 11. Line current vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

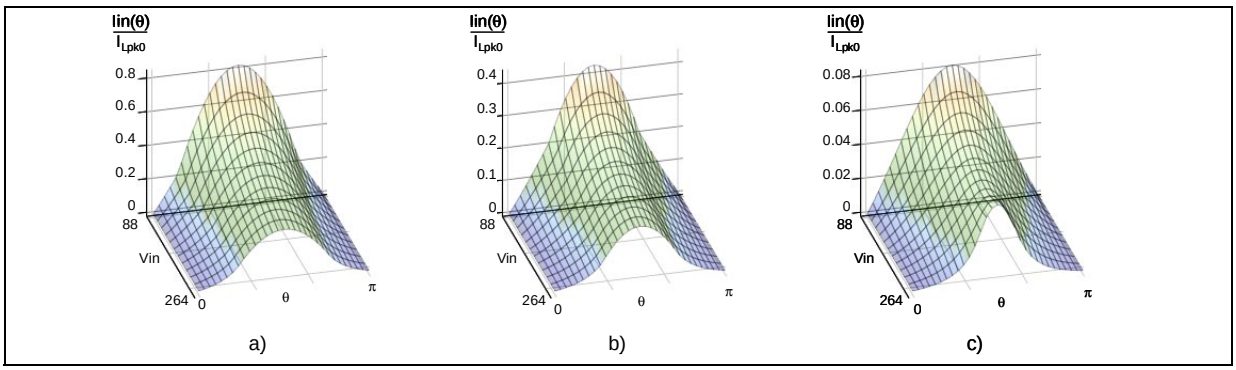


Figure 12. Inductor current ripple vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

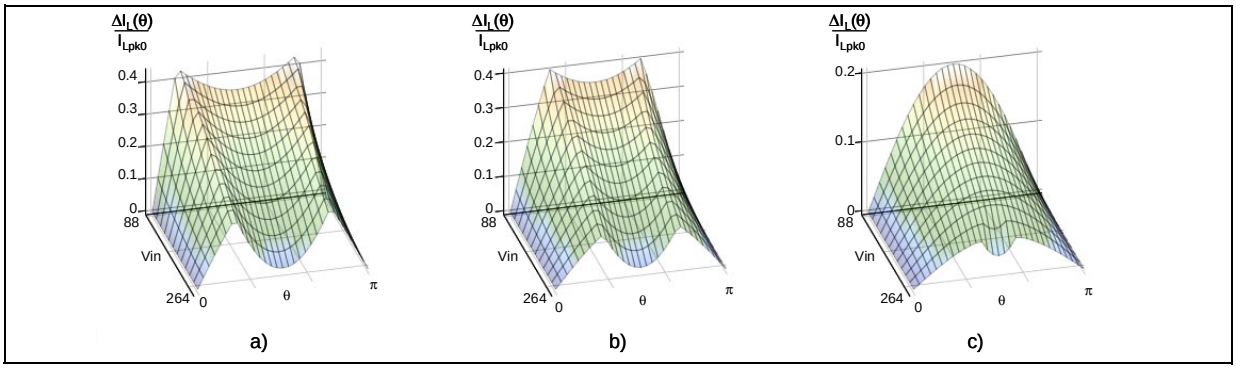


Figure 13. a) Normalized Inductor peak current; b) Normalized line peak current; c) Transition angle

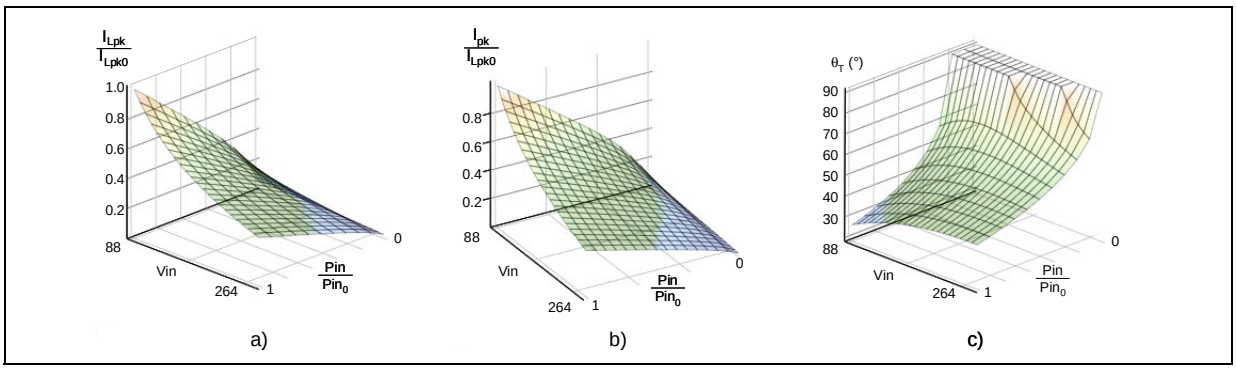
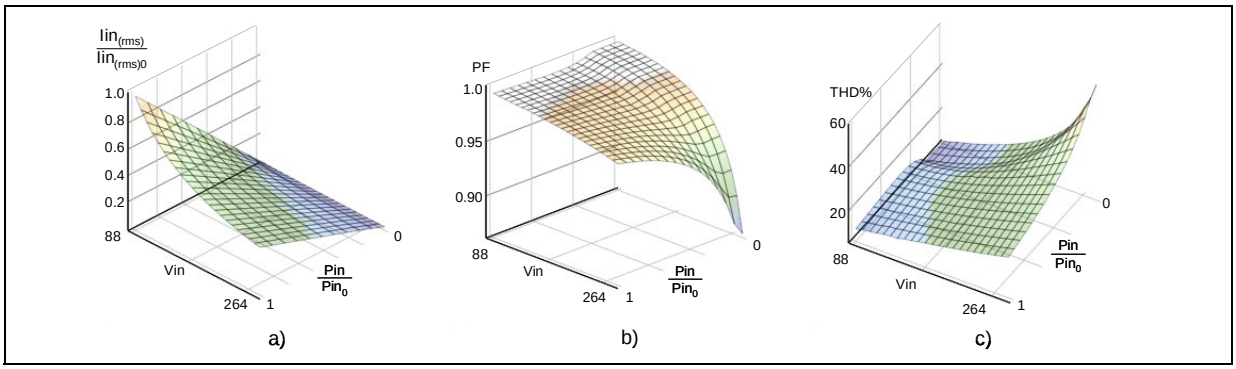


Figure 14. a) Normalized line RMS current; b) Power Factor; c) Total Harmonic Distortion

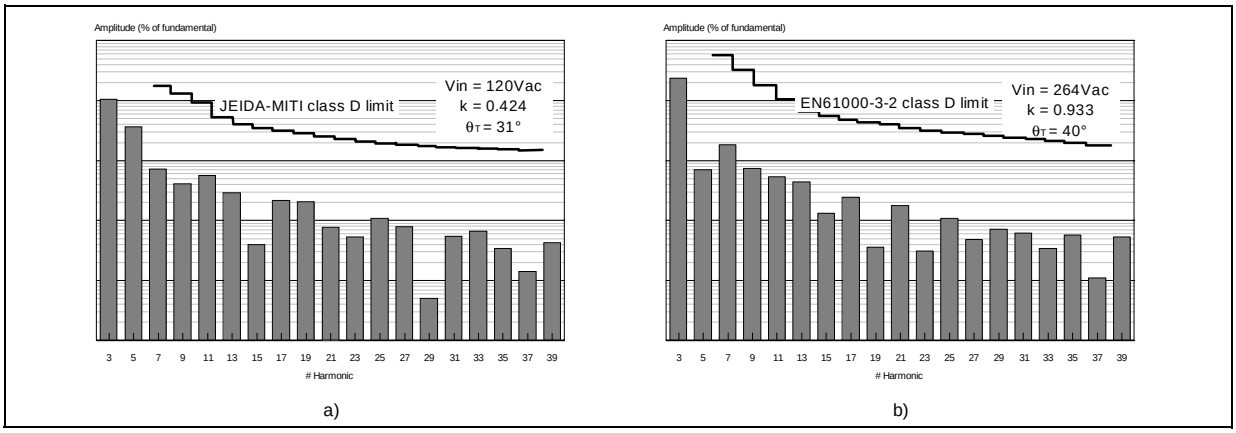


The pictures of figure 11 show clearly the distortion of the line waveform, quite limited at low line, more and more accentuated as the line voltage increases and the output power decreases. This is confirmed by the PF and THD% plots of figure 14.

It is important to evaluate the harmonic content of this current waveform, at least at nominal load, in order to compare it with the limits envisaged by regulations. The Japanese JEIDA-MITI standard is considered at low input voltage (100Vac) and the European EN61000-3-2 at high input voltage (230Vac).

To do so, Fourier analysis needs to be done on the waveform Iin(θ). The bar diagrams of figure 15 show the worst-case harmonic contents of the line current ("odd counterpart" of the average inductor current shown in figure 11), along with the limits envisaged by the above mentioned norms, showing plenty of margin.

Figure 15. Harmonics of line currents against the class-D limits of: a) JEIDA-MITI; b) EN61000-3-2.

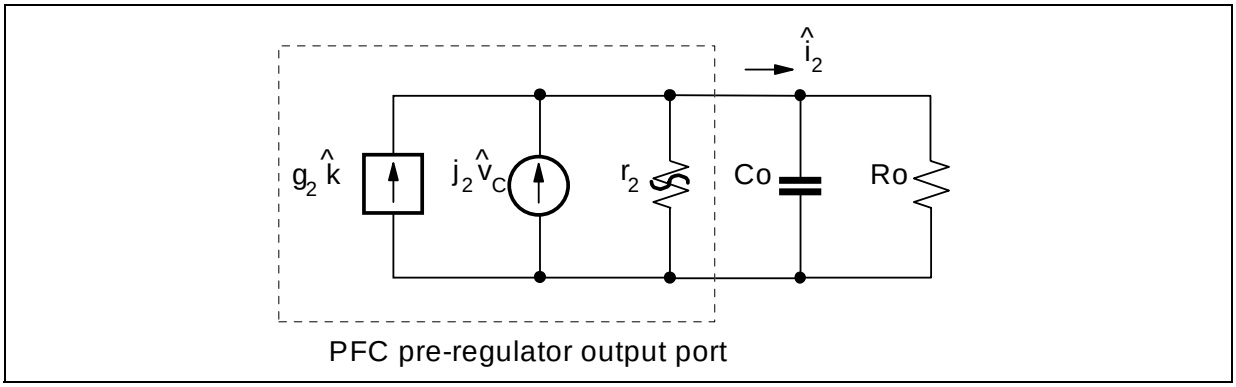


FOT-CCM PFC small-signal analysis.

A small-signal model for any PFC pre-regulator, valid for control, line and load variations at frequencies sufficiently lower than the line frequency (quasi-static approximation), is illustrated in figure 16. This model is generally applicable, regardless of the control technique used: the control affects the values of the parameters g_2, j_2 and r_2 and not the circuit configuration.

The values for FOT control can be determined considering Pout=Pin and expanding the large-signal model given in [3] in a three-dimensional Taylor series to the first order around the operating point.

Figure 16. General low-frequency small-signal PFC model.



After a symbolism change and some algebraic manipulations it is possible to arrive at the following result:

$$g_2 = \frac{\partial i_2}{\partial k} = \frac{Pin}{kVout} + \frac{k\Gamma}{4}, \; j_2 = \frac{\partial i_2}{\partial V_c} = \frac{k^2 K_M K_P}{2} \frac{Vout}{Rsense}, \; -\frac{1}{r_2} = \frac{\partial i_2}{\partial Vout} = \frac{Pin}{Vout^2} - \frac{k\Gamma}{\pi Vout},$$

where V_C is the control voltage (the output of the error amplifier of the L6562, pin #2 COMP), K_M the multiplier gain, K_P the divider ratio of R1 and R2 and Rsense the current sense resistor (see figure 3).

K_M [dimensionally, 1/V] is actually a function of the operating point (an intentional non-linearity vs. V_C is introduced in the multiplier of the L6562 to partly compensate for the gain changes with the input voltage: in particular, j_2 is proportional to k^2), but the value specified in the datasheet can be used with good approximation.

R_o is the incremental load resistance. The nature of the load driven by the PFC pre-regulator determines its value. If the load is of resistive type, Ro coincides with the static resistance value:

$$Ro = \frac{\partial Vout}{\partial Iout} = \frac{Vout}{Iout} = \frac{Vout^2}{Pout}.$$

In the important case of a DC-DC converter, which can be regarded as a constant power load, the low-frequency incremental load resistance is negative:

$$Ro = \frac{\partial Vout}{\partial Iout} = -\frac{Pout}{Iout^2} = -\frac{Vout^2}{Pout}$$

The control-to-output transfer function is:

$$\frac{\hat{v}out}{\hat{v}_c} = j_2 \cdot \frac{Ro // r_2}{1 + sCoRo // r_2},$$

while the line-to-output transfer function is:

$$\frac{\hat{v}out}{\hat{k}} = g_2 \cdot \frac{Ro // r_2}{1 + sCoRo // r_2}.$$

In the case of constant power load (PFC stage supplying a cascaded DC-DC converter), unlike TM and FF-CCM systems, where the parallel combination of r_2 and Ro tends to an open circuit, thus placing the pole of the transfer functions at the origin, in FOT-CCM systems the combination maintains a finite value:

$$Ro // r_2 = \frac{\pi Vout}{k\Gamma},$$

so that the pole is still at a finite frequency that moves with the line voltage:

$$f_p = \frac{1}{2\pi(Ro // r_2)Co} = \frac{k\Gamma}{2\pi^2 VoutCo} = \frac{k\,T_{OFF}}{2\pi^2 LCo}.$$

The DC gain of the control-to-output transfer function is:

$$G_0 = \left.\frac{\hat{v}out}{\hat{v}_C}\right|_{s=0} = j_2(Ro // r_2) = \frac{\pi k K_M K_P}{2\Gamma}\frac{Vout^2}{R_{sense}} = \frac{\pi k K_M K_P}{2}\frac{VoutL}{T_{OFF}Rsense}.$$

FOT-CCM PFC pre-design considerations.

Operating frequency and T_{OFF} selection. When specifying the operating frequency of a FOT-controlled PFC stage, some care must be taken of the resulting minimum ON-time of the power switch T_{ONmin}. As it can be easily derived from table 2, this occurs on the top of the sinusoid at maximum line voltage and its value is:

$$T_{ONmin} = \frac{1 - k_{max}}{k_{max}} T_{OFF}. \quad (2)$$

If one wants to ensure the operation described by the large-signal model considered so far over the full input voltage range, this value has to be greater than the minimum ON-time that the L6562 is able to handle (350 ns max.) plus the MOSFET's turn-on and turn-off delays (assume 150ns total). In wide-range mains applications this means a minimum value of 6.96µs for T_{OFF} and a maximum operating frequency (i.e. on the top of the sinusoid) at minimum line voltage not greater than 45 kHz, which could be quite a limitation, especially in view of a small-size inductor (see next paragraph). Actually, if the condition $T_{ON} > T_{ONmin}$, with T_{ONmin} given by (2), is not met in an area around the top of the sinusoid, there will be a temporary unbalance of the volt·second across the inductor, so that the cycle-by-cycle average inductor

current will grow. If the system is designed so that this occurs at high line, where the inductor current is considerably lower than its maximum values (less than one half), there is no risk of core saturation.

The most conspicuous consequence will be an increased line current distortion: the energy in excess around the top of the sinusoid will be balanced by a corresponding reduction across the zero crossings, so that the current waveform will get narrower and more peaked. As a result, at high line the harmonic contents will be higher than expected. This increased distortion may be still acceptable, provided the class-D limits of the EN61000-3-2 standards are not exceeded at rated load and Vin=230Vac, as prescribed by the standard, with some safety margin. However, a slight modification of the control technique can significantly improve this situation (see "An improvement of FOT control" section) and allow compliance with the standard over a wider load range.

Ripple current (Kr) selection. The selection of the ripple current is a trade-off between inductor size, ease of EMI filtering and line current distortion. Low values of Kr, which result in low inductor current ripple and a lighter input line filter for EMI compliance, lead also to a lower line current distortion because the CCM region inside a line half-cycle is extended, hence making the sinusoidal portion of $I_{in}(\theta)$ more and more dominant. On the other hand, however, a low Kr results in a larger inductance L and, in the end, in a larger magnetic core. Typical values for Kr range from 0.25 to 0.40.

Inductor selection. If a ferrite core is to be used, due to the moderate switching frequency, the maximum flux density B_{max} will be typically limited by core saturation and not by core losses. This also means that transformer's power losses will be located mostly in the windings. Referring to commonly used Area-Product formulae [5], a first-cut estimate of the minimum required core size is:

$$AP_{min} \approx 186\left(\frac{1-k_{min}Kr}{k_{min}Kr}\cdot\frac{Pin_0 T_{OFF}}{B_{max}}\right)^{1.31} \quad [cm^4] .$$

This formula accounts also for the tolerance of the current limit threshold of the L6562 (see next section). At a higher operating frequency core losses might be dominant, but usually the losses related to diode recovery force to select a switching frequency where core losses do not dominate yet. As to core losses, there is no worry about the frequency increase with the line voltage pointed out by figure 8 (there is a factor of three): at high line the inductor ripple, and then the flux swing, becomes very small (typically, 10 times smaller).

In case the system is operated at a moderate switching frequency, it is worthwhile trying to use ferrous alloy powder toroidal cores like Kool-Mμ from Magnetics or -xx from Micrometals, especially if working with quite low Kr values. Typically, core losses will be higher than in a ferrite core and the resulting total efficiency will be not as high as, but in some cases this could be a tolerable penalty.

"Tracking boost" configuration. In some applications it may be advantageous to regulate the output voltage of the PFC pre-regulator so that it tracks the RMS input voltage rather than at a fixed value like in conventional boost pre-regulators. This approach, commonly referred to as "tracking boost" or "follower boost", brings some benefits, such as reduction of the MOSFET's RMS current and of transformer's size, and some drawbacks, such as increased diode current, increased low-frequency output ripple and requiring the downstream converter to accommodate a larger input voltage range.

Basically, the tracking boost approach reduces the range of the parameter k increasing its minimum value k_{min}. This stated, the benefit of core size reduction becomes apparent if one looks at the above given AP_{min} formula. Also the frequency change is reduced and the limits concerning T_{ONmin} for a full FOT operation are pushed upwards.

For instance, if the regulated output voltage @Vin=88Vac is set at 250V (and at 400V @Vin=264Vac), k_{min} will be 0.498 (instead of 0.311), thus the maximum switching frequency @Vin=88Vac for a full FOT operation can be as high as 70 kHz; @Vin=88Vac the MOSFET current is reduced by 11% and its conduction losses by about 22%, whereas the DC and RMS diode current are increased by 60% and 27% respectively; the $2\cdot f_L$ output ripple will be typically increased by about 60%; the minimum AP required for the inductor core, for the same Kr and B_{max}, is reduced by 50%.

FOT-CCM PFC design procedure.

The starting point is the electrical design specification, which we assume is as shown in table 5. Actually, a number of requirements is not directly related to the FOT control technique and will be used exactly like in the design of standard TM or FF-CCM PFC pre-regulators. Of course, in this context special emphasis will be given only to the points directly related to FOT control.

Table 5. Basic electrical specification of a FOT-CCM PFC stage

Parameter	Symbol
Line voltage range	$Vin_{(RMS)min} \div Vin_{(RMS)max}$
Minimum Line frequency	f_{Lmin}
Regulated output voltage	Vout
Rated output power	$Pout_0$
Maximum $2f_L$ output voltage ripple	$\Delta Vout_{pk-pk}$
Hold-up time	T_H
Min./max./mean switching frequency (@Vin=$Vin_{(RMS)min}$, Pout=$Pout_0$)	$f_{swmin}/f_{swmax}./f_{sw(m)}$
Estimated efficiency	η
Max. inductor current ripple-to-peak ratio (@Vin=$Vin_{(RMS)min}$, Pout=$Pout_0$)	Kr (= $sin\,\theta_T$)
Ambient temperature range	$Tamb_{min} \div Tamb_{max}$

Based on this information and on the results presented in the previous sections, the recommended step-by-step design procedure is the following:

1) Calculate the range of k ($k_{min} \div k_{max}$) associated to the line voltage range:

$$k_{min} = \sqrt{2} \cdot \frac{Vin_{(RMS)min}}{Vout} \quad , \quad k_{max} = \sqrt{2} \cdot \frac{Vin_{(RMS)max}}{Vout} \quad .$$

2) Calculate the required T_{OFF} from the specification on the switching frequency. If f_{swmax} is specified use:

$$T_{OFF} = \frac{k_{min}}{f_{swmax}} \quad ;$$

if f_{swmin} is specified use:

$$T_{OFF} = Kr\frac{k_{min}}{f_{swmin}} \quad ;$$

if $f_{sw(m)}$ (average value within a line half-cycle) is specified use:

$$T_{OFF} = \frac{1 + Kr}{2}\frac{k_{min}}{f_{sw(m)}} \quad .$$

3) Calculate $Pin_0=Pout_0/\eta$ and determine Γ:

$$\Gamma = \frac{Pin_0}{k_{min}Vout} \quad \frac{4\pi Kr}{2\pi - Kr(4 + \pi k_{min})} \quad .$$

4) From the value of Γ calculate the required inductance L of the boost inductor:

$$L = \frac{Vout}{\Gamma} T_{OFF} .$$

5) Calculate the maximum inductor peak current I_{Lpkmax} using the value of Γ found in step 3:

$$I_{Lpk\ max} = \frac{Pin_0}{k_{min} Vout} \frac{4\pi(1 - Kr\ k_{min})}{2\pi - Kr(4 + \pi k_{min})} = \Gamma \frac{1 - Kr\ k_{min}}{Kr} .$$

6) Determine the maximum sense resistor $Rsense_{max}$:

$$Rsense_{max} = \frac{1.6}{I_{Lpk\ max}} ,$$

and select a resistor value Rsense < $Rsense_{max}$. 1.6V is the minimum value of the pulse-by-pulse current limiting threshold on the current sense pin of the L6562. Take into account that the value of this threshold can go as high as 1.8V, hence the inductor must not saturate up to a current equal to 1.8/Rsense.

7) Calculate the current stress of all components, design the boost inductor with any commonly used procedure, and select the MOSFET and the diode. Use either the output voltage ripple or the hold-up specification, whichever gives the higher capacitance value, to select the output capacitor.

8) Design the bias component around the controller IC (multiplier setpoint and feedback) using the same criteria given for TM systems [6], just considering the different small-signal model as to the feedback design. Finally design the circuit that sets up FOT control:
   8a. Select a capacitor C in the hundred pF or few nF. Like in an FF controller, the tolerance of this capacitor and its temperature drift will affect the resulting timing.
   8b. Select the timing resistor value R from (α):

$$R = 0.7 \frac{T_{OFF}}{C}$$

   and pick the closest standard value.
   8c. Select the limiting resistor Rs using (β) and the speed-up capacitor Cs using (γ).

A practical FOT-CCM PFC design with the L6562.

As an example, a 375W design, e.g. suitable for a 300W ATX12V PSU will be now described following the procedure previously given. The electrical spec, listed in table 6, is consistent with ATX12V specification.

Table 6. Electrical specification of the design example of a 375W, L6562-based FOT-CCM PFC stage

Parameter	Value
Line voltage range	90 to 265 Vac
Minimum Line frequency	47 Hz
Regulated output voltage	400V
Rated output power	375 W
Maximum $2f_L$ output voltage ripple	20V pk-pk
Hold-up time	17 ms
Maximum switching frequency (@Vin=88Vac, Pout=375W)	100 kHz
Estimated efficiency (@Vin=88Vac, Pout=375W)	90%
Max. inductor current ripple-to-peak ratio (@Vin=88Vac, Pout=375W)	40%
Maximum ambient temperature	50 °C

Following the step-by-step procedure:

1) The range of k is:

$$k_{min} = 90\sqrt{2} / 400 = 0.318; \quad k_{max} = 265\sqrt{2} / 400 = 0.937.$$

2) The required OFF-time is:

$$T_{OFF} = \frac{0.318}{100 \cdot 10^3} = 3.18\mu s \ ;$$

the minimum ON-time will be:

$$T_{ONmin} = 3.18 \cdot 10^{-6} \frac{1 - 0.937}{0.937} = 0.21\mu s \ ,$$

which is shorter than the minimum ON-time handled by the L6562, hence significant additional distortion of the line current is expected at high line.

3) The expected maximum input power is:

$$Pin_0 = 375/0.9 = 417 \text{ W},$$

and Γ is:

$$\Gamma = \frac{417}{0.318 \cdot 400} \frac{4 \cdot \pi \cdot 0.4}{2 \cdot \pi - 0.4(4 + 0.318 \cdot \pi)} = 3.85 \quad [A].$$

4) The required inductance L of the boost inductor is:

$$L = \frac{400 \cdot 3.1 \cdot 10^{-6}}{3.85} = 322\mu H$$

that will be rounded up to 330 µH. Using the same value of Kr will give a small additional margin.

5) The maximum inductor peak current is calculated:

$$I_{Lpkmax} = 3.85 \cdot \frac{1 - 0.4 \cdot 0.318}{0.4} = 8.4A \ .$$

6) The maximum sense resistor $Rsense_{max}$ is:

$$Rsense_{max} = \frac{1.6}{8.4} = 0.19\Omega \ ;$$

it will be realized with four 0.68Ω, 1W-rated paralleled resistors, for a total resistance of 0.17Ω. The inductor peak current that the inductor must be able to carry without saturating will be:

$$I_{Lpksat} = \frac{1.8}{0.17} = 10.6A \ .$$

7) From the formulae in table 4, the MOSFET RMS current is:

$$I_{Q(rms)} = \frac{417}{0.318 \cdot 400} \sqrt{2 - \frac{16 \cdot 0.318}{3 \cdot \pi}} = 3.96A \ ;$$

the diode RMS current is:

$$I_{Q(rms)} = \frac{417}{0.318 \cdot 400}\sqrt{\frac{16 \cdot 0.318}{3 \cdot \pi}} = 2.41A \ ;$$

the dissipation on the sense resistor will be $0.17 \cdot 3.96^2 = 2.7W$, which justifies the use of four resistors; the selected MOSFET is the STW26NM50, a 0.12Ω/500V MdmeshT^M type from STMicroelectronics, housed in a TO247 package; the selected diode is an STTH8R06, a 8A/600V Turbo 2 Ultrafast recovery rectifier again from STMicroelectronics, housed in a TO220 package. Both of these must be dissipated to keep their temperature within safe limits.

As for the inductor, assuming a peak flux density B_{max}=0.3T, a core with a AP_{min} = 1.91 cm^4 is needed and an E42 core has been chosen. The complete inductor spec can be found in the electric circuit diagram in figure 17.

The output capacitor is determined by the hold-up time requirement. Assuming a minimum voltage of 300V after the line drop, a minimum of 180 µF is needed and a 220µF/450V capacitor will be used.

8) a) A C=560 pF film capacitor is selected.

b) The timing resistor is:

$$R = 0.7\frac{3.18 \cdot 10^{-6}}{560 \cdot 10^{-12}} = 3975\Omega \ ;$$

the closest standard value (3.9 kΩ) will be selected.

c) The limiting resistor Rs will be such that:

$$\frac{15 - 5.7 - 0.5}{10 \cdot 10^{-3} + \frac{5.7}{3.9 \cdot 10^{-3}}} = 768\Omega < Rs < 3.9 \cdot 10^{-6}\frac{10 - 5.7 - 0.5}{5.7} = 2600\Omega \ ;$$

since there is no need to stress the clamp a 2.4 kΩ resistor will be chosen. The maximum speed-up capacitor is:

$$Cs < 560 \cdot 10^{-12}\frac{5.7}{15 - 5.7 - 0.5} = 362pF \ ;$$

a 330 pF film capacitor will be used.

The electrical schematic is shown in figure 17. A prototype of this circuit has been realized and evaluated on the bench. Figures 18 and 19 show a series of diagrams illustrating its performance.

Figure 17. 375W FOT-CCM PFC pre-regulator: electrical schematic.

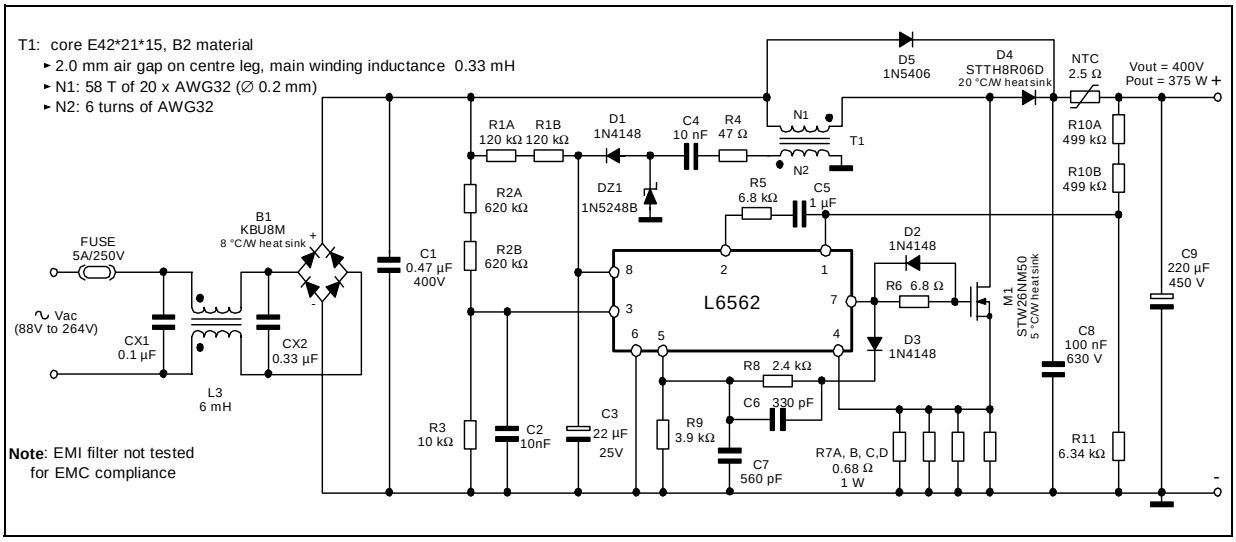


Figure 18. 375W FOT-CCM PFC pre-regulator: evaluation data.

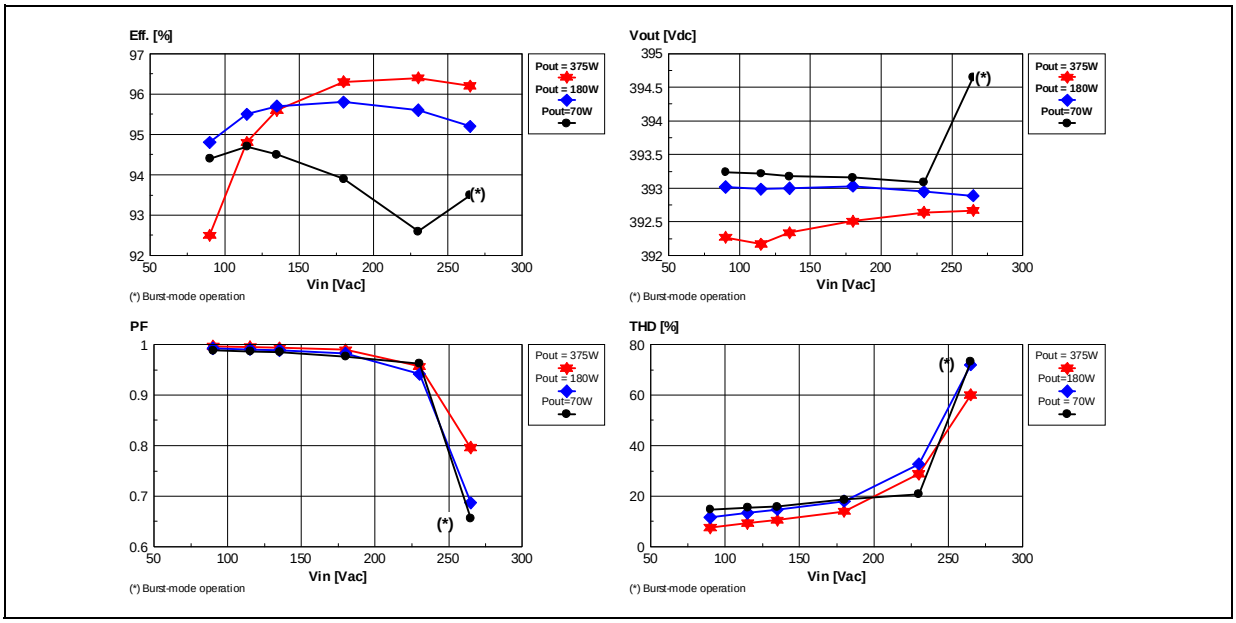
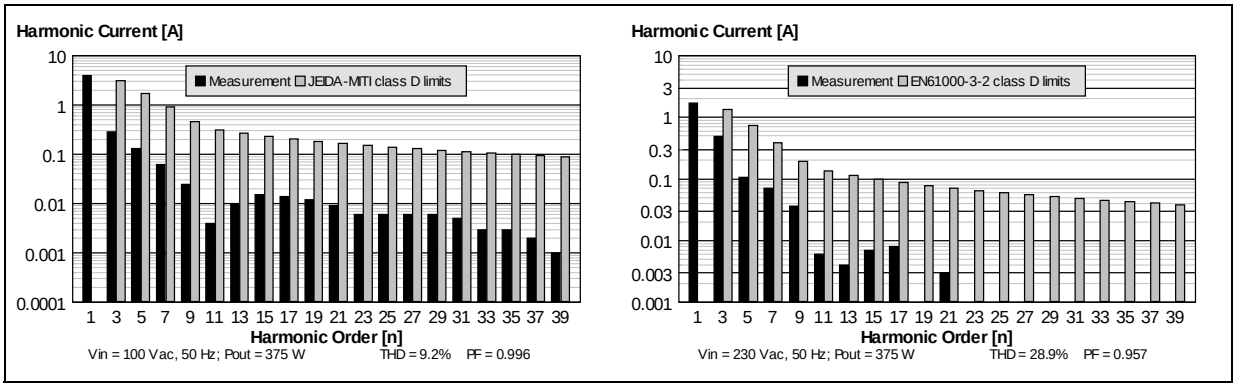


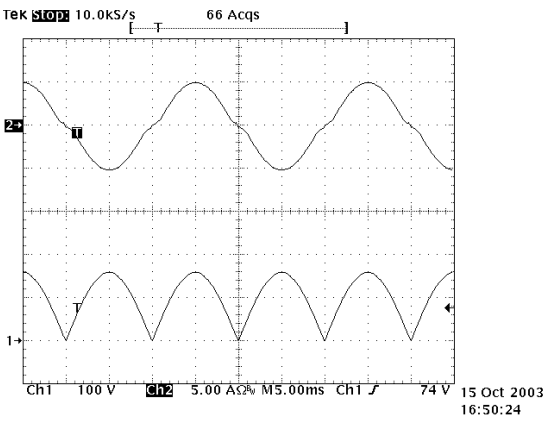
Figure 19. 375W FOT-CCM PFC pre-regulator: conformity to JEIDA-MITI and EN61000-3-2 standards.



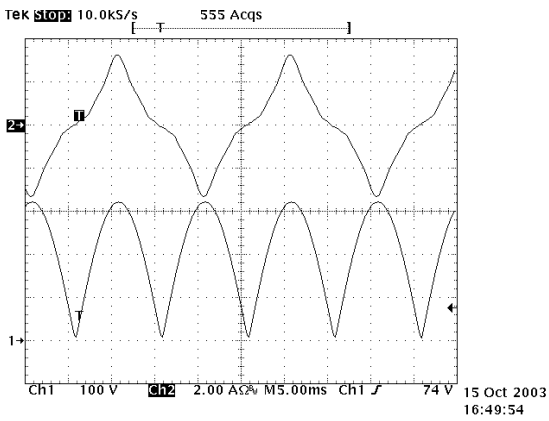
Figures 20 to 22 show the line current waveforms under the operating conditions considered in the diagrams of figure 18 (100%, 50% and 20% of the rated load) at nominal voltage of both US and European mains. Note: the waveforms are taken with an acquisition method that eleminates high frequency ripple, just to show the low frequency component, the "odd counterpart" of the average inductor current.

Figure 23 shows a close image of the line current waveform under two different operating conditions: on the left (a), the waveform is taken at low line, and one can easily recognize the shape as well as the DCM and the CCM portions as per the theory; on the right (b), the waveform, taken at high line, clearly shows the distortion due to the condition $T_{ON}>T_{ONmin}$, with T_{ONmin} given by (2), not met throughout a line cycle. Note that in the portion where this occurs, the system is running at a fixed frequency $f_{sw}= 1/(T_{ONmin}+T_{OFF})$. The theoretical current, which assumes it is always $T_{ON}>T_{ONmin}$ and does not exhibit additional distortion, is shown in red.

Figure 20. 375W FOT-CCM PFC pre-regulator: line current waveforms @ Pout=375W.

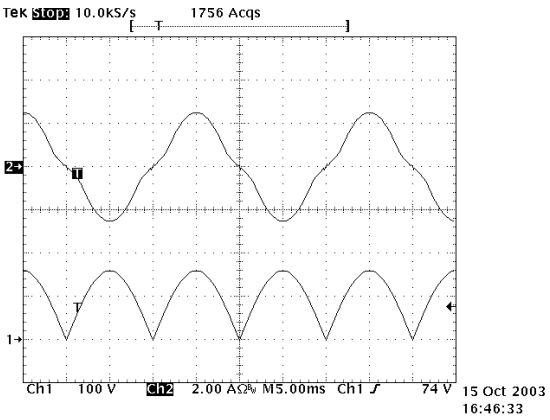


Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=115Vac, Pout=375W)

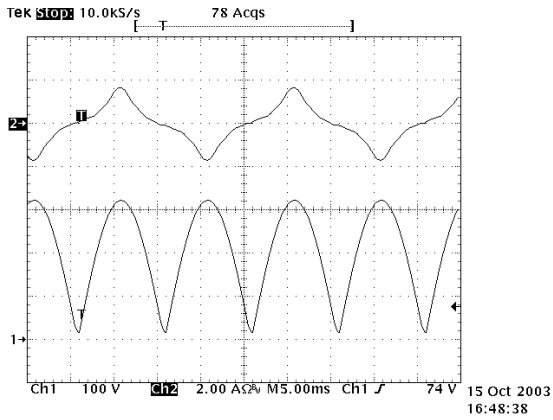


Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=230Vac, Pout=375W)

Figure 21. 375W FOT-CCM PFC pre-regulator: line current waveforms @ Pout=180W.

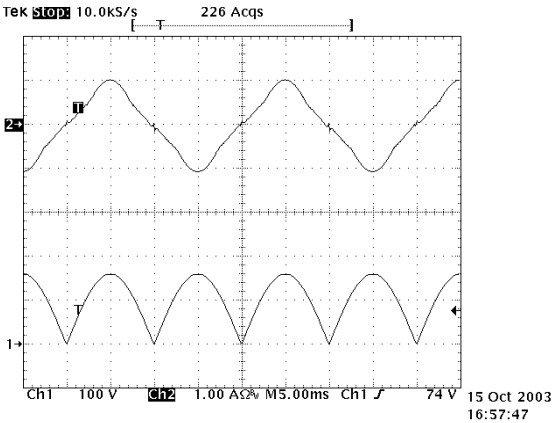


Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=115Vac, Pout=180W)

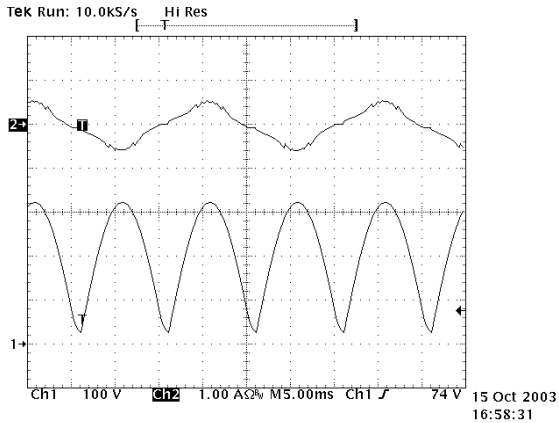


Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=230Vac, Pout=180W)

Figure 22. 375W FOT-CCM PFC pre-regulator: line current waveforms @ Pout=70W.

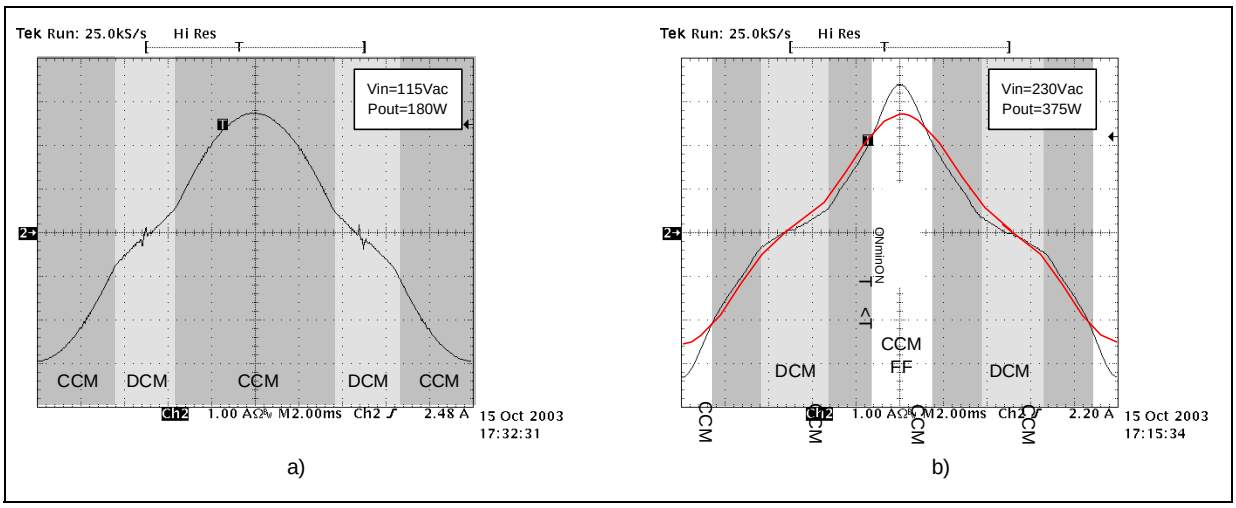


Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=115Vac, Pout=70W)



Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=230Vac, Pout=70W)

Figure 23. Line current: a) at low line; b) at high line, with the additional distortion due to violation of the condition $T_{ON}>T_{ONmin}$ for some part of the line cycle (in red the theoretical curve).



An improvement of FOT control

The most severe limitation of FOT control seems to be the trade-off between operating frequency and distortion of the line current waveform pointed out in the *"Operating frequency and T_{OFF} selection"* sub-section. As a matter of fact, if T_{OFF} is selected for an operating frequency above 60-70 kHz on the top of the sinusoid at minimum line voltage, the harmonics of the line current may exceed the class-D limits of EN61000-3-2 at maximum line voltage (264Vac). Actually the standard prescribes the measurement of the harmonic current emissions to be done at the nominal voltage (230 Vac) and rated load but sometimes the PSU is specified to stay within the limits under a range of operating conditions, e.g. throughout the input voltage range and/or from rated load down to a minimum value. In this case a trade-off could be difficult or even impossible to find.

A simple modification of the standard Fixed-Off-Time technique can overcome this possible issue. The idea behind is to make T_{OFF} a function of the line voltage, so that at high line it is long enough to ensure that the condition $T_{ON}>T_{ONmin}$, with T_{ONmin} given by (2), is met throughout the entire line cycle. Probably the simplest way to do so is shown in figure 24a, where T_{OFF} is made a function of the instantaneous line voltage. The circuit of figure 24b makes T_{OFF} a function of the RMS line voltage thanks to the peak-holding effect of T1 (which acts as a buffer) along with Ra and Ca whose time constant is significantly longer than a line half cycle. In the following, reference will be made only to the circuit of figure 24a.

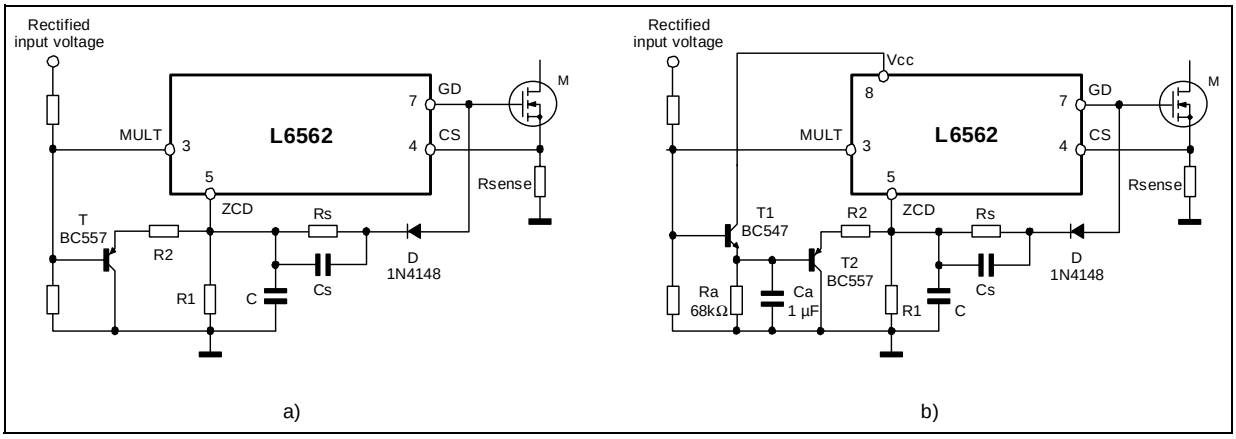
With the addition of R2 and T, as long as the voltage on the ZCD pin during T_{OFF} is above $V_{MULT}+V_{BE}$, C is discharged through R1 and R2, following the law:

$$V_{ZCD}(t) = \left[V_{ZCDclamp} - \frac{R1}{R1+R2}(V_{MULT}+V_{BE})\right]e^{-\frac{t}{(R1//R2)C}} + \frac{R1}{R1+R2}(V_{MULT}+V_{BE});$$

as $V_{ZCD}(t)$ falls below $V_{MULT}+V_{BE}$, T is cut off and C is discharged through R1 only, so that its evolution from that point on is described by:

$$V_{ZCD}(t) = \frac{R1}{R1+R2}(V_{MULT}+V_{BE})e^{-\frac{t}{R1C}}.$$

Figure 24. Improved FOT control; T_{OFF} changes with: a) the instantaneous, b) the RMS line voltage.



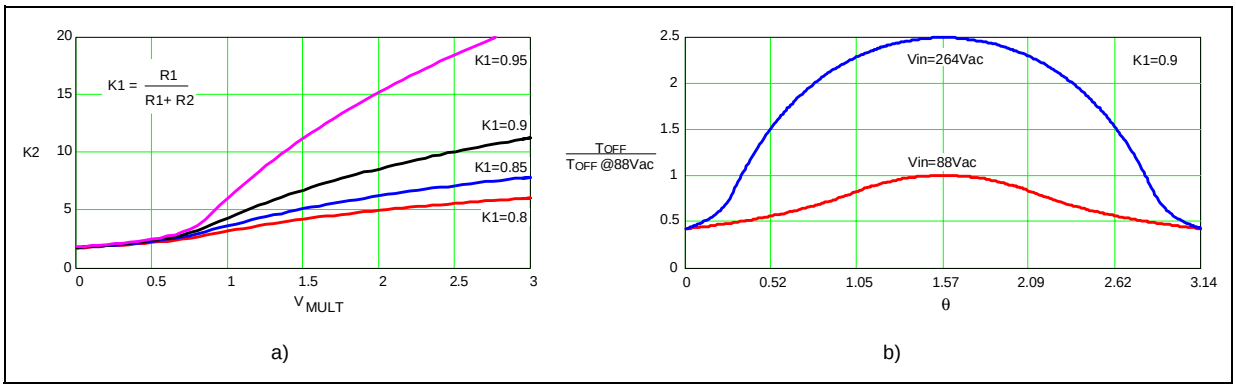
In this way, once fixed the multiplier operating point (that is, the V_{MULT} /Vin ratio), with a proper selection of R1 and R2 it is possible to increase T_{OFF} with the line voltage so that at maximum line voltage it is always T_{ON}>T_{ONmin}. It is easy to see that T_{OFF} is now a function of the instantaneous line voltage. We will refer to this technique as "Line-modulated Fixed-Off-Time" (LM-FOT).

This modification, though simple, introduces profound changes in the timing relationships, with a positive influence on the energetic relationships. From the control point of view, modulating T_{OFF} is a feedforward term that modifies the gain but does not change its characteristics. Then all of the properties of the standard FOT control are maintained.

Due to the highly non-linear nature of the T_{OFF} modulation introduced by T and R2, its effects will be discussed only qualitatively and the quantitative aspects will be provided graphically for a specific case.

Figure 25a shows the dependence of T_{OFF} upon the time constant $\tau = (R1//R2)\cdot C$, $T_{OFF} = K2\cdot\tau$, for different values of the (R1, R2) divider ratio K1 = R1/(R1+R2). In this diagram and the following ones, it is assumed V_{BE} = 0.55V. As long as it is $V_{MULT}+V_{BE} < V_{ZCDtrigger}$, that is V_{MULT} < 0.85V, there is little effect on T_{OFF}, while the effect becomes considerable for higher values of V_{MULT}. Figure 25b shows how T_{OFF} (normalized to the value on the top of the sinusoid at minimum line voltage) changes along a line half-cycle at minimum and maximum line voltage for the particular case of K1=0.9. The multiplier peak voltage @Vin=88Vac is assumed to be 1V, resulting in T_{OFF}@Vin=264Vac 2.5 times longer.

Figure 25. LM-FOT: a) T_{OFF} modulation with the circuit of fig. 25a; b) T_{OFF} change in a line half-cycle.



Figures 26 to 32 are the analogous of figures 8-14: they refer to the same representative system, with the addition of T_{OFF} modulation. The value of T_{OFF} on the top of the line voltage sinusoid at minimum mains is the same as in the system of figures 8-14, so that the switching frequency is the same in that point. Quantities are normalized with the same criteria.

At low line the switching frequency dos not change much, however, the noticeable point is that, since T_{OFF} gets shorter next to the line voltage zero-crossings, the CCM portion in a line half cycle is enlarged. The result is that peak currents will be lower and all RMS currents will be closer to those of a FF-CCM system. Also line current shape will get closer to a perfect sinusoid, then both PF and THD will improve (see figure 32).

At high line the switching frequency, which stays close to the minimum around the top of the sinusoid, is only about 20% higher than that at minimum line (instead of 3 times). Efficiency will definitely benefit from that. Around zero-crossings, the frequency increases about 2.5 times, but the power handled in those regions is not high, then the erosion on the efficiency improvement will be minimum. The minimum ON-time goes from 7.1% to 17.8% of the normalized T_{OFF} value but the CCM portion gets narrower: the THD will improve because it is now easy to have $T_{ON}>T_{ONmin}$, hence eliminating the related additional distortion, but the achievable value is slightly worse. However, diode reverse recovery-related losses will be further reduced, in favor of efficiency. Line current wave shape changes little. Note that the maximum inductor current ripple changes little as well but in a line half-cycle it does not occur on the CCM-DCM boundary any more.

Figure 26. Normalized switching frequency vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

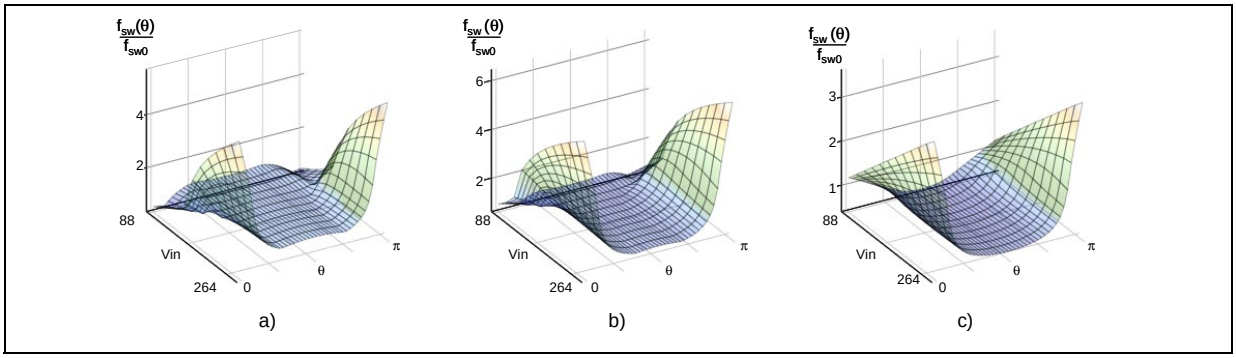


Figure 27. Normalized MOSFET's ON-time vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

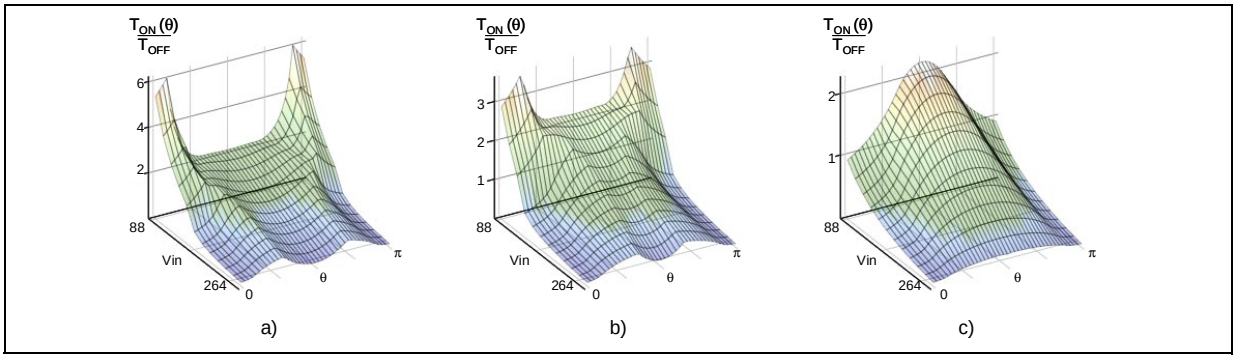


Figure 28. Inductor current conduction angle vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

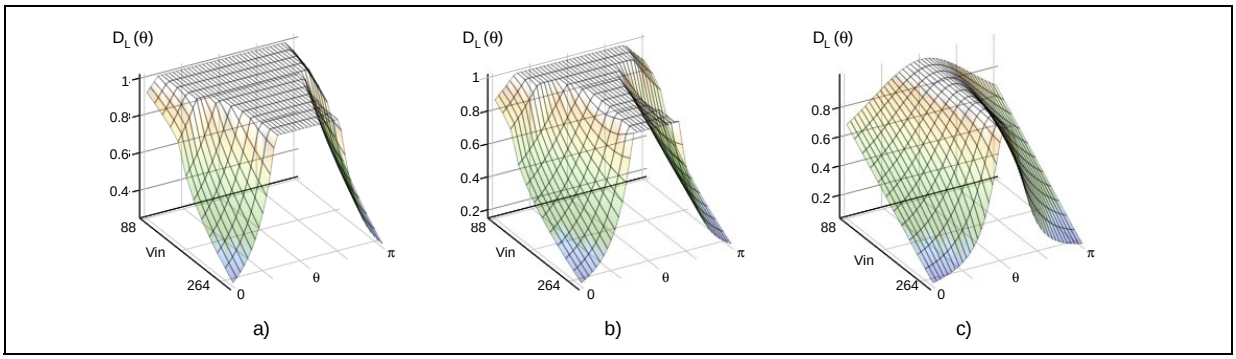


Figure 29. Line current vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

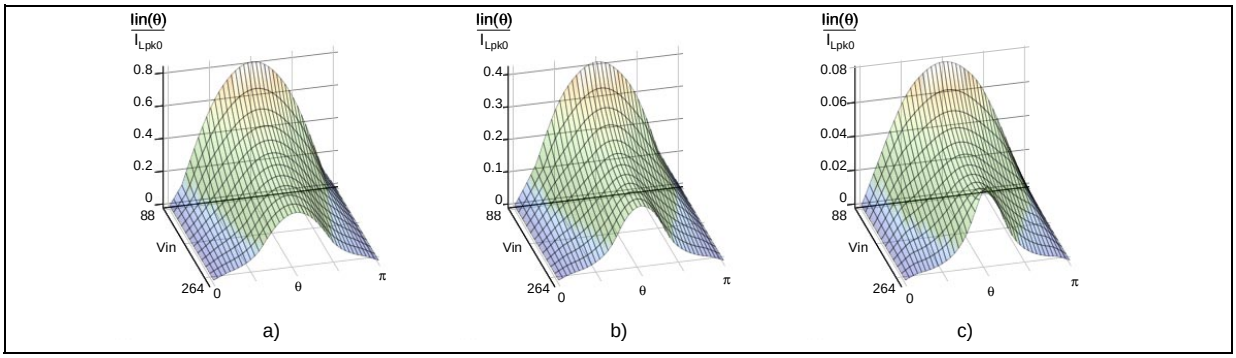


Figure 30. Inductor current ripple vs. phase angle: a) Full load Pin_0; b) $Pin_0/2$; c) $Pin_0/10$

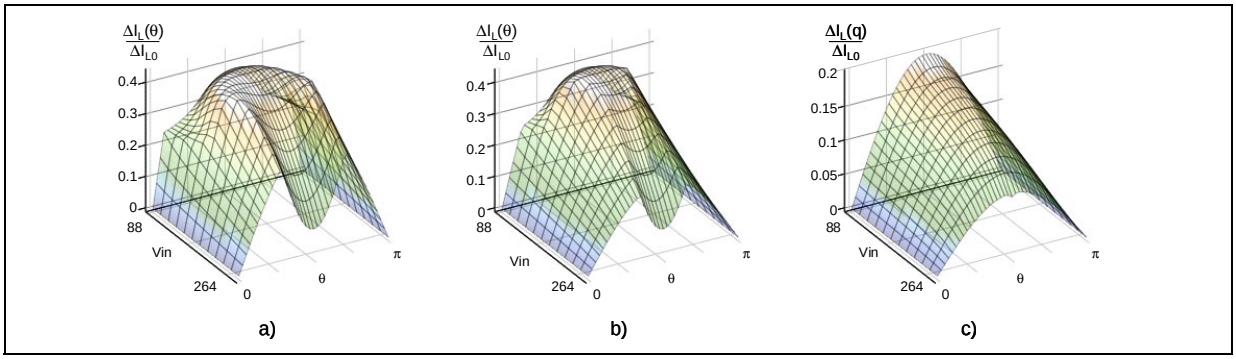


Figure 31. a) Normalized Inductor peak current; b) Normalized line peak current; c) Transition angle

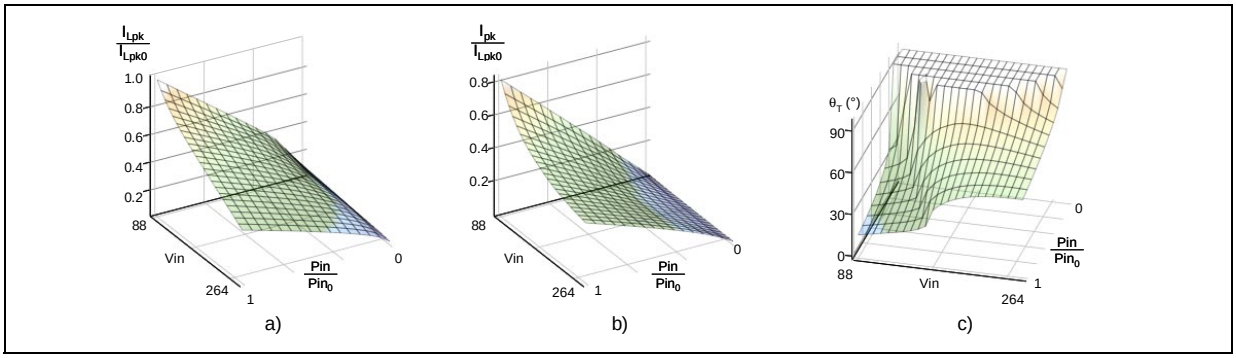
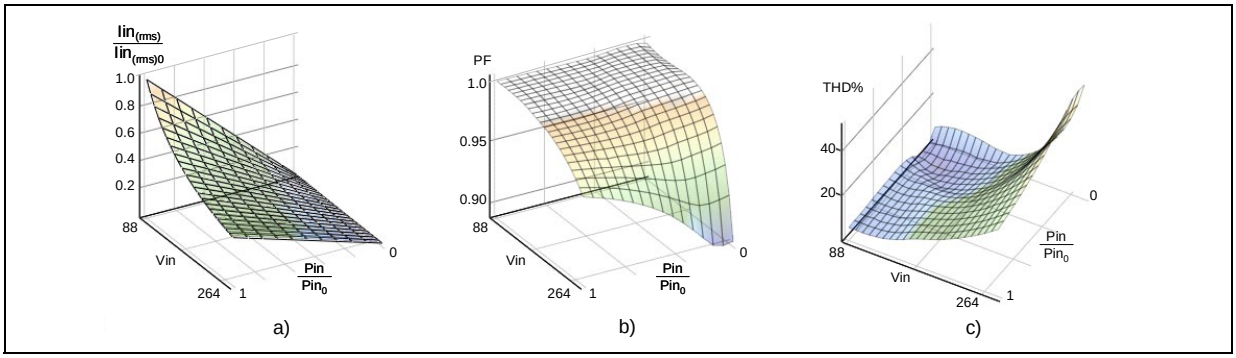
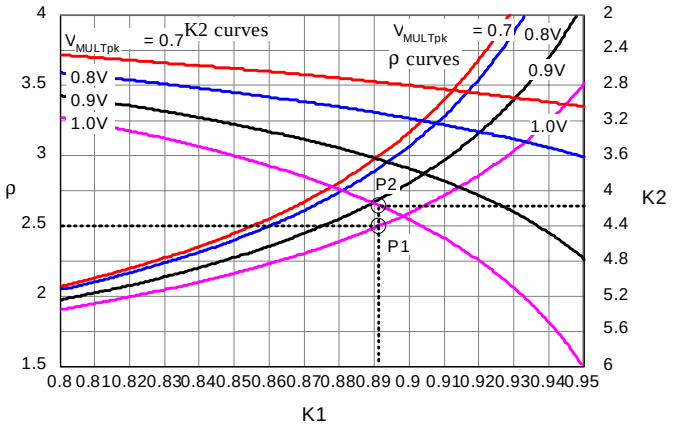


Figure 32. a) Normalized line RMS current; b) Power Factor; c) Total Harmonic Distortion



The starting point for the design of the circuit of figure 25a is the pair of the desired values for T_{OFF} on the top of the line voltage sinusoid at minimum (T_{OFF}@Vin=$Vin_{(RMS)min}$) and maximum line (T_{OFF}@Vin=$Vin_{(RMS)max}$). Let ρ their ratio: ρ = T_{OFF}@Vin=$Vin_{(RMS)max}$ / T_{OFF}@Vin=$Vin_{(RMS)min}$. With these data the design can be done with the aid of the diagrams in figure 33. The diagrams, which assume an input voltage range 88-264 Vac, features two sets of curves, ρ curves and K2 curves, each of them plotted for a particular value of the peak multiplier voltage V_{MULTpk} @88Vac.

Figure 33. Diagrams for the design of the circuit of figure 24a (valid for Vacmin=88V, Vacmax=264V).



The suggested step-by-step design procedure is the following:

1) Determine the multiplier setpoint using the same criteria given for TM systems [6] and take note of the resulting V_{MULTpk} @88Vac value. It should be between 0.7 and 1V.

2) Draw an horizontal line located at the desired value of ρ (on the left vertical axis) as long as it intercepts the curve relevant to the value V_{MULTpk} previously determined in P1. The abscissa of P1 gives the necessary value of the parameter K1.

3) From P1 draw a vertical line as long as it intercepts the K2 curve relevant to the same value of V_{MULTpk} in P2. The ordinate of P2 (on the right vertical axis) gives the necessary value of K2.

4) Calculate the time constant τ =(R1//R2) C necessary to achieve the desired T_{OFF}@88Vac:

$$\tau = \frac{T_{OFF}\ @\ 88Vac}{K2} \ .$$

5) Select a capacitor C in the hundred pF or few nF, and determine the required resistance value:

$$R' = R1//R2 = \frac{\tau}{C} \ .$$

6) Determine R1 and R2:

$$R1 = \frac{R'}{1-K1} \qquad R2 = \frac{R'}{K1} \ . \quad (23a, b)$$

7) Select the limiting resistor Rs according to the following inequalities:

$$\frac{V_{GDx} - V_{ZCDclamp} - V_F}{I_{ZCDx} + \frac{V_{ZCDclamp}}{R1}} < Rs < \frac{(V_{GD} - V_{ZCDclamp} - V_F)R1R2}{(V_{ZCDclamp} - V_{BE})R1 + V_{ZCDclamp}R2} \ ,$$

and the speed-up capacitor Cs using (γ).

The 375W design will now be modified to implement LM-FOT. The target is to keep T_{OFF} = 3.18 µs @90Vac and to get T_{OFF} = 8 µs @265Vac, thereby ρ = 8/3.18 ≈2.5. The input voltage range, although different from, is very close to that covered by the diagrams of figure 33, then these curves are still appli-

cable. Following the above given step-by-step procedure:

1) From the part values in the schematic diagram of figure 17, V_{MULTpk} @90Vac=1.02V, then the curves for V_{MULTpk} =1V will be considered.
2) In figure 33 the points P1 and P2 are shown; the resulting values for K1 and K2 are 0.891 and 4.17 respectively.
3) The required time constant is:

$$\tau = \frac{3.18 \cdot 10^{-6}}{4.17} = 0.76 \cdot 10^{-6} s \ .$$

4) The same capacitor (C=560 pF) will be used, then the associated resistance value will be:

$$R' = \frac{0.76 \cdot 10^{-6}}{560 \cdot 10^{-12}} = 1357\Omega \ .$$

5) R1 and R2 will be respectively:

$$R1 = \frac{1357}{1-0.891} = 12450\Omega \qquad R2 = \frac{1357}{0.891} = 1523\Omega \ ;$$

the standard values R1=12kΩ and R2=1.5kΩ will be chosen.

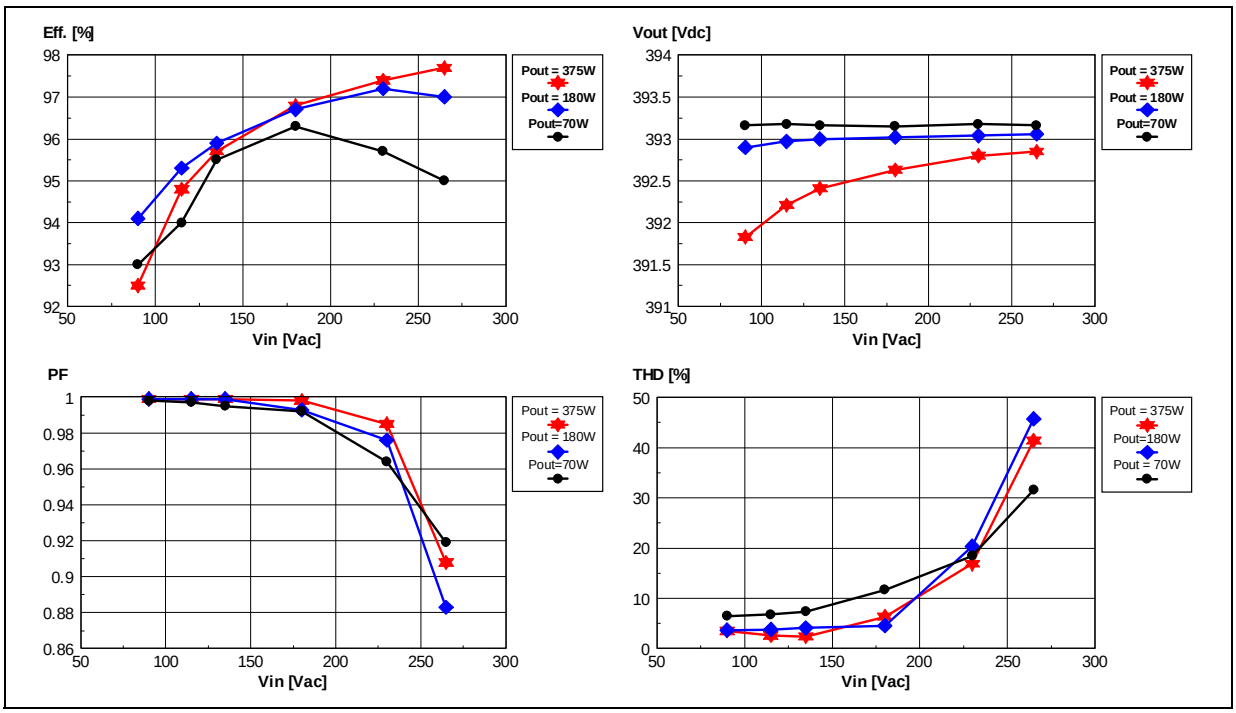
6) Under the worst-case condition, only R1 will divert some current from the ZCD pin to ground, then the limiting resistor Rs must be selected according to:

$$\frac{15-5.7-0.5}{10 \cdot 10^{-3} + \frac{5.7}{12 \cdot 10^{-3}}} = 840\Omega < Rs < \frac{(10-5.7-0.5)1.5 \cdot 10^{3} 12 \cdot 10^{3}}{(5.7-0.55)12 \cdot 10^{3} + 5.7 \cdot 1.5 \cdot 10^{3}} = 972\Omega \ ;$$

in this case a 910Ω resistor will be chosen. Cs will be the same 330 pF capacitor.

The prototype, modified as per the above guidelines, has been evaluated to check the actual differences with the former realization. Figures 34 to 38 show a series of diagrams illustrating its performance.

Figure 34. 375W LM-FOT-CCM PFC pre-regulator: evaluation data.



Comparing these results with those in figure 18, the full-load efficiency does not change significantly at low line, but improves by as much as 1% @230Vac and 1.5%@265Vac, getting close to 98%; also half-load efficiency exceeds 97% @230Vac; full-load PF at maximum line voltage increases from 0.8 to 0.91 thanks to a THD% reduction from 60% to 41%; even more significant is the THD% reduction at light load, which makes confident that EN61000-3-2 compliancy will be achieved not only at rated load but also at light load.

Figure 35. 375W LM-FOT-CCM PFC pre-regulator: conformity to JEIDA-MITI & EN61000-3-2 standards.

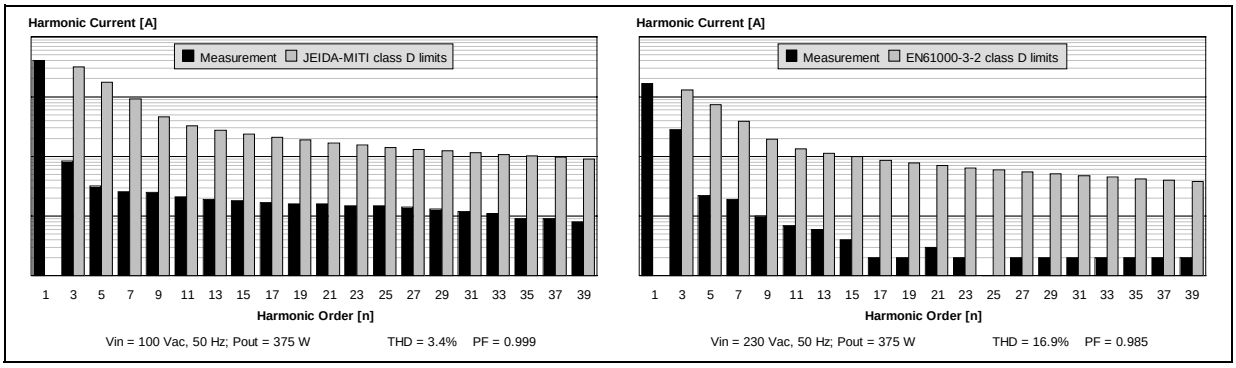


Figure 36. 375W LM-FOT-CCM PFC pre-regulator: harmonic emissions at half load (180W).

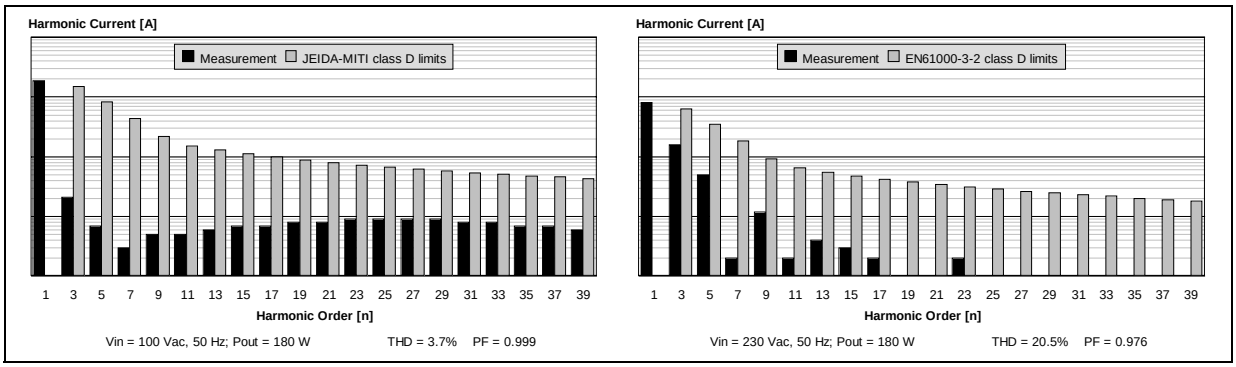


Figure 37. 375W LM-FOT-CCM PFC pre-regulator: harmonic emissions at light load (70W).

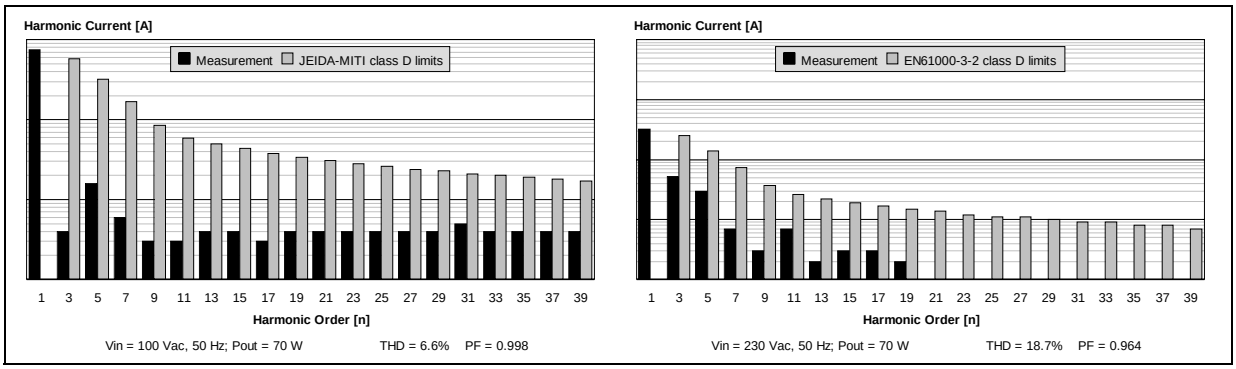
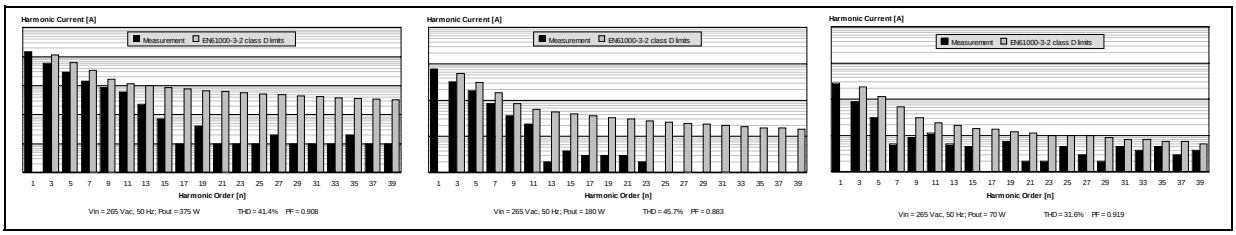
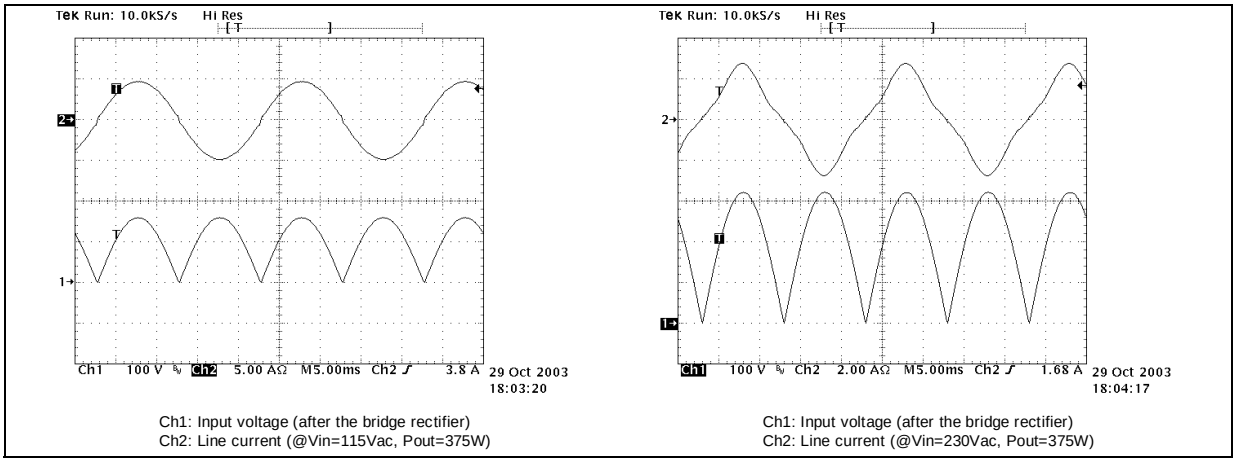


Figure 38. 375W LM-FOT-CCM PFC pre-regulator: harmonic emissions at 265Vac.



As to this point, the harmonic analysis shown in figures 35 to 38 confirms that. In particular, figure 38 shows that the emissions are within the limits even at light load and maximum line voltage. From the total distortion point of view, half-load seems to be the worst-case condition.

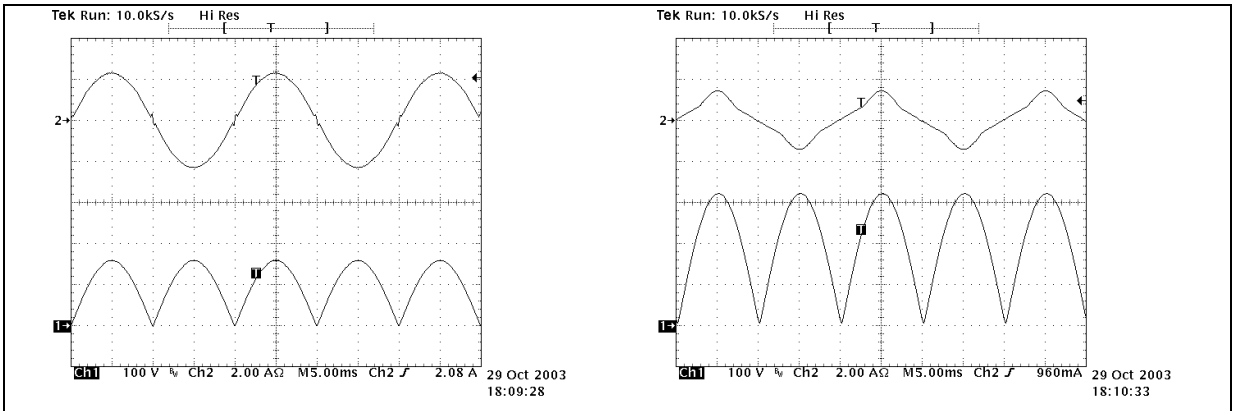
Figure 39. 375W LM-FOT-CCM PFC pre-regulator: line current waveforms @ Pout=375W.



Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=115Vac, Pout=375W)

Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=230Vac, Pout=375W)

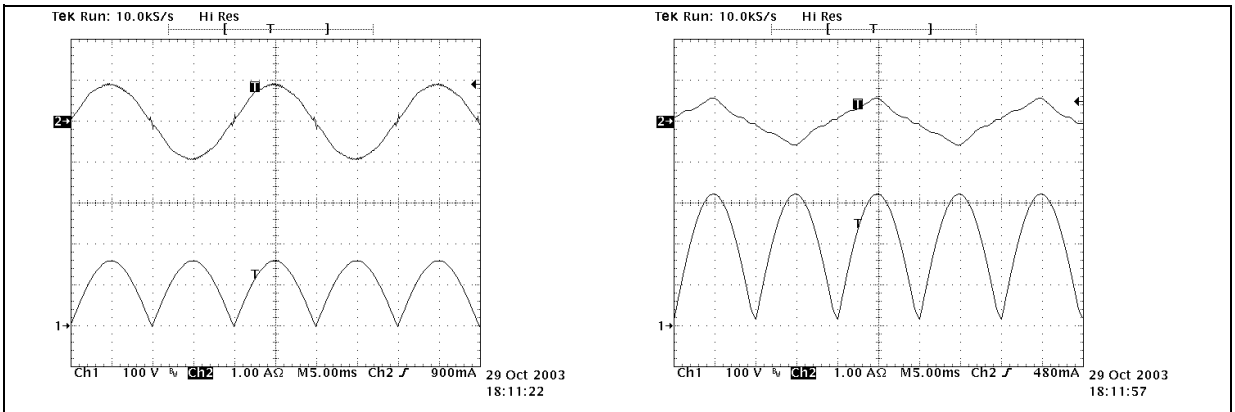
Figure 40. 375W LM-FOT-CCM PFC pre-regulator: line current waveforms @ Pout=180W.



Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=115Vac, Pout=180W)

Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=230Vac, Pout=180W)

Figure 41. 375W LM-FOT-CCM PFC pre-regulator: line current waveforms @ Pout=70W.

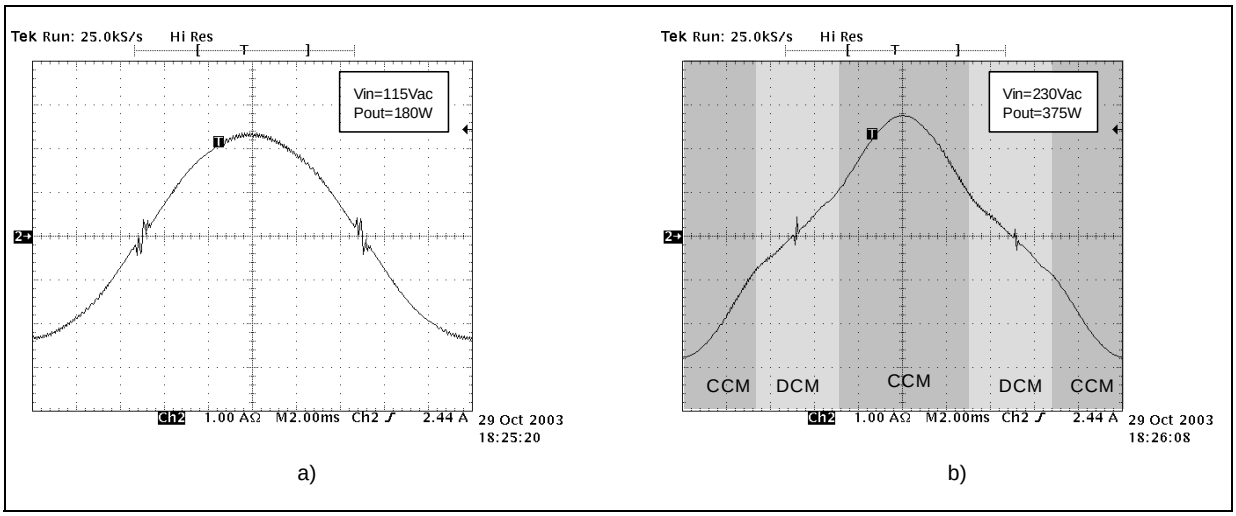


Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=115Vac, Pout=70W)

Ch1: Input voltage (after the bridge rectifier)
Ch2: Line current (@Vin=230Vac, Pout=70W)

Figures 39 to 41 show the line current waveforms under the operating conditions considered in the diagrams of figure 34 (100%, 50% and 20% of the rated load) at nominal voltage of both US and European mains. It is interesting to compare these waveforms with those in figures 20 to 22. The effect of the line modulation of T_{OFF} is conspicuous.

Figure 42. Line current a) nearly sinusoidal at low line; b) without additional distortion at high line.



This effect is clearly pointed out in figure 42 as well. It shows a close image of the line current waveform under the same two operating conditions as in figure 23. On the left (a), the waveform is taken at low line, half-load and one can easily recognize that it is very close to a sinusoid (its THD is 3.8%); this result is even better than the theoretical prediction because the theoretical CCM-DCM boundary falls in a region where the effect of the THD optimizer circuit of the L6562 becomes apparent (T_{ON} is forced to be longer than the value commanded by the control loop). As a consequence, in that region the peak inductor current is higher and the actual CCM-DCM boundary is virtually located at or extremely close to zero-crossings.

On the right (b), the waveform is taken at high line, full-load and in this case the waveform closely follows the theoretical one, unlike that in figure 23b, thus proving the effectiveness of a longer T_{OFF}.

Considering that at low line the system works almost entirely in CCM, so that the line current looks very much like that of a FF-CCM system, it is possible to face the design of the power stage with the same approach used in an FF-CCM type. The significant difference is the point where inductor current ripple amplitude is maximum: whereas it is well-defined with FF-CCM, it is not with LM-FOT and it is not possible to find a simple design formula that relates the inductance value L to the maximum desired ripple. As a rule of thumb, it is possible to refer to the ripple amplitude on the top of the sinusoid at minimum line voltage and determine L so that the ripple amplitude is 75% of the maximum desired.

This stated, the recommended step-by-step design procedure of an LM-FOT-controlled PFC is the following:

1) Calculate the range of k ($k_{min} \div k_{max}$) associated to the line voltage range:

$$k_{min} = \sqrt{2}\frac{Vin_{(RMS)min}}{Vout} \quad , \quad k_{max} = \sqrt{2}\frac{Vin_{(RMS)max}}{Vout} .$$

2) Calculate the required T_{OFFmin} from the specification on the maximum switching frequency (on the top of the line voltage sinusoid) f_{swmax} at minimum line voltage:

$$T_{OFFmin} = \frac{k_{min}}{f_{sw\ max}} .$$

3) Calculate $Pin_0=Pout_0/\eta$ and determine the maximum line peak current Ipk:

$$Ipk_{max} = \frac{2Pin_0}{k_{min}Vout} .$$

4) Determine the ripple amplitude on the top of the sinusoid at minimum line voltage, assuming it is 75% of the maximum specified, related to Kr:

$$\Delta I_{Lpk} = \frac{6Kr}{8-3Kr}Ipk_{max} = \frac{12Kr}{8-3Kr}\frac{Pin_0}{k_{min}Vout} .$$

5) Determine the required inductance L of the boost inductor:

$$L = (1-k_{min})\frac{Vout}{\Delta I_{Lpk}}T_{OFFmin} = \frac{8-3Kr}{12Kr}\frac{Vout^2}{Pin_0}k_{min}(1-k_{min})T_{OFFmin} .$$

6) Calculate I_{Lpkmax}:

$$I_{Lpkmax} = Ipk_{max} + \frac{1}{2}\Delta I_{Lpk} = \frac{8}{8-3Kr}Ipk_{max} = \frac{16}{8-3Kr}\frac{Pin_0}{k_{min}Vout} .$$

7) Determine the maximum sense resistor $Rsense_{max}$:

$$Rsense_{max} = \frac{1.6}{I_{Pkmax}}$$

and select a resistor value Rsense < $Rsense_{max}$. 1.6V is the minimum value of the pulse-by-pulse current limiting threshold on the current sense pin of the L6562. Take into account that the value of this threshold can go as high as 1.8V, hence the inductor must not saturate up to a current equal to 1.8/Rsense.

8) Calculate the current stress of all components, design the boost inductor with any commonly used procedure, and select the MOSFET and the diode. Use either the output voltage ripple or the hold-up specification, whichever gives the higher capacitance value, to select the output capacitor.

9) Design the bias component around the controller IC (multiplier setpoint and feedback) using the same criteria given for TM systems [6], just considering the different small-signal model as to the feedback design. Finally, once specified T_{OFF}@Vin=$Vin_{(RMS)max}$ > 7 µs, design the circuit that sets up LM-FOT control according to the given procedure.

Conclusions

Fixed-Off-Time control of PFC pre-regulators has been discussed and analyzed, highlighting its merits and drawbacks. Simplified large-signal and small-signal models have been described and a design procedure has been provided for its basic implementation. A prototype built following this procedure and utilizing the L6562, a cheap 8-pin Transition-Mode controller IC with some simple additions, has been evaluated on the bench and the results have been presented.

An improved version, denominated "Line-modulated Fixed-Off-Time" (LM-FOT) control, has been introduced and its benefits over the basic FOT control have been shown and proven by the bench evaluation of the prototype modified accordingly. In particular, from these results it is possible to conclude that an LM-FOT-controlled PFC pre-regulator, operated in CCM, at low line performs exactly like a conventional FF-CCM type. Thereby, the power stage can be designed with the same procedure and using the same relationships.

The good performance that the system has shown, especially in the improved LM version, validates this approach, which couples the simplicity and cost-effectiveness of TM operation with the high-current capability of CCM operation. FOT control can justifiably be added to these two popular techniques.

REFERENCES

[1] R. B. Ridley "A New Continuous-Time Model for Current-Mode Control with Constant Frequency, Constant On-Time and Constant Off-Time, in CCM and DCM", IEEE Power Electronics Specialists Conference Record, San Antonio, Texas, pp. 382-389, 1990.

[2] D. H. Venable "Current Mode Control", Venable Technical Paper #5, www.venableind.com

[3] C. Adragna "Fixed-Off-Time Control of PFC Pre-regulators", 10th European Conference on Power Electronics and Applications, EPE2003, Toulouse, France, paper 382.

[4] "L6562, Transition-Mode PFC Controller", Datasheet, www.st.com

[5] Lloyd H. Dixon, Jr. "Filter Inductor and Flyback Transformer Design for Switching Power Supplies", UNITRODE Power Supply Design Seminar Manual, 1994 (SEM-1000)

[6] "L6561, Enhanced Transition Mode Power Factor Corrector", AN966, www.st.com