LN3C63

High Performance Current Mode PWM Controller

Cycle Turning+

POWER FROM LIEMIC

For,

- **Adaptor & Charger**
- **Offline Power Supply**
- **Open Frame Power**
- **DVD&DVB Player**
- **Auxiliary Power for PC**
- **etc.....**

LN3C63AD

REV: 1.0.0

GENERAL DESCRIPTION

LN3C63 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in less than 35W range. PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved. VDD low startup current and low operating current contribute to a reliable power on startup design with LN3C63. A large value resistor could thus be used in the startup circuit to minimize the standby power. The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design. LN3C63 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). The Gate-drive output is clamped to maximum 18V to protect the power MOSFET. Excellent EMI performance is achieved with LIEMIC proprietary Cycle Turning technique together with soft switching control at the totem pole gate drive output.

Tone energy at below 20kHz is minimized in the design and audio noise is eliminated during operation. LN3C63 is offered in SOT23-6, SOP8 and DIP8 packages.

FEATURES

- LIEMIC Proprietary Cycle Turning Technology for Improved EMI Performance.
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
- Gate Output Maximum Voltage Clamp (18V)
- Line Input Compensated Over Universal Input Voltage Range.
- Cycle-by-Cycle Over-current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range.
- Overload Protection (OLP)

APPLICATIONS

- Offline AC/DC flyback converter
- Battery Charger
- Power Adaptor
- Set-Top Box Power Supplies
- Open-frame SMPS

PACKAGE DESCRIPTION

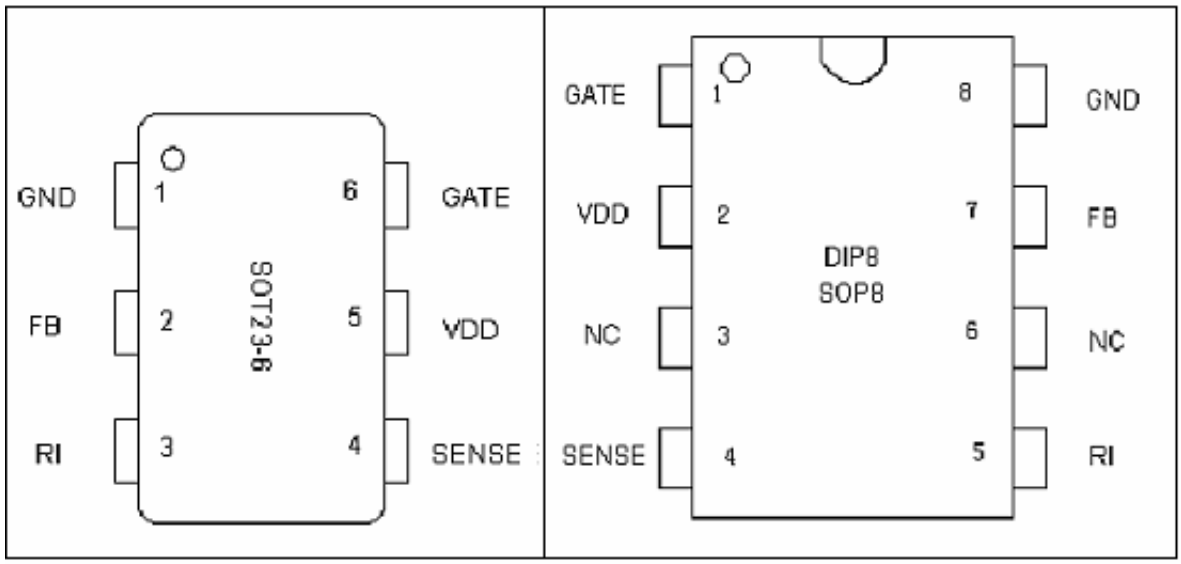
Part	Description	T.R.Rating
LN3C63D	DIP8 Pb Free	90℃/W
LN3C63M	SOP8 Pb Free	150℃/W
LN3C63P	SOT23-6 Pb Free	200℃/W

ORDER INFOMANTION

LN3C63 X X

| | | |_____ Packing Type: T:TUBE; R:Tape & Reel
| |_____ Package Type: D:DIP8; M:SOP8; P:SOT23-6
|_____ **LIEMIC** N Series AC/DC Controller

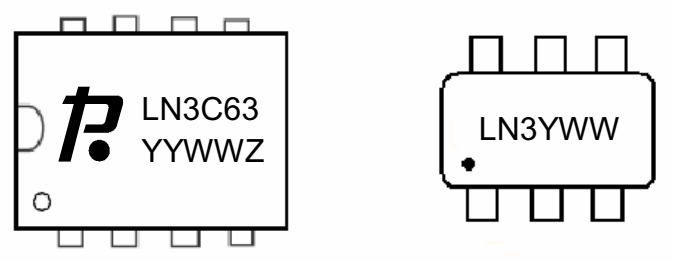
PIN CONFIGURATION



PIN ASSIGNMENTS

Pin Number		Pin Name	Function	Description
SOP8 & DIP8	SOT23-6			
1	6	GATE	O	Totem-pole drive output for the power MOSFET.
2	5	VDD	P	Chip DC power supply pin
3	/	NC	/	
4	4	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
5	3	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
6	/	NC	/	
7	2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
8	1	GND	P	Ground

MARKING INFOMATION



YY: Year Code, 01-99 à 2001-2099
WW: Week Code, 01-52 Week
Z: Other Information

ABSOLUTE MAXIMUM RATINGS *

VDD DC Supply Voltage 30V
VDD Clamp Voltage 34V
VDD DC Clamp Current 10mA
VFB Input Voltage ..... -0.3 to 7V
VSENSE Input Voltage to Sense Pin ..... -0.3 to 7V
VRI Input Voltage to RI Pin ..... -0.3 to 7V
Min/Max Operating Junction Temperature TJ ..... -20 to 150℃
Min/Max Storage Temperature Tstg ..... -55 to 160℃

ESD INFORMATION:

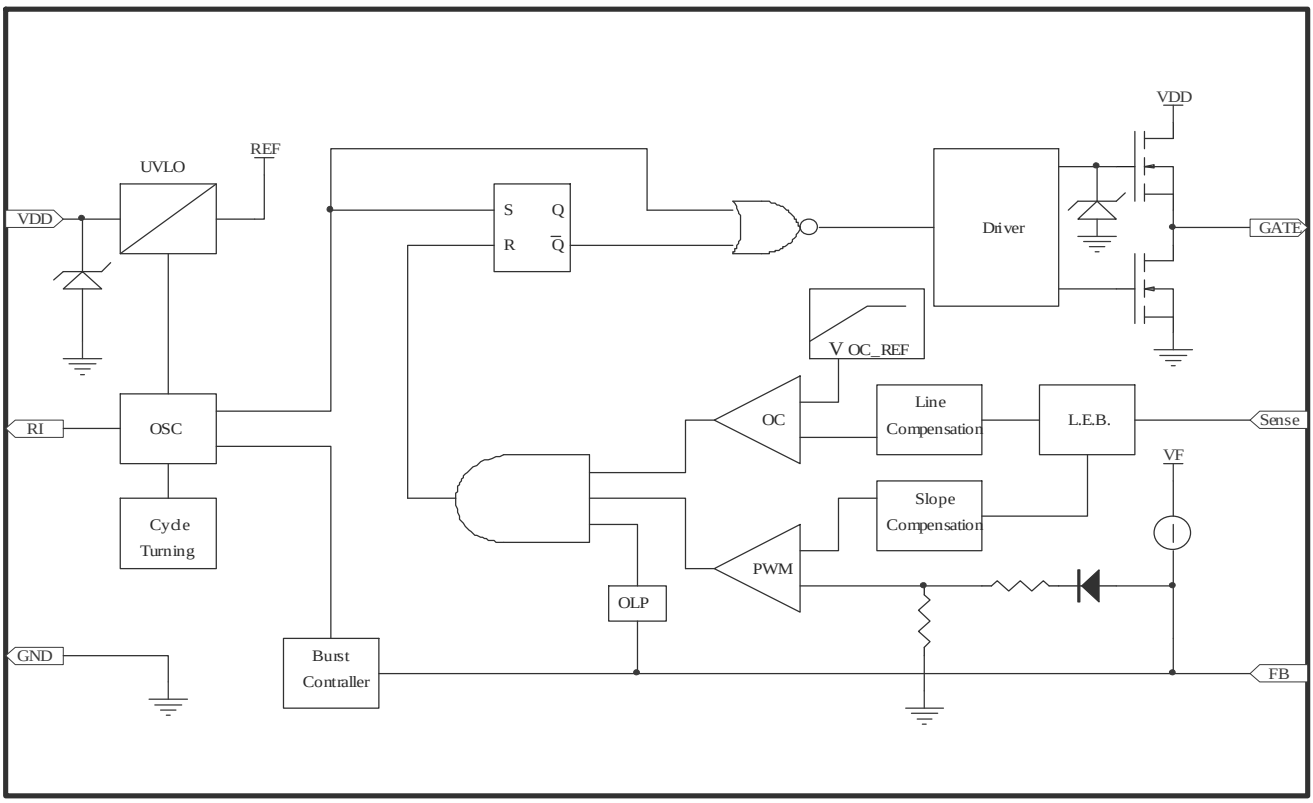
HBM Human Body Model 2.5KV
MM Machine Model 200V

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operat ion of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not im plied. Exposure to absolute maximum-rated conditions for ex tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Type	Max	Unit
VDD	VDD Supply Voltage	10		25	V
RI	RI Resistor Value		100		KΩ
TA	Operating Ambient Temperature	-20		85	℃

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(TA = 25℃ if not otherwise noted)

Supply Voltage (VDD)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{QS}	VDD Start up Current	VDD=12.5V,RI=100K,Measure Leakage current into VDD		3	20	uA
I_Q	Operation Current	VDD=16V,RI=100KΩ,VFB=3V		1.4		mA
V_{START}	UVLO Threshold Voltage	FB=0	7.8	8.8	9.8	V
V_{STOP}			13	14	15	V
VDD_CL	VDD Zener Voltage	IVDD=10mA		34		V

Feedback Input Section(FB Pin)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
A_{VCS}	PWM Input Gain	VFB / Vcs		2.0		V/V
V_{FB}	V_{FB} Open Loop Voltage	V_{FB}=Open		4.8		V
I_{FB_S}	FB short current	FB=0		0.8		mA
VTH_{MIN}	Zero Duty FB Threshold Voltage	VDD = 16V,RI=100KΩ			0.75	V
VTH_{MAX}	Power Limiting FB Threshold Voltage	VDD = 16V,RI=100KΩ		3.7		V
TD_{MAX}	Power limiting Debounce Time	VDD = 16V,RI=100KΩ		35		mS
Z_{FB}	FB Input Impedance			6		KΩ
D_{MAX}	Maximum Duty Cycle	VDD=18V,RI=100KΩ,FB=3V,CS=0		75		%

Current Sense Input(Sense Pin)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{LEB}	Leading edge blanking	RI = 100 KΩ		300		nS
Z_{CS}	CS Input Impedance			40		KΩ

(Continue)

T_{OCP}	OCP Delay	VDD=16V,CS>VTH_OC,FB=3.3V		75		nS
VTH_{OCP}	OCP Threshold Voltage	FB=3.3V, RI=100 KΩ	0.70	0.75	0.80	V

Oscillator

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{OSC}	Normal Oscillation Frequency	RI = 100 KΩ	60	65	70	kHz
ΔF_{OSC}_T	Frequency Temperature Stability	VDD = 16V,RI=100KΩ, TA=-20℃ to 100 ℃		5		%
ΔF_{OSC}_V	Frequency Voltage Stability	VDD = 12-25V,RI=100KΩ		5		%
RI	Operating RI Range		50	100	150	KΩ
V_{RI}	RI open voltage			2		V
F_{OSC}_min	Burst Mode Base Frequency	VDD = 16V, RI = 100KΩ		22		kHz

Gate Drive Output

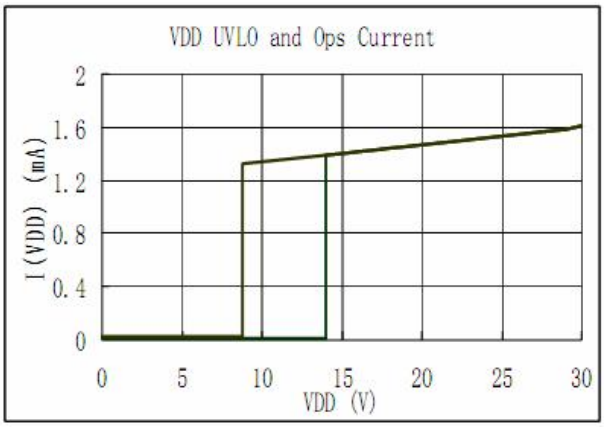
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Level	VDD = 16V, Io = -20 mA			0.8	V
V_{OH}	Output High Level	VDD = 16V, Io = 20 mA	10			V
V_O_CL	Output Clamp Voltage			18		V
T_r	Output Rising Time	VDD = 16V, CL = 1nF		220		nS
T_f	Output Falling Time	VDD = 16V, CL = 1nF		70		nS

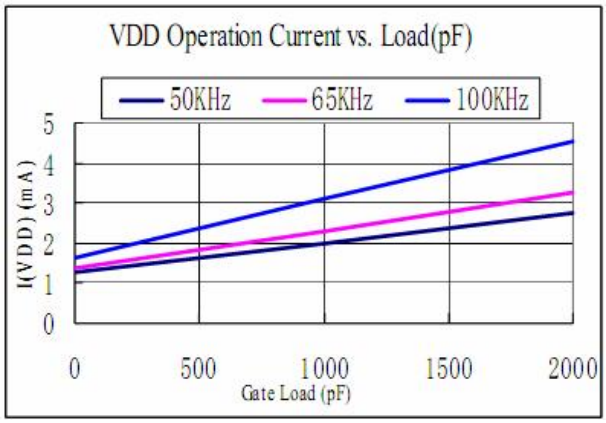
Cycle Turning+

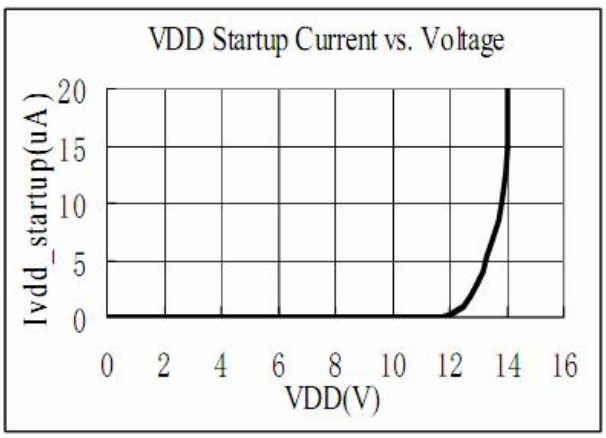
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔF_{OSC}	Cycle Turning range	RI=100KΩ	-2		+2	kHz
T_{CT}	Cycle Turning Time	RI=100KΩ		15		mS

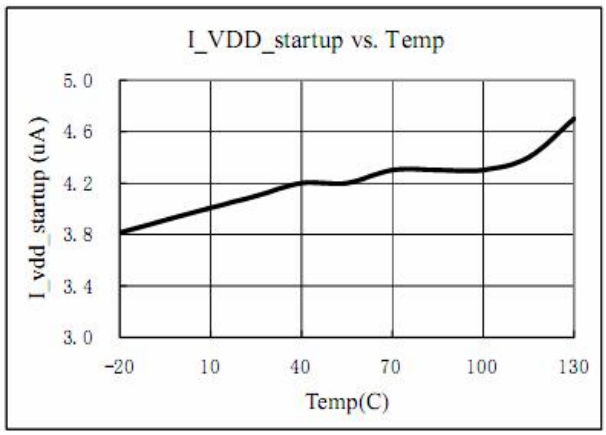
CHARACTERIZATION PLOTS

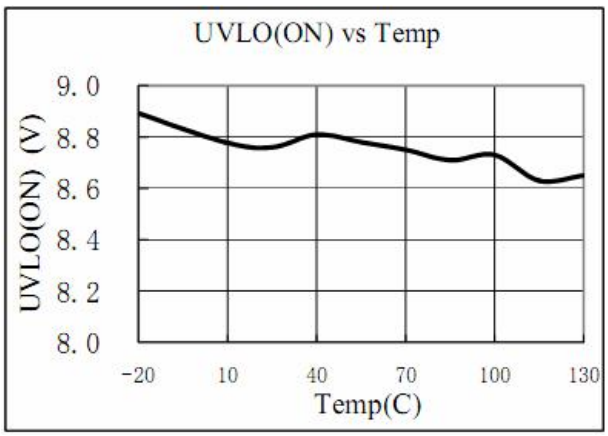
(VDD = 16V, RI = 100 KΩ, TA = 25℃ condition applies if not otherwise noted.)

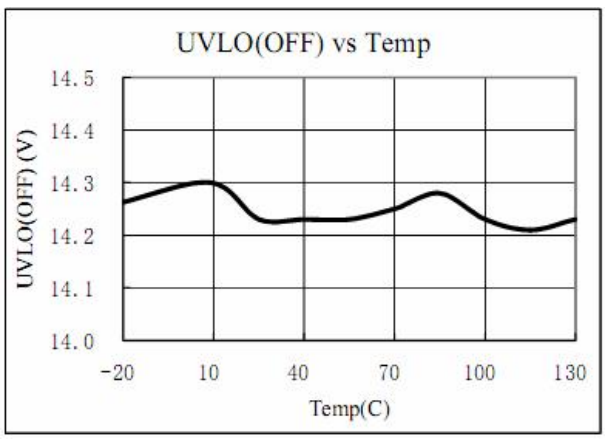












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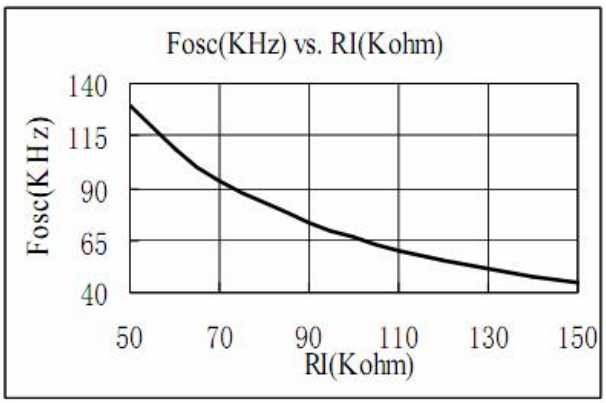
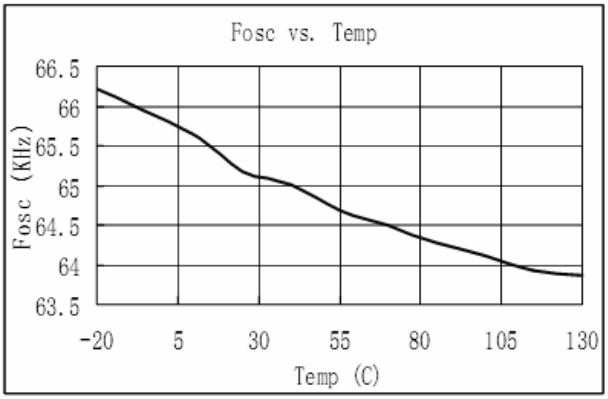
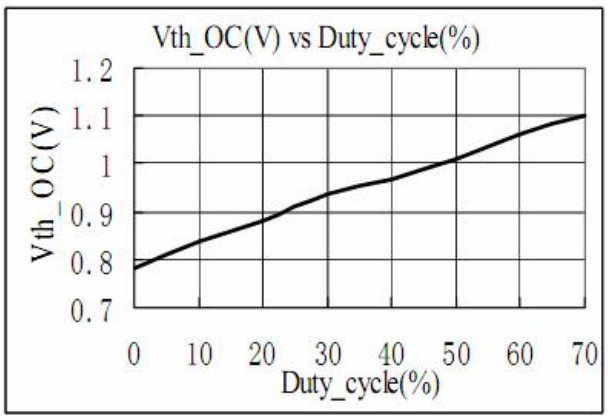

Fosc(KHz) vs. RI(Kohm)
Fosc(KHz)
140
115
90
65
40
50
70
90
110
130
150
RI(Kohm)


Fosc vs. Temp
Fosc (KHz)
66.5
66
65.5
65
64.5
64
63.5
-20
5
30
55
80
105
130
Temp (C)


Vth_OC(V) vs Duty_cycle(%)
Vth_OC(V)
1.2
1.1
1
0.9
0.8
0.7
0
10
20
30
40
50
60
70
Duty_cycle(%)

OPERATION DESCRIPTION

The LN3C63 is a highly integrated PWM controller IC optimized for offline flyback converter applications in sub 30W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of LN3C63 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application. For AC/DC adaptor with universal input range design, a 2 M , 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The Operating current of LN3C63 is low at 1.4mA. Good efficiency is achieved with LN3C63 low operating current together with extended burst mode control features.

Cycle Turning+ for EMI improvement

The Cycle Turning+/jittering (switching frequency modulation) is implemented in LN3C63. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

Extended Burst Mode Operation

At zero load or light load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. LN3C63 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$Fosc = \frac{6500}{RI(K\Omega)}(\text{kHz})$$

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in LN3C63 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

LN3C63 Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction

and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO).

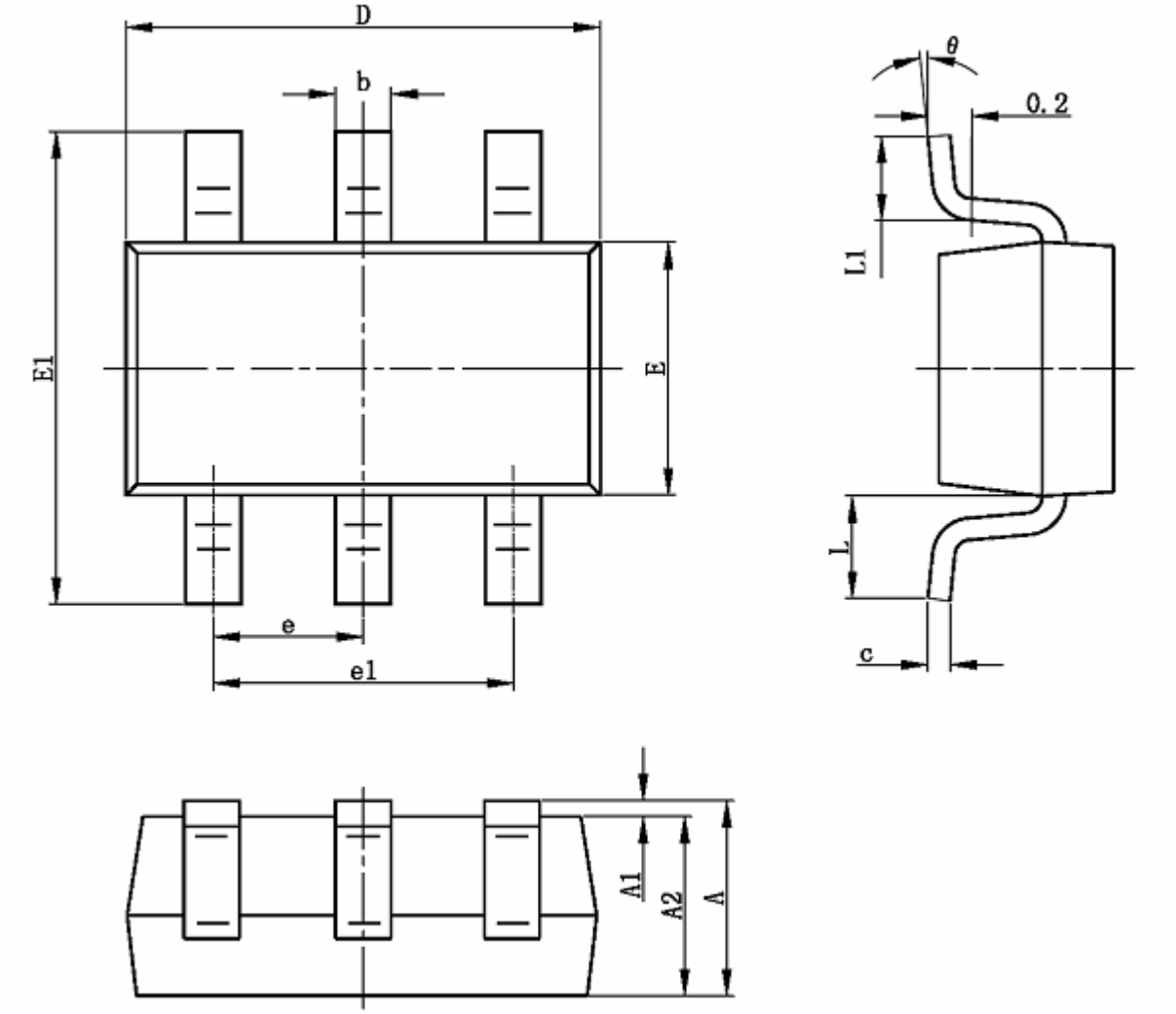
With LIEMIC Proprietary technology, the OCP threshold tracks PWM Duty cycles and is line voltage compensated to achieve constant output power limit over the universal input voltage range with recommended reference design.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit.

VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

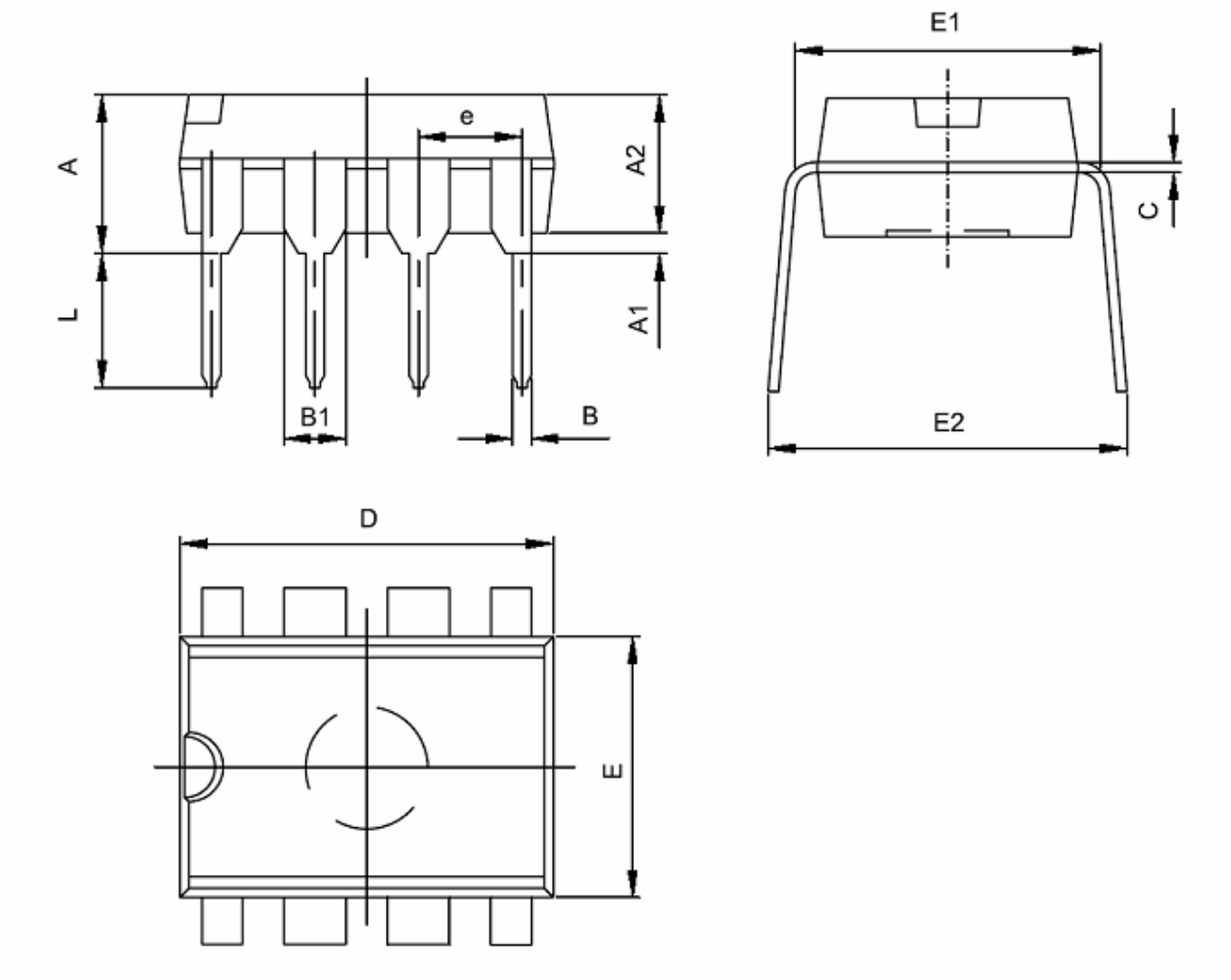
PACKAGE MECHANICAL DATA

SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

8-Pin Plastic DIP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

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