High Performance Green Mode PWM controller

General Description

The NE1101A/B is a current mode controller which contains advanced features to meet the stringent worldwide green energy requirements. Among the advanced energy saving functionalities include the NE1101A/B include a low leakage high voltage startup current source that minimize no load standby power losses

It has a PFC VCC pin which is capable of delivering 35mA to the front stage PFC controller. This bias will cut off automatically when the IC enters Green mode under light load. This feature simplifies the PFC circuit design and reduces power losses

Under light load, the NE1101A/B enters burst mode to maintain high efficiency operation

The NE1101 also features frequency dithering function that spreads the EMI spectrum and saves the cost on EMI solution.

Other features that incorporated in the NE1101 are latched OVP, OCP, OTP functions, which is triggered by pulling CS pin above 3.0V and reset by pulling it to ground. .

The switching frequency of NE1101A is internally fixed at 100KHz. The NE1101B is fixed at 65KHz. These two versions are available in SO8 and DIP8 packages

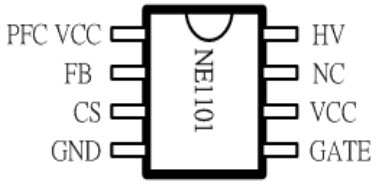
Features

- Current mode control with Internal slope compensation
- High-Voltage Startup current source
- Peak current limited Burst mode
- Internal 2.5mS softstart
- Internal 200nS Leading Edge Blanking
- Cycle-by-Cycle current limit
- Latched OCP & OVP functions
- Frequency Jittering for EMI reduction
- Over Temperature, over load protections
- Automatic PFC bias supply output

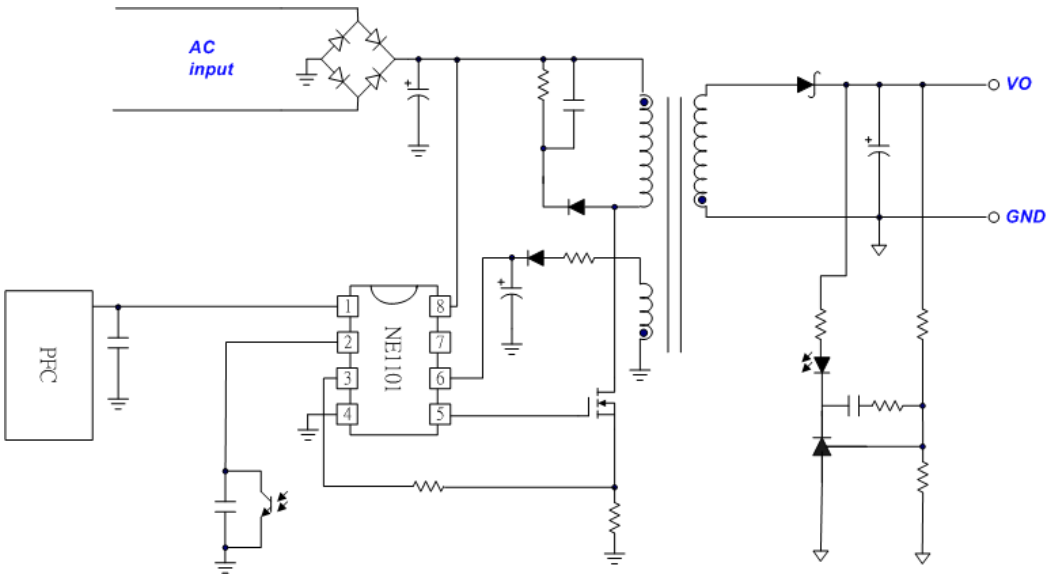
Applications

- General 30W-100W flyback SMPS
- AC adaptor for Notebooks, Printers
- Off-line battery chargers
- LCD monitors, Set-Top boxes, power tools
- Open-frame SMPS
- Standby power for TVs, PCs, Home appliances

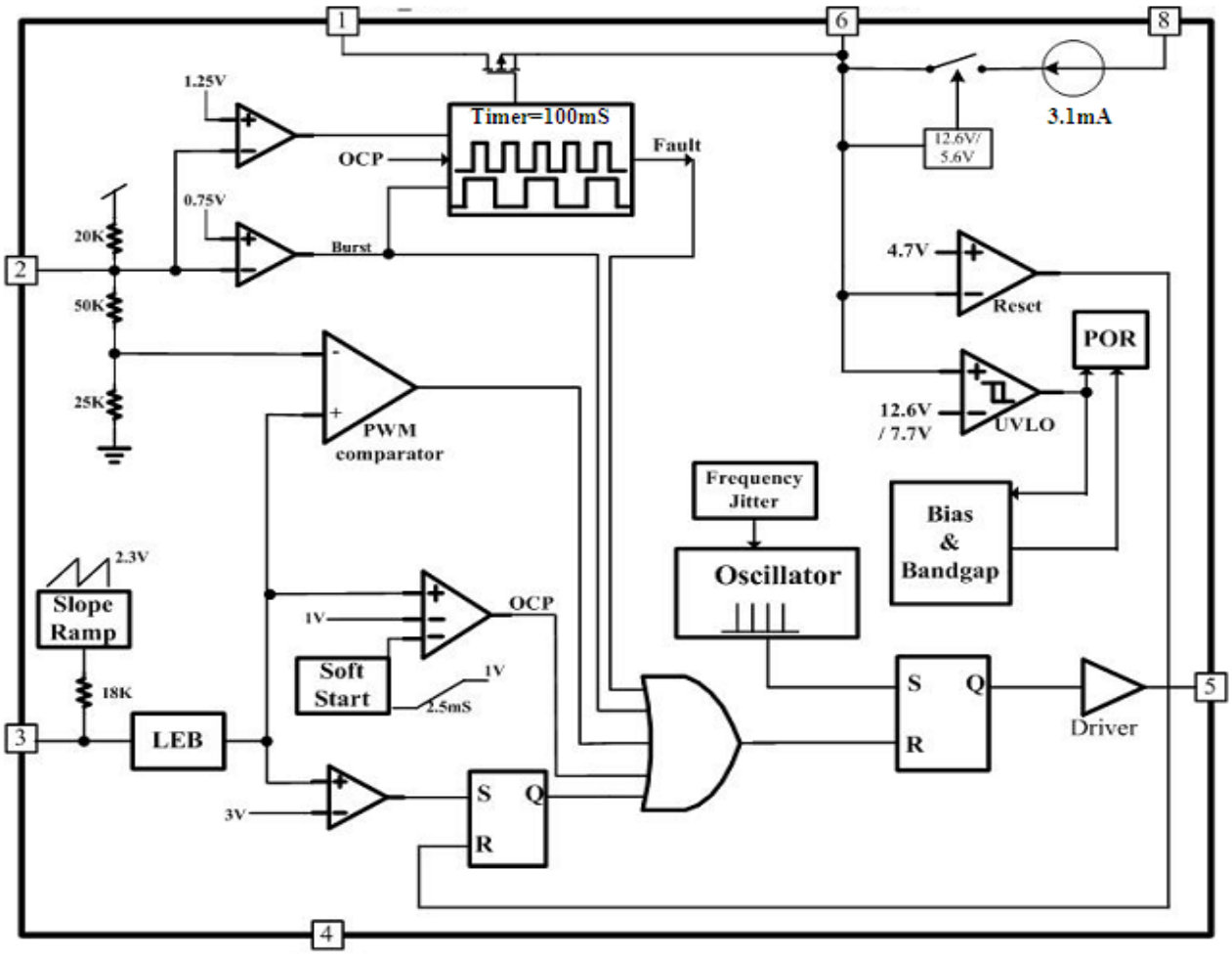
Package



Typical Application



Functional Block Diagram



Functional Pin Description

Pin Name	Pin	Function Description
PFC VCC	1	Provide bias of max 35mA to PFC controller under normal operation condition
FB	2	Voltage feedback pin. By connecting a photo-coupler to close control loop and achieve the regulation
CS	3	Senses the primary current
GND	4	Ground
GATE	5	Gate drive output to drive the external MOSFET
VCC	6	Power Supply pin
NC	7	No connection
HV	8	High voltage startup pin. Connect this pin to the bulk voltage rail

Absolute Maximum Ratings (Note 1)

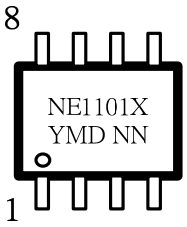
- Supply Input Voltage, VCC……21V
- GATE pin……...15V
- FB, CS pin……10V
- HV pin……500V
- PFC VCC pin……21V
- ICC……10mA
- Junction Temperature……150℃
- Lead Temperature (10sec)……260℃
- Storage Temperature Range……-60℃to150℃
- ESD Susceptibilty (Note 2)
  HBM (Human Body Mode)……3KV
  MM (Machine Mode)……200V
- Power Dissipation, PD@TA=25℃,
  SO8……0.76W
  DIP8……0.98W
- Package Themal Resistance θ_{JA} (Note4)
  SO8……165.5℃/W
  DIP8……127.0℃/W

Recommended Operating Conditions

- Supply Voltage ,VCC……7.7V to 18V
- Junction Temperature Range…… - 40°C to 125°C
- Ambient Temperature Range…….. - 40°C to 85°C

Marking Information:

Y = Year
M = Month
D = Date
NN = Serial No.
X = A: 100KHz
B: 65KHz



Ordering Information:

Part Number	Freq	Package	Shipment
NE1101A-S0	100KHz	SO8	Tape & Reel/2500ea
NE1101B-S0	65KHz	SO8	Tape & Reel/2500ea
NE1101A-S0T	100KHz	SO8	Tube/100ea, 100 Tubes/Box(10000ea)
NE1101B-S0T	65KHz	SO8	Tube/100ea, 100 Tubes/Box(10000ea)
NE1101A-D0T	100KHz	DIP8	Tube/50ea, 60 Tubes/Box(3000ea)
NE1101B-D0T	65KHz	DIP8	Tube/50ea, 60 Tubes/box(3000ea)

Electrical Characteristics

(Unless otherwise stated, all specifications apply for Tj=25℃,VCC=13V, V_{HV}=30V. Tj=0℃ to 125℃ for min/max values respectively

Parameter	Symbol	Test Conditions	Pin	Specifications			Units
				Min	Typ	Max	
Supply Voltage Section(VCC pin)							
V_{CC} On Threshold Voltage	V_{CC-On}	V_{FB}=2.0V	**6**	11.6	12.6	13.6	V
V_{CC} Off Threshold Voltage	V_{CC-Off}		**6**	7.0	7.7	8.4	V
V_{CC} Deep sleep Phase Ends	$V_{Deep-Off}$	V_{FB}=3.5V	**6**	5.0	5.6	6.2	V
V_{CC} Reset Internal Logic	$V_{CC-Reset}$		**6**	-	4.7	-	V
Operating Supply Current 1	I_{CC1}	V_{FB}=2.5V, C_{GATE}=open	**6**	0.4	0.72	1.8	mA
Operating Supply Current 2	I_{CC2}	V_{FB}=2.5V, C_{GATE}=1nF, A Version	**6**	1.18	1.76	3.0	mA
		V_{FB}=2.5V, C_{GATE}=1nF, B Version	**6**	1.18	1.55	2.5	mA
Operating Supply Current 3	I_{CC3}	V_{CS}=3.3V, Latch-Off Mode	**6**	0.4	0.52	1.0	mA
Internal Startup Current Source Section (HV Pin)							
HV current source , 1.0nF load	I_{HV1}	V_{CC}= V_{CC-On}-0.2V V_{FB}=2.5V V_{HV}=60V	**8**	0.94	1.77	4.2	mA
HV current source	I_{HV2}	V_{CC}= 0V V_{HV}=60V	**8**	1.8	3.1	5.6	mA
Minimum Startup Voltage	V_{HVmin}	V_{CC}= V_{CC-On}-0.2V V_{FB}=2.5V I_{HV}=0.5mA	**8**	-	15	18	V
Startup Leakage	I_{HVLeak}	V_{HV}=500V, V_{CC}= V_{CC-On}+0.5V	**8**	1	3.8	20	uA
Gate Drive Section (GATE Pin)							
Rising Time	T_R	V_{CC} = 13V, C_L = 1nF	**5**		28		nS
Falling Time	T_F	V_{CC} = 13V, C_L = 1nF	**5**		24		nS
Gate Output Clamping Voltage	V_{clamp}	V_{CC}=18V(Note 5)	**5**		14.3		V
Jitter Percentage	P_{jit}	V_{FB}=2.5V(Note 5)	**5**		±6.4		%
Jitter Period	T_{jit}	V_{FB}=2.5V(Note 5)	**5**		5		mS

Parameter	Symbol	Test Conditions	Pin	Specifications			Units
				Min	Typ	Max	
Oscillation Frequency	F_{osc}	T_J=25℃ , A Version	5	93	100	107	KHz
		T_J=0℃~+125℃		90	-	110	
		T_J=25℃ , B Version	5	60	65	70	KHz
		T_J=0℃~+125℃		58	-	72	
Maximum Duty Cycle	D_{max}	V_{CS}=0V, V_{FB}=2.5V	5	75	80	85	%
Feedback Section (FB Pin)							
Opto Current Source	I_{OPTO}	V_{FB}=0.75V	2	200	225	290	uA
FB Open Voltage	V_{FB-OP}		2	3.3	4.1	4.5	V
Burst Mode Entry Point	V_{Burst}		2	600	720	900	mV
Burst Mode Leaving Point	$V_{stby-out}$		2	1.0	1.2	1.5	V
Current-Sense Section(CS Pin)							
Input Bias Current	I_{IB}	Vcs=1V	3	2	8.5	20	uA
Maximum Internal Current Setpoint	V_{CSLim}	T_J=25℃	3	1.01	1.057	1.116	V
		T_J=0℃~+125℃		0.976	-	1.168	
Leading Edge Blanking Time	T_{LEB}		3	100	200	350	nS
Propagation Delay Time	T_{PD}	V_{GATE} 10V to Low C_{GATE}=1nF	3	-	90	180	nS
Soft-Start Period	T_{SS}	(Note 5)	3	-	2.5	-	mS
Latch-Off Level	V_{latch}		3	2.7	3.0	3.3	V
RFC Controller Source Section (PFC_Vcc Pin)							
R_{DSON} between Pin 1 and Pin 6	R_{PFC}	$R_{Load\ In\ Pin\ 1}$=680Ω	1	6	20	32	Ω
Internal Ramp Compensation							
Internal Ramp Compensation Resistor	R_{Ramp}	(Note 5)	3	9	18	36	KΩ
Ramp Compensation Sawtooth Ampitude			3	-	2.3	-	V
Protection							
Timeout before Validating Short-circuit	T_{DEL}	(Note 5)		-	100	-	mS
Temperature Shutdown	T_{SD}	(Note 5)		150	165	-	℃
Temperature Shutdown Hysteresis	T_{SDHY}	(Note 5)		-	25	-	℃

Note 1: Stresses beyond 'Absolute Maximum Ratings' may cause permanent damage to the device

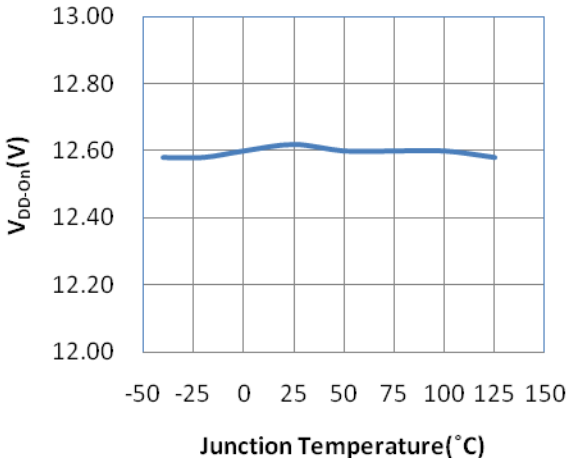
Note 2: Devices are ESD sensiive.Handling precaution recommended. The human body model is 100pF capactor discharged through a 1.5KΩ resistor into each pin.

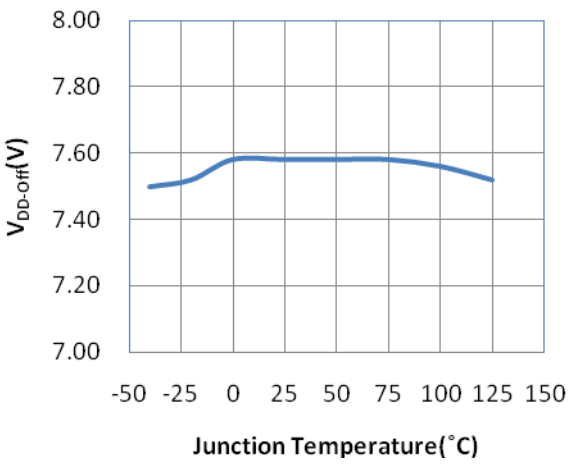
Note 3: The device is not guaranteed to function outside its operating conditions

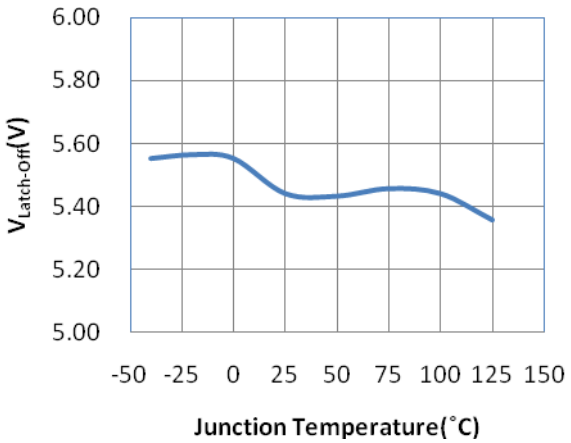
Note 4: θ_{JA} is measured in the natural convection at TA=25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

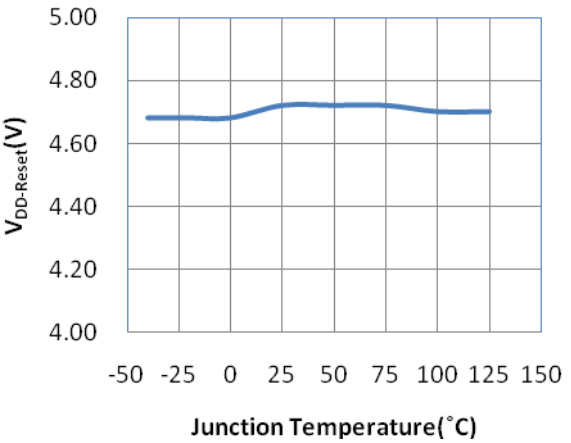
Note 5: Guaranteed by design

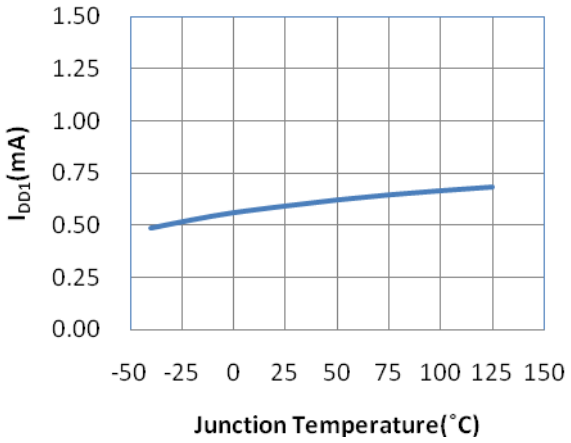
Typical Operating Characteristics

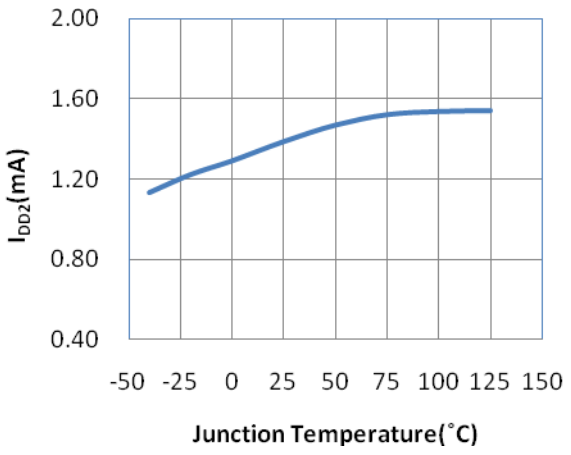












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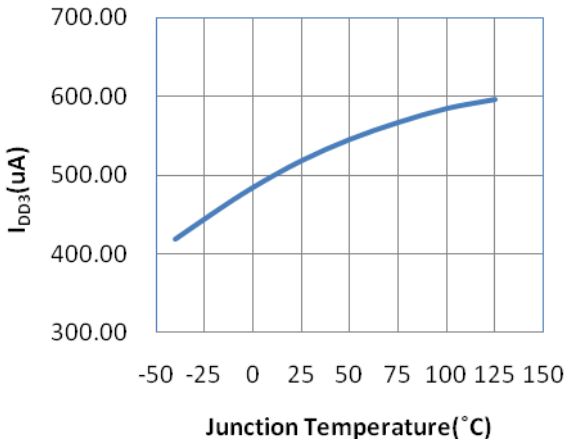

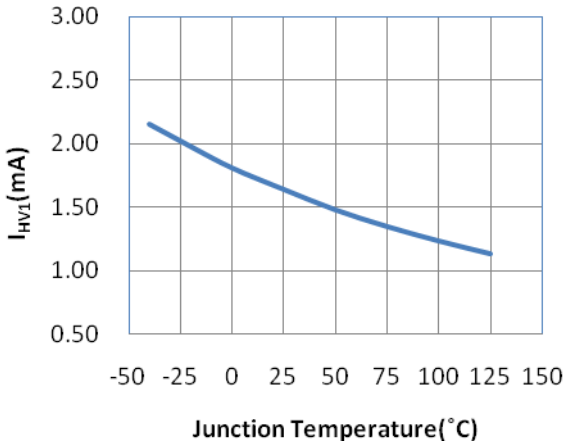

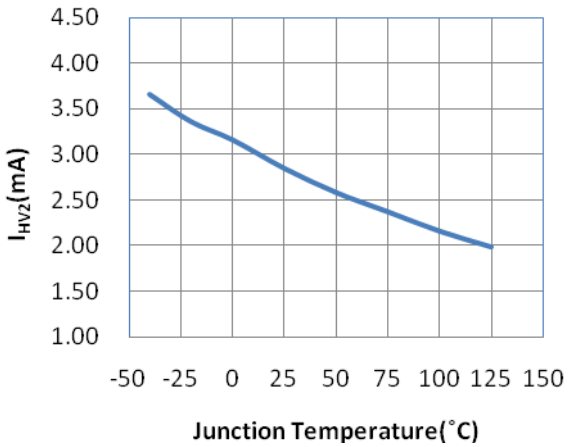

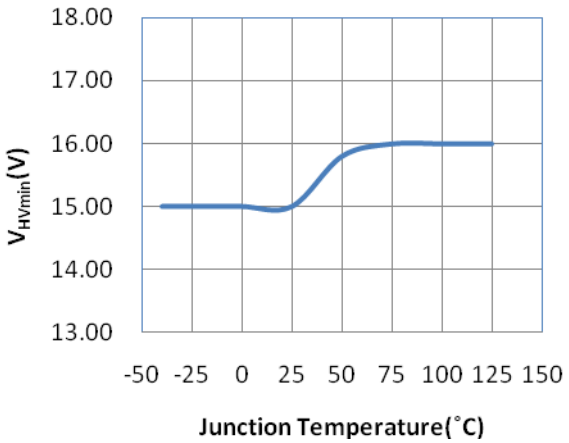

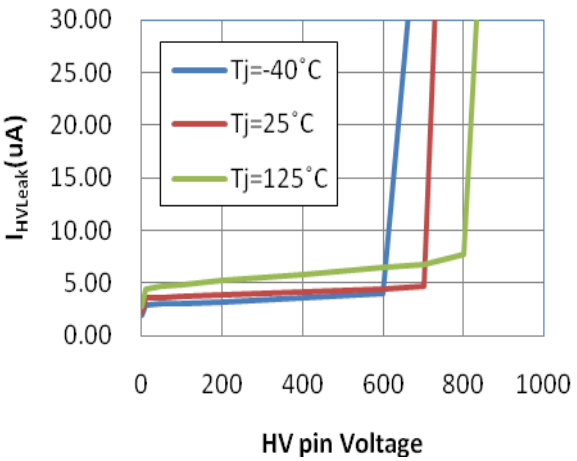

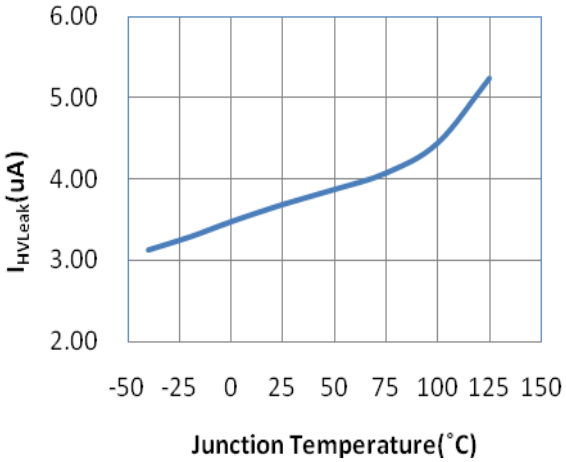

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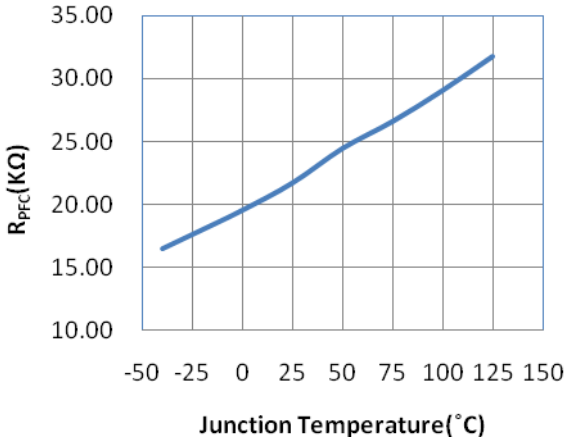

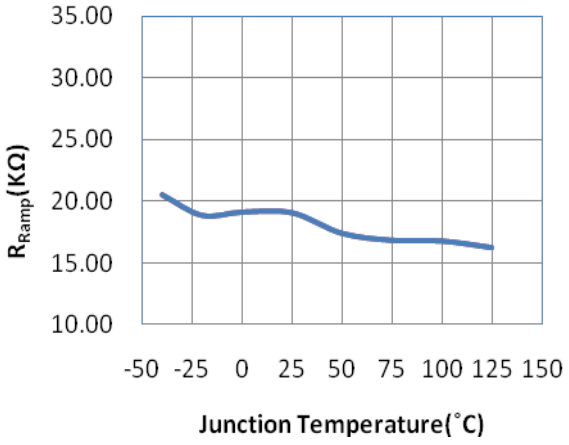

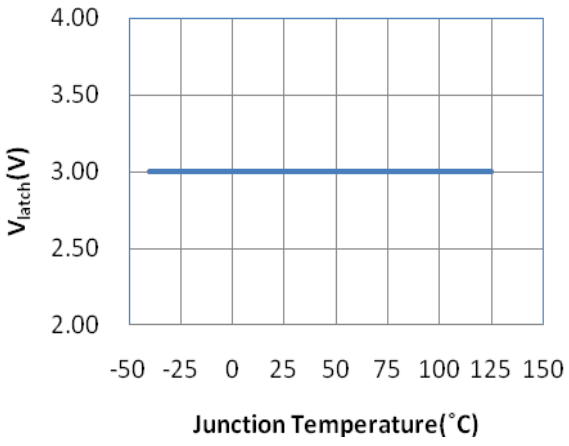

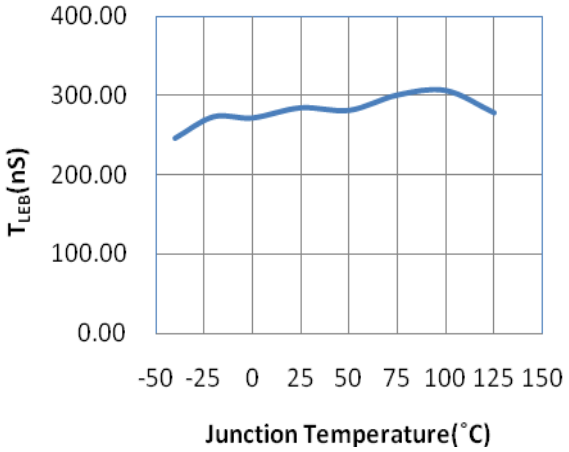

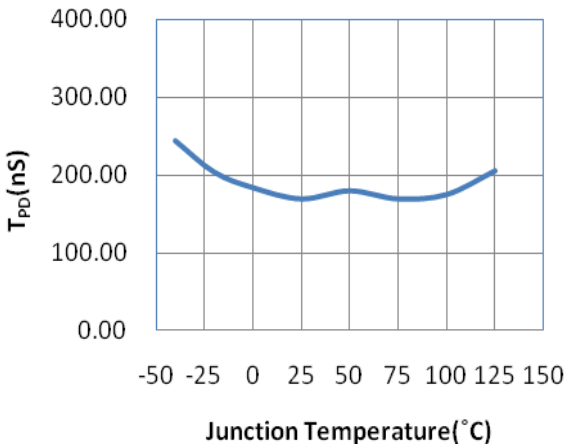

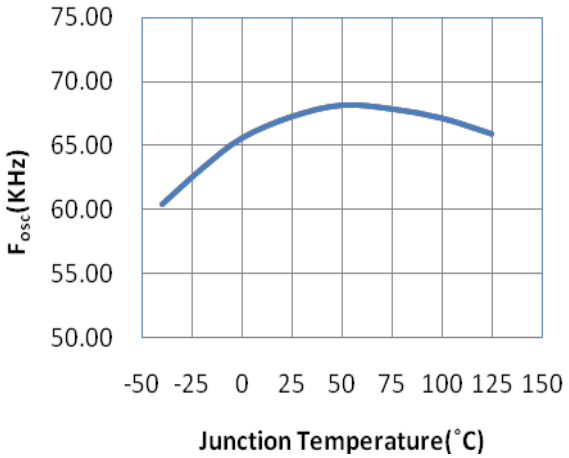

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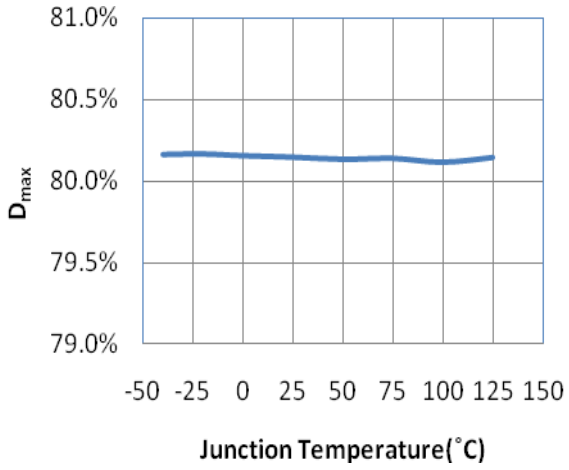

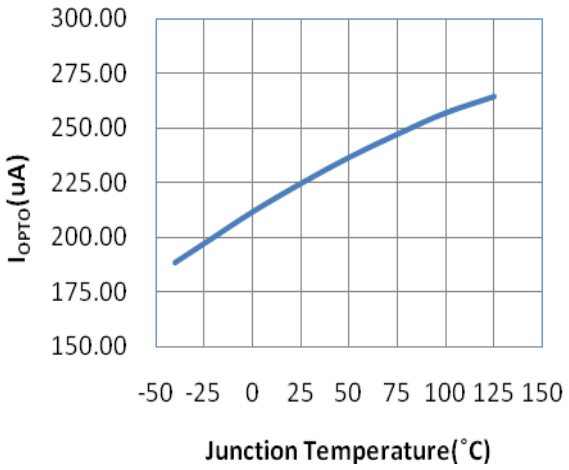

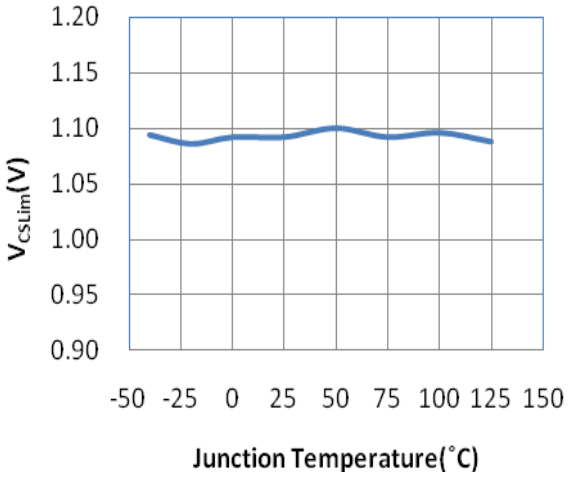

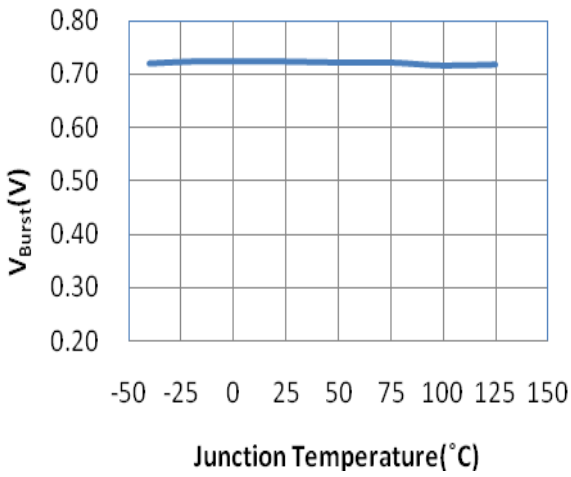

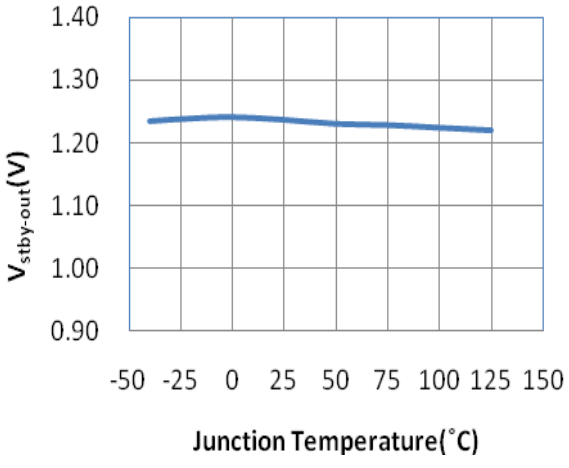

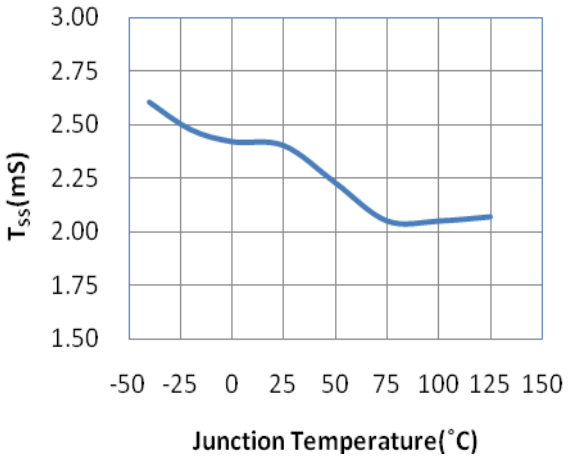

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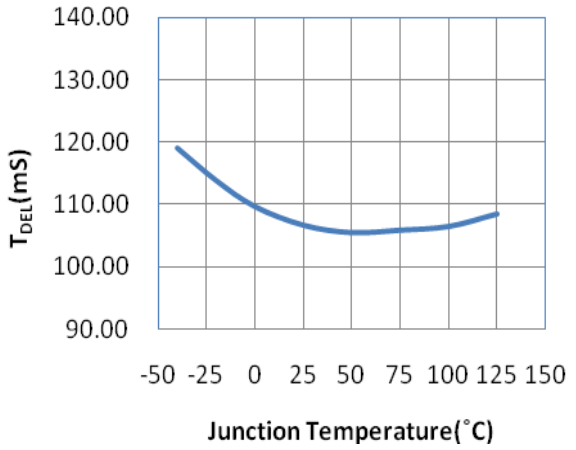


Operation Description:

HV Startup

The NE1101 contains an extremely low leakage High Voltage switch inside pin1 for low power dissipation startup function.

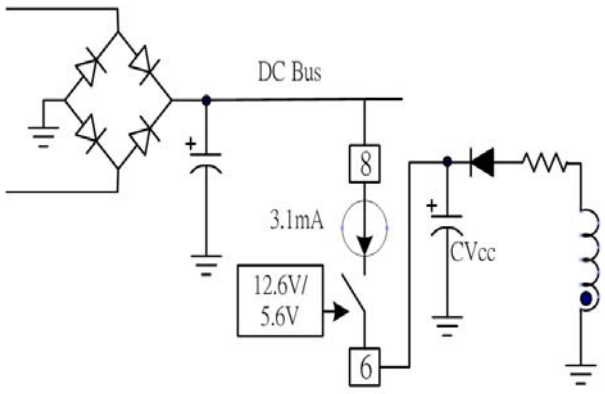


Figure 1

In Figure 1, when a high voltage of 120VDC-400VDC is applied to HV (pin8), the internal HV switch turns ON and connects a 3.1mA current source to Pin6 (Vcc). The capacitor at Vcc pin is charged up till it reaches 12.6V UVLO(ON) level that the controller starts operation. The HV switch is then turned Off to reduce the power dissipation in the startup circuit. It will remain Off during normal operation. The leakage current of the HV switch is less than 20uA typically for minimum power loss.

After the controller is started up, the Vcc subsequently draws power from the transformer auxiliary winding to continue the operation. . .

The HV switch is activated again whenever the Vcc voltage drops to 5.6V as shown in Fig.2 for short circuit condition. In this situation, the internal logic is reset and HV switch turned on to charge up the Vcc capacitor to 12.6V for start up the controller again. See also the description in Over Current Protection section.

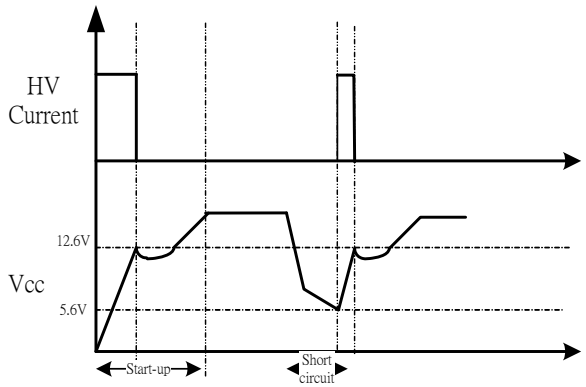


Figure 2

SoftStart

Softstart function is internally fixed at 2.5ms. When Vcc reaches 12.6V level, the controller starts up and performs a softstart immediately.

In Figure 5, the softstart circuit overrides the 1V peak current limit and ramp up the current limit from zero to 1V in 2.5ms. The softstart is also activated whenever the controller performs a Vcc recycled or re-start operation.

PFC_Vcc

The NE1101A/B features a PFC bias output pin which can provide power source to the external PFC controller or other circuits.

As shown in Figure 3 is the internal circuitry of pin1. The PFC_Vcc and Vcc pins are connected internally by a low impedance PFC switch. This switch is current limited to 35mA and capable of biasing an external PFC controller. A 0.1uF decoupling capacitor is recommended to be placed near to the Vcc pin of the PFC controller.

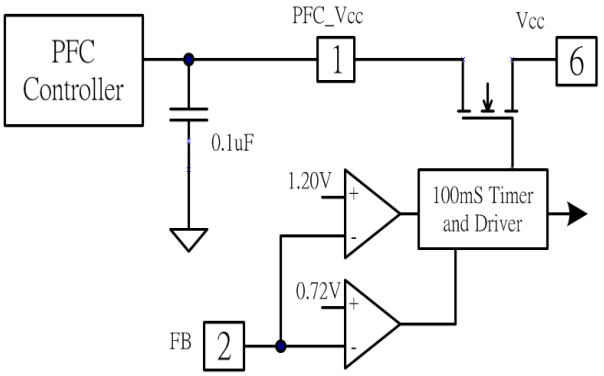


Figure 3

The PFC switch is disabled during softstart although the FB feedback voltage is much higher than the 1.20V ($V_{stby-out}$) level which PFC switch suppose to turn ON normally. The switch will turn ON after the controller completes the softstart and the power supply output voltage enters regulation. (Figure 4)

The PFC switch is disabled automatically when the power supply enters burst mode with feedback voltage (FB pin) is below 0.72V (V_{burst}) under light load condition. To prevent momentarily load changes from causing error operation, a time delay is added such that the PFC switch is disabled after the feedback voltage (FB pin) drops below 0.72V for 100ms (T_{DEL})

When the output load increases, the PFC switch turns ON as soon as FB voltage rises above 1.20V ($V_{STBY-OUT}$). See Figure 4.

The PFC_Vcc pin can be left floating if it is not used

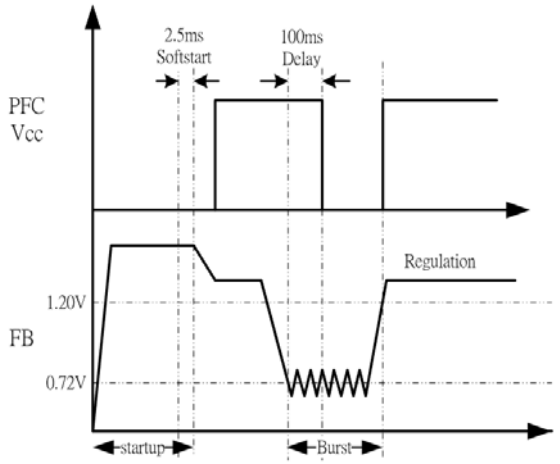


Figure 4

Current Sense

The CS (pin 3) is used for sensing the switching current for current mode control. The switching current information is sensed across the Rs resistor, which is connected to the source terminal of the Mosfet. (Figure 5). This signal is compared with 1/3*FB voltage for generatng the PWM output. In addition, the CS pin is internally clampped to 1V level and thus for maximum power, the value of Rs can be calculated as 1V/(Ipeak).

To prevent sub-harmonic oscillation when the power supply operates in continuous current mode at greater than 50% duty cycle, an internal slope compensation is added by injecting sawthooth waveform of 2.3Vpeak to CS pin via an 18K resistor.

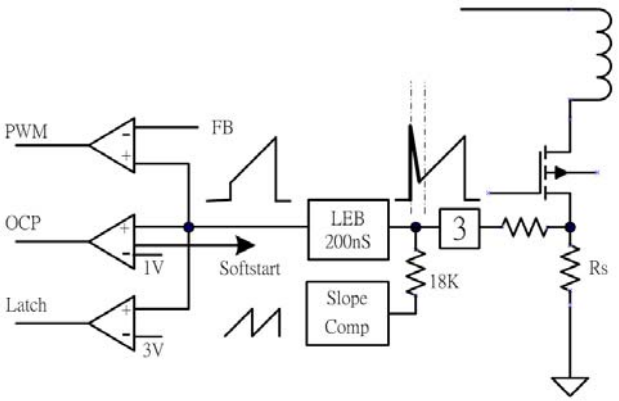


Figure.5

Leading Edge Blanking

The current signal at CS (pin3) consists of large turn-on current spike due to discharge of stray capacitances when the Mosfet turns on. If the amplitude of the spike is higher than the peak switching current of the Mosfet, it will result in the controller turns off the PWM output prematurely and cause unstable operation. In Figure 5, a 200ns leading edge blanking circuit is added in the CS path to mask out the initial 200ns spike and allow the controller to sense the correct peak current information internally.

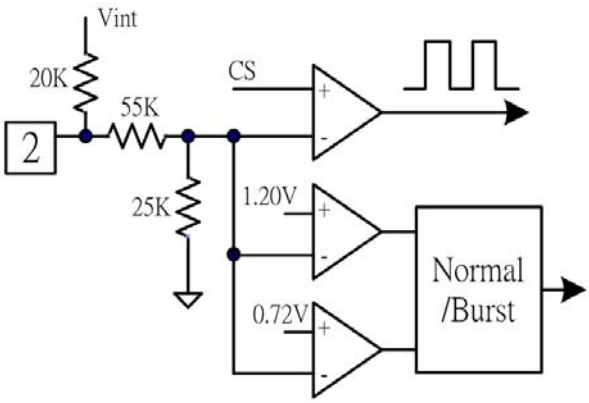


Figure 7

Latch protection

Latch off protection can be implemented by pulling CS (pin3) higher than 3V during the PWM off time. When the latch protection is triggered, the controller terminates the PWM output immediately, the PFC bias output (pin1) is shutdown and the controller stops operation as long as Vcc is above 4.7V, the voltage level at which the controller resets the internal logic.

Figure 6 shows an example on using the Latch function for Over Voltage protection. When the Vcc rail voltage (or output voltage) is too high, the PNP transistor turns ON during the PWM off time and applies a >3V voltage to the CS pin to latch off the controller. This circuit does not affect the current sense operation at CS pin since the PNP is turned OFF during the PWM On time.

This method can be used for protections that require Latch off function, such as Over Temperature protection.

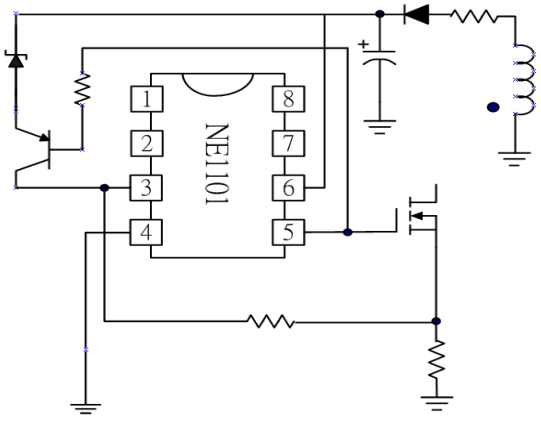


Figure 6

Feedback Voltage

In typical applications, the power supply output voltage is sampled and compared with a reference voltage in the secondary side. The error between these two voltages is sent to the NE1101A/B via an isolation opto coupler connected to the FB (pin2) of the NE1101A/B.

The FB pin is internally pull high by a 20K resistor to the internal bias. This signal is scaled down by a factor of three (V-) and sent to the inverting input of the PWM comparator. (Figure 7). The non-inverting input of the comparator is connected to the peak current signal. During operation, the V- signal sets the limit for the peak current signal. When the peak current reaches V- level, the internal logic turns off the PWM output for the rest of the swithcing cycle. After which, the PWM resets and starts deliver output in the next switching cycle (Figure 8)

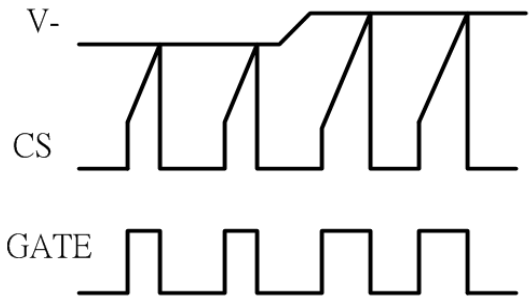


Figure 8

The NE1101A/B relies on the FB voltage level to determine the loading condition. In Figure 7, the FB signal is sent to two comparators whose thresholds are fixed at 0.72V and 1.20V for Burst and Normal mode operations respectively.

Under light load, the FB voltage will decrease in order to reduce the power deliver to the output. When FB voltage fells below 0.72V (V_{Burst}), the controller enters burst mode to maintain high efficiency operation. (See figures 7 and 9). When this occurs, an 100ms timer is activated. To prevent uncessary disruption of PFC bias due to momentarily load changes, the PFC_Vcc is turned off only after the timer expires. After which, the FB voltage oscillate at 0.72V±5% level as long as the output load is light..

When the load increases, the FB voltage will rise up to provide more power to the output. When FB voltge rises above 1.20V, the controller exits burst and resume normal operation. The PFC_Vcc begins to provide bias output immediately.

Over current protection

The NE1101A/B uses a timer function to differentiate Over current and momentarily large current transient conditions.

When over current occurs, the CS signal hwill rise to the 1V max limit and trigger a timer circuit. If the CS signal continues to hit the 1V limit for 100ms, the controller confirms the over current situation and turns off the PWM output. The Vcc supply to the controller will start dropping since the switching operation is halted.

When the Vcc decreases to 7.5V UVLO Off threshold, the controller enters deep sleep mode in which it will shutdown the internal functions further to reduce its operation current down to 520uA (typical). The Vcc decreases at much slower rate, which helps to cut down the auto-retry power dissipation further. When Vcc drops to 4.7V, the internal logic reset, the controller turns on the HV switch to charge the Cvcc capacitor to 12.5V UVLO On level and performs a softstart subsequently. If the over current situation persists and CS signal continues to hit 1V max peak current limit for 100ms timing delay, the above operation will repeat continusouly.

For momentarily transient load which the CS signal falls below 1V before the 100ms timer expires, the controller will reset the timer and resumes normal swiching operation.

Driver output

The NE1101A/B output is capable of delivering gate drive current that reaches rise time of 28ns and fall time of 24ns measured with a 1nF capacitive load. Its output voltage is clamped to 14.3V to protect the gate terminal of the external Mosfet and improve the reliablity of the power supply.

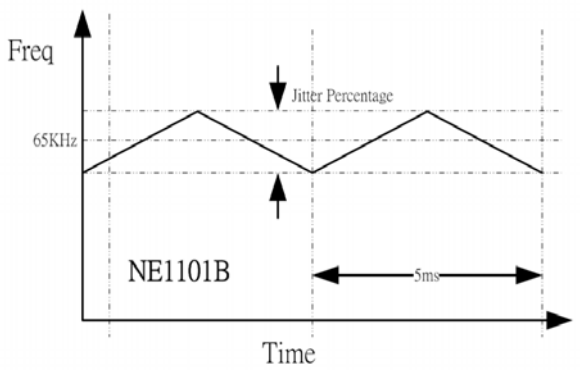


Figure 10

Frequency Jittering

The build-in frequency jittering function spreads the EMI spectrum and result in lower noise amplitudes. This features helps power designers meet the EMI requirements easier and at same time reduce the cost on EMI components. As shown in Figure 10 for NE1101B (65KHz), the switching frequency is modulated by +/-6.4% at interval of 5ms. The jittering function is disabled when the controller enters Burst mode under light load condition.

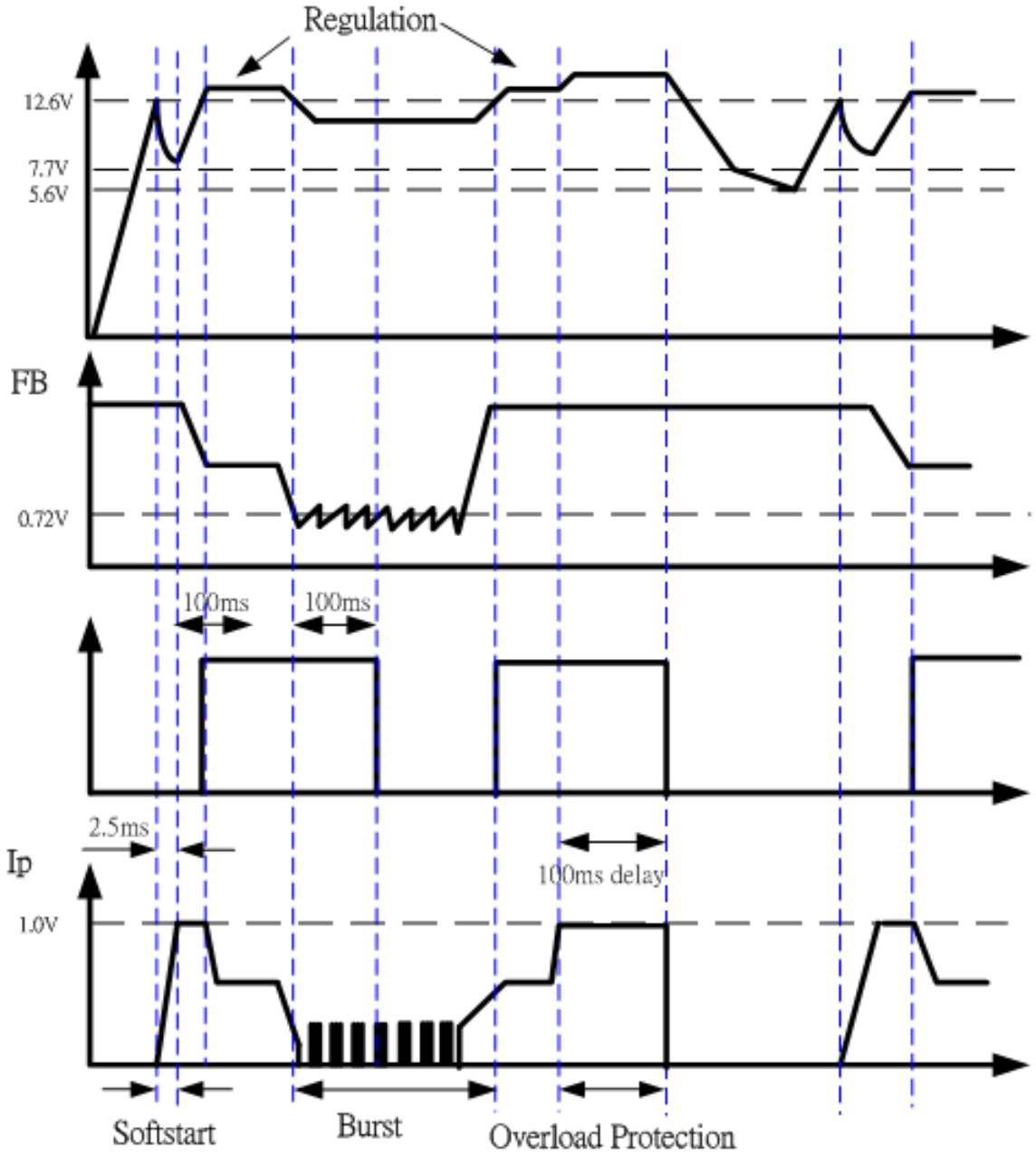
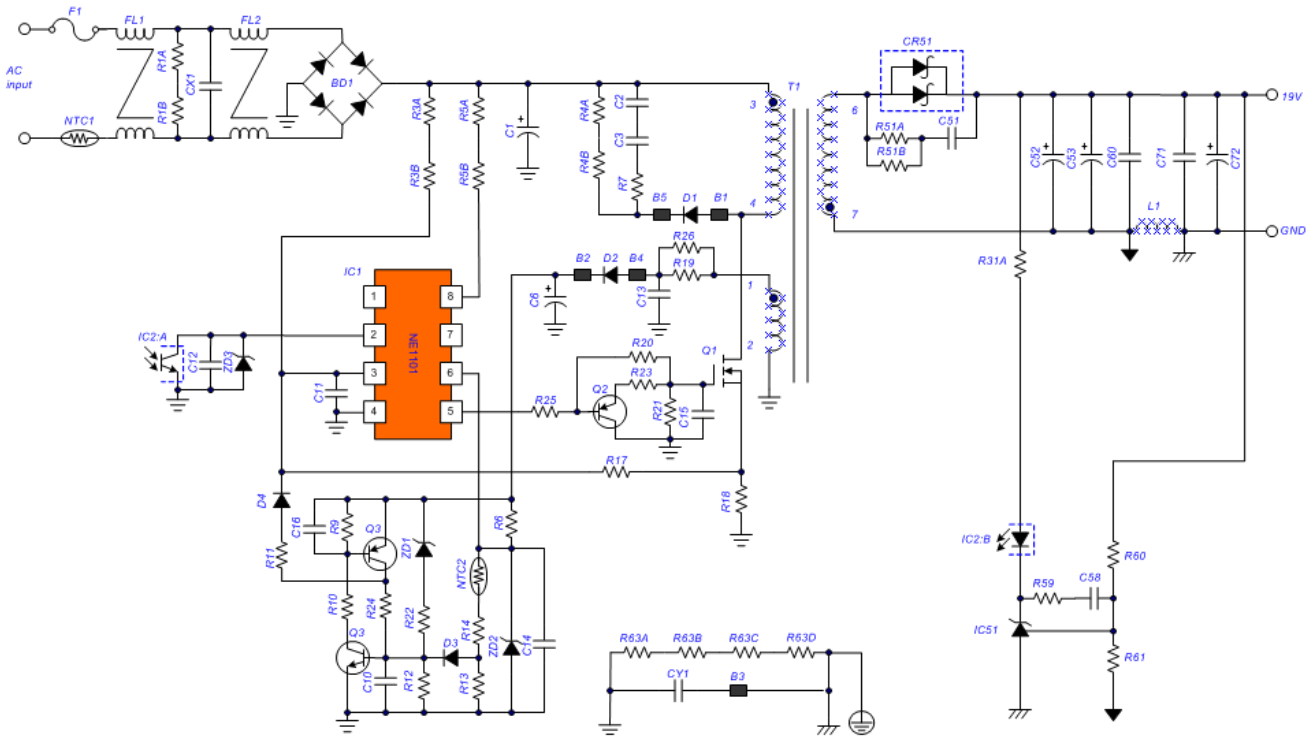


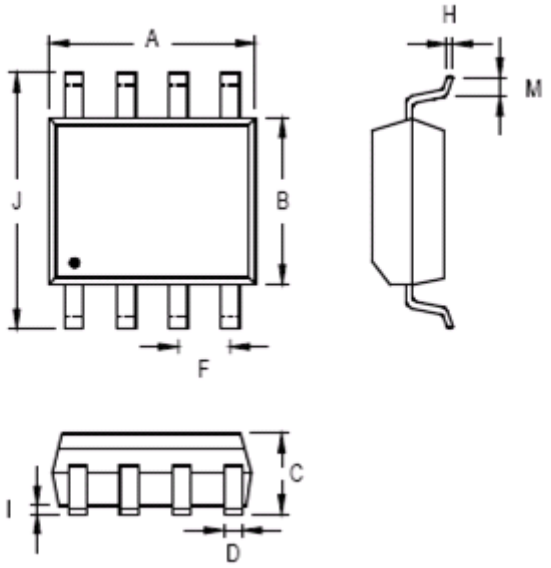
Figure 9 Timing diagram for Softstart, Burst and Overload protection

Typical Application: 12V output, 40W design



This is an application circuit that can deliver 12V, 40W power with all the protections such as OVP (latch), OTP (latch), OCP. Its AC input voltage is 90-270VAC. The open load standby power is 100mW and average efficiency is 87.15% with 230VAC input. Please contact NEM for evalaution board.

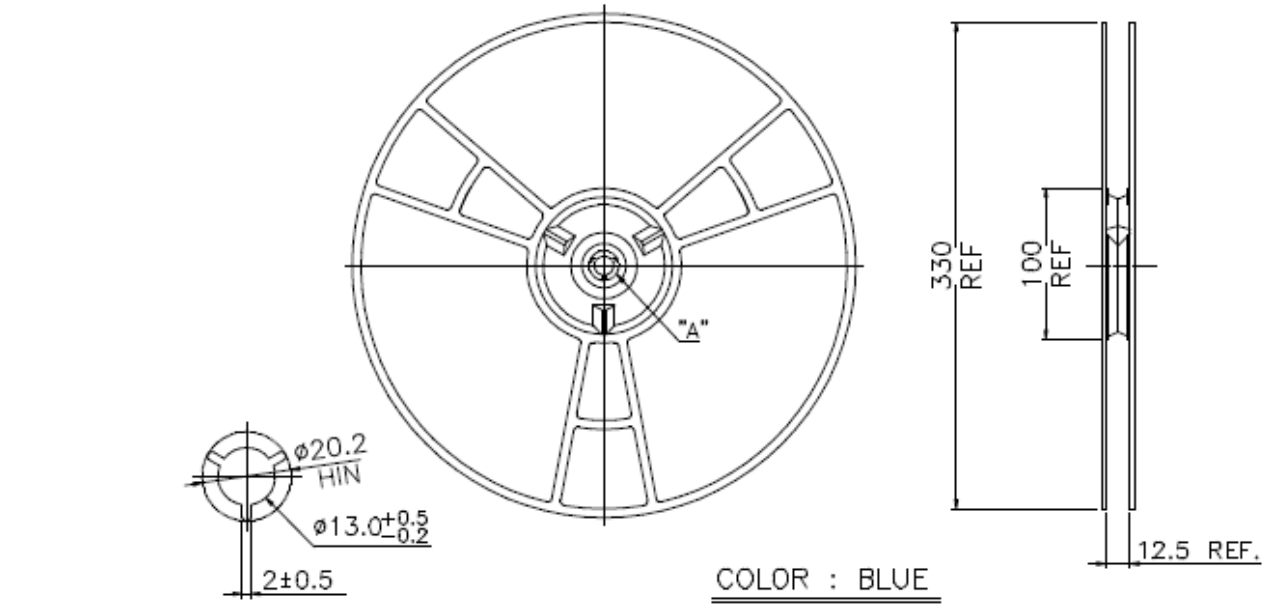
SO8 Package Outline Dimensions

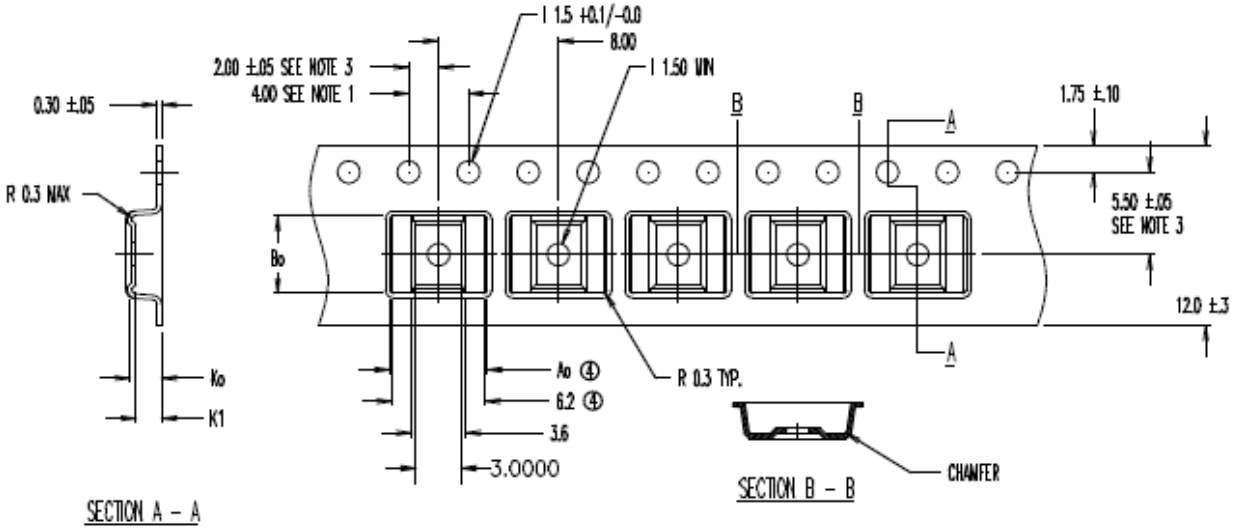


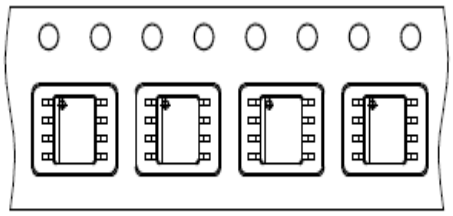
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

Tape and Reel Dimensions for SO8





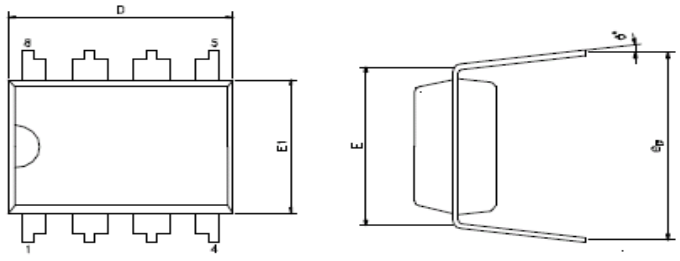


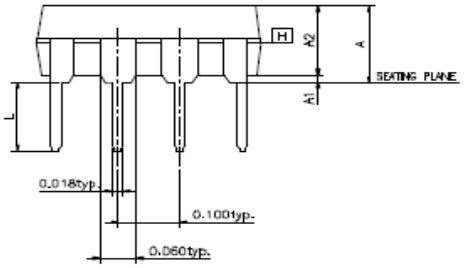
SOP 8N(150mil)

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2mm
2. Camber not to exceed 1mm in 100mm.
3. Material: Anti-Static Black Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

DIP8 Package Outline dimensions





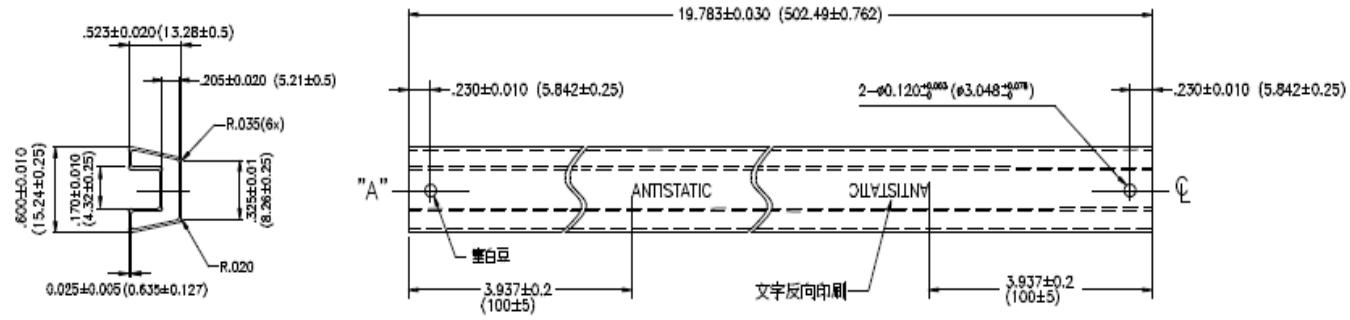
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

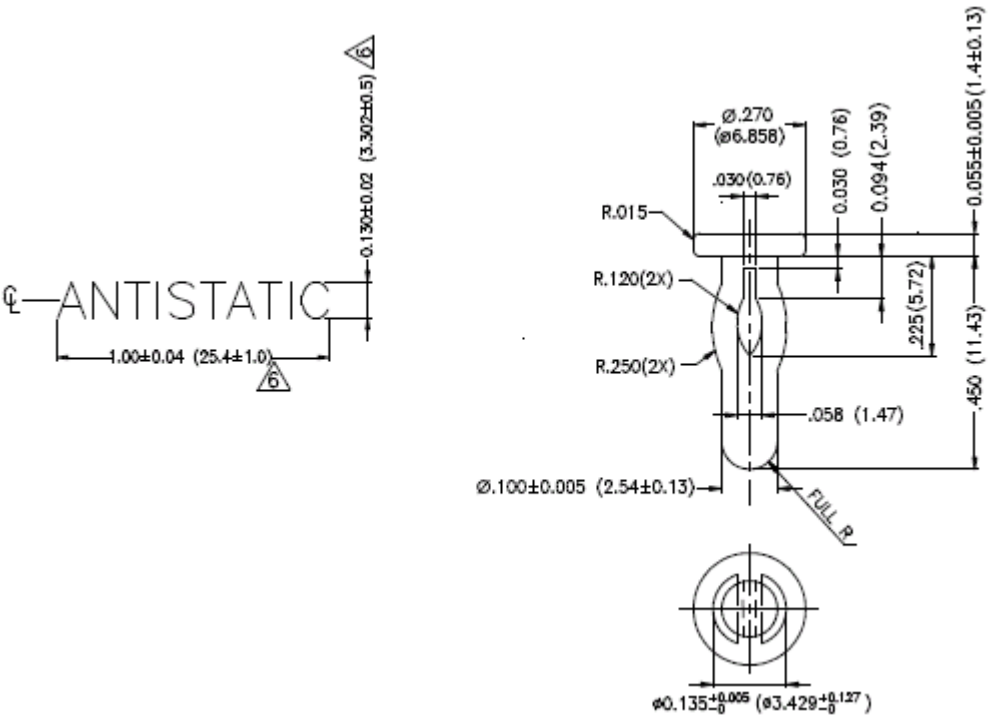
UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 BA
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

Tude Dimensions for DIP8





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