Executive Summary

This report presents a comprehensive analysis, modeling, simulation, and design optimization of the self-oscillating flyback converter, which is also known as the Ringing-Choke Converter (RCC). The self-oscillating flyback converter is a very popular topology in cost-sensitive applications such as, for example, auxiliary power supplies and mobile phone chargers due to a low component count. As a result, this circuit is designed into numerous Delta power supplies and chargers.

Although the self-oscillating flyback converter is a very simple circuit, the operation and design of the circuit is generally not well understood. The existing limited literature on this circuit only superficially addresses the operation of the circuit and its design. This lack of the full understanding of the operation and design of this popular and extensively used circuit prompted DPEL to dedicate significant resources to studying this circuit.

The major results of this study, which are included in this report, are:

- a very detailed analysis of the operation of the self-oscillating flyback converter power stage that fully explains the role of each component of the circuit, including the major parasitic components.

- The development of an accurate small-signal model of the power stage for feedback-loop design optimization.
- The development of a Saber simulation model of the circuit and its verification.
- The development of a step-by-step design procedure for the self-oscillating flyback power stage and its verification.
- The development of a detailed step-by-step feedback control procedure and its verification.

The report also presents a design example that uses the developed step-by-step design procedure. Finally, the source code of the developed Saber model and a MathCad worksheet developed to facilitate design optimization of the circuit are also included in the report.

Hopefully, the results of this study that are summarized in this report will help our engineers to come up with more cost-effective designs of the circuit by understanding its design trade-offs and by utilizing the provided design and simulation tools.

CONTENTS

1. INTRODUCTION

The self-oscillating flyback converter is a very attractive circuit because of a reduced component count [1] – [2]. Generally, in a self-oscillating converter the turn-on and turn-off instants are determined solely by power stage voltage and current conditions. Therefore, the self-oscillating converter operates with a variable switching frequency. In applications which does not require a tight output regulation in a wide range of input voltage and load current, the self-oscillating flyback converter is operated in open-loop fashion. However, in applications that require a tight output regulation, a feedback control is employed. The implementation of this control is simple and cost effective since the pulse-width modulator (PWM) and switch driver are implemented discretely using a single transistor, a positive-feedback winding, and a resistor/capacitor network.

The circuit diagram of a self-oscillating flyback converter is shown in Fig. 1. The circuit in Fig. 1 has two secondary windings: output winding N_{S1} and feedback winding N_{S2}. Output V_{O1} is tightly regulated by error amplifier E/A. The PWM modulator, which compares the error voltage V_e with a voltage proportional to the switch current, is implemented discretely using a single bipolar junction transistor (BJT) and two additional resistors.

Output voltage V_{O1} is sensed through a resistor divider consisting of resistors R_{d1} and R_{d2}, and compared at the input of a transconductance type amplifier (TL431) to a stable voltage reference located within the TL431 device. Components C_{EA1}, C_{EA2} and R_{EA1} are used as compensation to stabilize the voltage control loop. The difference between the sensed output voltage and voltage reference is amplified by TL431 and reflected to the primary side through optocoupler IC_1 as an error current i_e. The error current i_e is compared at the pulse width

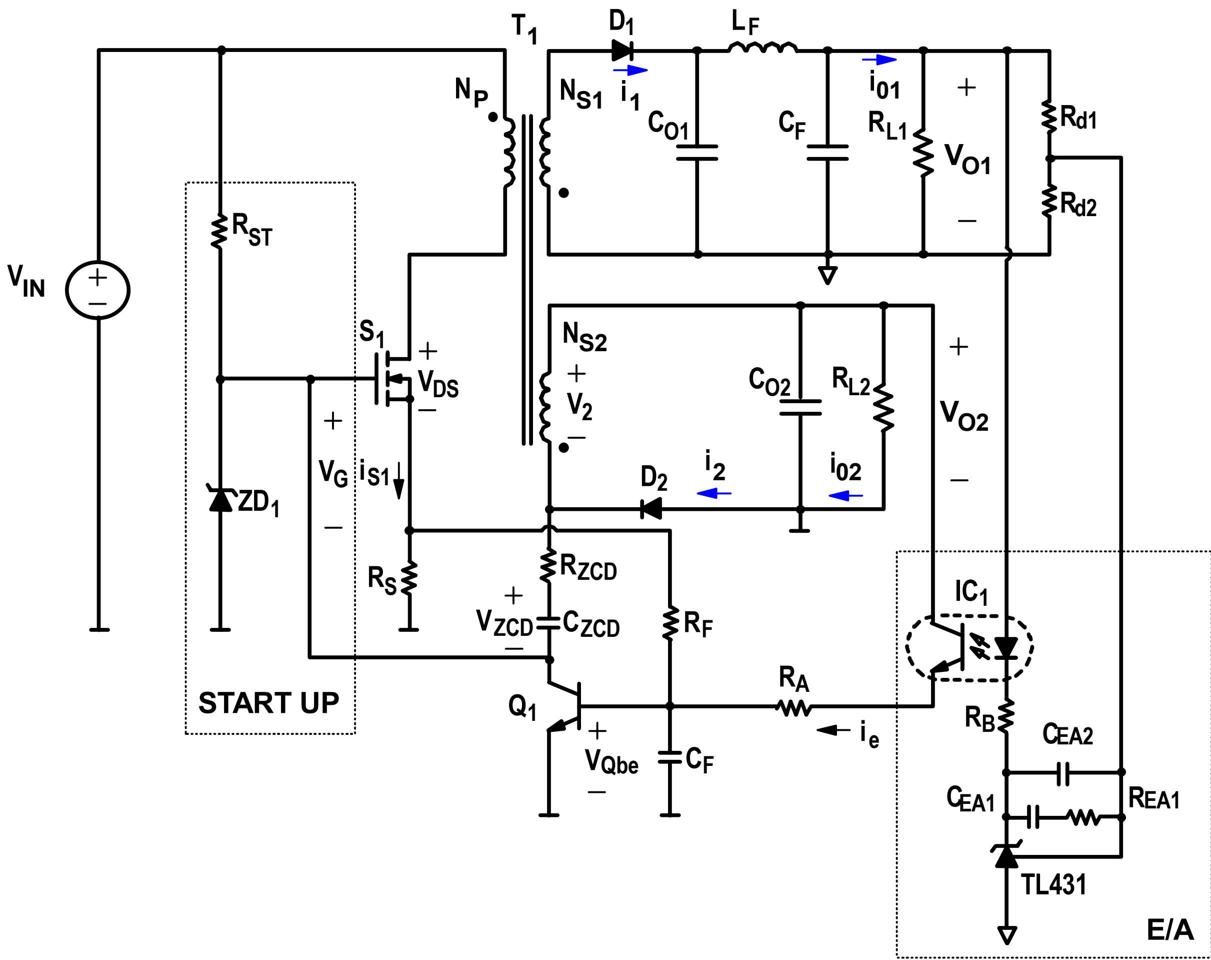


Fig. 1 Circuit diagram of self-oscillating flyback converter.

modulator (PWM), which consists of components Q_1, R_F, and C_F, to a voltage ramp which is proportional to switch current i_{S1} through resistor R_S.

Finally, a start-up circuit is implemented with components R_{ST}, ZD_1 and C_{ZCD}. When the input voltage V_{IN} is first applied, DC current is blocked by C_{ZCD} allowing the gate of S_1 to charge up to the clamp voltage set by ZD_1. Once switching action begins, charge is delivered to S_1 mainly by winding N_{S2}. Therefore, it is possible to ignore the start-up resistor R_{ST} during steady-state operation.

The self-oscillating flyback converter shown in Fig. 1 utilizes an n-channel enhancement mode metal-oxide-semiconductor field effect transistor (MOSFET) device as main switch S_1 and an npn bipolar transistor (BJT) device as auxiliary switch Q_1. Each transistor has different electrical characteristics and, therefore, different regions, or modes, of operation. The specific region of operation of a transistor device can be determined from it's terminal voltages and currents and an equivalent device model can be drawn for each mode of operation. The electrical characteristic curves of an n-channel MOSFET and an npn BJT, along with the equivalent device models used throughout this report, are shown in Fig. 2.

Typical output characteristics of the MOSFET device, i.e., drain current I_D as a function of drain-source voltage V_{DS} for different gate-source voltages V_{GS}, is shown in Fig. 2(a). In Fig. 2(a), three regions of operation are defined with three first-order-approximate equivalent device models for each region of operation. The first region of operation is the "off state" of the device (i.e., $I_D = 0$ A). In this region, the three terminal device is modeled with it's input capacitance C_{ISS} and it's output capacitance C_{OSS}. For the ohmic region (i.e., to the left of the dotted line and $I_D > 0$ A), the equivalent device model is the on-state resistance $R_{DS(on)}$ of the device. Generally, this is the desired region of operation for the device in switch-mode power converter topologies. The third region of operation is the constant-current region. In this region, the current does not change as a function of V_{DS}, but rather as a function of V_{GS}. This third region of operation is modeled as a dependent current source which draws current from the drain to the source and is controlled by voltage V_{GS}.

The output characteristics of the BJT device, i.e., collector current I_c as a function of collector to emitter voltage V_{ce} for different base currents I_b, is shown in Fig. 2(a). For the self-oscillating flyback converter shown in Fig. 1, quadrants I and III of the I_c vs. V_{ce} curves are used during a single switching period. For two-quadrant operation, five regions of operation are defined. In the first region of operation, that is for collector current $I_c = 0$ A, a first order approximation is made that all terminals have an infinite impedance between them (since the input and output capacitances of a BJT device are small and do not play a significant role in this application). The device transitions into quadrant I or III once it's base terminal voltage exceeds it's emitter terminal or collector terminal voltage level by it's intrinsic cut-off voltage level V_γ. Typically, voltage V_γ is in the 0.5 V to 0.6 V range for small-signal devices.

In quadrant I, i.e., in the region to the left of the dotted line and $I_c > 0$ A, the device operates in the saturation region. In this region, I_c increases linearly with V_{ce}. An equivalent device model is not shown since the circuit in Fig. 1 is generally not designed to operate in this region. The third region of operation, which lies to the right of the dotted line in quadrant I, is called the constant-current region. I_c in this region does not change (ideally) as a function of V_{ce} but only as a function of I_b. The equivalent device model for operation in the constant-current region of quadrant I (CC1) is drawn as a dependent current source that draws current from the collector to the emitter and which is controlled by base current I_b,, and a pn diode between base and emitter. It should be noted that there exists a large current gain between I_b and I_c in the constant-current region of operation.

The fourth and fifth regions of operation of the device are within quadrant III. Generally, the device is said to operate in it's "inverse" mode within this quadrant. The regions of operation in quadrant III are similar to quadrant I with the exception that the collector and emitter terminals are (effectively) interchanged and that the current gain between I_b and I_c is much smaller.

The fourth region of operation in quadrant III is the saturation region (S3). As in quadrant I, I_c changes linearly as a function of V_{ce}. As mentioned before, an equivalent device model is not shown since the circuit in Fig. 1 is generally not designed to operate in this region. The fifth region of operation in quadrant III is the constant-current region (CC3). As in quadrant I, I_c does not change (ideally) as a function of V_{ce} but as a function of I_b. The equivalent device model for operation in CC3 is drawn as a dependent current source which draws current from the emitter to the collector, and a pn diode between base and collector.

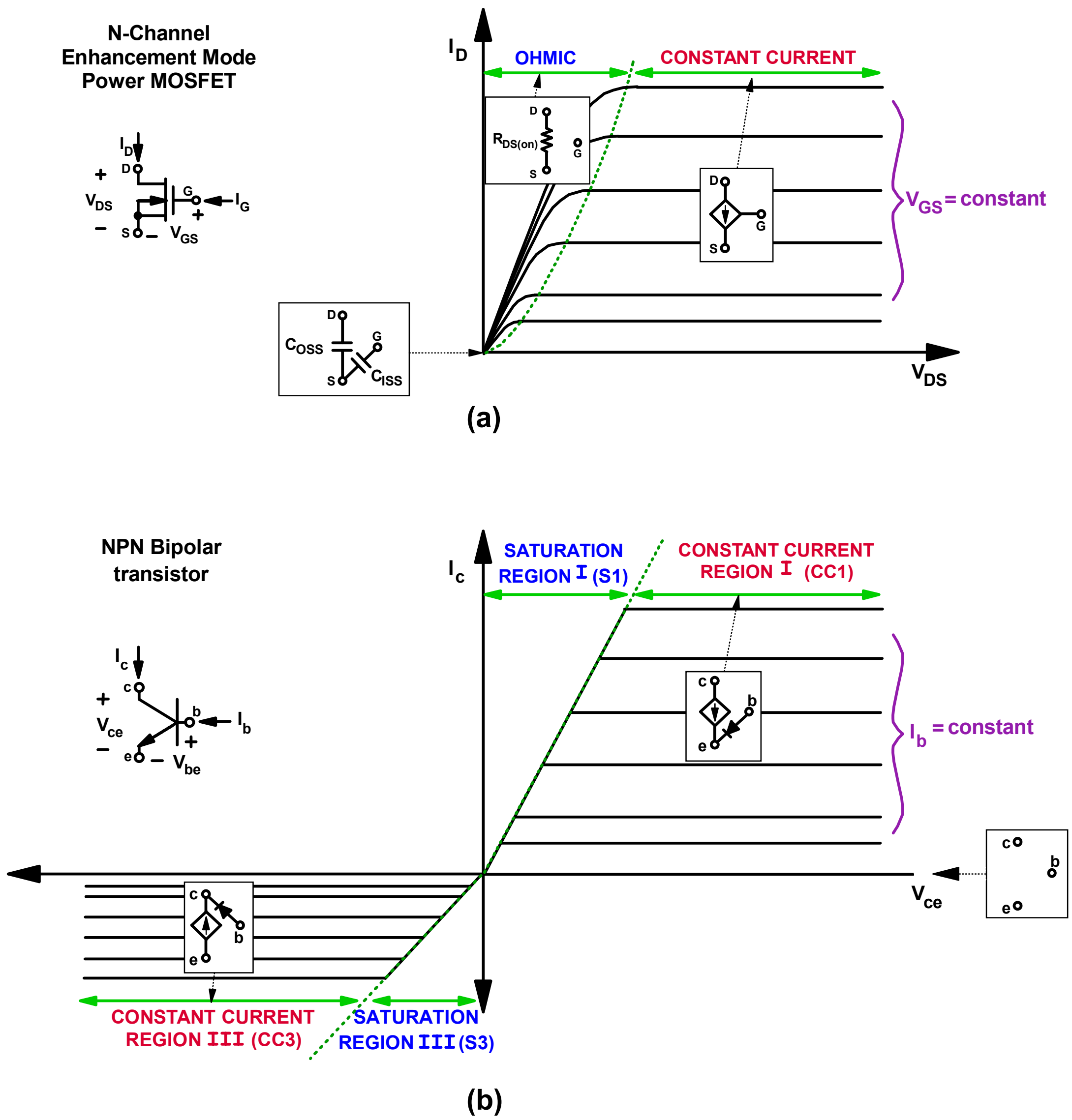


Fig. 2 Electrical characteristic curves and equivalent device models for: (a) n-channel enhancement mode power MOSFET and (b) npn BJT.

2. ANALYSIS OF OPERATION

In order to simplify the explanation of the converter shown in Fig. 1 during steady-state operation, several approximations have been made. The first approximation made was to neglect the leakage inductance of transformer T_1. This eliminated the need to consider the action of a voltage clamp across primary winding N_P which is implemented to protect main switch S_1 from voltage ringings.

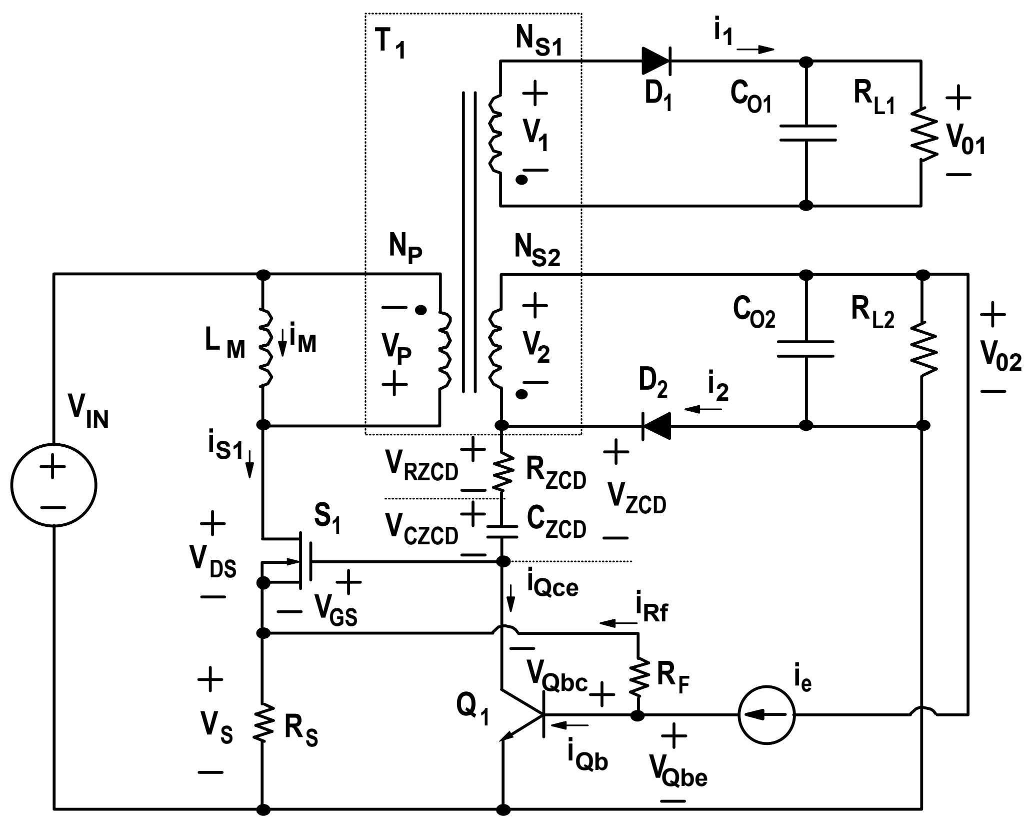


Fig. 3 Simplified circuit diagram of self-oscillating flyback converter.

The second approximation is to model the error current i_e as a constant-current source. This constant-current source replaces the compensated error amplifier TL431, the opto-coupler IC_1, the capacitor C_F, and the resistors R_{d1}, R_{d2}, R_A, and R_B. The final approximation is to neglect the capacitance C_{GD} between the gate and drain terminals of main switch S_1. The terminal capacitances between gate and source C_{GS} and between drain and source C_{DS} are modeled as input capacitance C_{ISS} and output capacitance C_{OSS}. In addition to these approximations, it is assumed that $C_{O1}>>C_{O2}$, $R_{L1}<<R_{L2}$,. The approximation $C_{O1} >> C_{O2}$ implies that the ripple voltage of output V_{O2} is greater than the ripple voltage of main output V_{O1}. Finally, it is assumed that rectifiers D_1 and D_2 are ideal (i.e., have zero forward voltage drop while conducting).

To facilitate the explanation of the converter operation, Fig. 4 shows eleven topological stages of the circuit in Fig. 1 during a switching cycle, whereas Fig. 5 shows key waveforms of the power-stage and control-stage. **Note that reference directions of currents and voltages are given in Fig. 3.**

Prior to $t = t_0$, switch S_1 is turning off because charge is drawn from the input capacitance C_{ISS} of main switch S_1 by transistor Q_1. As a result, drain-to-source voltage V_{DS} increases towards $V_{IN} + nV_O$. It is important to note that prior to $t = t_0$, voltage V_{CZCD} of capacitor C_{ZCD} is positive.

When, at $t = t_0$, V_{DS} reaches $V_{IN} + nV_O$, rectifiers D_1 and D_2 start conducting. During this stage, which is shown in Fig. 4 (a), magnetizing current i_M is instantaneously commutated from switch S_1 to output rectifiers D_1 and D_2 since it is assumed that leakage inductance L_{lkg} of the

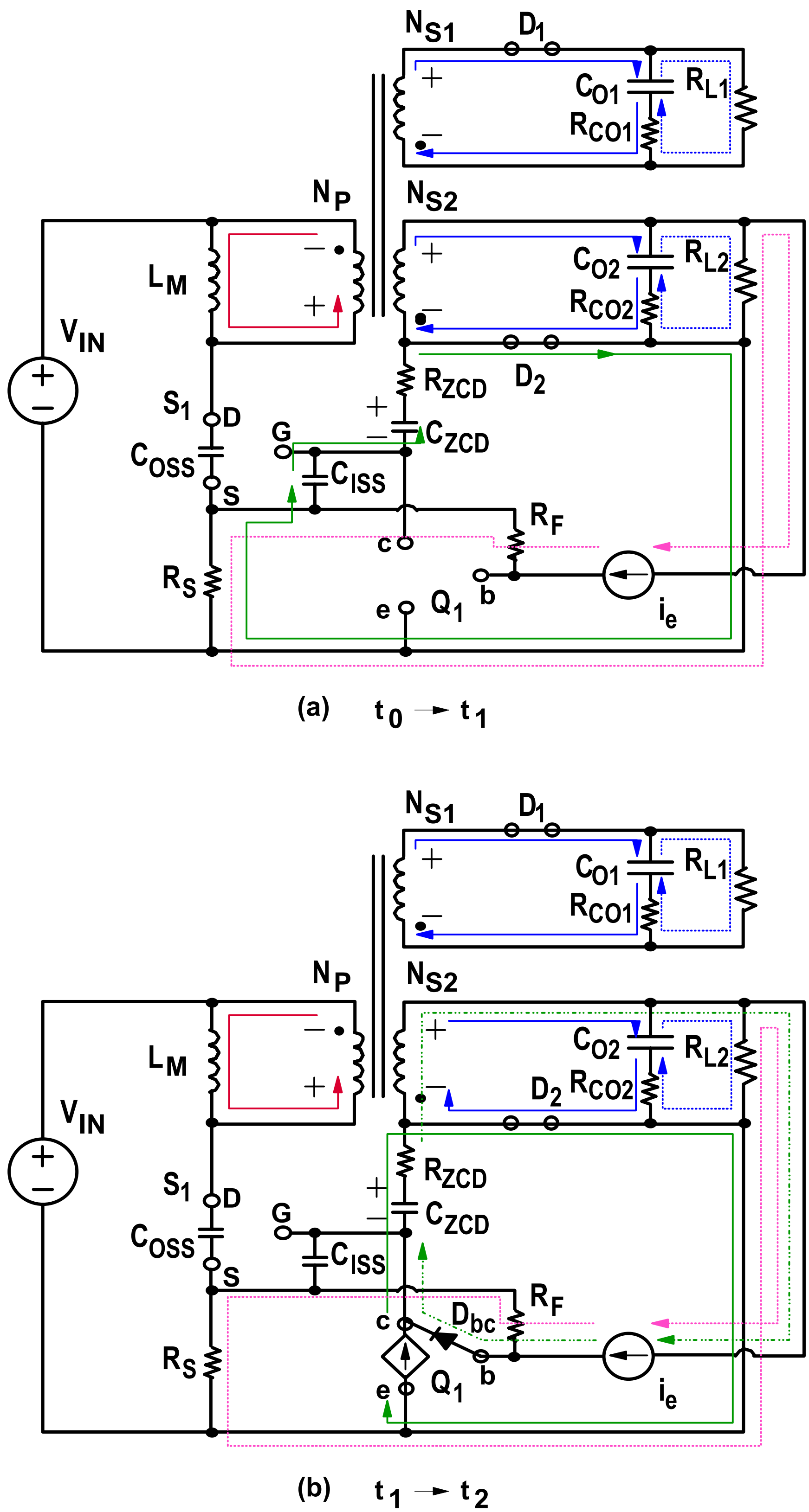
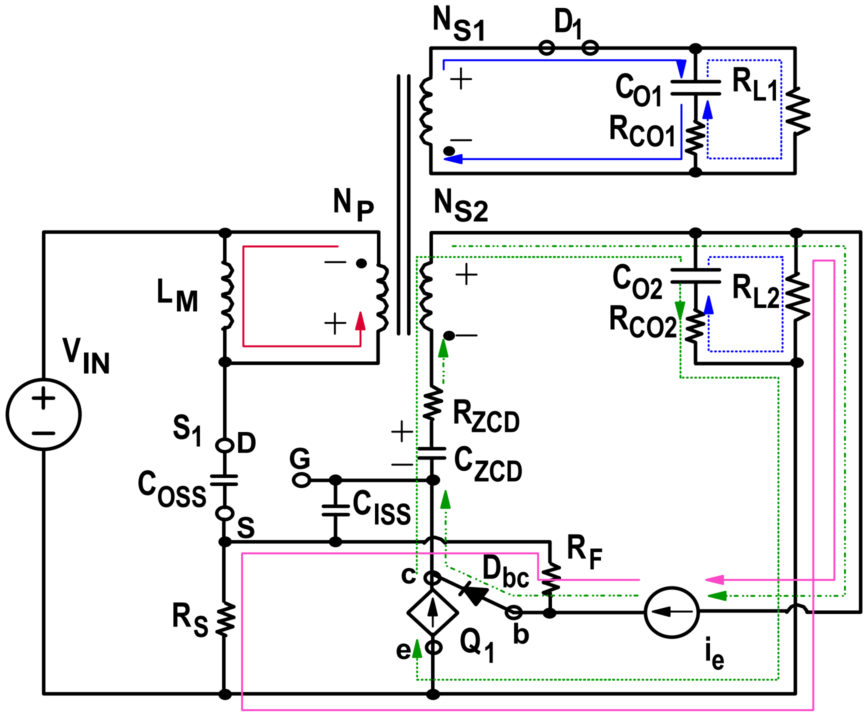
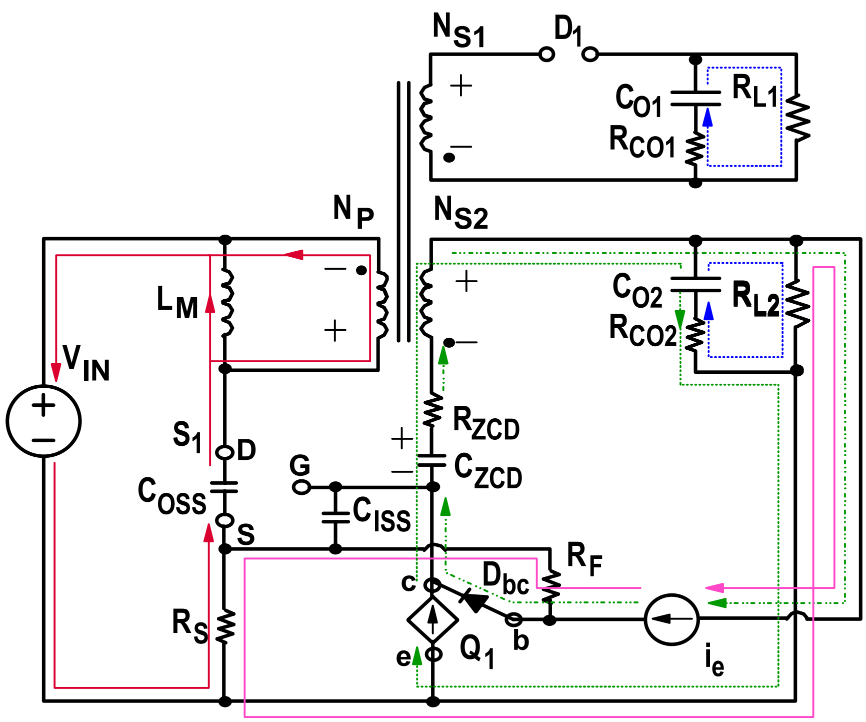


Fig. 4 Topological stages of self-oscillating flyback converter.

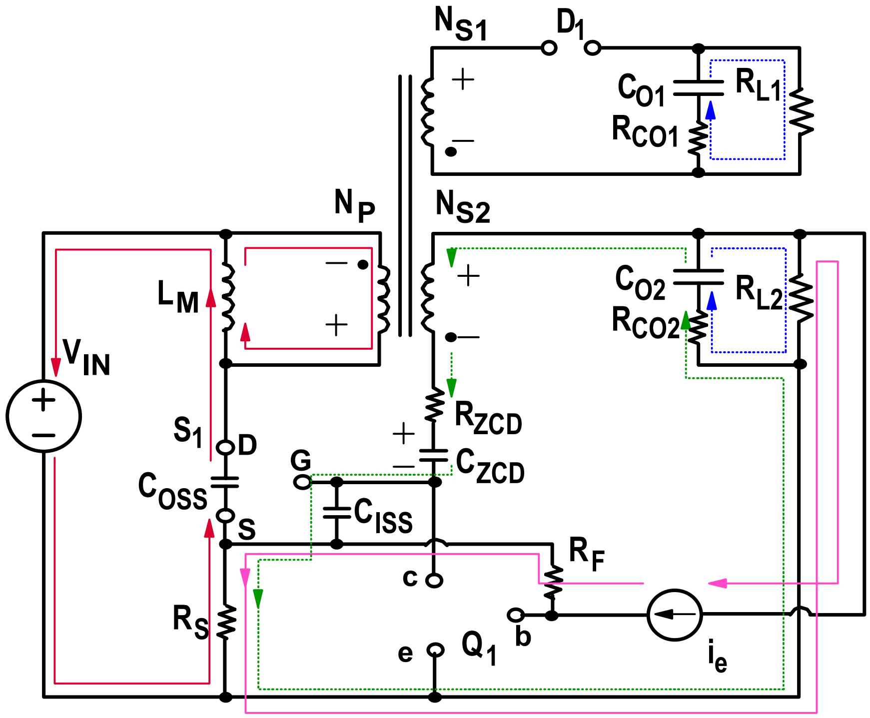


(c) $t_2 \rightarrow t_3$

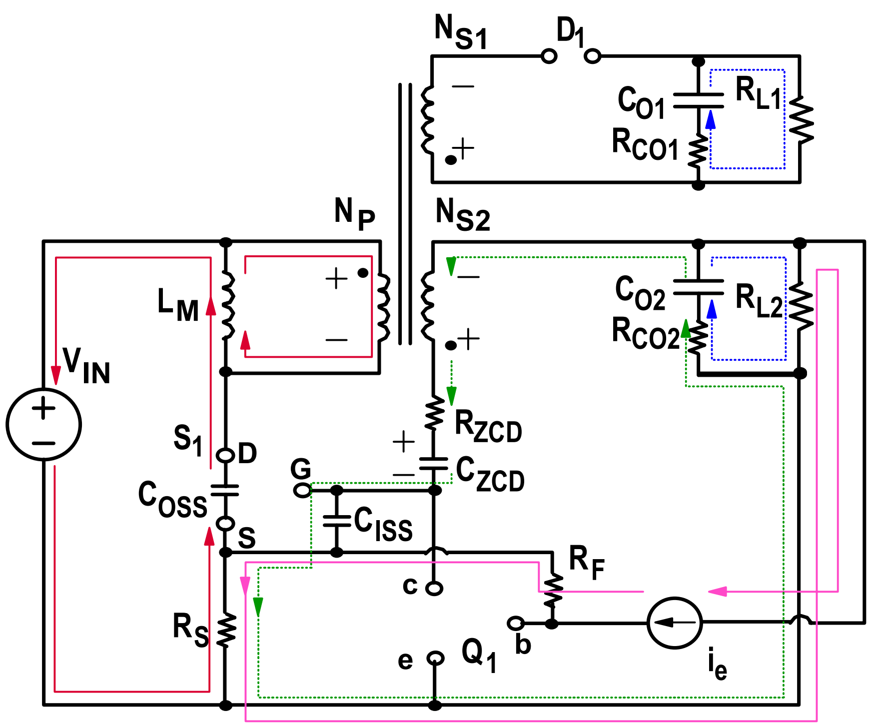


(d) $t_3 \rightarrow t_4$

Fig. 4 Topological stages of self-oscillating flyback converter (cont'd).

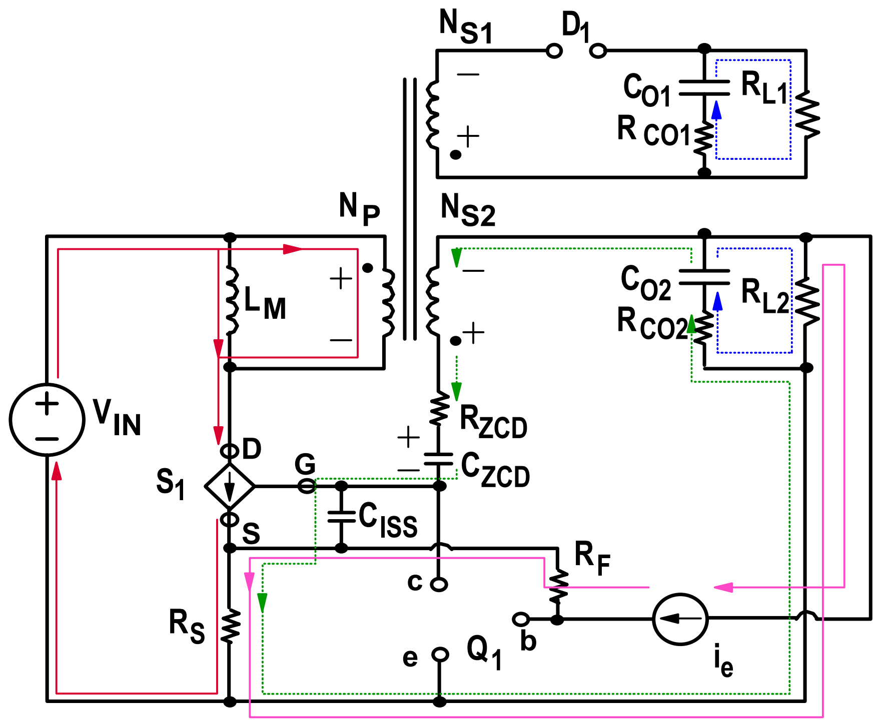


(e) $t_4 \rightarrow t_5$

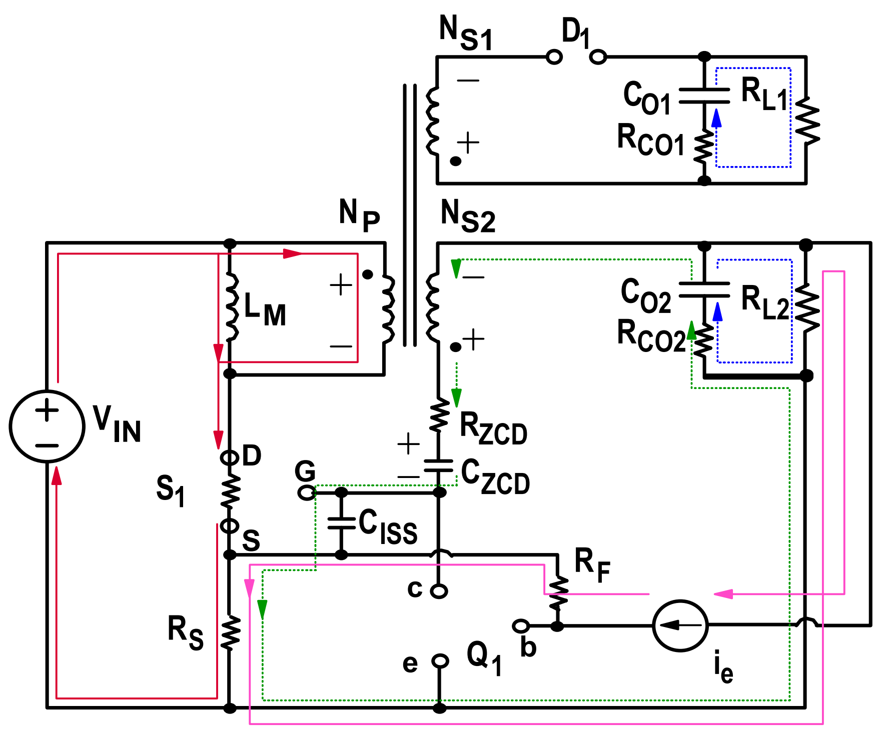


(f) $t_5 \rightarrow t_6$

Fig. 4 Topological stages of self-oscillating flyback converter (cont'd).

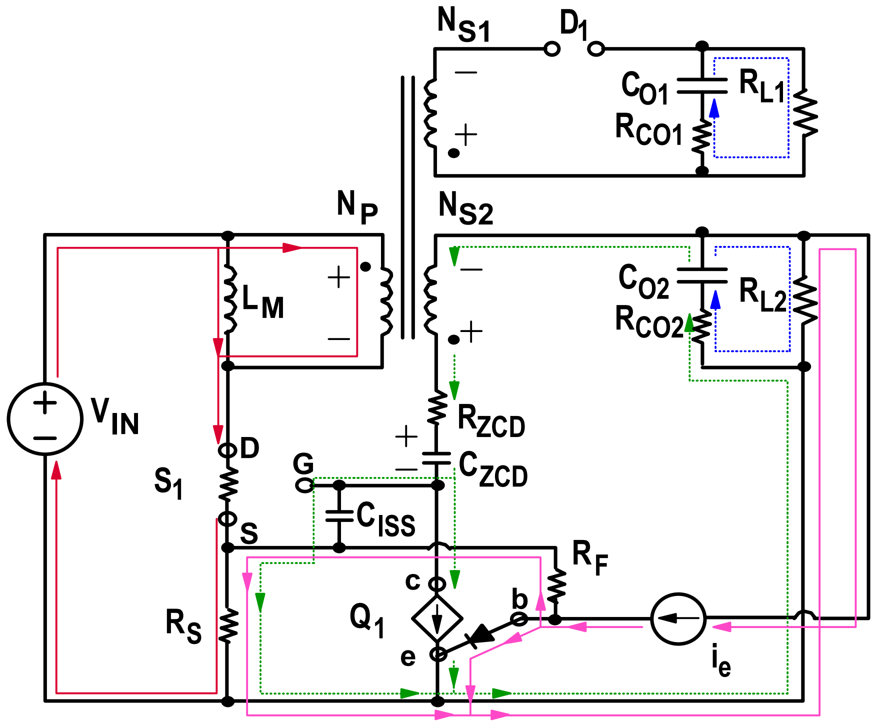


(g) $t_6 \rightarrow t_7$

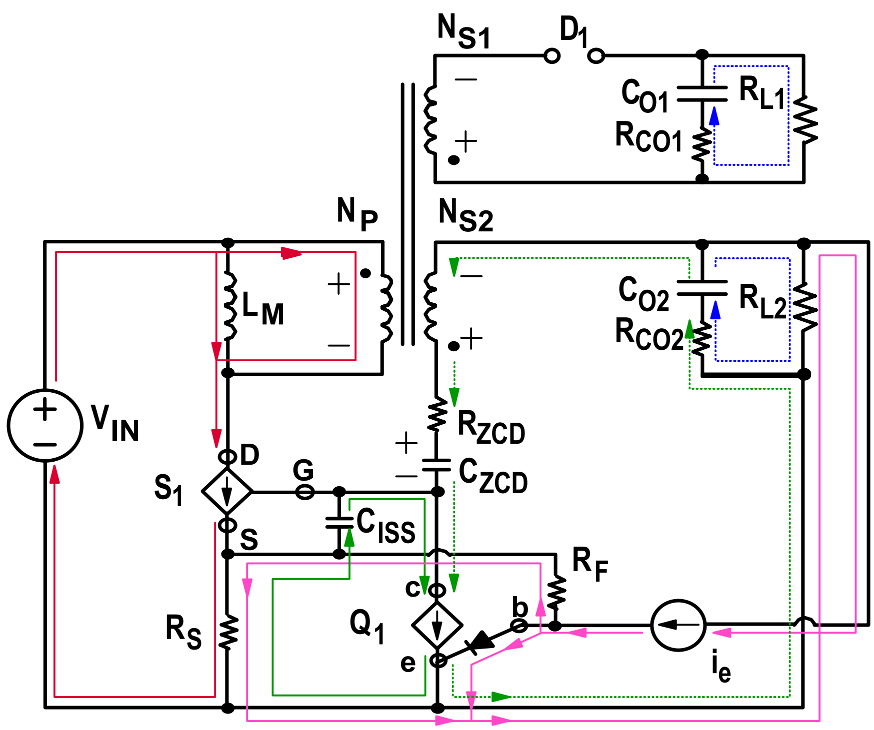


(h) $t_7 \rightarrow t_8$

Fig. 4 Topological stages of self-oscillating flyback converter (cont'd).



(i) $t_8 \rightarrow t_9$



(j) $t_9 \rightarrow t_{10}$

Fig. 4 Topological stages of self-oscillating flyback converter (cont'd).

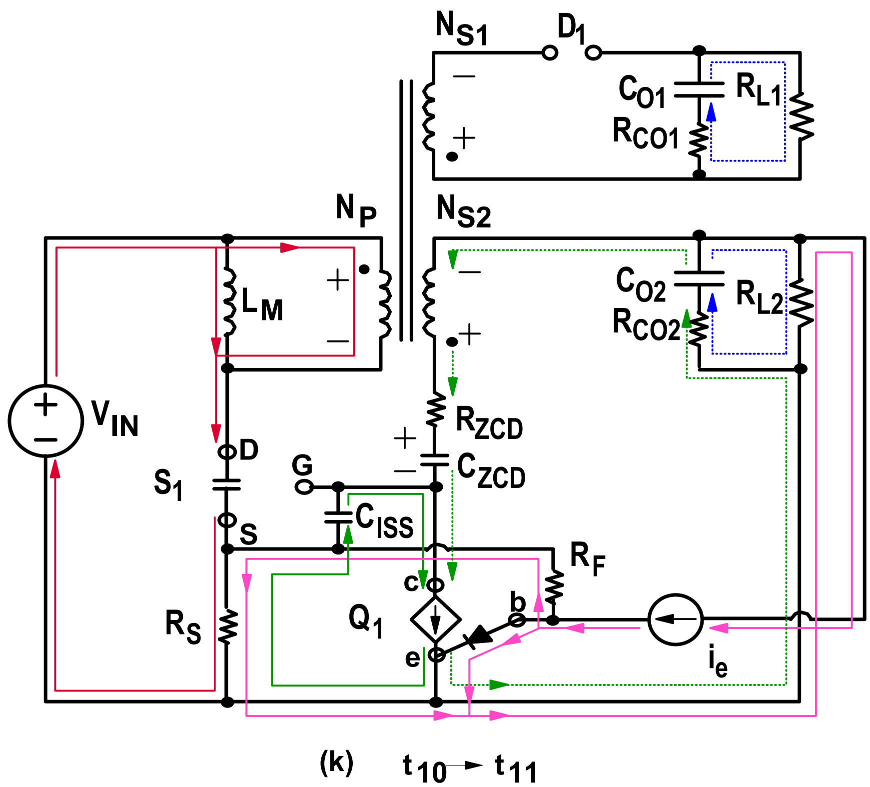


Fig. 4 Topological stages of self-oscillating flyback converter (cont'd).

transformer is zero. Due to the secondary-side parasitics such, for example, the leakage inductance and resistance of the windings (which are neglected in this analysis), the selection of the output capacitors such that $C_{O1}>>C_{O2}$ causes that voltage V_{O1} is approximately constant while voltage V_{O2} increases. This increase in output voltage V_{O2} results in a faster decrease of current i_2 with respect to current i_1, as shown in waveforms (d) and (e) of Fig. 5. Because during this topological stage rectifier D_2 is conducting, voltage V_{RZCD} across resistor R_{ZCD} is equal to $-(V_{GS} + V_S + V_{CZCD}) \approx -(V_{GS} + V_{ZCD})$ since $V_S << V_{GS} + V_{CZCD}$. This voltage induces current i_{ZCD} through resistor R_{ZCD} which discharges capacitors C_{ISS} and C_{ZCD}. At the same time, transistor Q_1 is off and current i_e flows through the loop consisting of resistors R_F, R_S, and R_{L2}. It should be

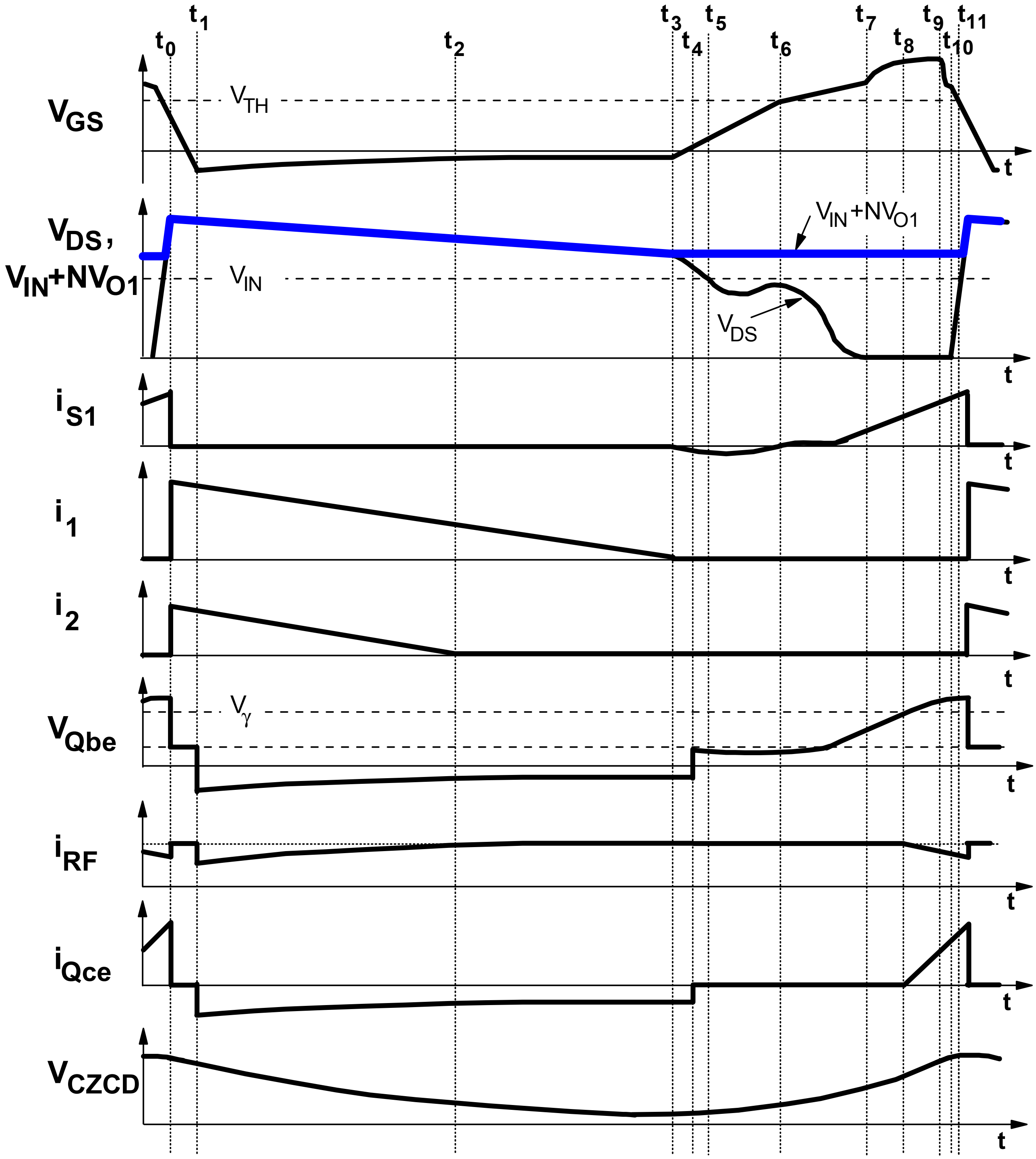


Fig. 5 Power stage and control stage key waveforms.

noted that transistor Q_1 will be in the off state only if it's base-emitter voltage V_{Qbe} is below it's cut-off voltage V_γ. Since from Fig. 4 (a) $V_{Qbe} = i_e R_F + i_{S1} R_S \approx i_e R_F$ because $i_{S1} R_S << i_e R_F$, transistor Q_1 is off during $t_0 < t < t_1$ if $i_e R_F < V_\gamma$. Stage in Fig. 4(a) ends at $t = t_1$ when V_{GS} has decreased to the voltage level which is approximately one diode voltage drop (0.6 – 0.7 V) below V_{Qbe} and base-collector pn junction is forward biased.

After base-collector diode D_{bc} starts conducting at $t = t_1$, current i_e is divided between resistor R_F and the base of Q_1. Because collector-emitter voltage V_{Qce} is negative, transistor Q_1 operates in the inverse-constant-current region (CC3) and current i_{Qce} flows from the emitter to the collector, as shown in Fig. 4 (b). During this stage, capacitor C_{ZCD} continues to discharge by the sum of currents i_{Qce} and i_{Qbc}. As a result, voltage V_{Qbe} increases exponentially as illustrated in waveform (f) of Fig. 5. At the same time, currents i_1 and i_2 continue to decrease. This stage ends at $t = t_2$ when rising voltage V_{O2} reaches the winding voltage V_2 and rectifier D_2 turns off.

After rectifier D_2 turns off at $t = t_2$, capacitor C_{ZCD} continues to discharge through winding N_{S2}, as shown in Fig. 4 (c). During this stage, current i_1 continues to decrease. This stage ends at $t = t_3$ when current i_1 reaches zero, i.e., when magnetizing energy of the transformer is completely discharged.

Since at the beginning of the topological stage shown in Fig 4 (d), $t = t_3$, drain-to-source voltage V_{DS} of S_1 is $V_{IN} + nV_O$, i.e., it is higher than the input voltage V_{IN}, C_{OSS} starts to resonantly discharge through magnetizing inductance L_M, as can be seen in waveform (b) of Fig. 5. As a result, primary voltage V_P decreases causing a proportional decrease in secondary voltage V_2. As the secondary voltage decreases, the voltage across R_{ZCD} also decreases which decreases the current i_{ZCD}. This topological stage ends at $t = t_4$ when current i_{ZCD} reaches zero.

After $t = t_4$, current i_{ZCD} starts flowing in the opposite direction so that capacitors C_{ZCD} and C_{ISS} start to charge, as shown in Fig. 4 (e). Since the increase of voltage V_{GS} leads to the increase of collector-emitter voltage V_{Qce}, diode D_{bc} turns off causing the turn off of transistor Q_1. At the same time, capacitor C_{OSS} continues to resonantly discharge, which further decreases secondary winding voltage V_2. As a result, the voltage across resistor R_{ZCD} increases which causes a further increase of current i_{ZCD}. This topological stage ends at $t = t_5$ when the voltage across the windings of the transformer become equal to zero.

After $t = t_5$, capacitor C_{OSS} continues to discharge and the winding voltages change polarity, as shown in Fig. 4 (f). Because in this topological stage voltage $V_{O2} + V_2$, which drives current i_{ZCD}, continues to increase, current i_{ZCD} also continues to increase. This increased i_{ZCD} causes an increase of voltage V_{GS}, which in turn produces a further discharge of capacitor C_{OSS} and consequently a further increase in the sum of voltages $V_{O2} + V_2$. This positive feedback continues until V_{GS} reaches threshold voltage V_{TH} at $t = t_6$ and switch S_1 is turned on by entering it's constant-current region.

After $t = t_6$, gate-source voltage V_{GS} continues to increase as current i_{ZCD} continues to flow through capacitor C_{ISS}, as shown in Fig. 4 (g). The stage in Fig. 4 (g) ends at $t = t_7$ when gate-source voltage V_{GS} reaches the level where switch S_1 begins operating in the ohmic region, i.e., when switch S_1 is fully turned on.

After switch S_1 is fully turned on at $t = t_7$, drain-source current i_{S1} starts increasing linearly with slope $di_{S1}/dt = V_{IN}/L_M$. As a result, voltage drop $V_S = i_{S1}R_S$ across sensing resistor R_S also increases with the same slope. This increases the potential of the source terminal of S_1, which also increases the potentials of the gate terminal of S_1 and the base terminal of Q_1, as shown in waveforms (a) and (f) of Fig. 5. When at $t = t_8$, base-emitter voltage V_{Qbe} reaches it's cut-off voltage V_γ, transistor Q_1 starts conducting, as shown in Fig. 4 (i). It should be noted that to prevent the gate voltage of S_1 of exceeding the maximum rated voltage level, a voltage clamp (such as a zener diode) should be connected between the gate terminal of S_1 and ground. Once the gate voltage is clamped, current is diverted from input capacitance C_{ISS} to the voltage clamp until the gate voltage falls below the clamp voltage level.

Since after $t = t_8$ voltage V_{Qbe} continues to increase because voltage $V_S = i_{S1}R_S$ increases, base current i_{Qbe} of Q_1 increases causing the increase of current i_{Qce}. This topological stage ends at $t = t_9$ when current i_{Qce} becomes equal to current i_{ZCD} and gate-source capacitance starts discharging, as shown in Fig. 4 (j). As gate-source voltage decreases, transistor S_1 is turning off. At $t = t_{10}$, gate-source voltage V_{GS} decreases to the threshold voltage V_{TH} of S_1 so that S_1 is turned off.

After S_1 is turned off at $t = t_{10}$, the output capacitance C_{OSS} of S_1 begins to charge so that voltage V_{DS} begins to increase. This topological stage shown in Fig. 4 (k) ends when voltage $V_{DS} + V_S \approx V_{DS}$ reaches $V_{IN} + nV_O$. At the same time, secondary rectifier D_1 and D_2 start conducting and transistor Q_1 turns off, which completes a switching cycle.

3. VERIFICATION OF ANALYSIS OF OPERATION

To verify the presented analysis of operation, Saber™ simulation models were developed for the self-oscillating flyback converter used as the stand-by power supply in Delta power supply DPS-250AB A. The schematic diagram of this 5 V/2 A auxiliary circuit, which operates with a 310 V nominal input voltage, is included in Appendix A for reference. Note that the protection circuitry, such as over-voltage and thermal shutdown, have been excluded from these simulation models.

3.1. Simplified Simulation Model

The first simulation model, shown in Fig. 6, has a similar circuit schematic as the simplified circuit shown previously in Fig. 3. The differences between them are the inclusion of the start-up resistor R_{ST}, and the zener diode ZD_1, which clamps the gate voltage to 18 V. For simplicity, the input voltage source is modeled with a constant DC source, rather than the bulk capacitor and rectifier front end used in the Delta circuit. It should be noted that the value of error current source i_e was experimentally determined to maintain the appropriate output voltage.

3.1.1. Full Load Operation

Simulation waveforms generated using the simulation model shown in Fig. 6 at the full load condition are shown in Fig. 7. These waveforms, which are drawn using the chart function of Lotus Freelance Graphics™ software (to obtain a better picture quality than the quality offered by Saber Scope™), show that at the full load condition, the gate-source voltage

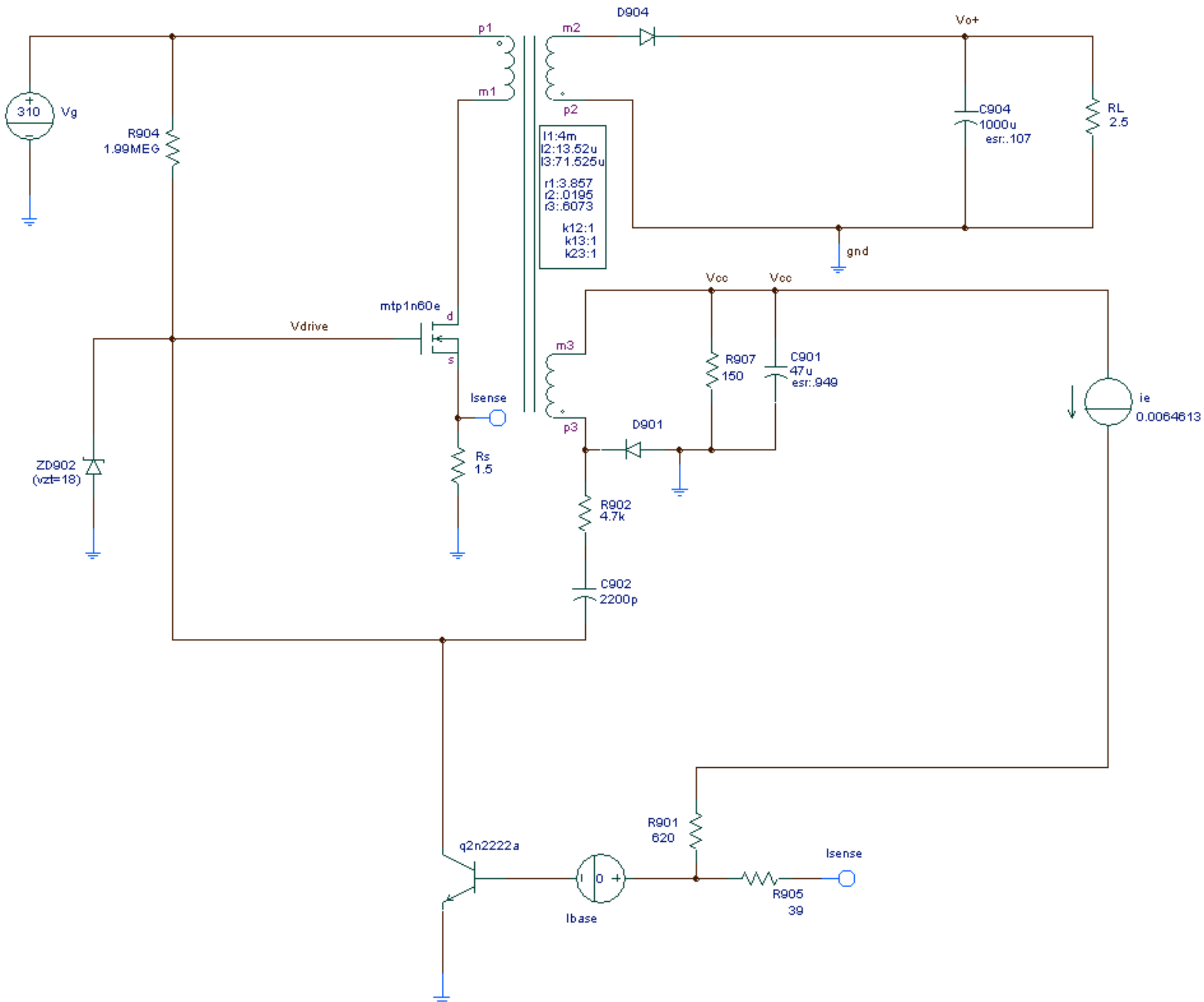


Fig. 6 Simplified simulation model of auxiliary circuit used in Delta power supply DPS 250AB A.

V_{GS} is clamped by the zener diode ZD_1 for the majority of the on time. This is an indication that the device operates mainly within it's ohmic region, and, therefore, a higher energy conversion efficiency is achieved. The main switch S_1 is shown to turn on very near the moment that drain-source voltage V_{DS} reaches it's resonant valley which is an indication that the power stage operates very near it's CCM/DCM boundary (i.e., the dead time t_D is very small compared with the switching period). This boundary operation is also evident from switch current i_{S1} and secondary current i_1 waveforms. In addition, secondary current i_2 reaches a near zero level and rectifier D_2 turns off long before secondary current i_1 reaches zero, as expected because $C_{O1} >> C_{O2}$. In the control waveforms, the intersection of the base voltage V_{Qbe} with its intrinsic cut-off voltage level V_γ initiates turn-on of transistor Q_1, which draws current away from input capacitance C_{ISS} and leads to the turn off of main switch S_1. Finally, it is shown that current i_{RF}, which flows through resistor R_F, is equal to the error current i_e while switch S_1 is on, and is below current i_e during the off time, since transistor Q_1 operates in its inverse constant-current region as it discharges capacitor C_{ZCD}. Voltage V_{CZCD} decreases during this time, and increase during the on time as charge is delivered through it to the main switch S_1.

It should be noted that the effect of the gate-drain capacitance C_{GD}, which was not neglected in the simplified simulation model, is to introduce additional current resonances in the control circuit currents. These resonances are most apparent in waveform (g) of Fig. 7, especially at the moments of turn-off of main switch S_1, and are shown to have no effect on the fundamental operation of the circuit.

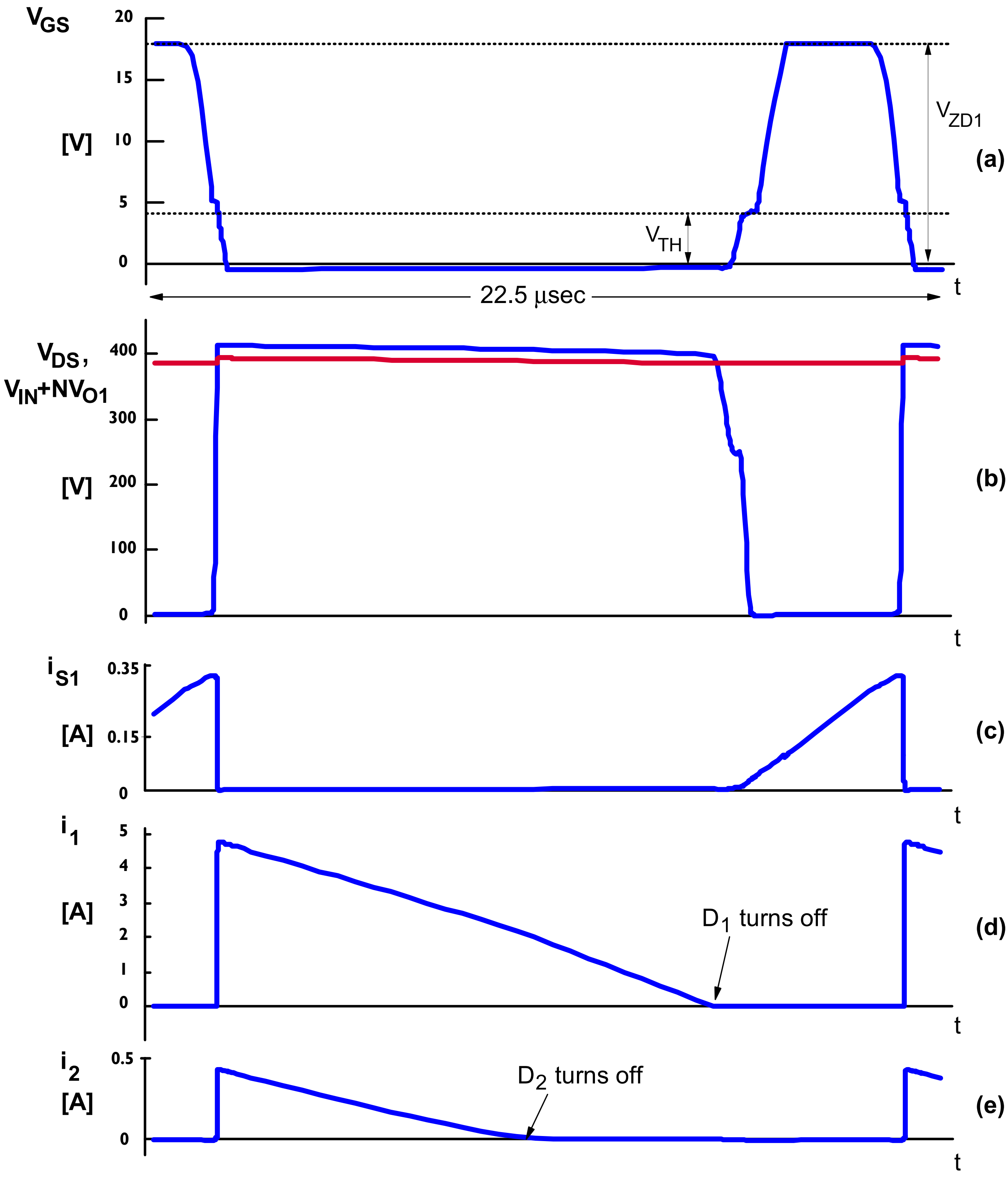


Fig. 7 Simplified simulation waveforms of the auxiliary circuit within Delta power supply DPS 250AB A operating at full load.

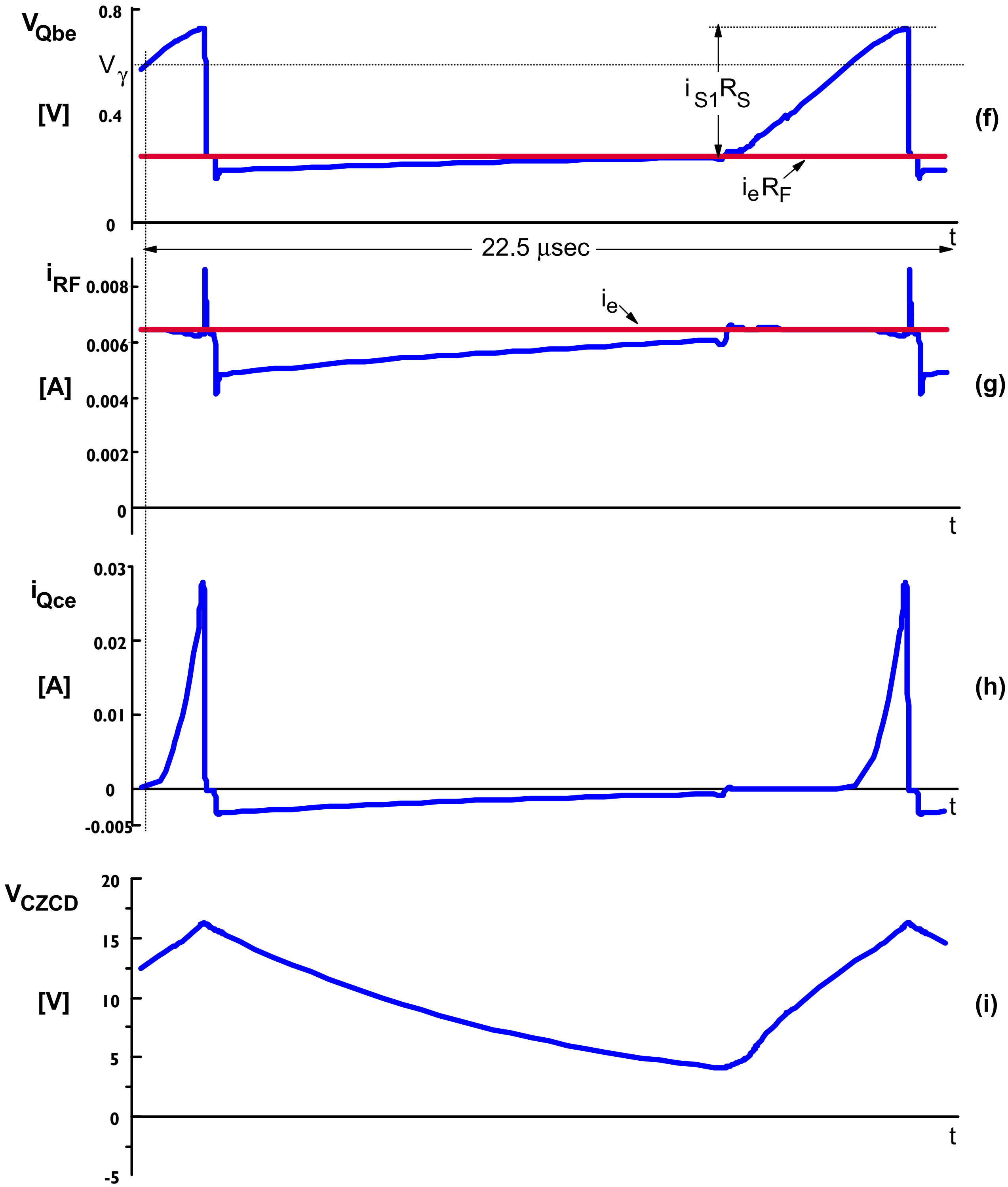


Fig. 7 Simplified simulation waveforms of the auxiliary circuit within Delta power supply DPS-250AB A operating at full load (cont'd).

3.1.2. *Light Load Operation*

Simulation waveforms at a light load condition (i.e., 25% full load) are shown in Fig. 8. Since the same time base was used for both Figs. 7 and 8, it can be seen that as the load decreases, the switching frequency of the converter increases, and the length of time that main switch S_1 operates in the ohmic region decreases. Because the time spent by switch S_1 in the constant-current region is nearly constant when the ripple voltage across capacitor C_{ZCD} is small, the gate-source voltage V_{GS} can drop below the clamp voltage level as shown in waveform (a) of Fig. 8. Switch S_1 is shown to turn on after the drain-source voltage reaches its resonant valley, and dead time t_D is slightly greater compared to full load operation.

Because at light load the current demand is decreased, the switch current i_{S1} and secondary winding current i_1 are decreased, whereas secondary current i_2 remains the same (since its load resistance remained unchanged). It should be noted from waveforms (d) and (e) in Fig. 5 that at light load, output rectifiers D_1 and D_2 turn off at approximately the same time. This happens because at light load the current demand on the output is decreased, while the current demand at the feedback winding stays the same.

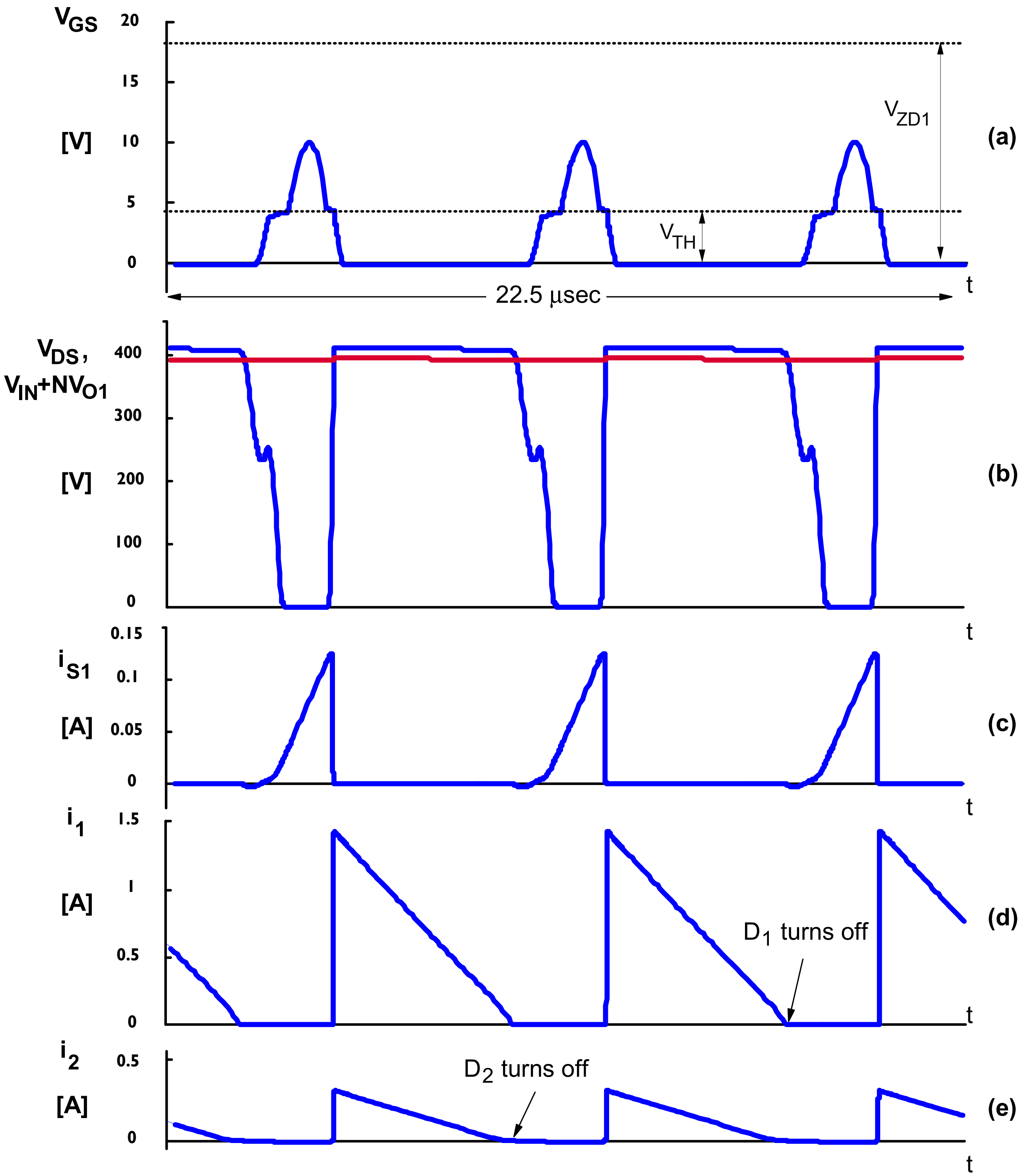


Fig. 8 Simplified simulation waveforms of the auxiliary circuit used in Delta power supply DPS 250AB A operating at 25 % full load.

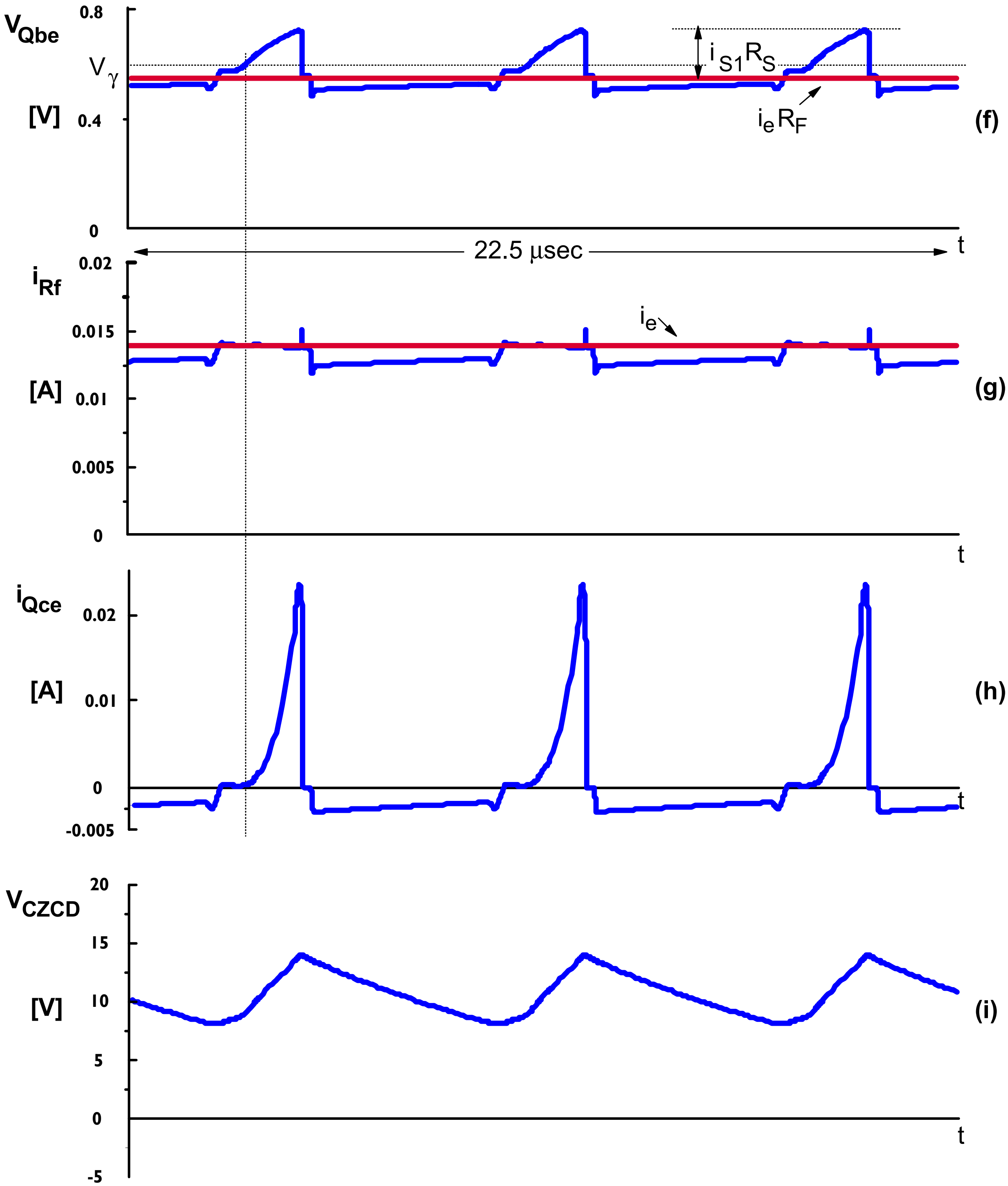


Fig. 8 Simplified simulation waveforms of the auxiliary circuit used in Delta power supply DPS 250AB A operating at 25 % full load (cont'd).

As the load current decreases, error current i_e increases, as shown in waveform (g) of Figs. 7 and 8, which results in an increase in the dc value of base-emitter voltage V_{Qbe}. As in the full load case, the turn off of switch S_1 begins once voltage V_{Qbe} reaches voltage level V_γ, and voltage V_{CZCD} across capacitor C_{ZCD} charges during the on time and discharges during the off time of switch S_1. However, the ripple voltage of voltage V_{CZCD} decreases since both the on time and off time of switch S_1 are shorter.

3.2. Complete Circuit Model

Previously, approximations were made to simplify the circuit schematic to its fundamental components for the purpose of analysis. The simplified circuit was divided into 11 topological stages, and through the analysis of each stage, an understanding of the circuit operation as a whole was obtained. Once an understanding of the simplified circuit is obtained, the simulation waveforms of the complete circuit can be understood.

To examine the effect of the neglected components, a complete simulation model, shown in Fig. 9, was developed. The model differs from the previous simplified simulation model in that it includes the leakage inductance of the transformer L_{lkg} , the clamp circuit across winding N_P, the error amplifier TL431, the optocoupler IC_1 and components R_{d1}, R_{d2}, C_{EA1}, C_{EA2}, R_{EA1}, R_B, R_A, and C_F.

3.2.1. Full Load Operation

With the circuit fully loaded, a time-domain transient analysis was performed and steady-state simulation waveforms were obtained. These simulation waveforms, shown in Fig. 10, are very similar to those obtained with the simplified model previously shown in Fig. 7. The

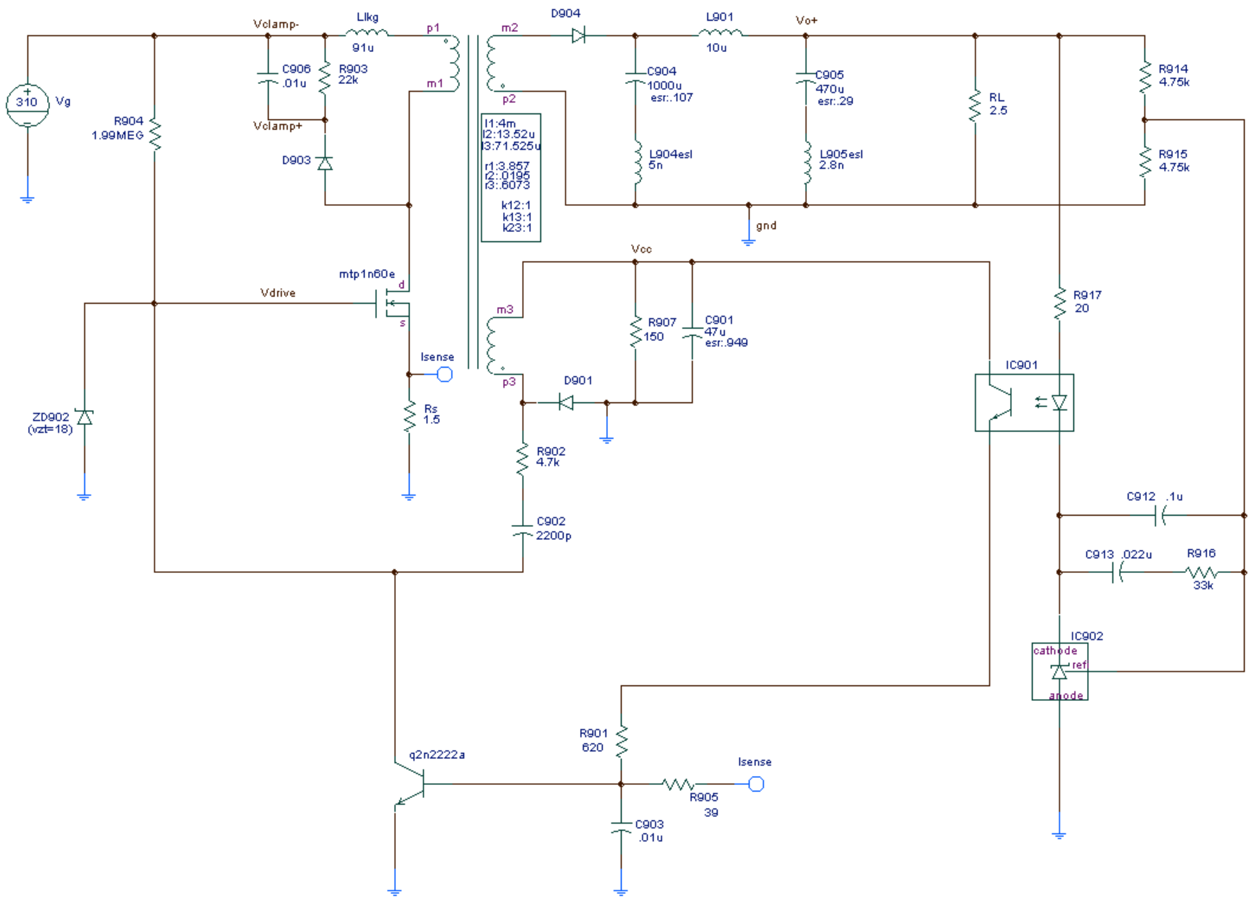


Fig. 9 Simulation model of auxiliary circuit within Delta power supply DPS-250AB A.

differences include the presence of voltage ringings in nearly every waveform, which is related to the addition of the leakage inductance of transformer T_1, and a slightly decreased switching frequency, which is due in part to the loss of the RCD clamp across winding N_{S1}. It should be noted that the leakage inductance not only resonates with circuit parasitic capacitances, but also prevents the current from commutating instantaneously from switch S_1 to rectifiers D_1 and D_2 as shown in waveforms (c), (d), and (e) of Fig. 10. It should also be noted that error current i_e is not constant (i.e., there is a small ripple current superimposed on the dc current). This small ac current is a result of a high output voltage ripple present at V_{O2} which is the output that the error current is derived from.

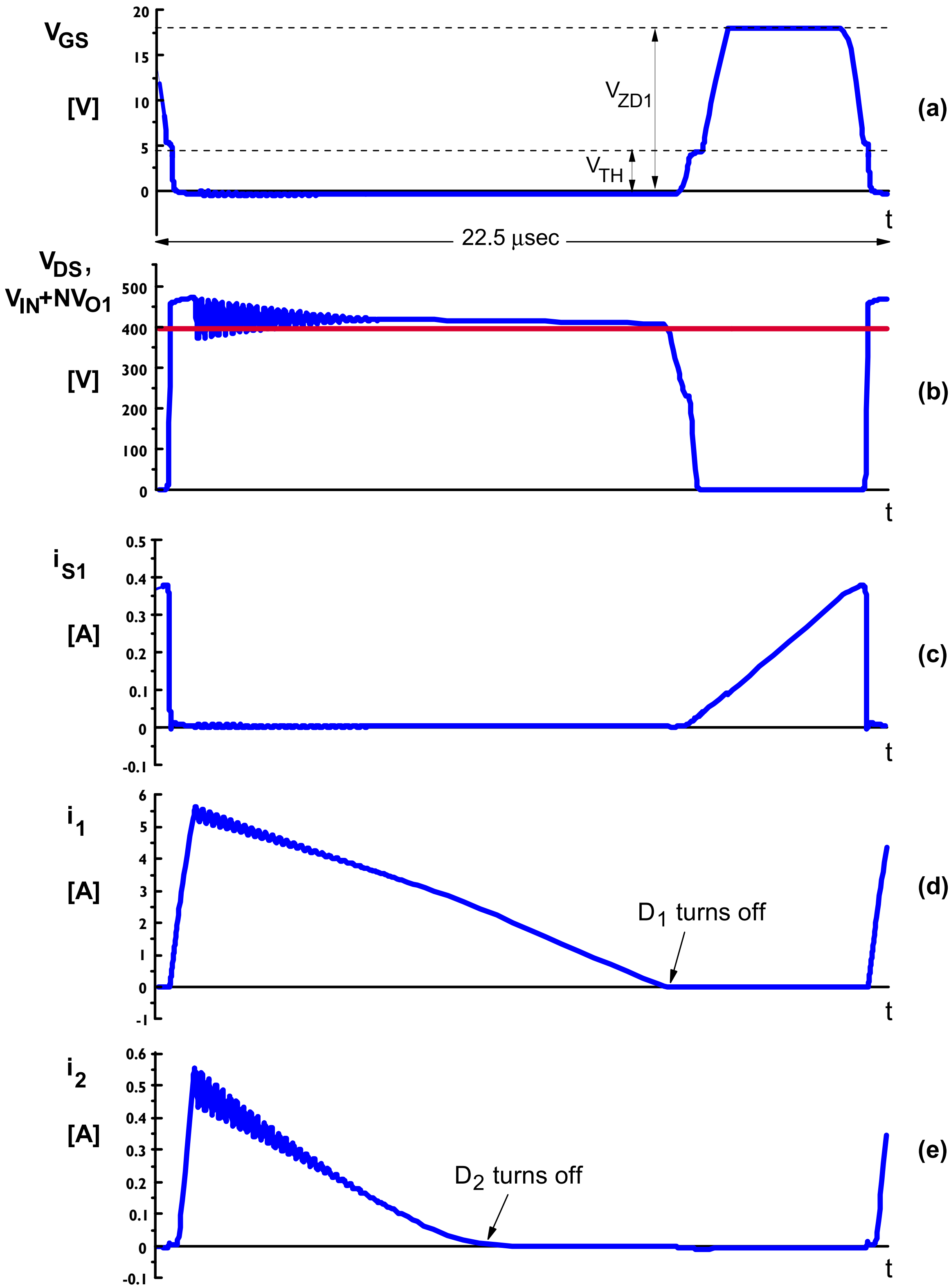


Fig. 10 Simulation waveforms of the auxiliary circuit used in Delta power supply DPS 250AB A operating at full load.

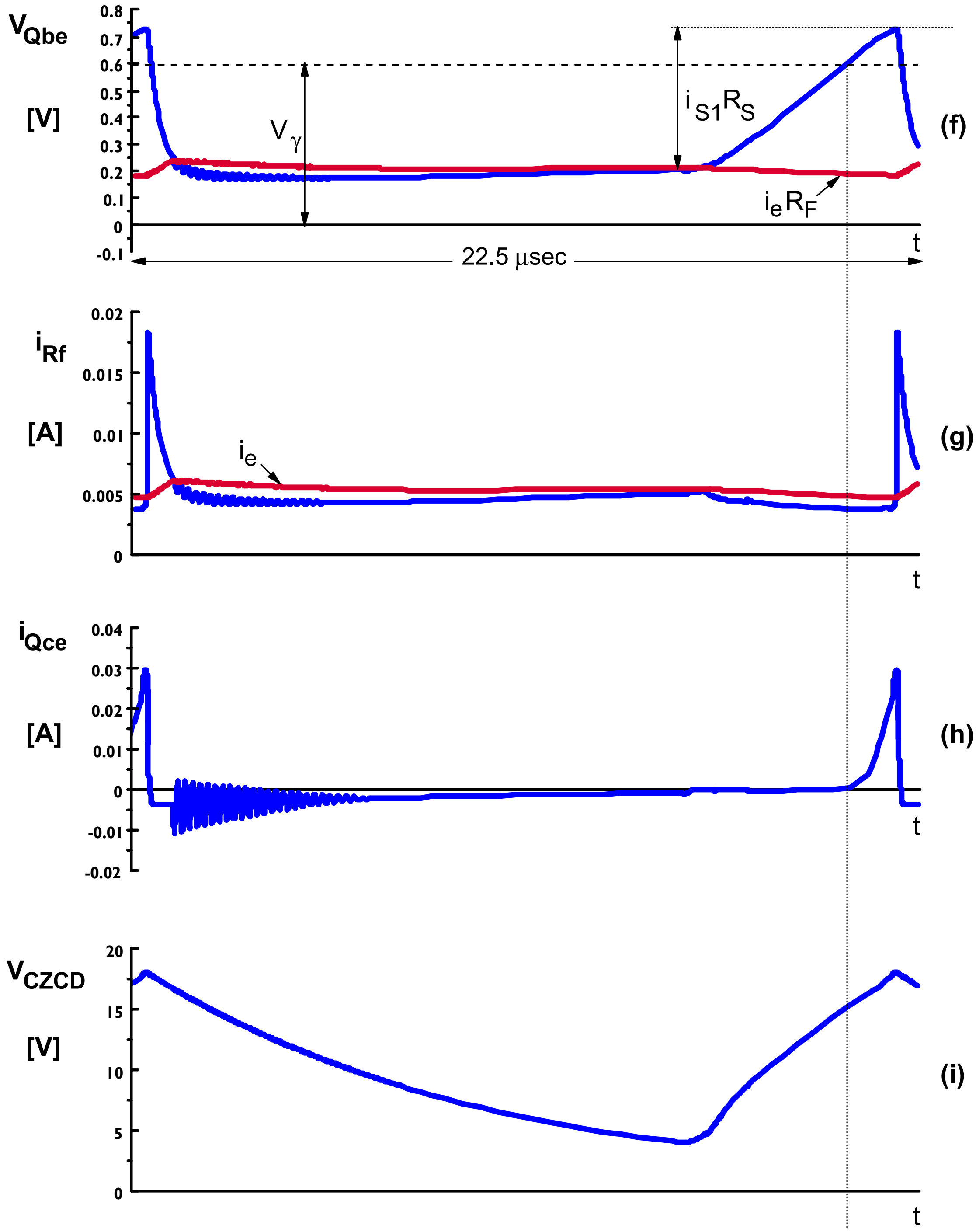


Fig. 10 Simulation waveforms of the auxiliary circuit within Delta power supply DPS 250AB A operating at full load (cont'd).

3.3. Experimental Verification

Oscillograms of key power stage and control stage waveforms were obtained from Delta power supply DPS-250 AB A and compared with Saber simulation waveforms generated with the complete simulation model at full load and light load condition, as shown in Figs. 11 and 12, respectively. At both the full load and light load (i.e., 25% full load) condition, the shape and level of the simulation waveforms is very similar to the measured waveforms. At the full load condition, the switching frequency is nearly matched with a percent deviation of 9 %, whereas at the light load condition, the measured switching frequency is significantly lower than the simulation waveforms, with a percent deviation of 34 %. Generally, this deviation in switching frequency is due to additional losses within the transformer which are not modeled in the simulation, especially the losses associated with the leakage inductance of the transformer. The difference between the modeled leakage inductance and the actual leakage inductance can be seen from the slope of current i_1 in Figs. 11 and 12 as the current commutates from main switch S_1 to rectifier D_1, where a larger current slope implies a smaller leakage inductance. This deviation between simulated and measured frequency can be decreased with a more precise transformer model. However, the behavior of the circuit at light load is generally of little interest to the designer since the transformer is designed based on the full load condition and, therefore, a more advanced model is generally not needed.

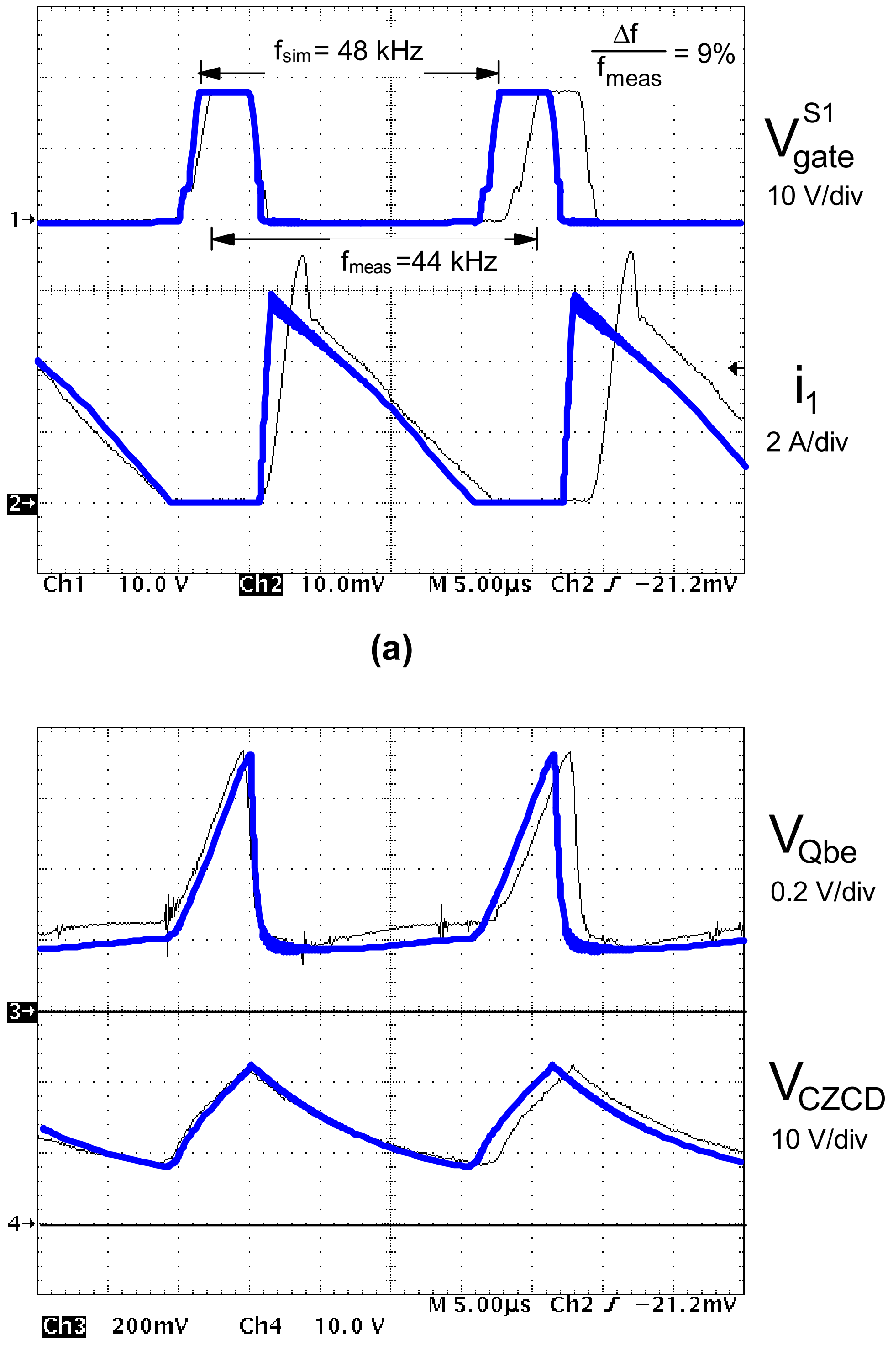
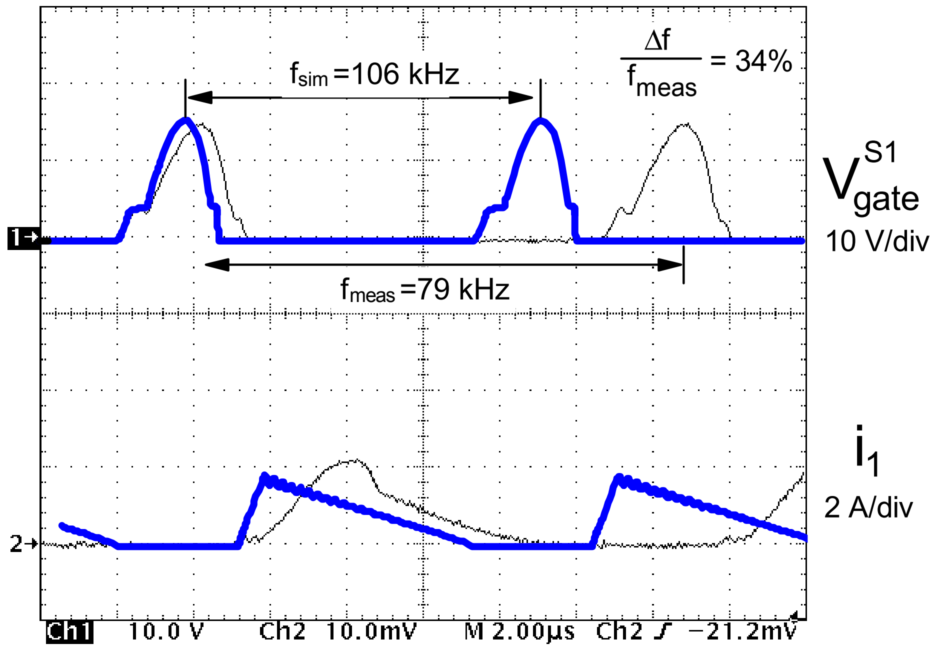
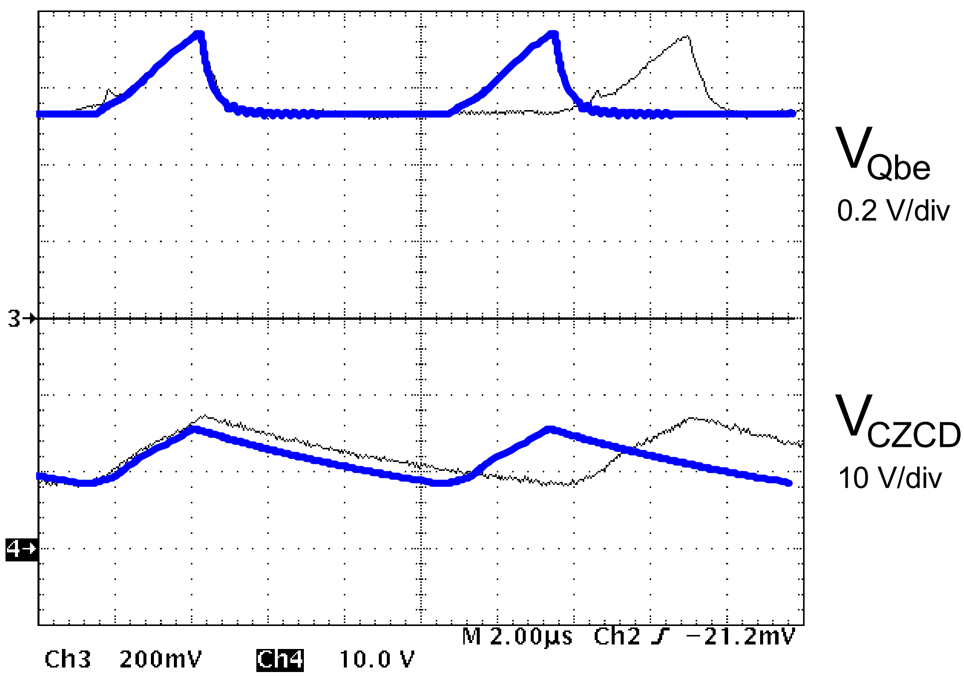


Fig. 11 Measurements of key waveforms vs. Saber simulation waveforms for DPS-250 AB A operating at full load: (a) power stage waveforms; (b) control stage waveforms.



(a)



(b)

Fig. 12 Measurements of key waveforms vs. Saber simulation waveforms for DPS-250 AB A operating at 25% load: (a) power stage waveforms; (b) control stage waveforms.

4. SMALL-SIGNAL MODEL

To achieve tight output voltage regulation and good dynamic performance in response to a system disturbance while ensuring system stability, compensation components C_{EA1}, C_{EA2} , and R_{EA1} of error amplifier TL431 shown in Fig. 1, needs to be determined. Generally, the compensation of the error amplifier is determined so that the closed-loop gain of the system has a high dc gain and an acceptable bandwidth and phase margin. However, the design optimization of the error amplifier compensation requires the knowledge of the small-signal transfer functions in the control loop.

To facilitate the design optimization of control loop, the self-oscillating flyback circuit in Fig. 1 has been simplified, as shown in Fig. 13. Based on this equivalent circuit, a small signal block diagram of the self-oscillating flyback converter shown in Fig. 14 is derived.

The block diagram shown in Fig. 14 consists of:

- Control-to-output voltage transfer function $G_{VeVo}(s) = \hat{V}_O / \hat{V}_e$
- Output voltage sensing gain $K_d = \hat{V}_1 / \hat{V}_O$
- Error amplifier transfer function $G_{EA}(s) = \hat{V}_{EA} / \hat{V}_1$
- Transconductance gain $G_1 = \hat{i}_{EA} / \hat{V}_B$
- Opto-coupler gain $G_2 = \hat{i}_e / \hat{i}_{EA}$
- Transresistance gain $G_3 = \hat{V}_e / \hat{i}_e$

The block diagram consists of inner loop $T_{INNER} = G_{VeVo}(s)G_1G_2G_3$ and outer voltage loop $T_V = G_{VeVo}(s)K_dG_{EA}(s)G_1G_2G_3$. Inner loop T_{INNER} is formed as a result of connecting one terminal of resistor R_B to output voltage $\hat{V}_O$ and the other terminal of resistor R_B to error amplifier voltage $\hat{V}_{EA}$.

The expression for power stage gain $G_{VeVo}(s)$, which is derived in Appendix C, is

$$G_{VeVo}(s) = M_{dc} \cdot \frac{(s/s_{z1}+1)(s/s_{z2}+1)}{(s/s_{p1}+1)(s^2/\omega_o^2 + s/(Q\omega_o)+1)} \tag{4.1}$$

where:

$$M_{dc} = -\frac{V_{IN}}{2R_S I_O}, \tag{4.2}$$

$$s_{z1} = \frac{1}{C_{O1}R_{CO1}}, \tag{4.3}$$

$$s_{z1} = \frac{1}{C_F R_{CF}}, \tag{4.4}$$

$$s_{p1} = -\frac{K_r}{C_{O1}+C_F}, \tag{4.5}$$

$$\omega_O = \frac{1}{\sqrt{\dfrac{L_F}{\dfrac{1}{C_{O1}}+\dfrac{1}{C_F}}}}, \tag{4.6}$$

$$Q = \sqrt{L_F \frac{C_F + C_{O1}}{C_F C_{O1}}} \cdot \left(\frac{1}{R_{CO1} + R_{CF} + R_{lf} + K_r \left(R_{CO1}R_{CF} - \dfrac{L_F}{C_{O1}+C_F} \right)} \right), \tag{4.7}$$

$$K_r = -\frac{I_O N}{V_{IN}\left(1 + N\dfrac{V_O}{V_{IN}}\right)}. \tag{4.8}$$

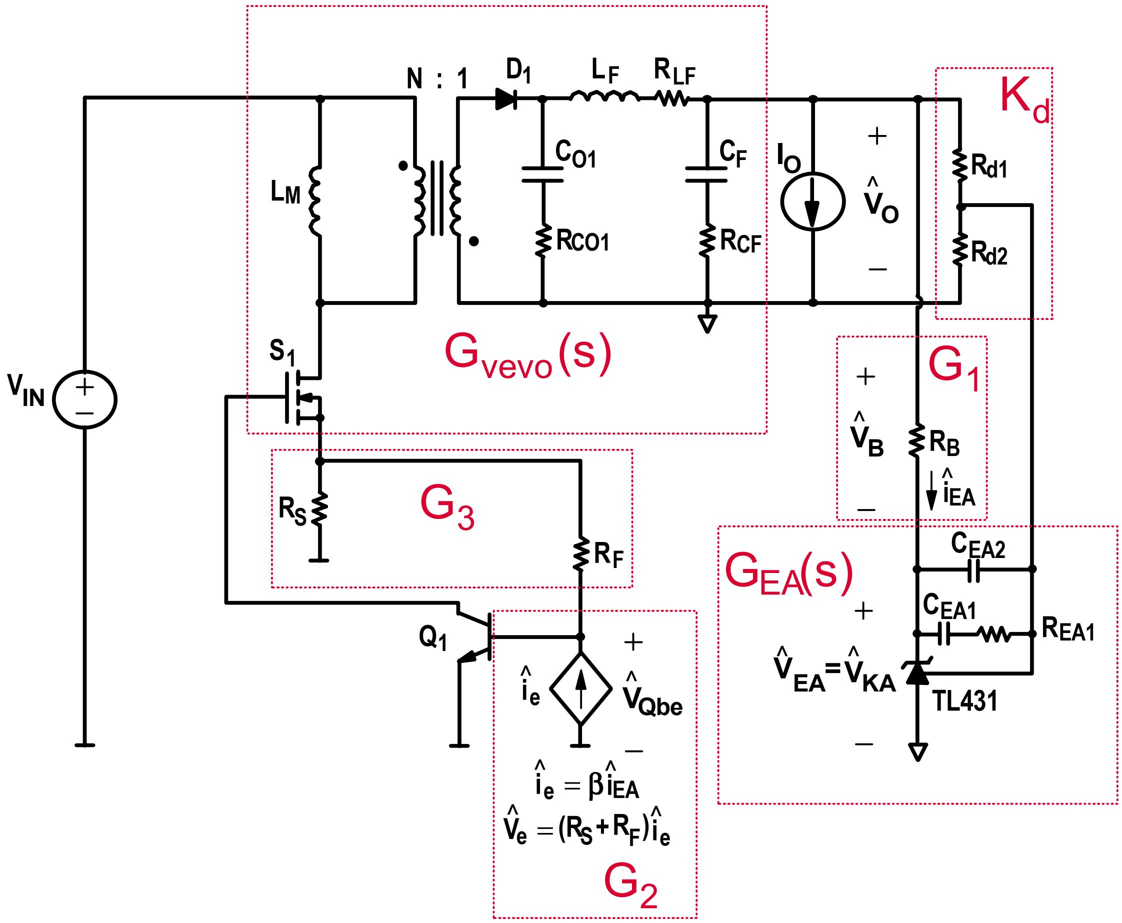


Fig. 13 Simplified self-oscillating flyback circuit for small-signal modeling and analysis.

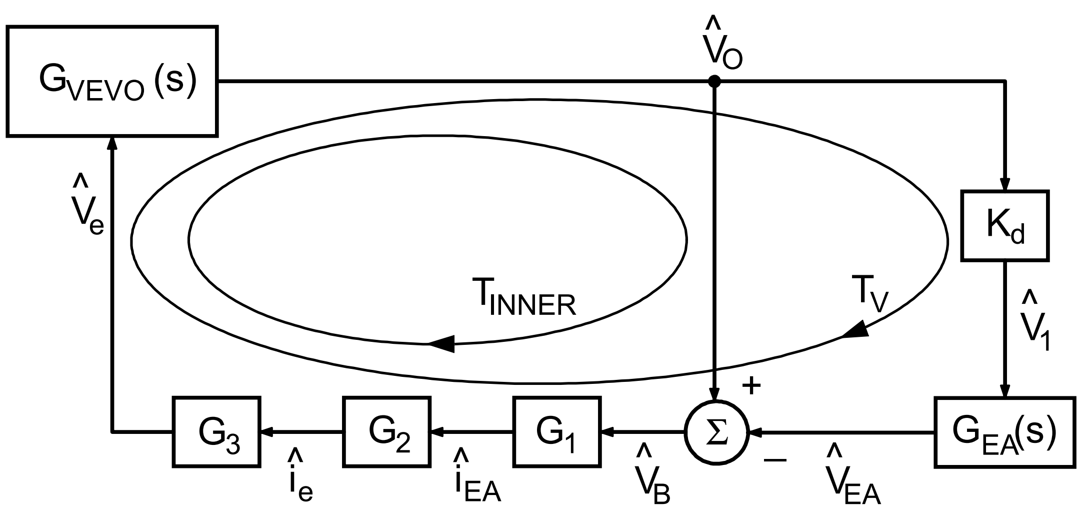


Fig. 14 Small-signal block diagram of self-oscillating flyback converter.

Sensing gain K_d is

$$K_d = \frac{\hat{V}_1}{\hat{V}_O} = \frac{R_{d2}}{R_{d1} + R_{d2}}. \tag{4.9}$$

As can be seen from Fig.13, transfer function G_1, which is defined as

$$G_1 = \frac{\hat{i}_{EA}}{\hat{V}_B} = \frac{\hat{i}_{EA}}{\hat{V}_O - \hat{V}_{EA}} \tag{4.10}$$

can be calculated as

$$G_1 = \frac{\hat{i}_{EA}}{\hat{V}_B} = \frac{\hat{i}_{EA}}{\hat{V}_O - \hat{V}_{EA}} = \frac{1}{R_B}. \tag{4.11}$$

Error current $\hat{i}_e$ is related to current $\hat{i}_{EA}$ through transfer function G_2, which is the dc current transfer ratio of the optocoupler,

$$G_2 = \frac{\hat{i}_e}{\hat{i}_{EA}} = \beta. \tag{4.12}$$

Finally, from Fig. 13, transfer function G_3, which relates error voltage $\hat{V}_e$ and error current $\hat{i}_e$ is

$$G_3 = \frac{\hat{V}_e}{\hat{i}_{EA}} = R_F + R_S. \tag{4.13}$$

The two loop system shown in Fig. 14 can be reduced to a single loop system, as shown in Fig. 15, by combining transfer functions $G_{VeVo}(s)$, G_1, G_2, and G_3 into a single transfer function $G_{V_{EA}Vo}(s)$,

$$G_{V_{EA}Vo}(s) = \frac{\hat{V}_O}{\hat{V}_{EA}} = \frac{KG_{VeVo}(s)}{1 + KG_{VeVo}(s)} = \frac{KG_{VeVo}(s)}{1 + T_{INNER}}, \tag{4.14}$$

$$K = G_1 G_2 G_3, \tag{4.15}$$

$$T_{INNER} = KG_{VeVo}(s). \tag{4.16}$$

As can be seen from Eq. (4.14), transfer function $G_{V_{EA}Vo}(s)$ has a low frequency gain which is less than 1. Also, because of inner loop T_{INNER}, poles of $G_{V_{EA}Vo}(s)$ are shifted to higher frequencies, as illustrated in Fig. 16. Figure 16 shows gain plots of transfer function $KG_{VeVo}(s)$, $1 + T_{INNER}$, and transfer function $G_{V_{EA}Vo}(s)$. As can be seen from Fig. 16, transfer function $G_{V_{EA}Vo}(s)$ has pole f_{p1}^{*} which is located at the cross-over frequency f_{INNER} of loop T_{INNER}. It can be shown that the frequency of this pole is related to the frequency of pole f_{p1} of power stage transfer function $G_{VeVo}(s)$ as

$$s_{p1}^{*} = (1 + KM_{dc})s_{p1} \approx KM_{dc}s_{p1}. \tag{4.17}$$

It should also be noted that **inner loop T_{INNER} shifts only poles of power stage transfer function $G_{VeVo}(s)$ which are within the bandwidth f_{INNER} of loop T_{INNER}**. In addition, it can be shown in Appendix C that **locations of zeroes of power stage transfer function $G_{VeVo}(s)$ are not affected by the existence of the inner loop.**

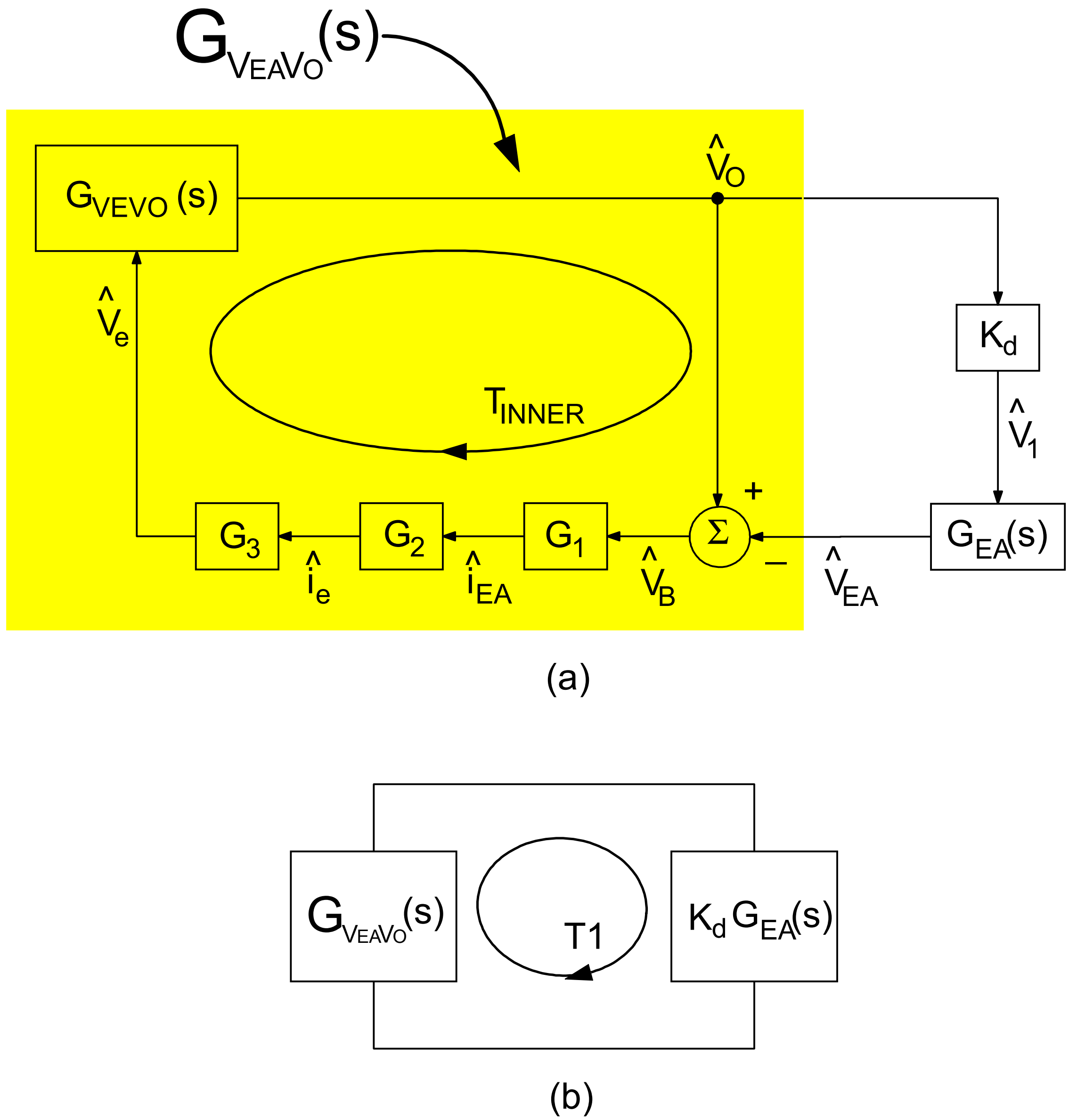


Fig. 15 Small-signal block diagram of self-oscillating flyback converter: (a) complete block diagram; (b) simplified block diagram.

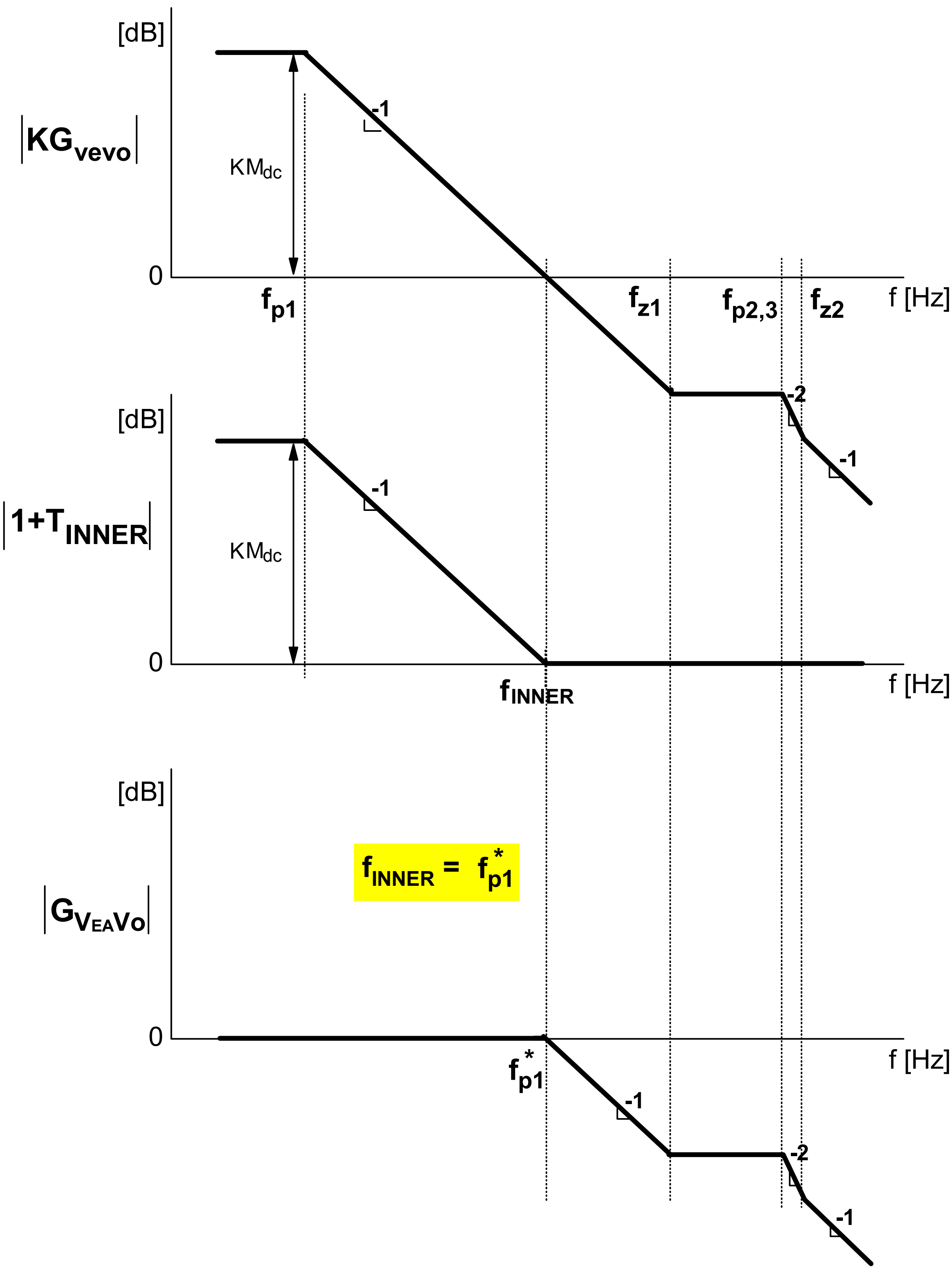


Fig. 16 Gain plots of power stage transfer function $G_{VeVo}(s)$, $1 + T_{INNER}$, and transfer function $G_{V_{EA}V_O}(s)$.

As a result, the zeroes of transfer function $G_{V_{EA}Vo}(s)$ coincide with the zeroes of power stage transfer function $G_{VeVo}(s)$.

Assuming that only pole f_{p1} of power stage transfer function $G_{VeVo}(s)$ is within the bandwidth f_{INNER} of loop gain T_{INNER}, as shown in Fig. 16, transfer function $G_{V_{EA}Vo}(s)$ can be expressed as

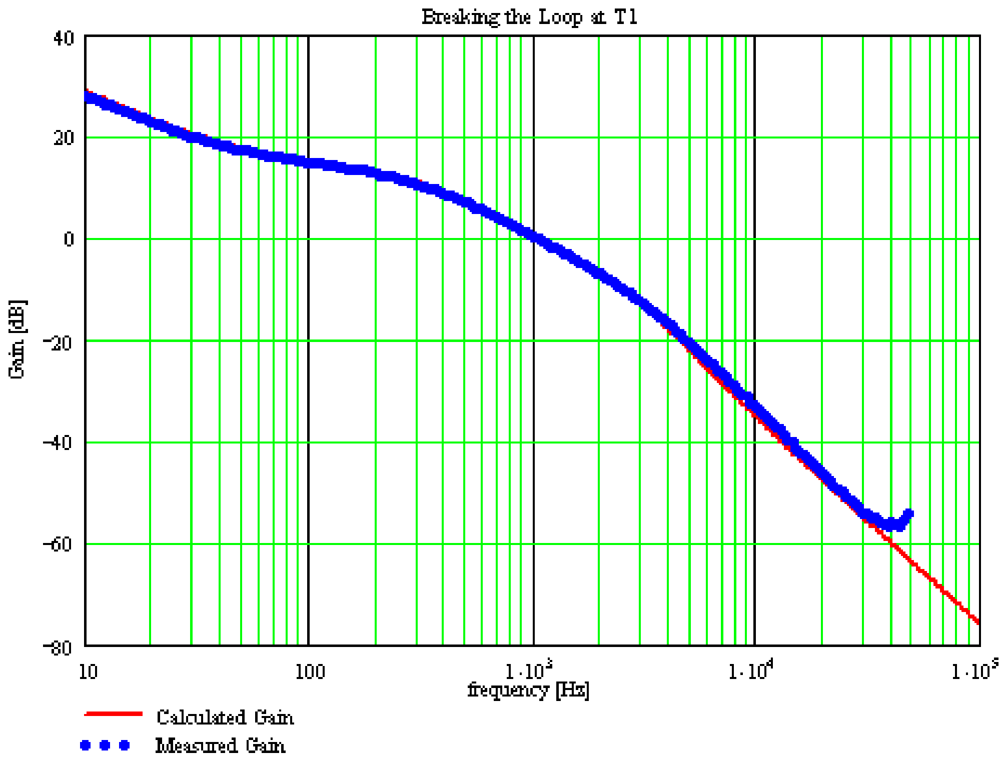
$$G_{V_{EA}Vo}(s) = \frac{KM_{dc}}{1 + KM_{dc}} \cdot \frac{(s / s_{z1} + 1)(s / s_{z2} + 1)}{\left(s/s^{*}_{p1} + 1\right)\left(s^2/\omega_o^2 + s/(Q\omega_o) + 1\right)}, \tag{4.18}$$

By defining transfer function $G_{V_{EA}Vo}(s)$, the system is reduced to a single loop system with loop gain

$$T_1 = K_d G_{EA}(s) G_{V_{EA}Vo}(s) . \tag{4.19}$$

The selection of compensation components of error amplifier transfer function $G_{EA}(s)$ to achieve the desired regulation accuracy, dynamic response and stability margin is explained in detail in Chapter 5.

The small-signal model was verified on Delta power supply DPS-250 AB A using original compensation component values. The calculated Bode plots of control loop T_1 are obtained using a MathCad™ worksheet presented in Appendix B, and measured control loop T_1 are shown in Fig. 17. As can be seen, both the measured and calculated gain and phase show an excellent agreement across the frequency range of interest.



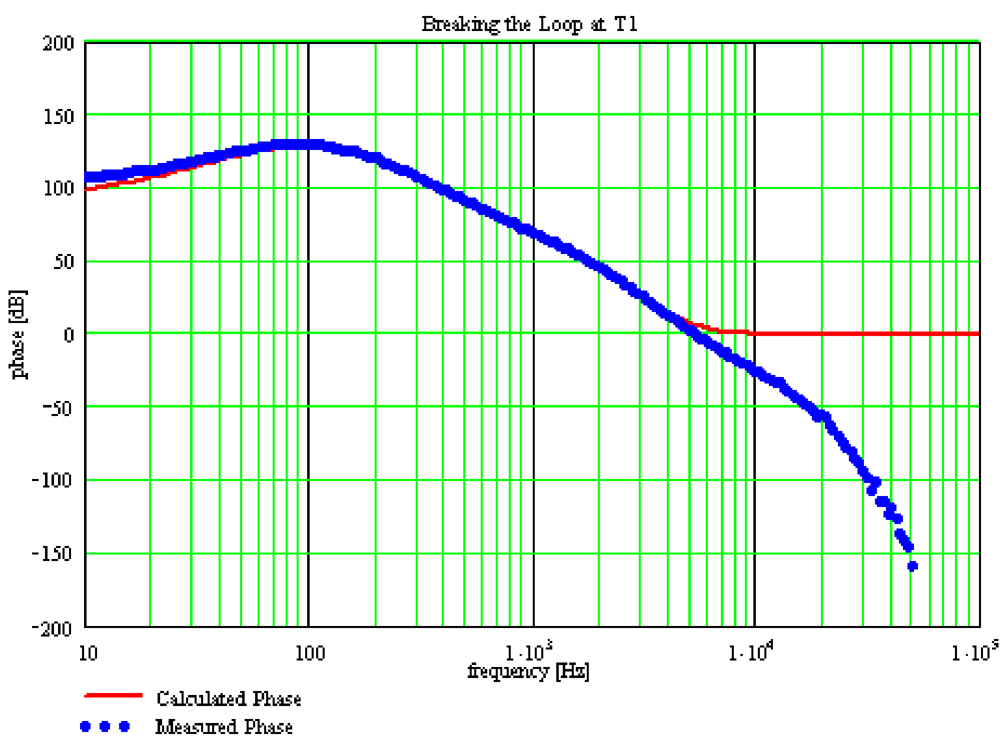


Fig. 17 Calculated and measured Bode plots of loop gain T_1 of Delta power supply DPS-250 AB A with original component values.

5. DESIGN GUIDELINES

Generally, the self oscillating flyback converter operates in the discontinuous-conduction mode (DCM) but close to the continuous/discontinuous conduction mode (CCM/DCM) boundary, as can be seen from its typical waveforms shown in Fig. 18. The power stage does not operate exactly at the boundary due to a resonance between the output capacitance C_{OSS} of main switch S_1 with magnetizing inductance L_M and a delay time introduced by control circuit components (e.g., C_{ZCD}, R_{ZCD}, and C_{ISS}). Time t_D between the CCM/DCM boundary and the start of the next switching period T_S , i.e., the DCM time, is nearly constant for a properly designed control

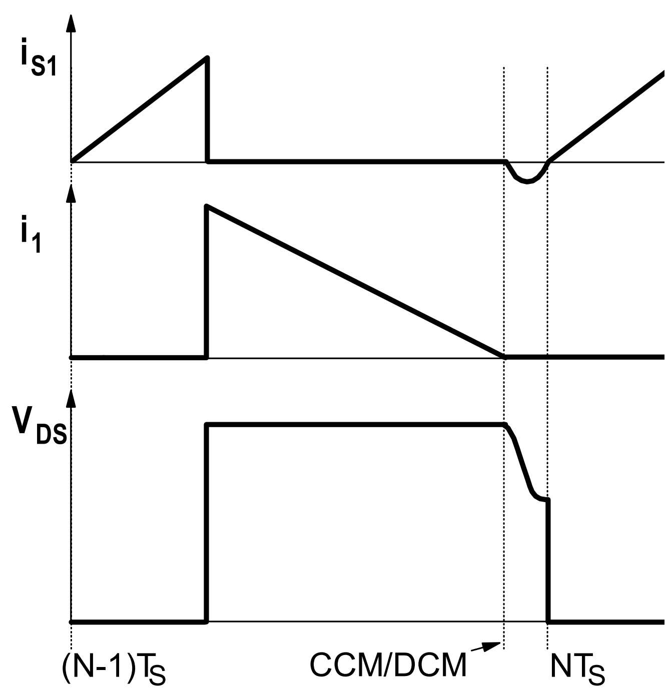


Fig. 18 General power stage waveforms of flyback converter operating at CCM/DCM boundary.

circuit and, can be neglected completely since usually $t_D<<T_S$. As a result, the design of the self-oscillating flyback power stage is the same as the design of the flyback converter operating at the CCM/DCM boundary.

5.1. Power Stage Design

To facilitate the design of the power stage, Fig. 19 shows a simplified circuit diagram of the self-oscillating flyback power stage and idealized key waveforms. In addition, the design procedure assumes that the power stage devices are nearly ideal, with the exception of a non-zero forward voltage drop V_F across output rectifiers D_1 and D_2.

Since while switch S_1 is on voltage V_{IN} is applied across magnetizing inductance L_M and

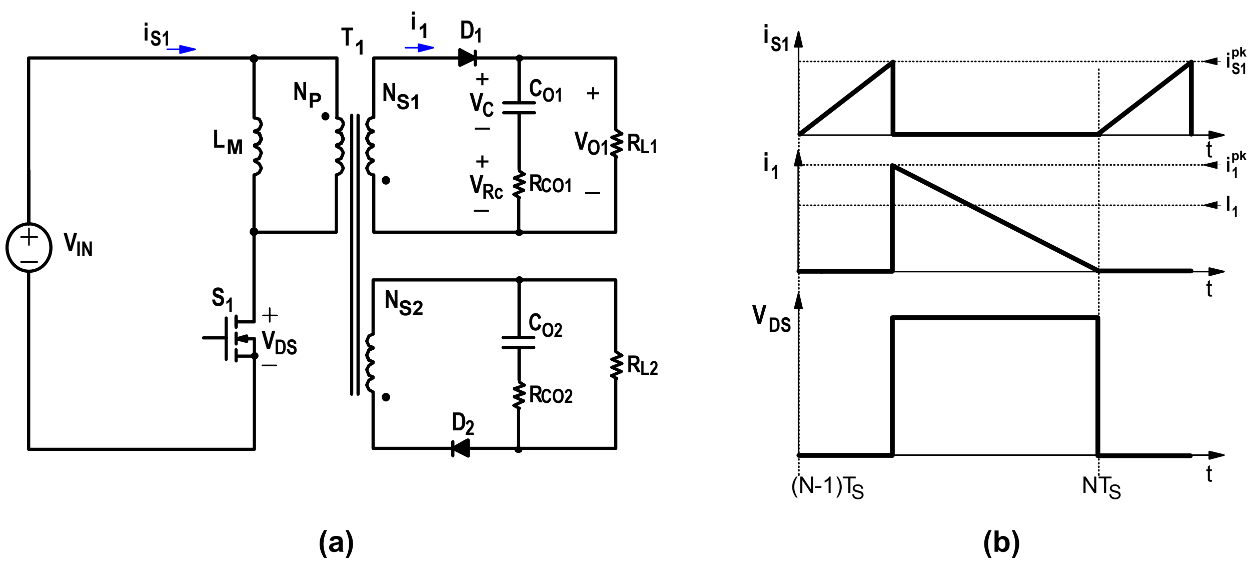


Fig. 19 Self-oscillating flyback converter: (a) simplified circuit diagram; (b) key waveforms.

switch current increases linearly, i.e., $i_{S1} = i_M = \frac{V_{IN}}{L_M} t$, peak switch current i_{S1}^{pk} is equal to

$$i_{S1}^{pk} = \frac{V_{IN}}{L_M} DT_S, \tag{5.1}$$

where D is the duty cycle. When switch S_1 is off, switch current $i_{S1} = 0$ and magnetizing energy discharges through the outputs. From Fig. 19 (b), the peak rectifier currents i_1^{pk} and i_2^{pk} can be determined as a function of the specified average output currents I_1 and I_2, as

$$I_1 = \frac{1}{2} i_1^{pk}(1-D) \Rightarrow i_1^{pk} = \frac{2I_1}{1-D}, \tag{5.2}$$

$$I_2 = \frac{1}{2} i_2^{pk}(1-D) \Rightarrow i_2^{pk} = \frac{2I_2}{1-D}. \tag{5.3}$$

From the volt-second balance of magnetizing inductance L_M, the voltage conversion ratio is

$$\frac{V_O}{V_{IN}} = \frac{D}{N(1-D)}, \tag{5.4}$$

where $N = N_P / N_{S1}$. Solving Eq. (5.4) for duty cycle D,

$$D = \frac{1}{\frac{V_{IN}}{V_{O1} + V_F} \frac{N_{S1}}{N_P} + 1}. \tag{5.5}$$

Therefore, D is a function of the input voltage V_{IN}, output voltage V_{O1}, turns ratio N_{S1}/N_P and forward voltage drop V_F. The maximum duty cycle D^{max}, which occurs at low-line V_{IN}^{min} and full load P_O^{max}, is then given by

$$D^{max} = \frac{1}{\frac{V_{IN}^{min}}{V_{O1}+V_F}\frac{N_{S1}}{N_P}+1}. \tag{5.6}$$

When output voltage V_{O1} is tightly regulated, output voltage V_{O2} is

$$V_{O2} = (V_{O1}+V_F)\frac{N_{S2}}{N_{S1}} - V_F, \tag{5.7}$$

which is considered loosely regulated since forward voltage V_F changes as a function of output current i_1 and temperature.

The maximum voltage across main switch S_1 during the off time is

$$V_{S1}^{OFF} = V_{IN}^{max} + (V_{O1}+V_F)\frac{N_P}{N_{S1}}, \tag{5.8}$$

while the maximum voltage across the output rectifiers D_1 and D_2 during the on time is

$$V_{D1}^{ON} = V_{IN}^{max}\frac{N_{S1}}{N_P} + V_{O1} \text{ and} \tag{5.9}$$

$$V_{D2}^{ON} = V_{IN}^{max}\frac{N_{S2}}{N_P} + V_{O2}, \tag{5.10}$$

respectively.

The selection of turns ratio N_{S1}/N_P is based on a design trade-off between the maximum voltage stress across main switch S_1, which decreases as turns ratio N_{S1}/N_P increases, and the maximum voltage stress across output rectifiers D_1 and D_2, which decreases as N_{S1}/N_P decreases, as shown in Eqs. (5.8) and (5.9). The selection of turns ratio N_{S2}/N_P is made once N is selected using Eq. (5.4). Device performance also plays a role in the selection of the transformer turns ratio. For example, it is generally desirable to use a Schottky device as the output rectifier since it generally has a lower forward voltage drop than a fast-recovery type rectifier, which results in a lower conduction loss of the rectifier. However, the highest available breakdown voltage for a Schottky device is 200 V, which, based on converter specifications, often requires turns ratio N_{S1}/N_P to be generally low, which increases the voltage stress across main switch S_1. Generally, the on resistance of a MOSFET device increases as the rated voltage increases, which generally increases the conduction loss of S_1.

It should also be noted that the presence of transformer leakage inductance results in an increased voltage stress on all devices as it resonates with circuit parasitic capacitances during the turn-off of switch S_1. Often a voltage clamp is needed to limit the amplitude of the voltage ringings which results in higher losses as the clamp voltage decreases. This adds another design trade-off on the rated voltage of the device. Finally, a derating factor of 80% is usually used in the design process, which also affects the selection of the device, the clamp voltage level, and the transformer turns ratio. Therefore, the selection of transformer turns ratio's is often an iterative process, and should be carefully considered by the designer.

The selection of magnetizing inductance L_M is based on the selection of the minimum switching frequency f_S^{min}. Namely, from the power balance

$$P_{IN} = \langle i_{IN} \rangle V_{IN} = \frac{1}{2} i_{S1}^{pk} D V_{IN} = \frac{P_O}{\eta} \tag{5.11}$$

where P_{IN} is the input power, P_O is the output power, $\langle i_{IN} \rangle$ is the average input current, and η is the converter efficiency, it follows that L_M and f_S are related as

$$P_O = \frac{1}{2} \frac{V_{IN}^2}{L_M} \frac{D^2 \eta}{f_S}. \tag{5.12}$$

Since minimum switching frequency f_S^{min} occurs at full power P_O^{max} and low line V_{IN}^{min}, from Eq. (5.12) the relationship between P_O^{max} and f_S^{min} is

$$P_O^{max} = \frac{1}{2}\frac{V_{IN}^{min\,2}}{L_M}\frac{D^{max\,2}\eta}{f_S^{min}}. \tag{5.13}$$

Solving Eq. (5.13), it follows that

$$L_M = \frac{1}{2}\frac{\eta V_{IN}^{min\,2} D^{max\,2}}{P_O^{max} f_S^{min}}. \tag{5.14}$$

Generally, the minimum switching frequency f_S^{min} is chosen to reduce the maximum switching frequency that occurs at the minimum load and high line. Generally, 20 kHz is the lowest permitted switching frequency since it is the upper threshold of the audible range. However, such a low switching frequency often results in a larger size transformer core. Therefore, the selection of the minimum switching frequency requires a careful consideration of trade-offs between the size and performance of transformer T_1.

The selection of output capacitor C_{O1} is generally made based on the output-voltage ripple ΔV_O requirements. The output voltage ripple is the sum of voltage V_{Rc} and voltage V_C in quadrature,

$$\Delta V_O = \sqrt{(V_{Rc})^2 + (V_C)^2}, \tag{5.15}$$

where:

$$V_{Rc} = i_1^{pk} R_{CO1}, \tag{5.16}$$

$$V_C = \frac{1}{C_{O1}} \int_0^{t_P} i_C dt = \frac{1}{2C_{O1}} \frac{V_{O1} N^2}{L_M} t_P{}^2 , \tag{5.17}$$

and

$$t_P = \frac{\left(i_1^{pk} - I_O\right)}{V_{O1}} \frac{L_M}{N^2} . \tag{5.18}$$

Substituting Eq. (4.16) into Eq. (4.15),

$$V_C = \frac{\left(i_1^{pk} - I_O\right)^2}{2C_{O1}} \frac{L_M}{V_{O1} N^2} . \tag{5.19}$$

Generally, $V_{Rc} >> V_C$ for the boundary operating converter and Eq. (5.15) reduces to $\Delta V_O = V_{Rc}$ due to it's high peak winding current i_1^{pk}. **For this case, the selection of output capacitor C_{O1} is often made based on resistance R_{CO1}**, as well as capacitor volume and voltage rating. If the allowed board space is too small for the required output capacitors, a second stage LC filter can be added to further attenuate the output voltage ripple. In addition, it should be noted that R_C changes as a function of temperature. Therefore, careful consideration of expected component temperature should be included when the output capacitor is selected.

5.2. Control Stage Design

The design of the control stage, shown in Fig. 20(a), is also an iterative process consisting of a series of design steps which were developed based on several design constraints. The goal of this design procedure is to ensure stable voltage regulation over the entire line and load range.

5.2.1. *Steady State Considerations*

To achieve good output voltage regulation during steady state operation, the ramp voltage $i_{S1}R_S$ summed with the DC voltage $i_e(R_F + R_S)$ must fit within the "regulation window" throughout the line and load range, as illustrated in Fig. 20(b). The upper limit of the regulation window is the threshold voltage V_γ of transistor Q_1, which is inherent to the transistor selected, whereas the lower limit of the regulation window is defined by the full load current. To achieve output voltage regulation, resistors R_B, R_S, and R_F must be carefully selected to limit the error current within the regulation window.

The maximum error current occurs at minimum load, as shown in Fig. 20(b). At minimum load, less energy is needed to maintain the output voltage which is why the on time of switch S_1 is very short. Conversely, the minimum error current occurs at full load, as shown in Fig. 20(b), because a longer on time is needed to store the required energy. It should be noted that the duty cycle is still independent from the load since a proportional change in the on time t_{ON} results in a proportional change in the switching period T_S, and an inverse proportional change in the switching frequency f_S. It should also be noted that unlike the standard PWM, whose on time is determined at the moment the ramp voltage reaches the control voltage, the on time of this control circuit is determined once sufficient charge is removed from input capacitance C_{ISS} by transistor Q_1. Transistor Q_1 is turned on at the moment that base voltage V_{Qbe} reaches its threshold voltage V_γ.

The **design constraints** for the selection of the control circuit components for steady state operation are based on the operating range of the circuit as well as on component ratings. Specifically, the cathode-anode voltage V_{KA} and cathode current I_K of error amplifier TL431 are limited to

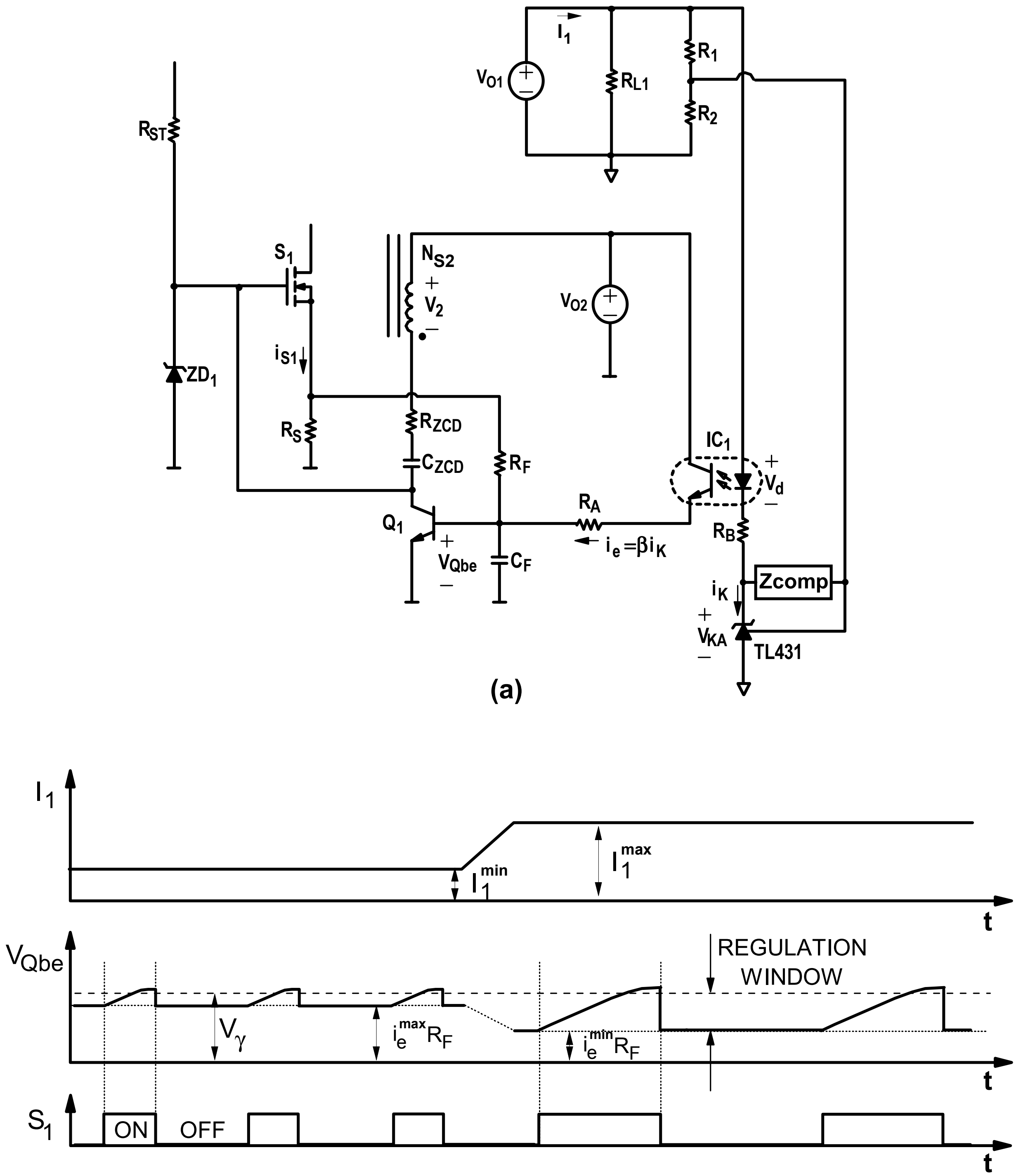


Fig. 20 Self-oscillating flyback converter: (a) Equivalent control stage schematic of circuit operating at steady state, (b) key control circuit waveforms at minimum and maximum load current.

$$
\begin{aligned}
&V_{REF} < V_{KA} < 36\,\mathrm{V} \\
&1\,\mathrm{mA} < I_K < 100\,\mathrm{mA}
\end{aligned}. \tag{5.20}
$$

From Fig. 20, V_{KA} can be expressed as,

$$
V_{KA} = V_O - V_d - I_K R_B. \tag{5.21}
$$

Since at minimum load, current I_K is maximum, as seen from Fig. 20, and voltage V_{KA} is minimum, resistor R_B is determined from

$$
R_B < \frac{V_O - V_d - V_{KA}^{min}}{I_K^{max}}. \tag{5.22}
$$

The selection of sense resistor R_S is limited by its maximum power dissipation. If maximum power dissipation P_{RS} of resistor R_S is limited to below 0.1% of maximum input power, than resistor R_S is given by

$$
P_{RS} \approx (0.1\%)P_{IN}^{max} \Rightarrow R_S = \frac{(0.1\%)P_{IN}^{max}}{\left(i_{S1}^{pk}\sqrt{D^{max}/3}\right)^2}. \tag{5.23}
$$

The selection of resistor R_F is limited at minimum load by maximum error current i_e^{max}, sense resistor R_S, and cut-off voltage V_γ,

$$
i_e^{max}(R_F + R_S) \le V_\gamma, \tag{5.24}
$$

where R_F must be much greater than R_S. At full load, the selection of resistors R_F and R_S are further limited by the minimum error current i_e^{min} and the maximum switch current i_{S1}^{pk},

$$i_e^{min}(R_F + R_S) + i_{S1}^{pk(max)} R_S > V_\gamma, \qquad (5.25)$$

where: $i_{S1}^{pk(max)} = V_{IN}^{max} D^{max} \Big/ (L_M f_S^{min})$.

Finally, error current i_e is related to cathode current I_K through dc current transfer ratio β of optocoupler IC_1,

$$i_e = \beta I_K . \qquad (5.26)$$

The **design procedure** for the selection of the control circuit components R_F, R_S, and R_B for steady state operation begins with the selection of the maximum cathode current I_K^{max} using the device ratings for error amplifier TL431.

STEP 1 Choose I_K^{max} based on constraint (5.20).

STEP 2 Determine i_e^{max} from constraint (5.26).

STEP 3 Determine resistor R_S from constraint (5.23).

STEP 4 Determine resistor R_F from constraint (5.24).

STEP 5 Determine resistor R_B from constraint (5.22).

It should be noted that resistor R_B , whose value also affects the voltage loop dc gain, should be chosen as low as possible while still adhering to STEP 5 in order to maximize the loop gain. Generally, a 20 Ω resistor serves as a good first iteration for output voltage V_{O1} less than 35 V. Later, when system stability is considered, the value of resistor R_B will be re-evaluated.

STEP 6 Determine I_K^{min} from constraint (5.25). Check result against constraint (5.22).

STEP 7 Check V_{KA}^{max} using Eq. (5.21) at the maximum load condition (i.e., minimum cathode current i_K^{min}).

Following STEPS 1-7 will ensure that the control circuit operates within the regulation window. However, the calculated values are only a starting point and are still subject to further optimization at the hardware level.

The design of components R_A, C_{ZCD}, R_{ZCD}, ZD_1, and R_{ST} can be determined independently from STEPS 1-7 once all the constraints are satisfied. For example, the role of resistor R_A is to reduce the power loss of the phototransistor within optocoupler IC_1 by developing a maximum voltage across it equal to $i_e^{max} R_A$. The power dissipated by the phototransistor, which is limited by the device manufacturer, is then

STEP 8 $$P_{IC1} = V_{CE} i_e^{max} = (V_{O2} - i_e^{max} R_A - V_{Qbe}) i_e^{max} < \text{device power rating}.$$

The role of capacitor C_{ZCD} is to block DC current during start-up, allowing charge to be delivered from the input voltage through resistor R_{ST} until switch S_1 turns on for the first time. Otherwise, capacitor C_{ZCD} merely delays the full turn on of switch S_1 by increasing the length of time spent in the constant-current region, which is undesirable from a power conversion efficiency point of view. Therefore, it is recommended that C_{ZCD} be set ten times greater than input capacitance C_{ISS}. Since C_{ZCD} and C_{ISS} form a voltage divider at the gate of S_1, steps should be taken to clamp the gate voltage V_G with a zener clamp ZD_1, to avoid exceeding the terminal voltage rating. This zener breakdown voltage should be set as per the device rating.

STEP 9 Select $C_{ZCD} = 10x\ C_{ISS}$.

The role of resistor R_{ZCD} is to limit the power dissipated by zener clamp ZD_1. Therefore,

STEP 10
$$\text{Select } R_{ZCD} = \frac{V_{IN}^{max}\frac{N_{S2}}{N_P} - V_{ZD1}}{P_{ZD1}} V_{ZD1},$$

where $P_{ZD1} < 80\%$ of maximum specified power rating of ZD_1.

Start-up resistor R_{ST} should be chosen based on the maximum start-up time of the converter while limiting its maximum power dissipation. Generally,

STEP 11
$$\text{Select } R_{ST} \approx \frac{{V_{IN}^{max}}^2}{P_{ST}},$$

where $P_{ST} \approx (1\%)P_O$, though its actual value is generally not critical.

Finally, resistors R_1 and R_2 divide down output voltage V_{O1} to be compared to reference voltage V_{REF} which is internal to error amplifier TL431. Therefore,

STEP 12
$$\text{Select } R_1 = \frac{R_2}{\frac{V_{O1}}{V_{REF}} - 1}.$$

5.1.2. Compensation Calculations

The compensation components C_{EA1}, C_{EA2}, and R_{EA1} of the error amplifier are determined so that the control loop achieves the desired regulation accuracy and dynamic response of the output voltage while maintaining an acceptable phase margin (typically > 45^o) in the entire line and load range. Generally, a good regulation accuracy and fast transient response requires that closed loop T_1 has a high dc gain and high bandwidth. Typically, a dc gain of 20 to 60 dB is sufficient for good regulation accuracy, whereas crossover ferquency f_C less than one-fourth of f_S^{min}, i.e., $f_C < f_S^{min}/4$, is usually designed for.

Figure 21 shows the gain Bode plot of transfer function $G_{V_{EA}V_O}(s)$ (shown previously in Fig. 16), the desired closed loop gain T_1, and the gain plot of compensated error amplifier $G_{EA}(s)$ which produces desired closed loop gain T_1. As can be seen from Fig. 21, the optimum compensation of the error amplifier has 2 poles and 1 zero, i.e., the error amplifier transfer function can be expressed as

$$G_{EA}(s) = \frac{A}{s} \cdot \frac{s/s_{zcomp1} + 1}{s/s_{pcomp2} + 1}, \tag{5.27}$$

where A is the gain of the integrator, s_{zcomp1} is the compensation zero, and s_{pcomp2} is the second compensation pole.

The integrator in the error amplifier transfer function is used to increase the low-frequency gain of closed loop gain T_1, whereas high frequency pole s_{pcomp2} is introduced above the cross-over frequency f_C (at least 2 octaves above f_C) of loop T_1 to sufficiently attenuate the gain of T_1 at the switching frequency to achieve noise immunity of the loop. The compensation zero s_{zcomp1} of the error amplifier is placed at pole f_{p1}^* of transfer function $G_{V_{EA}V_O}(s)$.

Error amplifier transfer function $G_{EA}(s)$ can be realized with capacitors C_{EA1}, C_{EA2}, and resistor R_{EA1} arranged around TL431 IC circuit, as shown in Fig. 13. For the implementation of the error amplifier shown in Fig. 13,

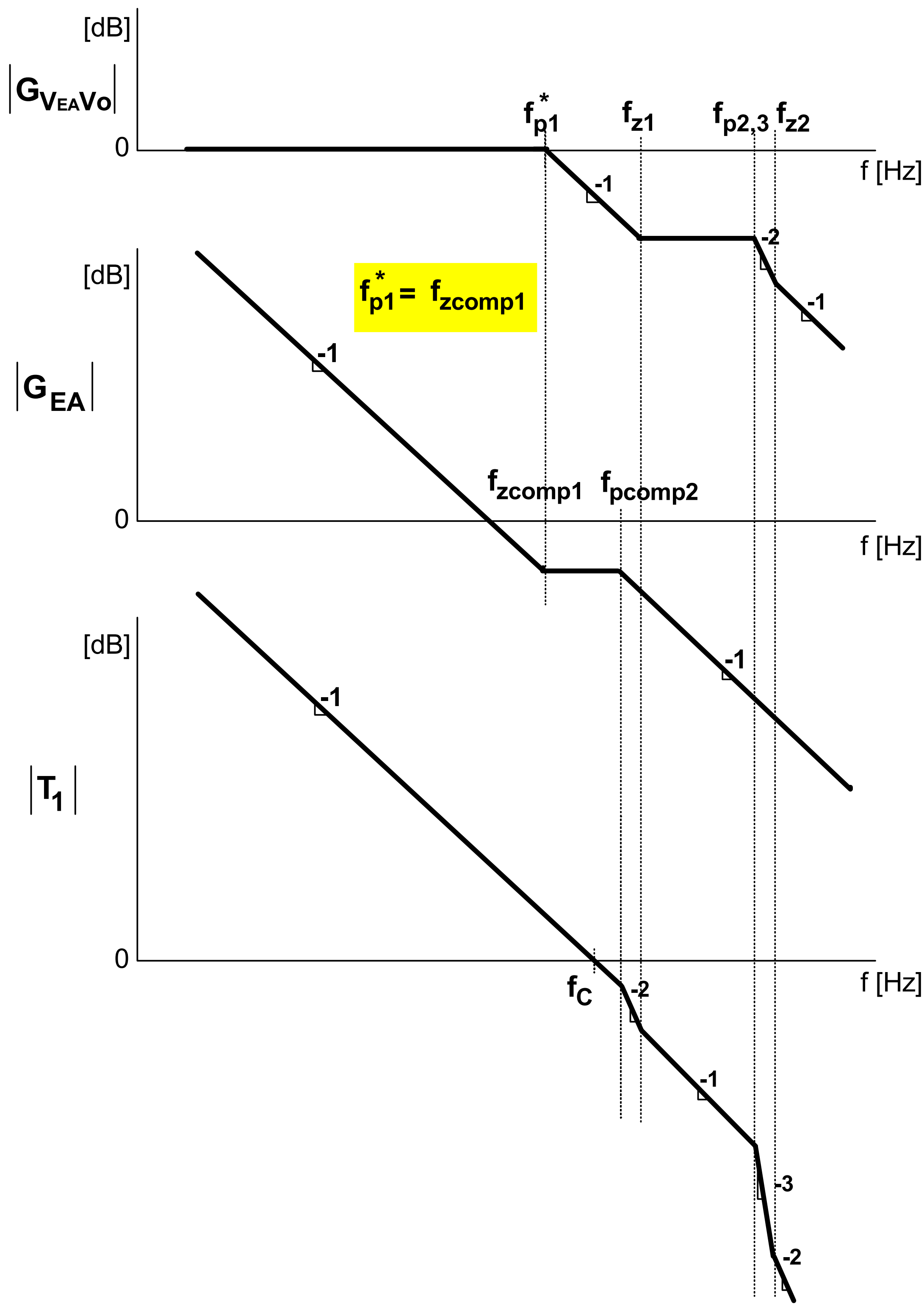


Fig. 21 Gain plots of transfer function $G_{V_{EA}V_O}(s)$, optimum compensation $G_{EA}(s)$, and open-loop transfer function at breakpoint T_1.

$$A = \frac{1}{C_{EA1} + C_{EA2}}, \tag{5.28}$$

$$s_{zcomp1} = \frac{1}{R_{EA1} C_{EA1}}, \tag{5.29}$$

$$s_{pcomp2} = \frac{1}{R_{EA1}} \cdot \left(\frac{1}{C_{EA1}} + \frac{1}{C_{EA2}} \right). \tag{5.30}$$

For a desired crossover frequency f_C of loop T_1 and pole frequency f_{p1}^* of transfer function $G_{EA}(s)$, ans the selection of f_{zcomp1} and f_{pcomp2} so that

$$f_{zcomp1} = f_{p1}^*, \tag{5.31}$$

$$f_{pcomp2} > 4 f_C, \tag{5.32}$$

the compensation components C_{EA1}, C_{EA2}, and R_{EA1} can be calculated from Eqns. (C.33) - (C.35) as derived in Appendix C.

$$C_{EA1} = \frac{.73}{2\pi f_C R_{d1}}, \tag{5.33}$$

$$R_{EA1} = \frac{1}{s_{p1}^*} \cdot \frac{1}{C_{EA1}}, \tag{5.34}$$

$$C_{EA2} = \frac{C_{EA1}}{10}. \tag{5.35}$$

6. DESIGN EXAMPLE

A design example is presented of a 16 V/1 A converter operating with a dc input voltage range 255<V_{IN}<373, an output power range 10 %<Po<100 %, and an output voltage ripple of 1%, using the proposed design procedure.

The design of the power stage begins with the selection of main switch S_1. A 600 V MOSFET device is chosen based on design experience. Assuming 83 % derating of the main switch, the maximum voltage across the drain-source is 500 V. The turns ratio N_P/N_{S1} is next chosen using Eq. (5.8),

$$\frac{N_P}{N_{S1}} = \frac{V_{S1}^{OFF} - V_{IN}^{max}}{V_{O1} + V_F} = \frac{500 - 373}{16 + 0.8} \approx 7.56\,. \tag{6.1}$$

The resulting reverse voltage across rectifier D_1 is then determined using Eq. (5.9),

$$V_{D1}^{ON} = V_{IN}^{max} \frac{N_{S1}}{N_P} + V_{O1} = 373 \cdot \frac{1}{7.56} + 16 \approx 65 \text{ V}. \tag{6.2}$$

When 80 % derating is observed, the rating of the rectifier should be at least 80 V. A 100 V rectifier is chosen as the closest standard value. The maximum duty cycle is then determined from Eq. (5.6),

$$D^{max} = \frac{1}{\frac{V_{IN}^{min}}{V_{O1}+V_F}\frac{N_{S1}}{N_P}+1} = \frac{1}{\frac{255}{16+0.8}\frac{1}{7.56}+1} \approx 0.332\,. \tag{6.3}$$

Next, minimum switching frequency f_S^{min} is chosen as 40 kHz which occurs at minimum input voltage V_{IN}^{min} operating at full load P_O^{max}. Magnetizing inductance L_M is then chosen using Eq. (5.14) assuming 70 % overall efficiency,

$$L_M = \frac{1}{2}\frac{\eta {V_{IN}^{min}}^2 {D^{max}}^2}{P_O^{max} f_S^{min}} = \frac{1}{2}\frac{(0.7)(255)^2(0.332)^2}{(16)(40k)} \approx 3.9\ \text{mH}\,. \tag{6.4}$$

The maximum peak output current i_1^{pk} is then calculated using Eq. (5.2) for $D = D^{max}$,

$$i_1^{pk} = \frac{2I_1}{1-D^{max}} = \frac{2\cdot 1}{1-0.332} \approx 3\ \text{A}\,. \tag{6.5}$$

The output capacitor C_{O1} is determined based on the 1% output voltage ripple requirement. When it is assumed that peak-to-peak capacitor voltage V_C is much less than peak-to-peak resistor voltage V_{Rc}, i.e., $V_C << V_{Rc}$, Eq. (5.15) reduces to $\Delta V_O \approx V_{Rc}$. Solving for equivalent series resistance R_{CO1},

$$R_{CO1} = \frac{\Delta V_O}{i_1^{pk}} = \frac{(0.01)(16)}{3} \approx 0.053\ \Omega. \tag{6.6}$$

The factors under consideration for the selection of the output capacitance is then based on the calculated value of equivalent series resistance R_{CO1}, as well as capacitor volume and voltage rating. The capacitance selected, based on manufacturer's datasheet and calculated equivalent series resistance R_{CO1}, is

$$C_{O1} = 220\,\mu F. \tag{6.7}$$

In addition, to further attenuate the switching ripple a second stage LC filter is added whose values are $L_F = 12\,\mu H$, $C_F = 470\,\mu F$, and equivalent series resistance $R_{LF} = 42\,m\Omega$ and $R_{CF} = 0.19\,m\Omega$, respectively.

Finally, for simplicity, the turns ratio from primary winding N_P to auxiliary winding N_{S2} is chosen as

$$\frac{N_P}{N_{S2}} = \frac{N_P}{N_{S1}} = 7.56 \tag{6.8}$$

The design of the control stage follows the aforementioned design procedure. It begins with STEP 1, the selection of maximum cathode current I_K^{max},

$$I_K^{max} = 20\text{ mA}. \tag{6.9}$$

From STEP 2, the maximum error current which is reflected through the opto-coupler is then

$$i_e^{max} = \beta I_K^{max} = (0.8)(20) = 16\text{ mA}, \tag{6.10}$$

for dc current transfer ratio β=0.8.

The selection of the sensing resistor R_S is made next based on it's maximum power dissipation, as discussed in STEP 3,

$$R_S = \frac{P_{RS}^{max}}{\left[i_{S1}^{pk} \sqrt{\frac{D^{max}}{3}} \right]^2} = \frac{(0.001)(16)}{(0.39)^2 \left(\sqrt{\frac{0.332}{3}} \right)^2} \approx 1\,\Omega, \tag{6.11}$$

where $i_{S1}^{pk} = i_1^{pk} \frac{N_{S1}}{N_P} = \frac{2I_1}{1 - D^{max}} \frac{N_{S1}}{N_P} = (3)(\frac{1}{7.56}) \approx 0.396$ A

The selection of resistor R_F is made next using STEP 4 and the selected value of R_S,

$$R_F = \frac{V_\gamma}{i_e^{max}} - R_S = \frac{0.6}{16\ \text{m}} - 1 \approx 37\ \Omega. \tag{6.12}$$

Using the selected value of I_K^{max} and knowing that the forward voltage drop V_d of the photodiode is 1 V and that the reference voltage V_{REF} within error amplifier TL431 is $V_{REF} = 2.5$ V, STEP 5 is performed,

$$R_B < \frac{V_O - V_d - V_{REF}}{I_K^{max}} = \frac{16 - 1 - 2.5}{20\ \text{m}} = 625\ \Omega. \tag{6.13}$$

Therefore, it is necessary that R_B be less than 625 Ω. However, since the output voltage is much less than 35 V (the maximum rating of TL431), it is desirable to have a low value of R_B to maximize the dc gain of the voltage loop. Therefore, **choose resistor R_B = 20 Ω as a first iteration.** Later when system dynamics are considered, resistor R_B will be re-evaluated.

STEP 6 ensures that I_K^{min} is greater than the minimum recommended current of device TL431,

$$I_K^{min} = \frac{i_e^{min}}{\beta} = \frac{V_\gamma - i_{S1}^{pk} R_S}{\beta(R_F + R_S)} = \frac{0.6 - (0.396)(1)}{0.8(37+1)} \approx 6.7 \text{ mA}. \tag{6.14}$$

STEP 7 ensures that V_K^{max} is below its maximum device rating,

$$V_K^{max} = -R_B I_K^{min} + V_O - V_d = (-20)(6.7 \text{ m}) + 16 - 1 \approx 15 \text{ V} < 35 \text{ V}. \tag{6.15}$$

It is desirable to have the maximum power dissipation of the optocoupler to be below 0.125 W. Therefore, according to STEP 8, resistor R_A must be at least

$$R_A = \frac{-\dfrac{P_{IC1}}{i_e^{max}} + V_{O2} - V_\gamma}{i_e^{max}} = \frac{-\dfrac{0.125}{16 \text{ m}} + 16 - 0.6}{16 \text{ m}} \approx 474\,\Omega. \tag{6.16}$$

Based on this value, resistor R_A is selected as **R_A = 1 kΩ**.

The MOSFET device selected as main switch S_1 is MOTOROLA device MTP1N60E. It has an input capacitance C_{ISS} = 310 pF. Based on this, capacitor C_{ZCD} is selected according to STEP 9,

$$C_{ZCD} = 10 \cdot C_{ISS} \approx 3.3\ \mathrm{nF}. \tag{6.17}$$

The zener clamp reverse breakdown voltage should be maximized as permitted by the main switch device. For this design, V_{ZD1} is chosen to be 18 V. The purpose of resistor R_{ZCD} is to limit the power dissipated by ZD_1, which, for this design, should be no more than 0.125 W. Using STEP 10,

$$R_{ZCD} = \frac{V_{IN}^{max} \frac{N_{S1}}{N_P} - V_{ZD1}}{P_{ZD1}} V_{ZD1} = \frac{(373)\left(\frac{1}{7.56}\right) - 18}{0.125} \cdot 18 \approx 4.5\ \mathrm{k\Omega}. \tag{6.18}$$

The selection of start-up resistor R_{ST} is also based on maximum power dissipation. Using STEP 11,

$$R_{ST} \approx \frac{\left(V_{IN}^{MAX}\right)^2}{P_{ST}} = \frac{(373)^2}{0.125} \approx 1.2\ \mathrm{MEG}\,\Omega. \tag{6.19}$$

Finally, the selection of output voltage sensing resistors R_{d1} and R_{d2} is made using STEP 12,

$$R_{d2} = \frac{R_{d1}}{\frac{V_{O1}}{V_{REF}} - 1}. \tag{6.20}$$

Setting R_{d1} = 5.1 kΩ, R_{d2} is then equal to 940 Ω.

The design of circuit compensation relies upon the pole and zero positions of transfer function $G_{V_{EA}V_O}(s)$ from Eq. (4.17), as shown in Fig. 22. The design guidelines, summarized in Eqs. (5.31) and (5.32), are written for a system whose inner loop T_{INNER} has shifted only the pole s_{p1}. To ensure that the remaining poles and zeroes are above unity gain of T_{INNER}, resistor R_B is adjusted within the limits $20 \le R_B \le 625\,\Omega$ using the MathCad worksheet provided in Appendix B, and the optimum value of resistor **R_B = 200 Ω**, as shown in MathCad Fig. 23.

The compensation component values are then calculated from Eqs. (5.33) to (5.35) based on pole s_{p1}^* of transfer function $G_{V_{EA}V_O}(s)$ and a desired crossover frequency f_C = 1 kHz,

$$C_{EA1} = \frac{0.73}{2\pi f_C R_{d1}} = \frac{0.73}{2\pi(1\,K)(5.1\,K)} \approx 22\,nF, \tag{6.21}$$

$$R_{EA1} = \frac{1}{s_{p1}^*} \cdot \frac{1}{C_{EA1}} = \frac{1}{180} \cdot \frac{1}{22\,n} \approx 39\,K\Omega, \tag{6.22}$$

$$C_{EA2} = \frac{C_{EA1}}{10} = \frac{22\,n}{10} = 2.2\,nF. \tag{6.23}$$

The Bode plot of loop T_1 using the calculated compensation component values is shown in Fig. 24.

The calculated values are incorporated into the simulation model, shown in Fig. 25, and the simulation is evaluated at minimum input voltage (255V dc), full load (1 A) condition and maximum input (373 V dc), minimum load condition (0.1 A), with comparitive results shown in

Fig. 26. It should be noted that the comparison axis have the same limits in order to make a clear, visual comparison.

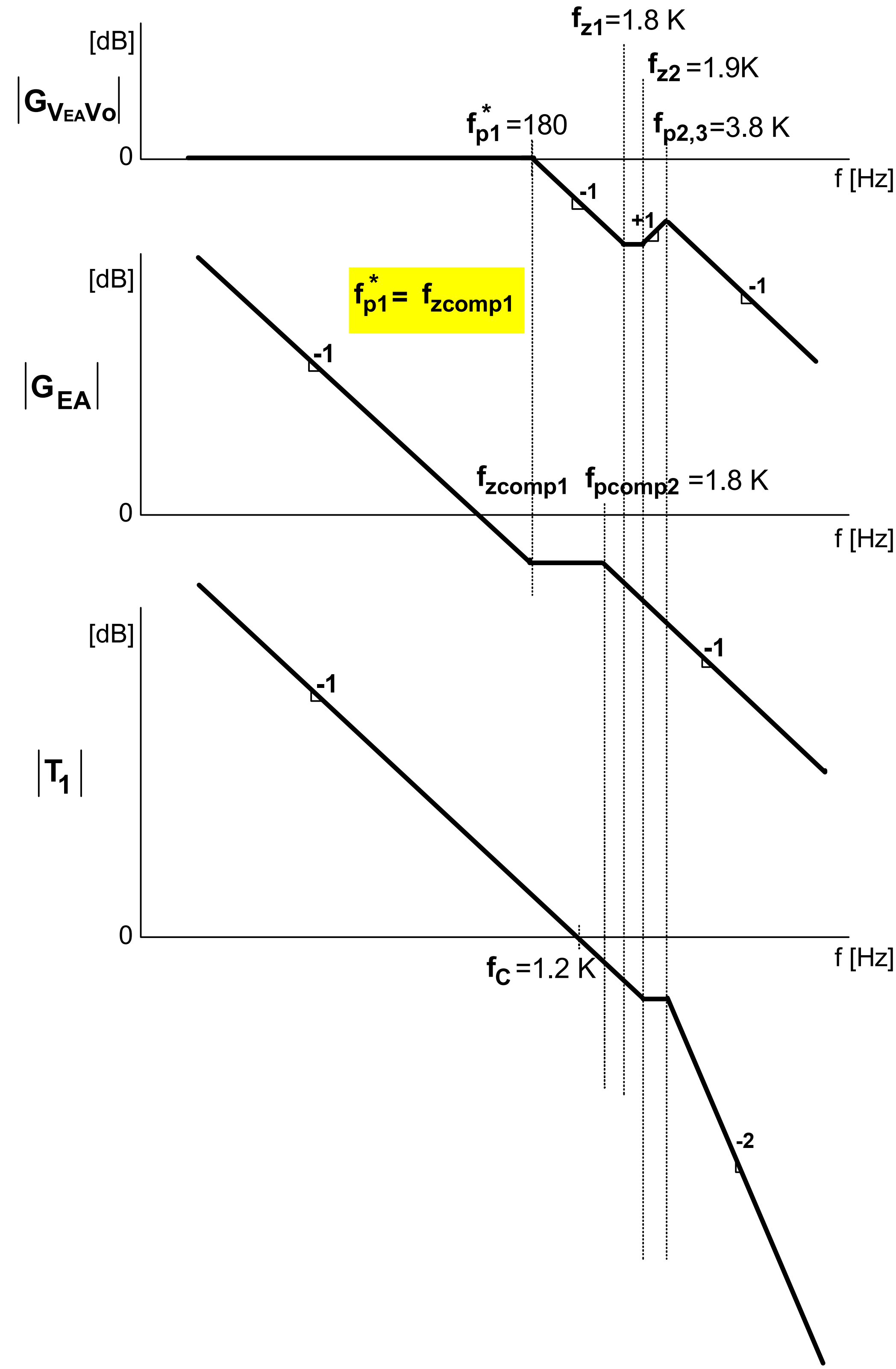


Fig. 22 Gain plots of transfer function $G_{V_{EA}V_O}(s)$, expression $1+T_{INNER}$, and loop gain T_1 for design example of self-oscillating flyback converter.

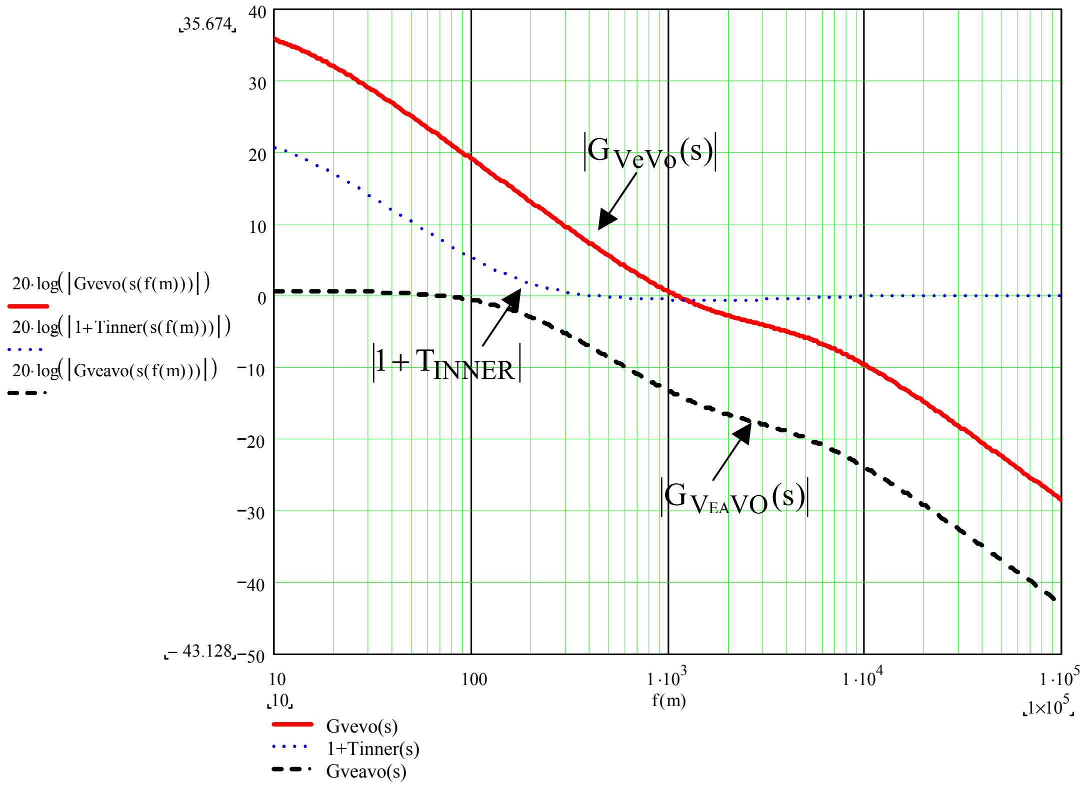
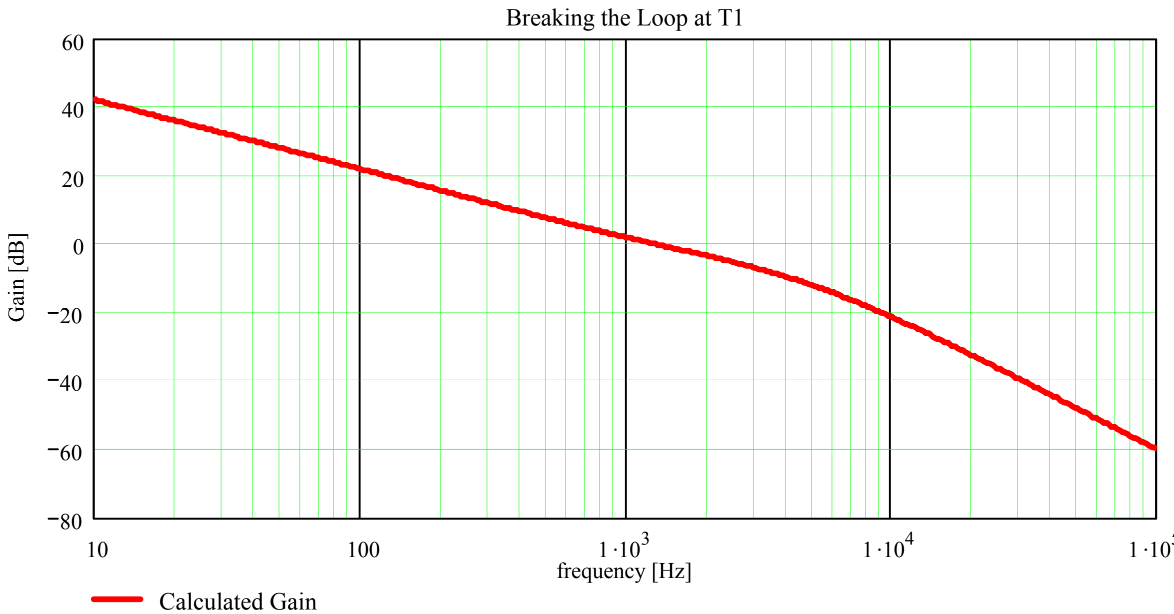


Fig. 23 MathCad results of power stage gain $G_{EA}(s)$, inner loop gain $1 + T_{INNER}$, and gain $G_{V_{EA}V_o}(s)$ of 16 V/1 A self-oscillating flyback converter using calculated values determined in design example.



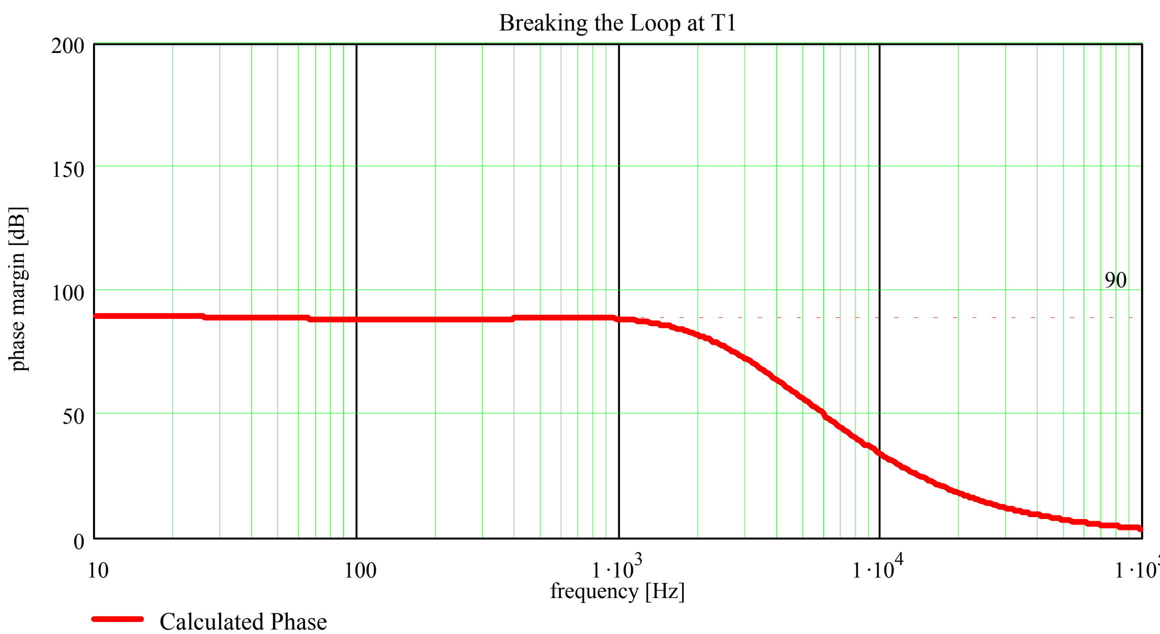


Fig. 24 Bode plot of 16 V/1 A design example circuit using compensation component values $C_{EA1}(s) = 22$ nF, $C_{EA2}(s) = 2.2$ nF, $R_{EA1}(s) = 39$ kΩ and resistor $R_B = 200$ Ω.

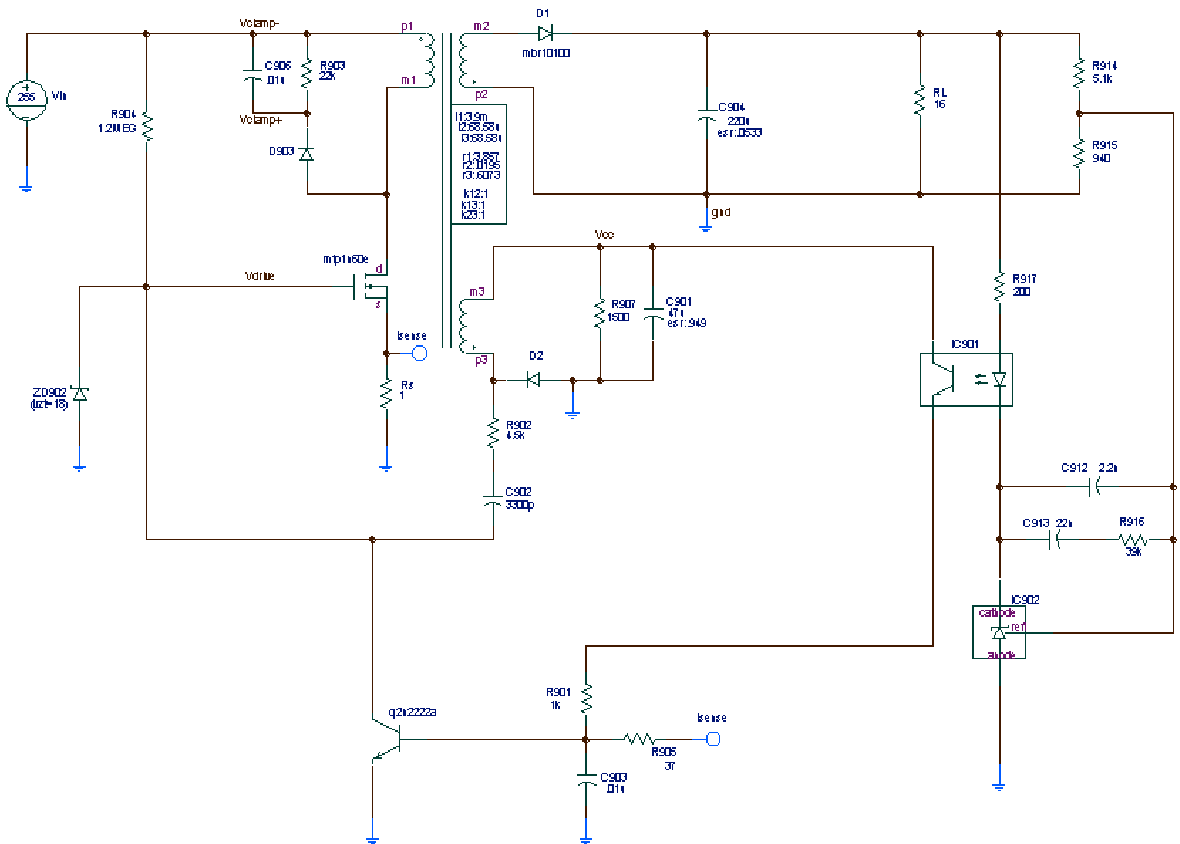
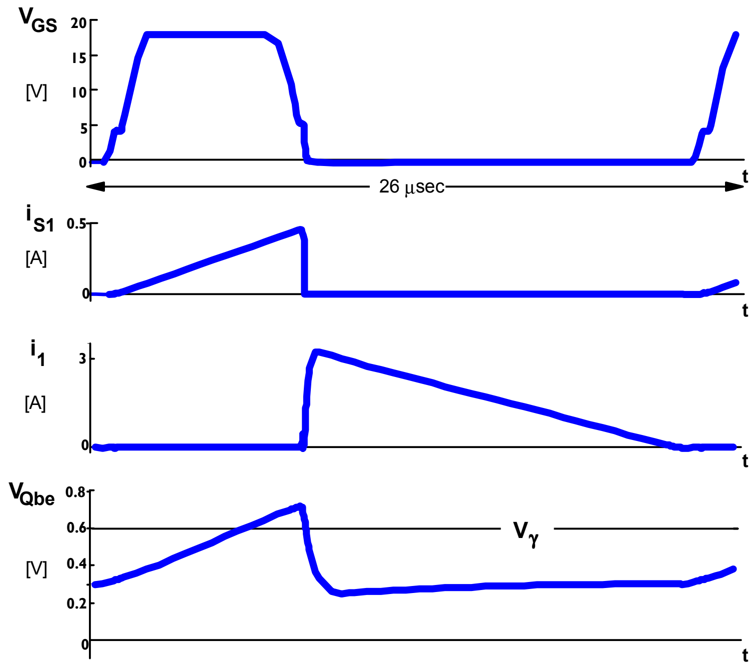
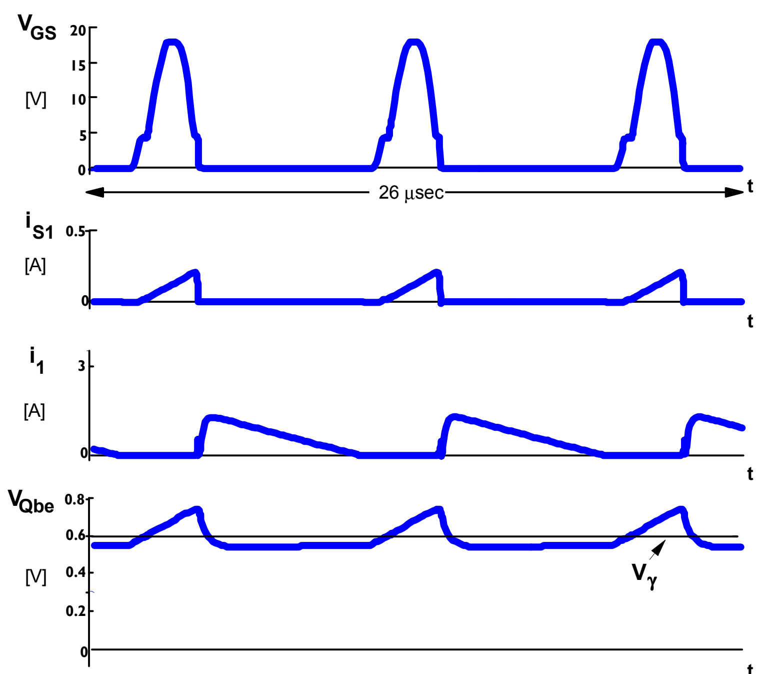


Fig. 25 Simulation schematic of 16 V/1 A self-oscillating flyback converter using calculated component values determined in design example.



(a)



(b)

Fig. 26 Simulation results of design example circuit at (a) 255 V dc input voltage, 16 W output power, and (b) 373 V dc input voltage, 1.6 W output power.

REFERENCES

[1] K. Billings, "*Switchmode Power Supply Handbook*", New York, NY: McGraw-Hill, Inc., 1989.

[2] L. Hayes and J. Spangler, *"Pair of controller ics provide critical conduction switching power supply with voltage and current limiting"*, Power Conversion and Intelligent Motion (PCIM) Magazine, pp. 42 - 50, Nov. 2000.

APPENDICES

APPENDIX A

DPS-250 AB A schematic

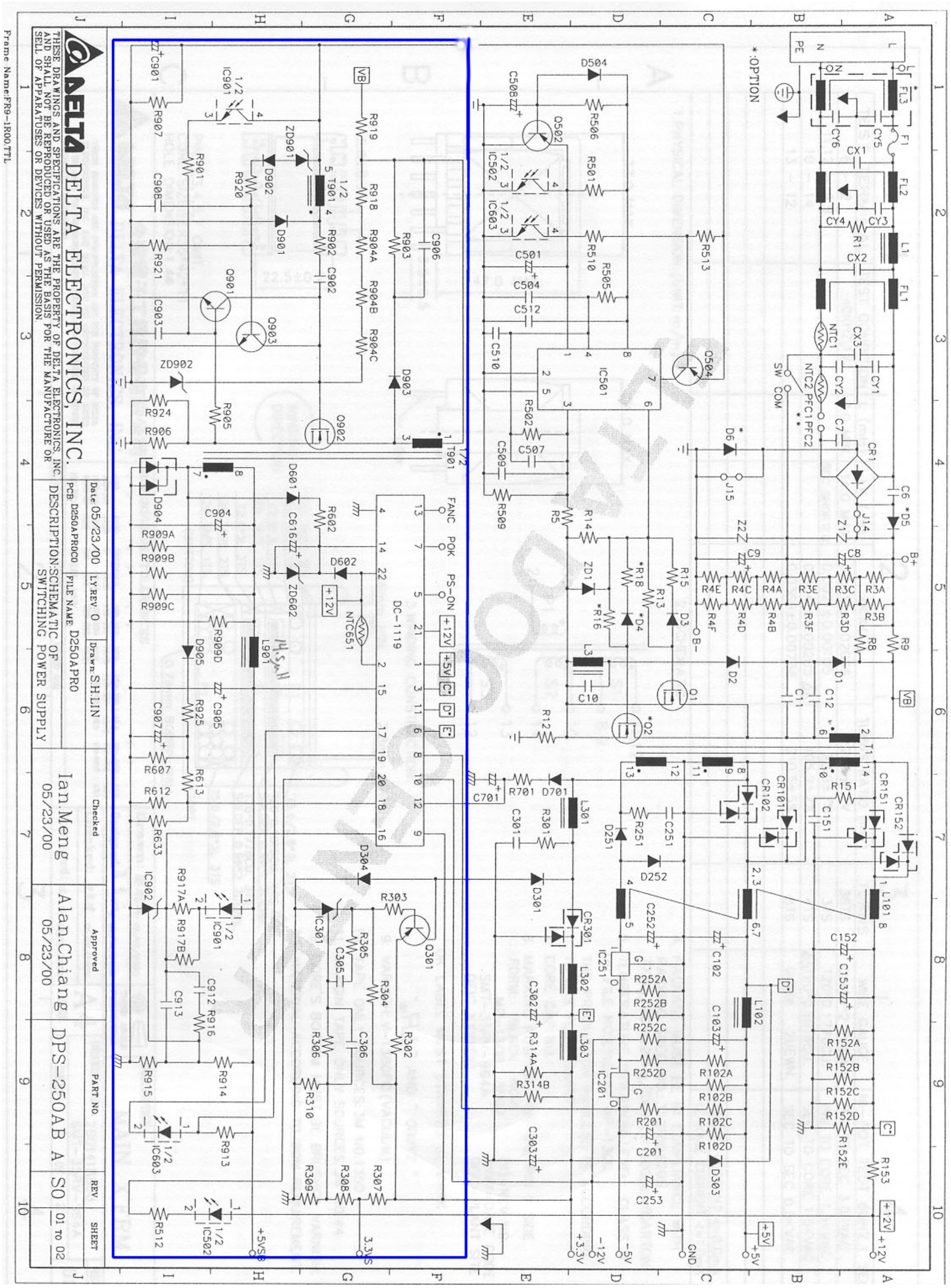


Fig. A1 Schematic of DPS-250AB A. Boxed area contains self-oscillating flyback

APPENDIX B

MathCad™ Worksheet: Stability Design Example

SELF-OSCILLATING FLYBACK CONVERTER

by: Brian T. Irving

Short Hand Notation: $k := 10^3$ $u := 10^{-6}$ $p := 10^{-12}$ $Meg := 10^6$

$mil := 10^{-3}$

Input/Output: $Vin := 255$ $Vo := 16$ $Io := 1$ $Po := Vo \cdot Io$ $\eta := 0.7$

Power Stage Component Values: $Lm := 4.5 \cdot mil$ $n := \frac{1}{7.56}$ $C1 := 220 \cdot u$ $N := \frac{1}{n}$

$Rc1 := 0.38$ $Rf := 37$ $Rs := 0.65$ $Rd1 := 5.1 \cdot k$ $Rd2 := 944 \cdot k$ $Rlf := 42 \cdot mil$

$Lf := 12 \cdot u$ $Cf := 470 \cdot u$ $Rcf := 0.19$ $Vy := 0.6$ $\beta := 1$ $RB := 200$

General Equations: $Vg := \frac{Vin}{N}$ $D := \frac{Vo}{Vg + Vo}$ $parallel(x,y) := \frac{x \cdot y}{x+y}$ $Iin := \frac{Po}{\eta} \cdot \frac{1}{Vin}$

$fs := \frac{1}{2} \cdot \frac{\eta \cdot Vin^2 \cdot D^2}{Po \cdot Lm}$ $m := 1, 1.01 .. 5$ $f(m) := 10^m$ $s(f) := i \cdot 2 \cdot \pi \cdot f$ $Ton := \frac{D}{fs}$

$fs = 3.272 \times 10^4$

Block diagram:

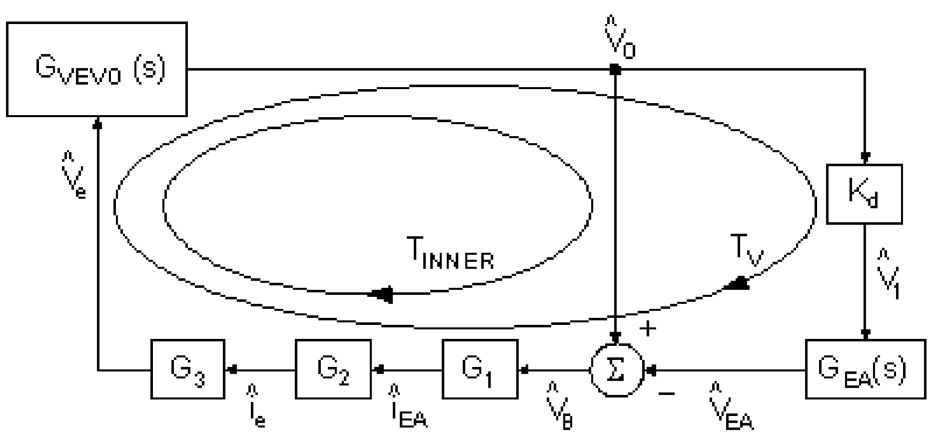


Fig. B1 Stability analysis of design example using MathCad™ software, pg.1.

Individual Transfer Function Blocks:

note: a minus sign is artificially included to match block diagram sign convention

Power Stage Gain Gvevo(s):

$$Ke := -\frac{N}{2\cdot\left(1+\frac{Vo}{Vin}\cdot N\right)\cdot Rs} \qquad Kr := -\frac{Io\cdot N}{Vin\cdot\left(1+N\cdot\frac{Vo}{Vin}\right)} \qquad Mdc := (-1)\cdot\left(-\frac{Vin}{2\cdot Rs\cdot Io}\right)$$

$Ke = -3.944$ $\qquad$ $Kr = -0.02$ $\qquad$ $Mdc = 196.154$

$$\omega o := \frac{1}{\sqrt{Lf\cdot\left(\frac{C1\cdot Cf}{C1+Cf}\right)}} \qquad Q := \sqrt{\frac{Lf}{\left(\frac{Cf\cdot C1}{C1+Cf}\right)}}\cdot\frac{1}{Rc1+Rcf+Rlf+Kr\cdot\left(Rc1\cdot Rcf-\frac{Lf}{C1+Cf}\right)}$$

$$sz1 := \frac{1}{Cf\cdot Rcf} \qquad sz2 := \frac{1}{C1\cdot Rc1} \qquad sp1 := -\frac{Kr}{C1+Cf}$$

$$Gvevo(s) := Mdc\cdot\frac{\left(\frac{s}{sz1}+1\right)\cdot\left(\frac{s}{sz2}+1\right)}{\left(\frac{s}{sp1}+1\right)\cdot\left(\frac{s^2}{\omega o^2}+\frac{s}{\omega o\cdot Q}+1\right)}$$

dc Gain: $Mdc = 196.154$

Poles:	single pole:	$fp1 := \frac{sp1}{2\cdot\pi}$	$fp1 = 4.638$	Hz
	double pole:	$fp2and3 := \frac{\omega o}{2\cdot\pi}$	$fp2and3 = 3.753\times10^3$	Hz
Zeroes:	single zero:	$fz1 := \frac{sz1}{2\cdot\pi}$	$fz1 = 1.782\times10^3$	Hz
	single zero:	$fz2 := \frac{sz2}{2\cdot\pi}$	$fz2 = 1.904\times10^3$	Hz

Fig. B1 (cont.) Stability analysis of design example using MathCad™ software, pg.2.

Sensing Gain Kd: $Kd := \frac{Rd2}{Rd1 + Rd2}$

Transconductance Gain G1: $G1 := \frac{1}{RB}$

Opto-coupler Gain G2: $G2 := \beta$

Transresistance Gain G3: $G3 := Rf + Rs$

Checking to see which poles are shifted by inner loop:

$$Tinner(s) := Gvevo(s) \cdot G1 \cdot G2 \cdot G3 \qquad Gveavo(s) := \frac{Tinner(s)}{1 + Tinner(s)}$$

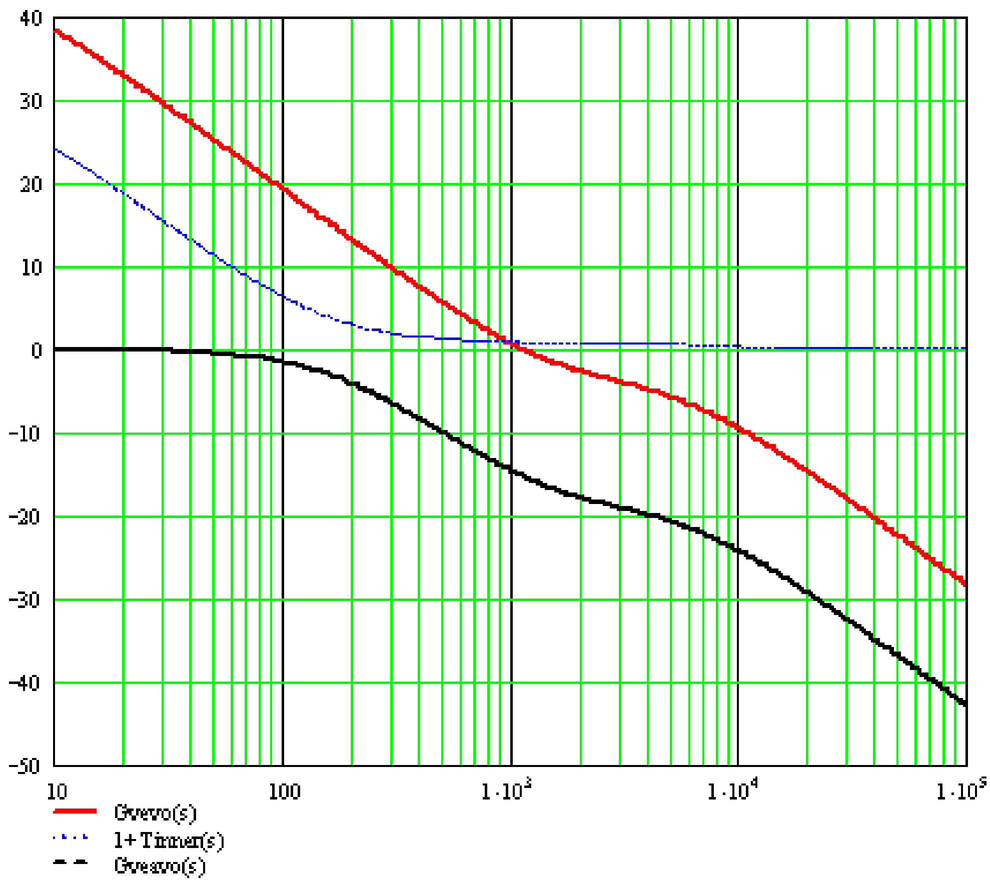
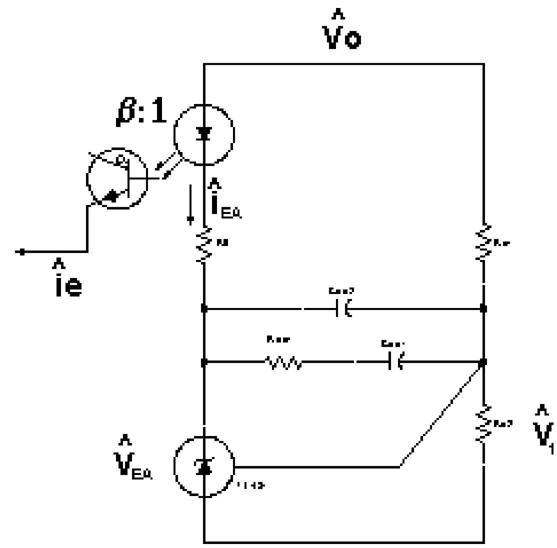


Fig. B1 (cont.) Stability analysis of design example using MathCad™ software, pg.3.

Gain Gea(s):

Optimal Compensation Design Guidelines:

Choose Desired Band Width fc: $fc := 1 \cdot k$



Expression for Reduced Power Stage block Gveavo:

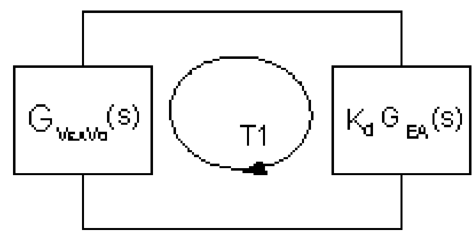
$K := G1 \cdot G2 \cdot G3$ $\qquad K = 0.188$

Shifted Pole sp1star:

$sp1star := sp1 \cdot (1 + K \cdot Mdc)$ $\qquad sp1star = 1.105 \times 10^{3}$

$fp1star := \dfrac{sp1star}{2 \cdot \pi}$ $\qquad fp1star = 175.909$

$$Gveavo(s) := \frac{K \cdot Mdc}{1 + K \cdot Mdc} \cdot \frac{\left(\dfrac{s}{sz1} + 1\right) \cdot \left(\dfrac{s}{sz2} + 1\right)}{\left(\dfrac{s}{sp1star} + 1\right) \cdot \left(\dfrac{s^2}{\omega o^2} + \dfrac{s}{\omega o \cdot Q} + 1\right)}$$



(b)

Determine Values of Compensation Components:

$Cea1 := \dfrac{0.727}{2 \cdot \pi \cdot fc \cdot Rd1} \cdot \dfrac{K \cdot Mdc}{1 + K \cdot Mdc}$ $\qquad Rea1 := \dfrac{1}{Cea1 \cdot sp1star}$ $\qquad Cea2 := \dfrac{Cea1}{10}$

$Cea1 = 2.209 \times 10^{-8}$ $\qquad Rea1 = 4.096 \times 10^{4}$ $\qquad Cea2 = 2.209 \times 10^{-9}$

$Cea1 := 21000 \cdot p$ $\qquad Rea1 := 39 \cdot k$ $\qquad Cea2 := 2200 \cdot p$ $\qquad$ --using the nearest standard component values

$A := \dfrac{1}{(Cea1 + Cea2) \cdot parallel(Rd1, Rd2)}$ $\qquad szcomp1 := \dfrac{1}{Rea1 \cdot Cea1}$ $\qquad spcomp2 := \dfrac{1}{Rea1} \cdot \left(\dfrac{1}{Cea1} + \dfrac{1}{Cea2}\right)$

$A = 8.497 \times 10^{3}$

$Gea(s) := (-1) \cdot \left(\dfrac{A}{s} \cdot \dfrac{\dfrac{s}{szcomp1} + 1}{\dfrac{s}{spcomp2} + 1}\right)$ $\qquad fzcomp1 := \dfrac{szcomp1}{2 \cdot \pi}$ $\qquad fzcomp1 = 194.328$

$fpcomp2 := \dfrac{spcomp2}{2 \cdot \pi}$ $\qquad fpcomp2 = 2.049 \times 10^{3}$

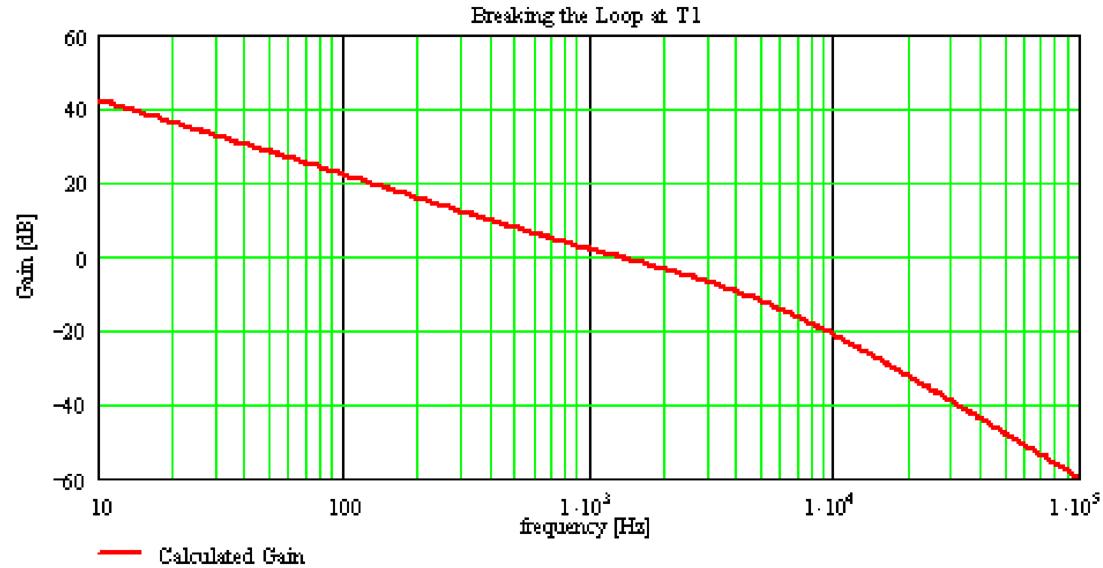
Note: minus sign is removed to comply with block diagram sign convention

Fig. B1 (cont.) Stability analysis of design example using MathCad™ software, pg.4.

Defining Loop T1:

$$T1(s) := Gveavo(s) \cdot Kd \cdot Gea(s)$$

$$T1gain(s) := 20 \cdot \log(|T1(s)|) \qquad T1p(s) := \arg(T1(s)) \cdot \frac{180}{\pi} + 180 \qquad T1phase(s) := if(T1p(s) > 180, T1p(s) - 360, T1p(s))$$



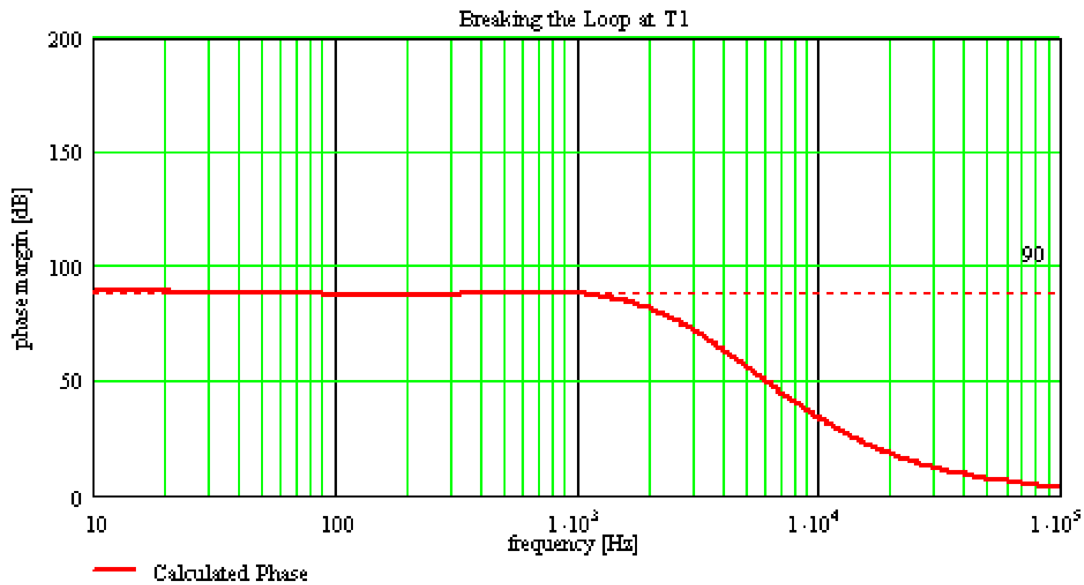


Fig. B1 (cont.) Stability analysis of design example using MathCad™ software, pg.5.

APPENDIX C

Transfer Function Block Derivations

C.1 **Error-Voltage to Output-Voltage Transfer Function** $G_{VeVo}(s) = \hat{V}_O / \hat{V}_e$

The power stage transfer function $G_{VeVo}(s)$ is actually the product of two transfer functions

$$G_{VeVo}(s) = \frac{\hat{V}_O}{\hat{V}_e} = \frac{\hat{I}_1}{\hat{V}_e}\frac{\hat{V}_O}{\hat{I}_1}, \tag{C.1}$$

where $\hat{I}_1$ is the small signal change in the average current of winding N_{S1}. By deriving each transfer function independently, the overall power stage transfer function $G_{VeVo}(s)$ is obtained.

C.1.1 Error-voltage-to-average output current transfer function $\hat{I}_1 / \hat{V}_e$

To facilitate the derivation of transfer function error voltage $\hat{V}_e$ to average output current $\hat{I}_1$, Fig. C.1. represents the control plant. The output of the plant is average output current I_1, and the inputs of the plant include error voltage V_e, input voltage V_{IN}, and output voltage V_O. From Fig. C.1, the output of the control plant is expressed as a function of its inputs,

$$\hat{I}_1 = I_1\left(V_e, V_{IN}, V_O\right) = K_e\hat{V}_e + K_f\hat{V}_{IN} + K_r\hat{V}_O, \tag{C.2}$$

where:

$$K_e = \frac{\partial I_1}{\partial V_e}, \tag{C.3}$$

$$K_f = \frac{\partial I_1}{\partial V_{IN}}, \tag{C.4}$$

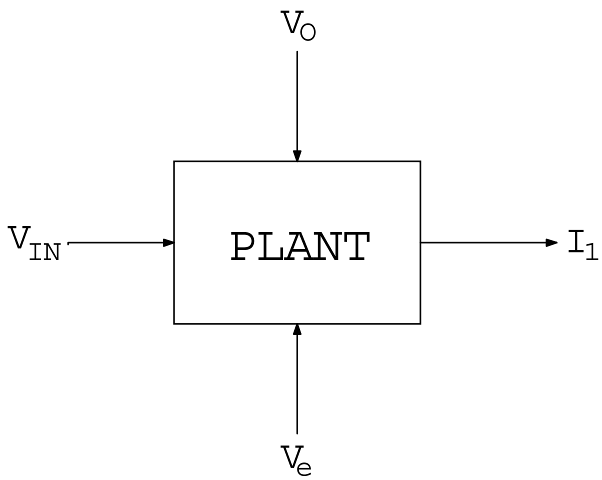


Fig. C.1 Control plant representing relationship between average output current I_1 and control variables V_e, V_{IN}, and V_O.

$$K_r = \frac{\partial I_1}{\partial V_O}. \qquad (C.5)$$

Equation C.2 can be represented as a circuit diagram as shown in Fig. C.2.

For the self-oscillating flyback converter, average winding current I_1 is expressed as

$$I_1 = \frac{i_1^{pk}}{2}(1 - D) = I_O, \qquad (C.6)$$

where

$$i_1^{pk} = N i_{S1}^{pk} = N \frac{V_{IN}}{L_M} t_{ON}. \qquad (C.7)$$

From Fig. C.2, on time t_{ON} is,

$$t_{ON} = t_1 + t_2, \qquad (C.8)$$

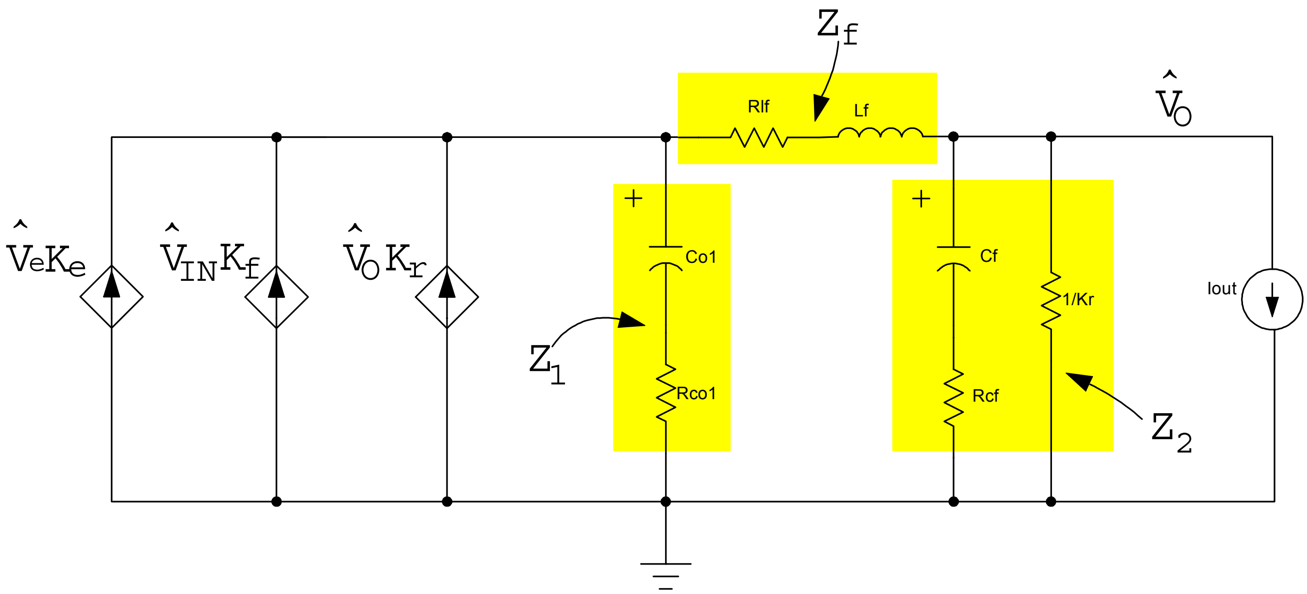


Fig. C.2 Circuit diagram which represents Eq. (C.2)

where t_1 represents the time it takes voltage V_{Qbe} to reach the threshold voltage level V_γ,

$$t_1 = \frac{V_\gamma - V_e}{R_S\, V_{IN}/L_M}, \tag{C.9}$$

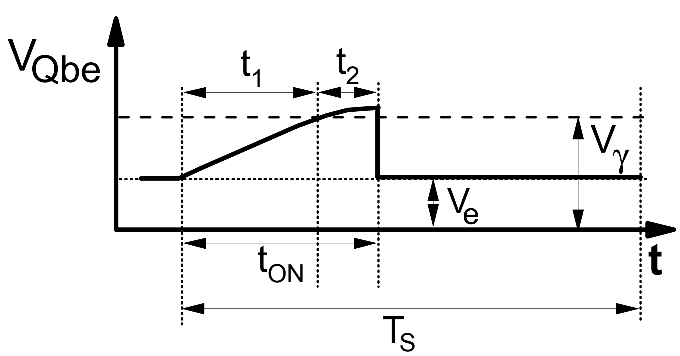


Fig. C.3 Base-emitter voltage V_{Qve} for a single switching cycle T_S of self-oscillating flyback converter.

and t_2 represents the time it takes transistor Q_1 to discharge input capacitance C_{ISS} of main switch S_1 to the threshold voltage level V_{TH}.

$$t_2 = \text{constant}. \tag{C.10}$$

Generall\y, time t_2 is constant over the line and load range, and, therefore, can be neglected from a small-signal analysis, i.e., $\hat{t}_1 + t_2 = \hat{t}_1 = \hat{t}_{ON}$.

Subsituting Eqs. (C.7)-(C.10) into Eq. (C.6),

$$I_1 = I_O = \frac{N}{2R_S} \frac{V_\gamma - V_e}{1 + N\dfrac{V_O}{V_{IN}}}. \tag{C.11}$$

Taking the derivative of Eq. (C.11) with respect to error voltage V_e,

$$\frac{\partial I_1}{\partial V_e} = K_e = -\frac{N}{2R_S\left(1 + N\dfrac{V_O}{V_{IN}}\right)}. \tag{C.12}$$

Taking the derivative of Eq. (C.11) with respect to input voltage V_{IN},

$$\frac{\partial I_1}{\partial V_{IN}} = K_f = \frac{NV_O}{V_{IN}^2} \frac{1}{\left(1 + \dfrac{NV_O}{V_{IN}}\right)^2}. \tag{C.13}$$

Taking the derivative of Eq. (C.12) with respect to output voltage V_O,

$$\frac{\partial I_1}{\partial V_O} = K_r = -\frac{N^2}{2} \frac{(V_\gamma - V_e)}{V_{IN}R_S\left(1 + N\dfrac{V_O}{V_{IN}}\right)^2}. \tag{C.14}$$

It should be noted that Eqs. (C.12)-(C.14) contains steady-state variables. The steady state expression for error voltage V_e is obtained from Eq. (C.11), where

$$V_e = V_\gamma - \frac{2I_O R_S\left(1 + N\frac{V_O}{V_{IN}}\right)}{N}. \tag{C.15}$$

Substituting into Eq. (C.14),

$$K_r = -\frac{I_O N}{V_{IN}\left(1 + N\frac{V_O}{V_{IN}}\right)}. \tag{C.16}$$

When deriving error-voltage-to-output-voltage transfer function $G_{VeVo}(s)$, it is assumed that $\hat{V}_{IN} = 0$, and Eq. (C.2) reduces to

$$\hat{I}_1 = K_e \hat{V}_e + K_r \hat{V}_O. \tag{C.17}$$

Relating small-signal current $\hat{I}_1$ to output voltage $\hat{V}_O$ through impedance Z of the output filter,

$$\hat{V}_O = Z \cdot \hat{I}_1 = \frac{Z_1 Z_2}{Z_1 + Z_F + Z_2}\hat{I}_1 = K_e \hat{V}_e + K_r \hat{V}_O,, \tag{C.18}$$

where:

$$Z_1 = \frac{sC_{O1}R_{CO1} + 1}{sC_{O1}}, \tag{C.19}$$

$$Z_F = R_{Lf} + sL_f, \tag{C.20}$$

$$Z_2 = \frac{sC_F R_{CF} + 1}{sC_F}. \tag{C.21}$$

Solving for output voltage $\hat{V}_O$,

$$\frac{\hat{V}_O}{\hat{V}_e} = \frac{Z \cdot K_e}{1 - Z \cdot K_r}. \tag{C.22}$$

Arranging Eq. (C.22) in pole zero form results in power stage transfer function $G_{VeVo}(s)$,

$$G_{VeVo}(s) = \frac{\hat{V}_O}{\hat{V}_e} = M_{dc} \cdot \frac{(s/s_{z1} + 1)(s/s_{z2} + 1)}{(s/s_{p1} + 1)(s^2/\omega_o^2 + s/(Q\omega_o) + 1)}, \tag{C.23}$$

where:

$$M_{dc} = -\frac{V_{IN}}{2R_S I_O}, \tag{C.24}$$

$$s_{z1} = \frac{1}{C_{O1} R_{CO1}}, \tag{C.25}$$

$$s_{z1} = \frac{1}{C_F R_{CF}}, \tag{C.26}$$

$$s_{p1} = -\frac{K_r}{C_{O1} + C_F}, \tag{C.27}$$

$$\omega_O = \frac{1}{\sqrt{\dfrac{L_F}{\dfrac{1}{C_{O1}} + \dfrac{1}{C_F}}}}, \tag{C.28}$$

$$Q = \sqrt{L_F \frac{C_F + C_{O1}}{C_F C_{O1}}} \cdot \left(\frac{1}{R_{CO1} + R_{CF} + R_{lf} + K_r \left(R_{CO1} R_{CF} - \dfrac{L_F}{C_{O1} + C_F} \right)} \right). \tag{C.29}$$

C.2 **Transfer Function** $G_{V_{EA}Vo}(s) = \hat{V}_O / \hat{V}_{EA}$

Generally, the presence of inner loop T_{INNER} has the effect of pole shifting on transfer function $G_{V_{EA}Vo}(s)$ with respect to power stage transfer function $G_{VeVo}(s)$. This effect can be generalized for any power stage $G_{VeVo}(s)$ as

$$G_{V_eVo}(s) = \frac{\hat{V}_O}{\hat{V}_e} = G\,\frac{Z(s)}{P(s)}, \tag{C.30}$$

where G represents dc gain of system, Z(s) represents system zeroes, and P(s) represents system poles. The general expression for transfer function $G_{V_{EA}Vo}(s)$ is

$$G_{V_{EA}Vo}(s) = \frac{\hat{V}_O}{\hat{V}_{EA}} = \frac{KG_{VeVo}(s)}{1+KG_{VeVo}(s)} = KG\,\frac{Z(s)}{P(s)+KGZ(s)} = KG\,\frac{Z(s)}{P(s)^*}, \tag{C.31}$$

where

$$K = G_1G_2G_3, \tag{C.32}$$

$$P(s)^* = P(s) + KGZ(s). \tag{C.33}$$

From Eq. (C.33), it is shown that **only the poles P(s) of the system are affected by the inner loop**. The poles $P(s)^*$ of transfer function $G_{V_{EA}Vo}(s)$ are shifted with respect to poles P(s) of power stage transfer function $G_{VeVo}(s)$ by dc loop gain KG and by zeroes Z(s) of the power stage.

Similarly, the expression for transfer function $G_{V_{EA}Vo}(s)$, given in Eq. (4.17), shows evidence of pole shifting. For simplicity, it is assumed that the second stage LC filter, which consists of filter inductor L_F and filter capacitor C_F, is small, and, therefore, its resonant frequency is relatively high with respect to the bandwidth of inner loop T_{INNER}. For this case, the only pole which remains below bandwidth f_{INNER} of inner loop T_{INNER} is pole s_{p1}. Considering only poles less than f_{INNER}, transfer function $G_{V_{EA}V_O}(s)$ reduces to

$$G_{V_{EA}V_O}(s)=\frac{KG_{VeVo}(s)}{1+KG_{VeVo}(s)}\approx\frac{KM_{dc}}{(s/s_{p1}+1)+KM_{dc}}=\frac{\dfrac{KM_{dc}}{1+KM_{dc}}}{(\dfrac{s}{s_{p1}(1+KM_{dc})}+1)}=\frac{KM_{dc}}{1+KM_{dc}}\cdot\frac{1}{s/s_{p1}^{*}+1}, \tag{C.34}$$

where $s_{p1}^{*}=(1+KM_{dc})s_{p1}$.

rewriting Eq. (C.34) to include remaining poles and zeroes,

$$G_{V_{EA}V_O}(s)=\frac{KM_{dc}}{1+KM_{dc}}\cdot\frac{(s/s_{z1}+1)(s/s_{z2}+1)}{(s/s_{p1}^{*}+1)(s^2/\omega_O^2+s/Q\omega_O+1)}. \tag{C.35}$$

C.3 Sense voltage to error-amplifier -current transfer function $G_{EA}(s)=\hat{i}_{EA}/\hat{V}_1$

To facilitate the derivation of the sense voltage $\hat{V}_1$ to error-amplifier current $\hat{i}_{ea}$, Fig. C.4 illustrates the small signal equivalent circuit diagram of the error amplifier TL431. The error amplifier TL431 has been approximated as a dependent current source and resistors R_{d1} and R_{d2} have been represented as a thevenin resistance R_{th},

$$R_{th}=\frac{R_{d1}R_{d2}}{R_{d1}+R_{d2}}, \tag{C.36}$$

connected to sense voltage $\hat{V}_1$,

$$\hat{V}_1 = \frac{R_{d2}}{R_{d1} + R_{d2}} \hat{V}_O = K_d \hat{V}_O . \tag{C.37}$$

The compensation components C_{EA1}, C_{EA2}, and R_{EA1} are lumped together into impedance block Z_{FB} for simplicity.

Small-signal cathode current $\hat{i}_k$ is $\hat{i}_k = K_O \hat{V}_r$, where K_O represents the transresistance gain of the error amplifier and voltage $\hat{V}_r$ is

$$\hat{V}_r = \hat{V}_1 \frac{Z_{FB}}{Z_{FB} + R_{th}} + \hat{V}_{ka} \frac{R_{th}}{Z_{FB} + R_{th}} . \tag{C.38}$$

As transresistance gain $K_O \to \infty$, voltage $\hat{V}_r \to 0$, and Eq. (C.38) reduces to

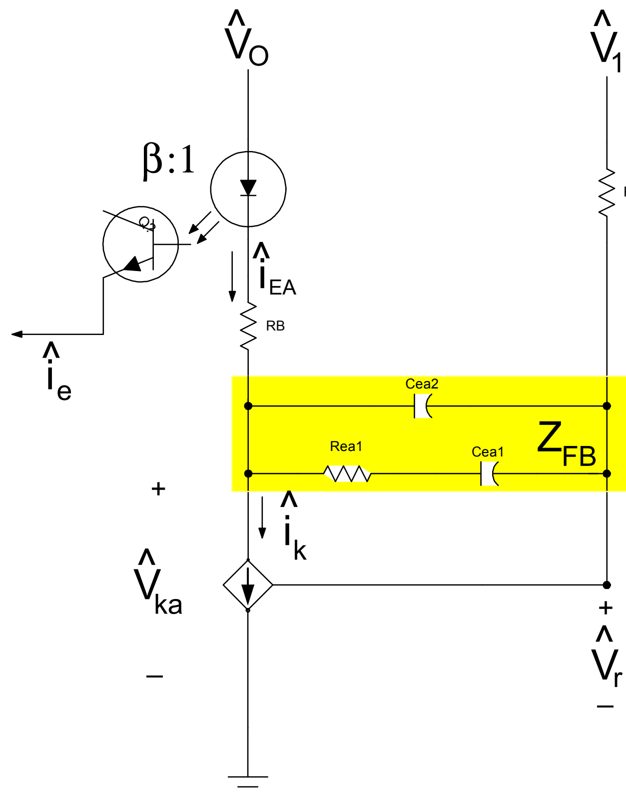


Fig. C.4 Equivalent small-signal model of error amplifier of self-oscillating flyback converter

$$G_{EA}(s) = \frac{\hat{V}_{ka}}{\hat{V}_1} = -\frac{Z_{FB}}{R_{th}}, \tag{C.39}$$

where
$$Z_{FB} = \frac{1}{s(C_{EA1} + C_{EA2})} \frac{sR_{EA1}C_{EA1} + 1}{s\dfrac{R_{EA1}C_{EA1}C_{EA2}}{C_{EA1} + C_{EA2}} + 1}. \tag{C.40}$$

Eq. (C.39) can be written generally as

$$G_{EA}(s) = \frac{A}{s} \cdot \frac{s/s_{zcomp1} + 1}{s/s_{pcomp2} + 1}, \tag{C.41}$$

$$A = \frac{1}{C_{EA1} + C_{EA2}}, \tag{C.42}$$

$$s_{zcomp1} = \frac{1}{R_{EA1} C_{EA1}}, \tag{C.43}$$

$$s_{pcomp2} = \frac{1}{R_{EA1}} \cdot \left(\frac{1}{C_{EA1}} + \frac{1}{C_{EA2}} \right). \tag{C.44}$$

C.4 Calculations of Error-Amplifier Compensation Component Values

Once the small-signal block diagram is reduced to a single loop system, loop T_1 simplifies to

$$T_1(s) = K_d G_{V_{EA}Vo}(s) G_{EA}(s) = K_d \cdot \frac{KM_{dc}}{1+KM_{dc}} \cdot A \cdot \frac{(s/s_{z1}+1)(s/s_{z2}+1)}{\left(s/s_{p1}^{*}+1\right)\left(s^2/\omega_O^2 + s/Q\omega_O + 1\right)} \cdot \frac{1}{s} \cdot \frac{\left(s/s_{zcomp1}+1\right)}{\left(s/s_{pcomp2}+1\right)}, \tag{C.45}$$

as given previously in Eq. (4.16), assuming a single shifted pole. Substituting Eq. (4.8), (4.17), and (5.27) into Eq. (C.45) and assuming $s_{zcomp1} = s_{p1}^{*}$ and $s_{pcomp2} = 8\pi f_C$, loop T_1 at unity gain crossover frequency f_C is,

$$T_1(s = 2\pi f_C) = \frac{KM_{dc}}{1+KM_{dc}} \cdot \frac{1}{R_{d1}(C_{EA1} + C_{EA2})} \cdot \frac{0.8}{2\pi f_C} = 1. \tag{C.46}$$

Solving for $C_{EA1}+C_{EA2}$,

$$C_{EA1} + C_{EA2} = \frac{0.8KM_{dc}}{1 + KM_{dc}} \cdot \frac{1}{2\pi f_C R_{d1}} . \tag{C.47}$$

Selecting $C_{EA2} = C_{EA1}/10$, compensation capacitor C_{EA1} and C_{EA2} are

$$C_{EA1} = \frac{0.727}{2\pi f_C R_{d1}}, \tag{C.48}$$

$$C_{EA2} = \frac{C_{EA1}}{10}. \tag{C.49}$$

Since compensation zero s_{zcomp1} is chosen to cancel pole s_{p1}^{*}, compensation resistor R_{EA1} is determined as

$$R_{EA1} = \frac{1}{C_{EA1}} \cdot \frac{1}{s_{p1}^{*}}. \tag{C.50}$$