2A 23V Synchrnous Step-Down Converter

FEATURES

- 2A Continuous Output Current
- Programmable Soft Start
- 130mΩ Internal Power MOSFET Switches
- Stable with Low ESR Output Ceramic Capacitors
- Up to 93% Efficiency
- <1μA Supply Current in Shutdown Mode
- Fixed 340KHz Frequency
- Thermal Shutdown
- Cycle by Cycle Over Current Protection
- Wide 4.75 to 23V Operating Input Range
- Ouput Adjustable from 0.925V to 12V
- Under Voltage Lockout

APPLICATIONS

- Networking Systems such as Modems & Routers
- Distributed Power Systems
- Pre-Regulator for Linear Regulators.
- Set-top Box

DESCRIPTION

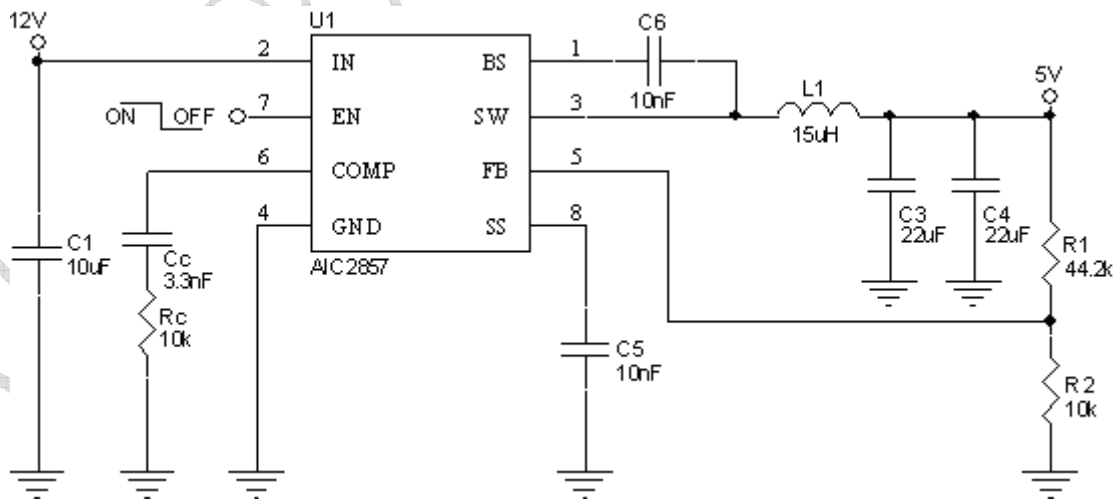
The AIC2857 is a synchronous step-down regulator with an integrated Power MOSFET. It achieves 2A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. Adjustable soft-start reduces the stress on the input source and the output overshoot at turn-on. In shutdown mode, the regulator draws 1μA or less of supply current.

The AIC2857 is available in SOP8 and SOP-8 with Exposed Pad Package.

TYPICAL APPLICATIONS CIRCUIT



Typical Application Circuit

PIN CONFIGURATION

AIC2857X<u>XXXX</u>

- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGING TYPE
  S: SOP-8
  R8: SOP-8 Exposed Pad (Heat Sink)
- G: GREEN PACKAGE

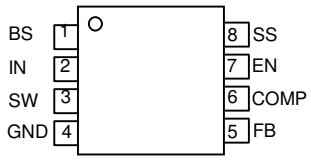
Example:

AIC2857GR8TR

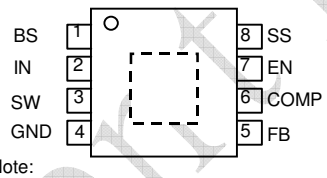
→ GREEN SOP-8 Exposed Pad (Heat Sink) Package and TAPE & REEL Packing Type

PIN CONFIGURATION

SOP-8 TOP VIEW



SOP-8 Exposed Pad (Heat Sink)
TOP VIEW



Note:
The exposed pad must be connected with GND pin.

ABSOLUTE MAXIMUM RATINS

Input Voltage (V_{IN}) ..... -0.3V to 26V
SW pin Voltage (V_{SW}) ..... -1V to V_{IN} +0.3V
BS Pin Voltage ..... V_{SW}-0.3V to V_{SW}+6V
EN Pin Voltage ..... -0.3V to V_{IN}
All Other Pins Voltage ..... -0.3V to 6V
Operating Ambient Temperature Range T_A ..... -40ºC~85ºC
Operating Maximum Junction Temperature T_J 150ºC
Storage Temperature Range T_{STG} ..... -65ºC~150ºC
Lead Temperature (Soldering 10 Sec.) 260ºC
Thermal Resistance Junction to Case SOP-8 ..... 40°C/W
SOP-8 Exposed Pad* ..... 15°C/W
Thermal Resistance Junction to Ambient SOP-8 ..... 160°C/W
SOP-8 Exposed Pad* ..... 60°C/W

(Assume no Ambient Airflow)

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

*The package is place on a two layers PCB with 2 ounces copper and 2 square inch, connected by 8 vias.

ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, V_{EN} =5V, T_A=25°C, unless otherwise specified.) (Note1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current		V_{EN} = 0V		0.3	3	μA
Supply Current		V_{EN} = 2.0V; V_{FB}= 1.0V		1.3	1.5	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 23V	0.90	0.925	0.950	V
Feedback Overvoltage Threshold				1.1		V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Erro Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ± 10μA		820		μA/V
High-Side Switch On-Resistance	$R_{DS (ON) 1}$			130		mΩ
Low-Side Switch On-Resistance	$R_{DS (ON) 2}$			130		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Upper Switch Current Limit		Minimum Duty Cycle	2.4	3.4		A
Lower Switch Current Limit		From Drain to Source		0.9		A
COMP to Current Sense Transconductance	G_{CS}			5.2		A/V
Oscillation Frequency	f_{OSC}		300	340	380	KHz
Short Circuit Oscillation Frequency		V_{FB}= 0V		110		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB}= 1.0V		90		%
Minimum On Time	T_{ON}			220		ns
EN Shutdown Threshold Voltage		V_{EN} Rising	1.1	1.5	2.0	V
EN Shutdown Threshold Voltage Hysteresis				220		mV
Under Voltage Lockout Threshold		V_{IN} Rising	2.4	3.4		V
Under Voltage Lockout Threshold Hysteresis				210		mV
Soft-Start Current		V_{SS} = 0V		6		μA
Soft-Start Period		V_{SS} = 0.1μF		15		ms
Thermal Shutdown				160		°C

Note 1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: It is recommended to use duty ratio above 10% for minimizing resultant duty cycle jitter.

Note 3: It is recommended to connect a soft start capacitor to soft start pin. Leave the soft start pin open may cause large inrush current and output overshooting.

TYPICAL PERFORMANCE CHARACTERISTICS

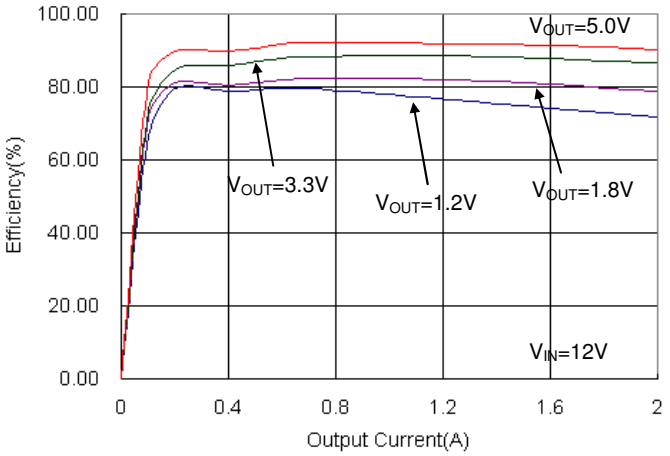


Fig. 1 Efficiency vs. Load Current

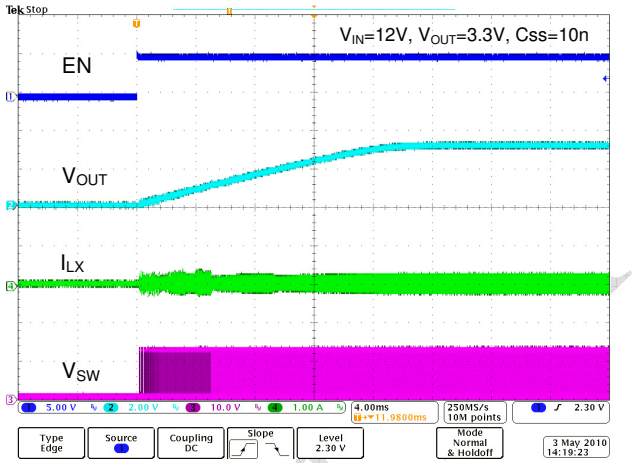


Fig. 2 Start-Up Waveform at V_{OUT}=3.3V, I_{OUT}=0A

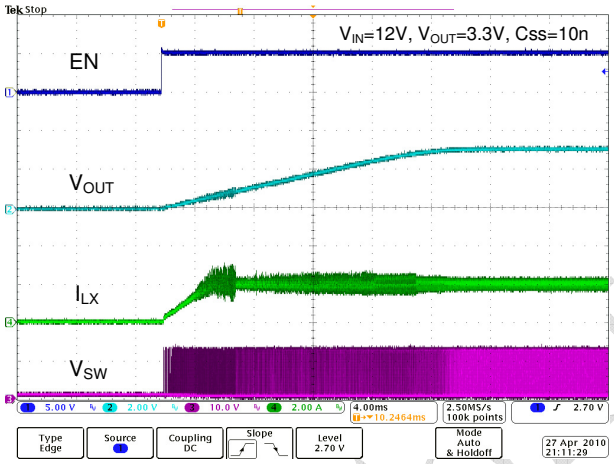


Fig. 3 Start-Up Waveform at V_{OUT}=3.3V, I_{OUT}=2A

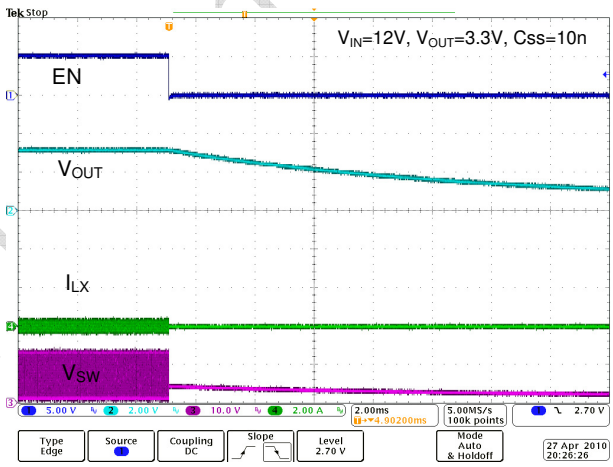


Fig. 4 Shutdown Waveform at V_{OUT}=3.3V, I_{OUT}=0A

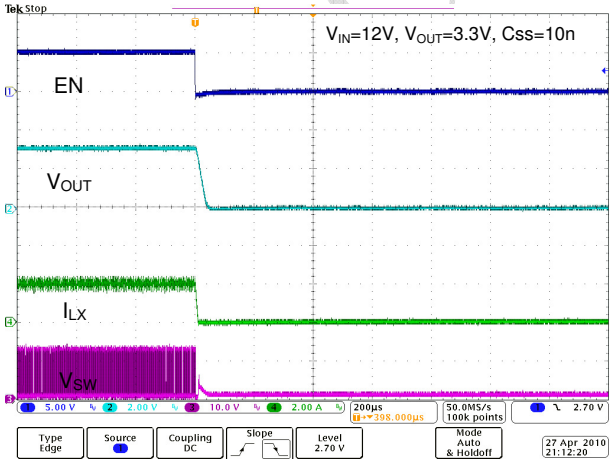


Fig. 5 Shutdown Waveform at V_{OUT}=3.3V, I_{OUT}=2A

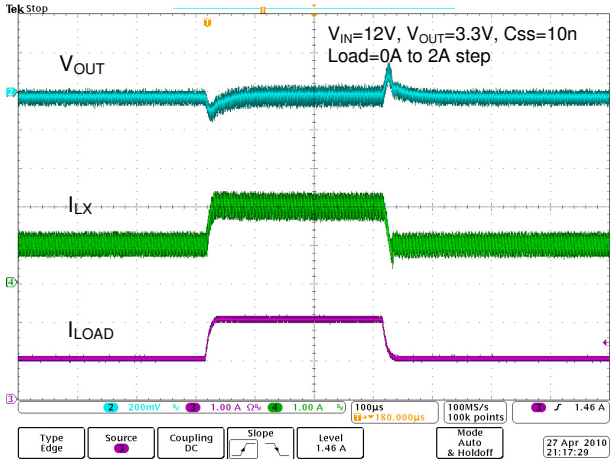


Fig. 6 Load Transient at V_{OUT}=3.3V, I_{OUT}=0A to 2A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

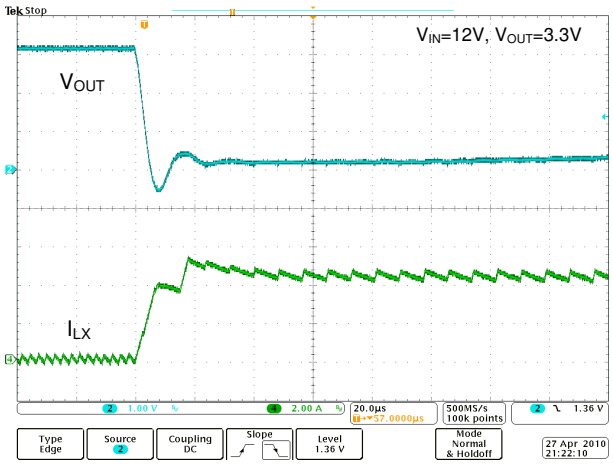


Fig. 7 Short Circuit Waveforms at V_{IN}=12V, V_{OUT}=3.3V

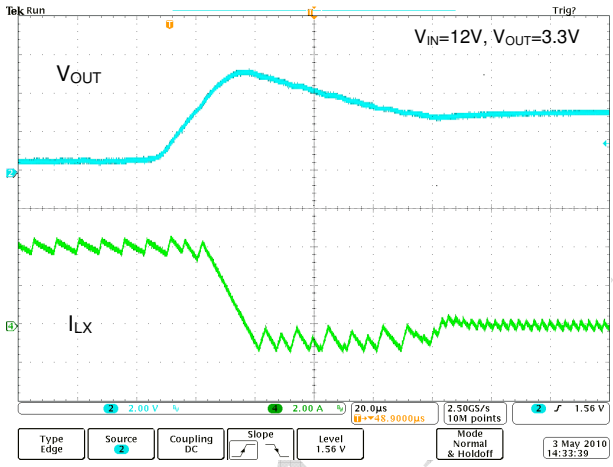


Fig. 8 Circuit Recovery Waveforms at V_{IN}=12V, V_{OUT}=3.3V

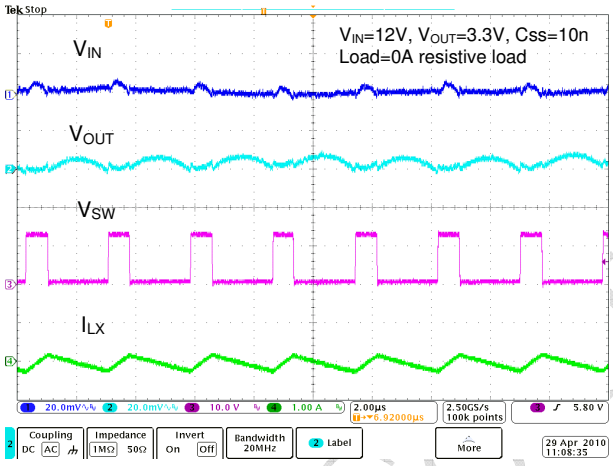


Fig. 9 Stability Waveform at V_{OUT}=3.3V, I_{OUT}=0A

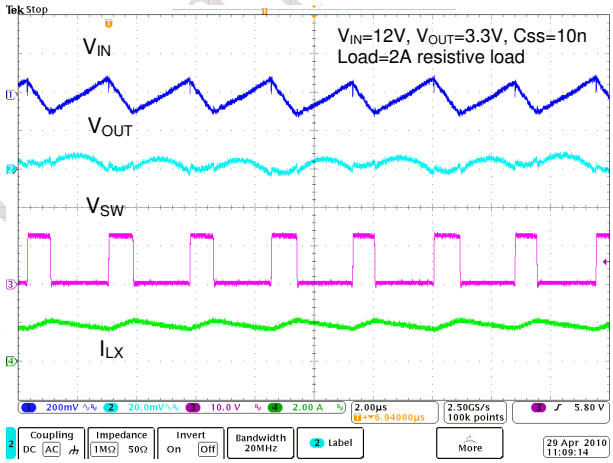
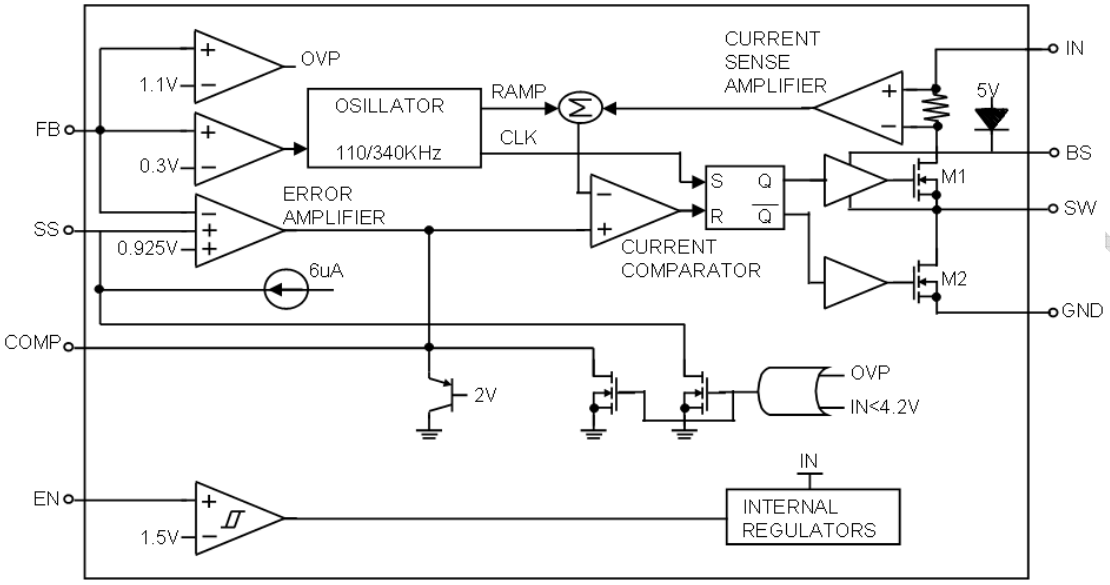


Fig. 10 Stability Waveform at V_{OUT}=3.3V, I_{OUT}=2A

BLOCK DIAGRAM



Functional Block Diagram of AIC2857

PIN DESCRIPTIONS

Pin 1: BS: High Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 10nF or greater capaitor from SW to BS to power the high-side switch.

Pin 2: IN: Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75 to 23V power source. By pass IN to GND with a suitabley large capacitor to eliminate noise on the input to the IC.

Pin 3: SW: Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from switch to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.

Pin 4:GND: Ground. Connect the exposed pad on backside to Pin 4.

Pin 5: FB: Feedback Input. FB senses the output voltage to regulate that voltage Drive feedback with a resistive voltage divider from the output voltage.

Pin 6: COMP: Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network form COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.

Pin 7: EN: Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator. Drive it low to turn it off. For automatic strat-up, attach to IN with a 100kΩ pull up resistor.

Pin 8: SS: Soft Star Contol Input. SS controls the soft star period. Connect a capacitor from SS to GND to set the soft-star period. A 0.1μF capacitor sets the soft-star period to 15ms. To disable the soft-star feature, leave the SS pin

APPLICATION INFORMATIONS

The AIC2857 is a synchronous high voltage buck converter that can support the input voltage range from 4.75V to 23V and the output current can be up to 2A.

Setting the Output Voltage

The output voltage is set using a resistive voltage divider connected from the output voltage to FB. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R3}{R2 + R3}$$

Thus the output voltage is:

$$V_{FB} = 0.925 \times \frac{R3}{R2 + R3}$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ.

Inductor

The inductor selection depends on the current ripple of inductor, the input voltage and the output voltage.

$$L \geq \frac{V_{OUT}}{f_{OSC} \cdot \Delta I_L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting a large current ripple of inductor allows the use of a smaller inductance. However, higher current ripple of inductor can cause higher output ripple voltage and large core loss. By setting an acceptable current ripple of inductor, a suitable inductance can be obtained from above equation.

In addition, it is important to ensure the inductor saturation current exceeds the peak value of inductor current in application to prevent core saturation. The peak value of inductor current can be calculated according to the following equation.

$$I_{PEAK} = I_{OUT(max)} + \frac{V_{OUT}}{2 \times f_{OSC} \cdot L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Soft-Start

The AIC2857 provides the soft-start function. Initially, the voltage at SS pin is 0V. Then an internal current source of 6μA (typ.) charges an external soft-start capacitor. During the soft-start period, the voltage at SS pin will limit the feedback threshold voltage at FB pin. When the voltage at SS pin is higher than 0.925V, the feedback threshold voltage at FB pin reaches the desired value. The soft-start time can be calculated in accordance with the following equation.

$$t_{SS} = C_{SS} \times \frac{0.925V}{6\mu A}$$

The soft-start capacitor is discharged to GND when the $\overline{SHDN}$ pin is connected to GND.

Optional Schottky Diode

An Optional schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency.

Input Capacitor and Output Capacitor

To prevent the high input voltage ripple and noise resulted from high frequency switching, the use of low ESR ceramic capacitor for the maximum RMS current is recommended. The approximated RMS current of the input capacitor can be calculated according to the following equation.

$$I_{CINRMS} \approx \sqrt{I_{OUT(MAX)}^2 \times \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}^2} + \frac{\Delta I_L^2}{12}}$$

The selection of output capacitor depends on the required output voltage ripple. The output voltage ripple can be expressed as:

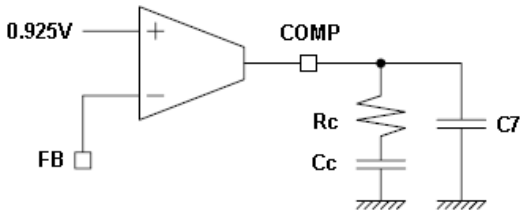
$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times f_{OSC} \cdot C_{OUT}} + ESR \cdot \Delta I_L$$

For lower output voltage ripple, the use of low ESR ceramic capacitor is recommended. The tantalum capacitor can also be used well, but its ERS is larger than that of ceramic capacitor.

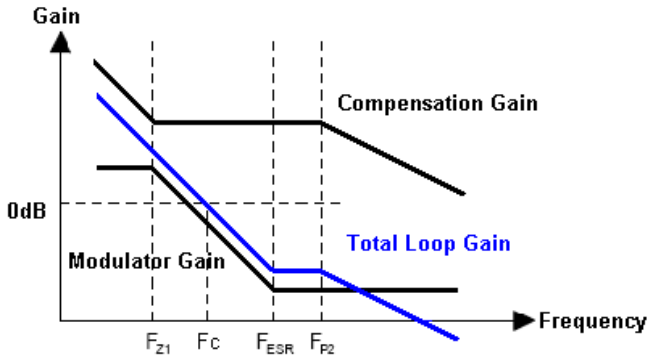
When choosing the input and output ceramic capacitors, X5R and X7R types are recommended because they retain their capacitance over wider ranges of voltage and temperature than other types.

When using the ceramic capacitor as the input capacitor, the high input voltage transient may be generated at some start-up conditions, such as connecting the input to a live power source. By adding a small resistor in series with the input ceramic capacitor, the high input voltage transient can be improved.

Loop Compensation



In order to avoid the poor output voltage ripple and low efficiency caused by instability, AIC2857 requires a proper external compensation network to compensate its feedback loop. In this external compensation network, the compensation resistor, R_C, and the compensation capacitor, C_C, are used to set the high-frequency integrator gain and the integrator zero. C7 is used to cancel the zero caused by the output capacitor and it's ESR. While using the ceramic capacitor as the output capacitor, C7 can be omitted due to the small ESR.



Where V_{FB} is the feedback voltage (0.925V), and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor, Cc and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$F_{P1} = \frac{1}{2\pi \times C3 \times R_{LOAD}}$$

The system has one zero of importance, due to the compensation capacitor, Cc and the compensation resistor, Rc. This zero is located at:

$$F_{Z1} = \frac{1}{2\pi \times Cc \times Rc}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$F_{ESR} = \frac{1}{2\pi \times C3 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor, C7 and the compensation resistor, Rc is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$F_{P2} = \frac{1}{2\pi \times C7 \times Rc}$$

The values of the compensation components given in this data sheet yield a stable control loop for the given output voltage and capacitor. If different conversions

and output capacitors are requires, some values of the compensation components may need to be adjusted to ensure stability.

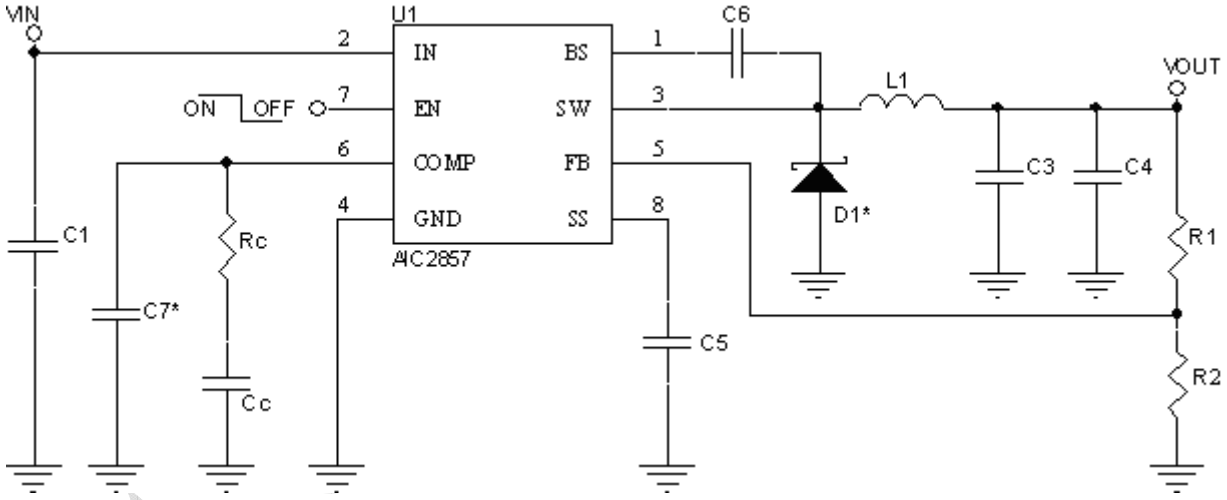
Layout Consideration

In order to ensure a proper operation of AIC2857, the following points should be managed comprehensively.

1. The input capacitor and V_{IN} should be placed as close as possible to each other to reduce the input voltage ripple and noise.
2. The output loop, which is consisted of the inductor, the internal power switch, the Schottky diode and the output capacitor, should be kept as small as possible.
3. The routes with large current should be kept short and wide.
4. Logically the large current on the converter should flow at the same direction.
5. In order to prevent the effect from noise, the IC's GND pin should be placed close to the ground of the input bypass capacitor and should be away from the ground of the Schottky diode.

The FB pin should be connected to the feedback resistors directly and the route should be away from the noise sources.

APPLICATION CIRCUIT



* Note: Optional D1 may be paralleled between the SW pin and GND pin to improve overall efficiency.

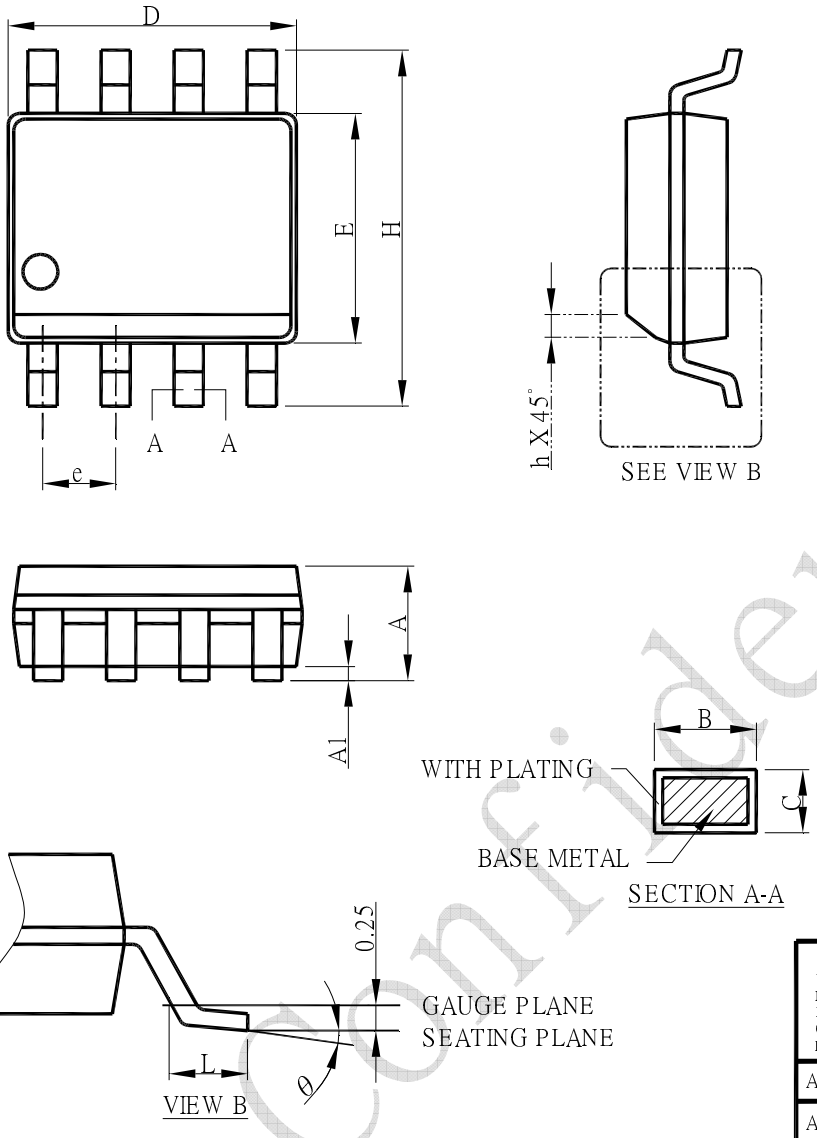
** Note: C7 is needed for high ESR output capacitor

COMPONENT SELECTION

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	Rc (kΩ)	Cc (nF)	C7 (pF)
12	1.2	4.7 (Taiyo Yuden NR8040T4R7N)	22 ceramic (Taiyo Yuden EMK325BJ226MM-T)	2.4	10	None
12	1.8	6.8 (Lee Yu LYB1207-6R8)	22 ceramic (Taiyo Yuden EMK325BJ226MM-T)	3.6	8.2	None
12	3.3	10 (COOPER Buss-mann DR125)	22 ceramic (Taiyo Yuden EMK325BJ226MM-T)	6.8	3.9	None
12	5.0	15 (Lee Yu LYS104S-150M)	22 ceramic (Taiyo Yuden EMK325BJ226MM-T)	10	3.3	None

PHYSICAL DIMENSIONS

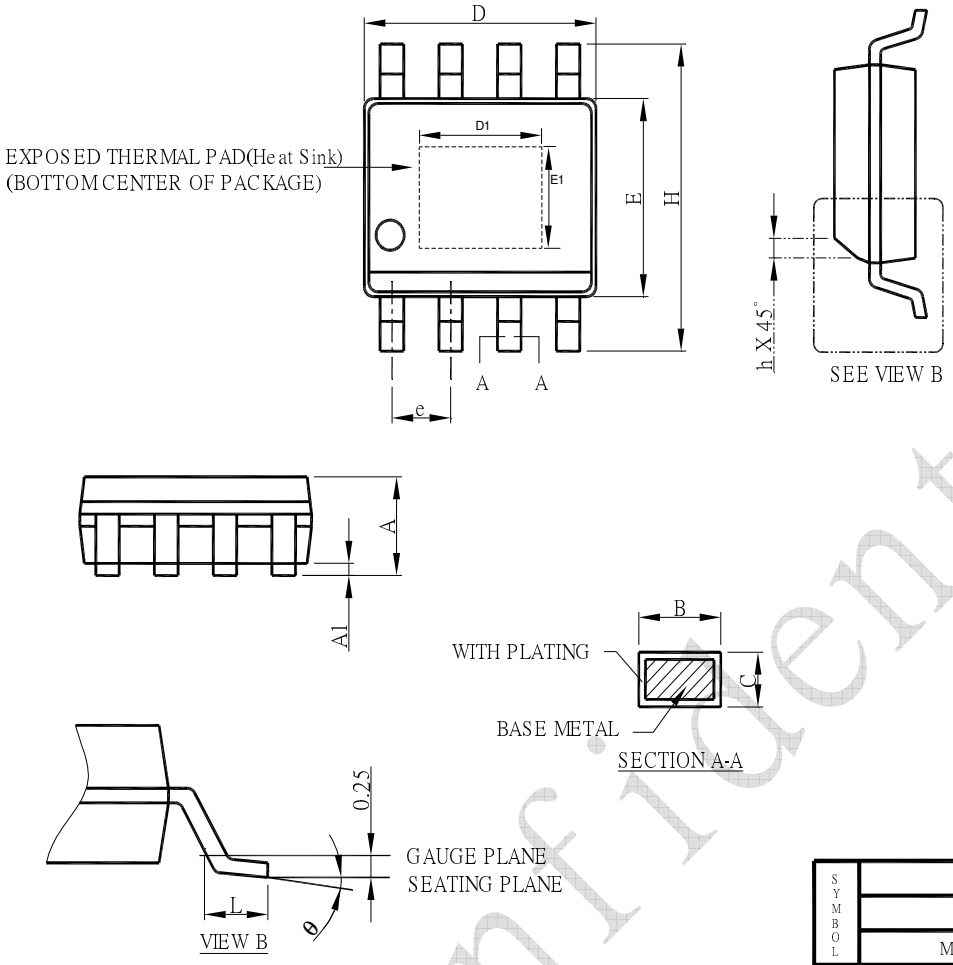
● SOP-8 PACKAGE OUTLINE DRAWING



SYMBOL	SOP-8	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

Note: 1. Refer to JEDEC MS-012AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

● SOP-8 Exposed Pad (Heat Sink) PACKAGE OUTLINE DRAWING



SYMBOL	SOP-8Exposed Pad(Heat Sink)	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
q	0°	8°
D1	1.5	3.5
E1	1.0	2.55

Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.