3520D

ADAPTIVE BALLAST CONTROL IC

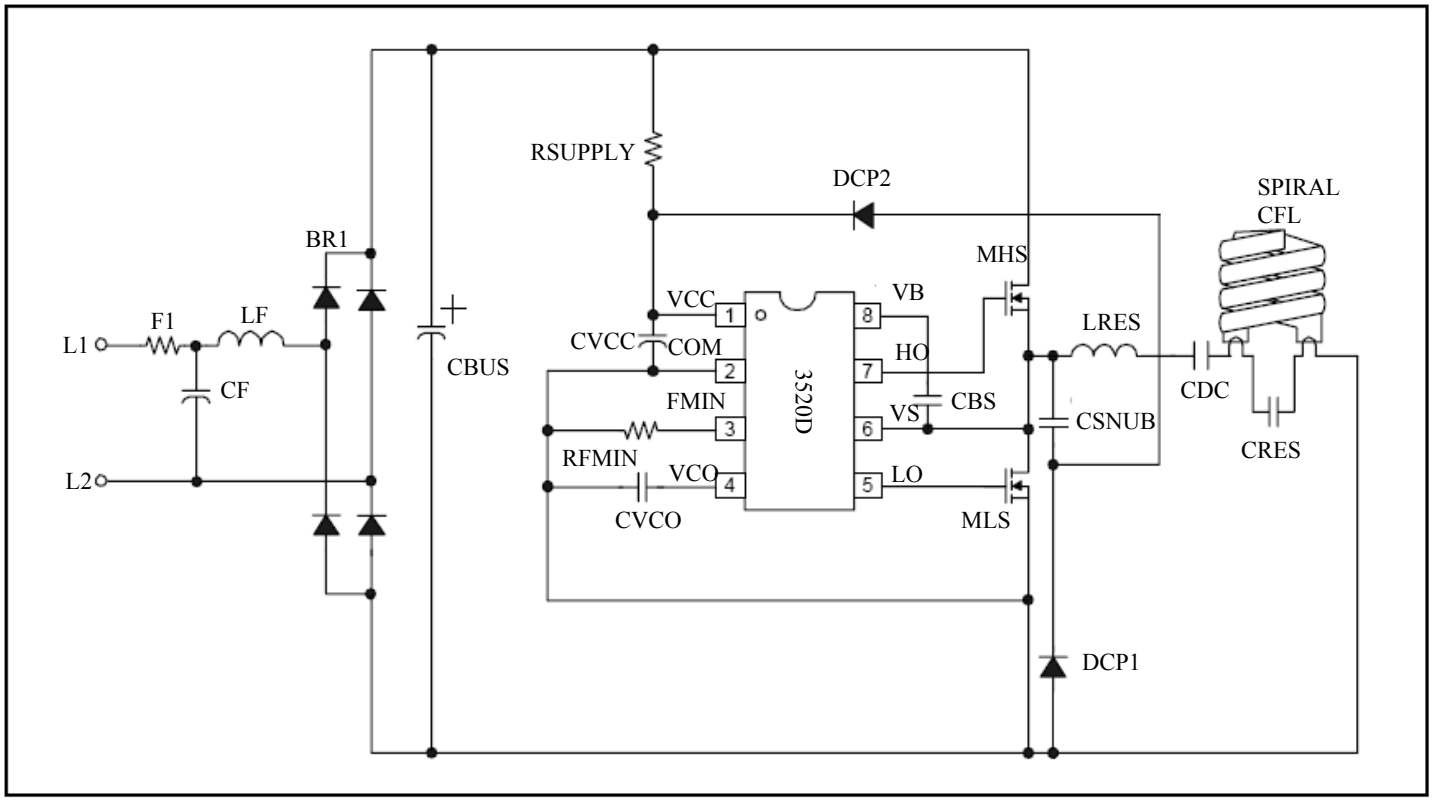
General Description

The 3520D(S) is a complete adaptive ballast controller and 600V half-bridge driver integrated into a single IC for fluorescent lighting applications. The IC includes adaptive zero-voltage switching (ZVS), internal crest factor over-current protection, as well as an integrated bootstrap FET. The heart of this IC is a voltage controlled oscillator with externally programmable minimum frequency. All of the necessary ballast features are integrated in a small 8-pin DIP or SOIC package.

Key Features

-600V Half Bridge Driver
-Integrated Bootstrap FET
-Adaptive zero-voltage switching (ZVS)
-Internal Crest Factor Over-Current Protection
-0 to 6VDC Voltage Controlled Oscillator
-Programmable minimum frequency
-Micropower Startup Current (80uA)
-Internal 15.6V zener clamp on Vcc
-Small DIP8/SO8 Package
-Also available LEAD-FREE (PbF)

Typical Application



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
I_{VCO}	Voltage controlled oscillator input current (Note 1)		-5	+ 5	mA
I_{CC}	Supply current (Note 2)		-25	25	mA
dV_S/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Package power dissipation @ T_A <=+25°C	8-Lead PDIP	—	1	W
	$PD=(T_{JMAX}-T_A)Rth_{JA}$	8-Lead SOIC	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	8-Lead PDIP	—	125	°C/W
		8-Lead SOIC	—	200	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: This IC contains a zener clamp structure between the chip VCO and COM, which has a nominal breakdown voltage of 6V. Please note that this pin should not be driven by a DC, low impedance power source greater than 6V.

Note 2: This IC contains a zener clamp structure between the chip VCC and COM, which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

Recommended Operating Conditions

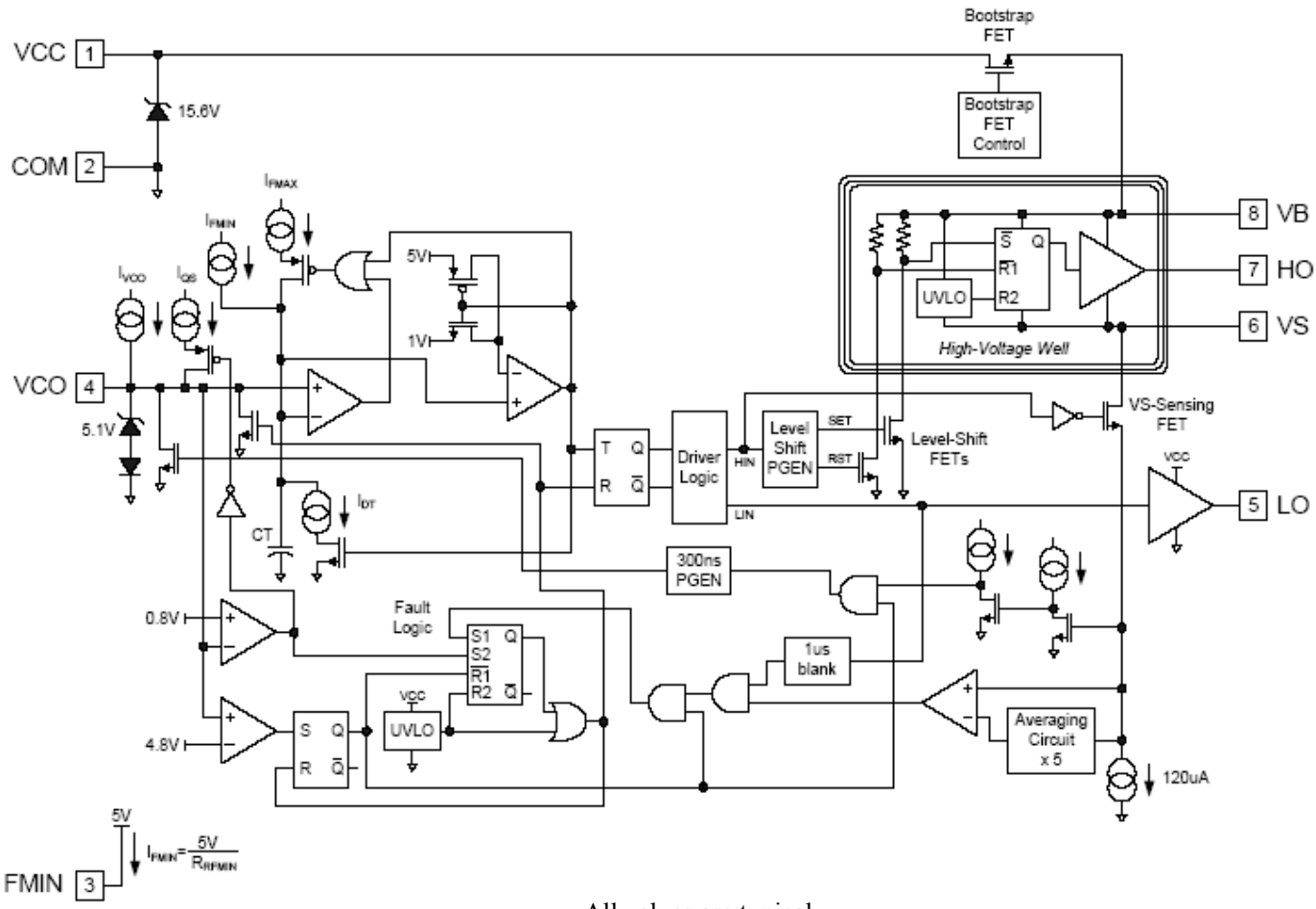
For proper operation the device should be used within the recommended conditions.

Symbol	**Definition**	**Min.**	**Max.**	**Units**
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	-1	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	Note 3	10	mA
R_{FMIN}	Minimum frequency setting resistance	20	140	kΩ
V_{VCO}	VCO pin voltage	0	5	V
T_J	Junction temperature	-25	125	℃

Note 3: Enough current should be supplied into the VCC pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage, VCLAMP.

ADAPTIVE BALLAST CONTROL IC

Block Diagram



All values are typical

Electrical Characteristic

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, CLO=CHO=1000pF, RFMIN = 82kΩ and TA = 25°C unless otherwise specified.

Electrical Characteristic (Continued)

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	11.4	12.6	13.8	V	V_{CC} rising from OV
V_{CCUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	9.0	10.0	11.0		
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	—	2.7	—		
I_{QCCUV}	UVLO quiescent current	—	45	80	μA	V_{CC} = 10V
I_{QCCFLT}	Fault mode quiescent current	—	100	—		
I_{CCHF}	V_{CC} supply current f=85KHz	—	4.5	—	mA	V_{VCO}=0V
I_{CCLF}	V_{CC} supply current f=35KHz	—	2.0	—		V_{VCO}=6V
V_{CLAMP}	V_{CC} Zener clamp voltage	14.4	15.4	—	V	I_{CC} = 10mA
Floating Supply Characteristics						
I_{QBS0}	Quiescent V_{BS} supply current	—	80	150	μA	V_{CC}=10V, V_{BS}=14V
I_{QBSUV}	Quiescent V_{BS} supply current	—	20	40		V_{CC}=10V, V_{BS}=7V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.7	9.0	10.3	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.8	8.0	9.2	V	
I_{LK}	Offset supply leakage current	—	—	50	μA	V_B = V_S = 600V
Oscillator I/O Characteristics						
$f_{(min)}$	Minimum oscillator frequency (Note 4)	29.6	34	38.2	kHz	V_{VCO}=6V
$f_{(max)}$	Maximum oscillator frequency (Note 4)	67	86	96		V_{VCO}=0V
D	Oscillator duty cycle	—	50	—	%	
DT_{LO}	LO output deadtime	—	2.0	—	μS	
DT_{HO}	HO output deadtime	—	2.0	—		
I_{VCOQS}	I_{VCO} quick start	—	50	—	μA	V_{VCO}=0V
I_{VCOFS}	I_{VCO} frequency sweep	0.8	1.3	1.7		V_{VCO}=2V
I_{VCO_5V}	I_{VCO} when VCO is at 5V	—	1.1	—		
V_{VCO_max}	Maximum VCO voltage	—	6	—	V	
Gate Dr iver Output Characteristics						
V_{LO}=LOW	LO output voltage when LO is low	—	COM	—		
V_{HO}=LOW	HO output voltage when HO is low	—	COM	—	mV	
V_{LO}=HIGH	LO output voltage when LO is high	—	VCC	—		
V_{HO}=HIGH	HO output voltage when HO is high	—	VCC	—		
T_{RISE}	Turn on rise time	—	150	230	nS	
T_{FALL}	Turn off fall time	—	75	120		
IO+	Output source short circuit pulsed current	—	140	—	mA	
IO-	Output sink short circuit pulse current	—	230	—	mA	

Note 4: Frequency shown is nominal for RFMIN=82kΩ. Frequency can be programmed higher or lower with the value of R_{FMIN}.

Electrical Characteristic (Continued)

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, C_{LO}=C_{HO}=1000pF, R_{FMIN} = 82kΩ and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Protection Characteristics						
V_{VCO_RUN}	VCO voltage when entering run mode	—	4.8	—	V	
CSCF	Crest factor peak-to-average fault factor	—	5.0	—	N/A	V_S offset = 0.5V
VS_ OFFSET_MAX	Maximum crest factor VS offset voltage	—	3.0	—	V	
V_{VCOSD}	VVCO shutdown voltage	0.74	0.82	0.91	V	
Minimum Frequency Setting Characteristics						
V_{FMIN}	FMIN lead voltage during normal operation	4.8	5.1	5.4	V	
$V_{FMINFLT}$	FMIN lead voltage during fault mode	—	0	—	V	
Bootstrap FET						
IBS1	VB current	30	70	—	mA	C_{BS}=0.1uF, V_S=0V
IBS2	VB current	10	20	—		VBS = 10V

Under-voltage Lock-Out Mode

The under-voltage lock-out mode (UVLO) is defined as the state the 3520D is in when VCC is below the turn-on threshold of the IC. The 3520D UVLO is designed to maintain an ultra-low supply current (IQCCUV<80uA), and to guarantee that the 3520D is fully functional before the high- and low-side output gate drivers are activated. The VCC capacitor, CVCC, is charged by current through supply resistor, RSUPPLY, minus the start-up current drawn by the 3520D (Figure 1). This resistor is chosen to provide sufficient current to supply the 3520Dfrom the DC bus. Once the capacitor voltage on VCC reaches the start-up threshold, VCCUV+, the 3520D turns on and HO and LO start oscillating. Capacitor CVCC should be large enough to hold the voltage at VCC above the VCCUV+ threshold for one half-cycle of the line voltage or until the external auxiliary supply can maintain the required supply voltage and current to the IC.

Electrical Characteristic (Continued)

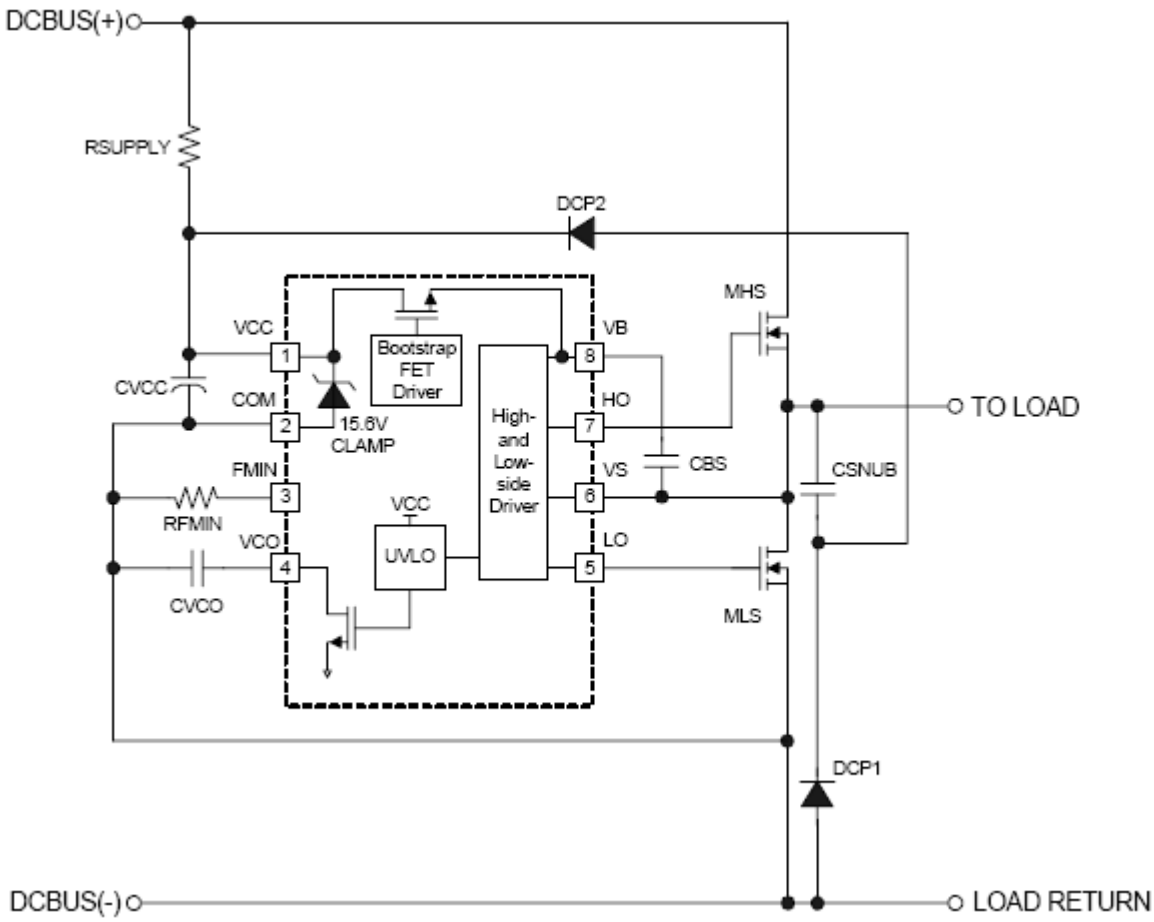


Fig. 1 Start-up circuitry

An internal bootstrap MOSFET between VCC and VB and external supply capacitor, CBS, determine the supply voltage for the high-side driver circuitry. An external charge pump circuit consisting of capacitor CSNUB and diodes DCP1 and DCP2, comprises the auxiliary supply voltage for the low-side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. LO may oscillate several times until VB-VS exceeds the high-side UVLO rising threshold, VBSUV+ (9 Volts), and the high-side driver is enabled. During UVLO mode, the high- and low-side gate driver outputs, HO and LO, are both low and pin VCO is pulled down to COM for resetting the starting frequency to the maximum.

Frequency Sweep Mode

When VCC exceeds VCCUV+ threshold, the 3520D enters frequency sweep mode. An internal current source (Figure2) charges the external capacitor on pin VCO, CVCO, and the voltage on pin VCO starts ramping up linearly. An additional quick-start current (IVCOQS) is also connected to the VCO pin and charges the VCO pin initially to 0.85V. When the VCO voltage exceeds 0.85V, the quick-start current is then disconnected internally and the VCO voltage continues to charge up with the normal frequency sweep current source (IVCOFS) (Figure 3). This quick-start brings the VCO voltage quickly to the internal range of the VCO.

Electrical Characteristic (Continued)

The frequency ramps down towards the resonance frequency of the high-Q ballast output stage causing the lamp voltage and load current to increase. The voltage on pin VCO continues to increase and the frequency keeps decreasing until the lamp ignites. If the lamp ignites successfully, the voltage on pin VCO continues to increase until it internally limits at 6V (V_{VCO_MAX}). The frequency stops decreasing and stays at the minimum frequency as programmed by an external resistor, RFMIN, on pin FMIN. The minimum frequency should be set below the high-Q resonance frequency of the ballast output stage to ensure that the frequency ramps through resonance for lamp ignition (Figure 4). The desired preheat time can be set by adjusting the slope of the VCO ramp with the external capacitor CVCO

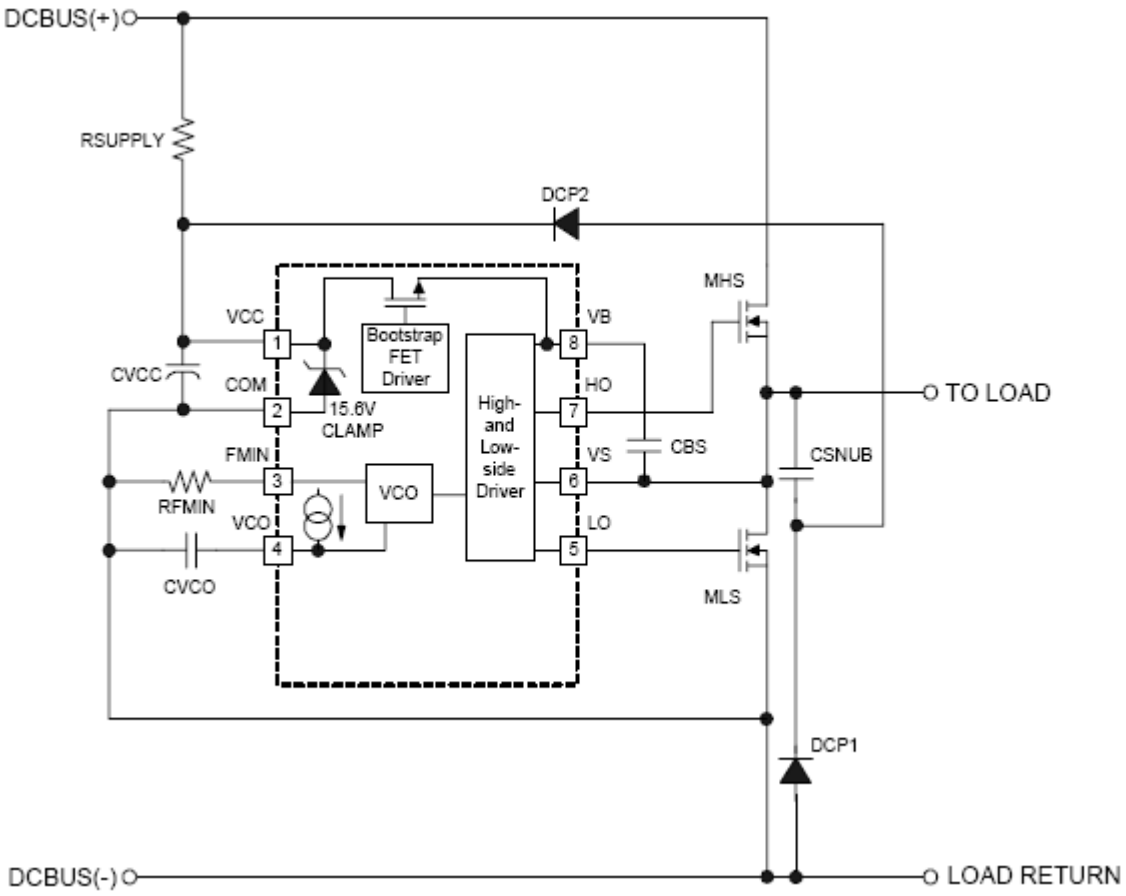


Fig. 2 Frequency sweep circuitry mode circuitry

Electrical Characteristic (Continued)

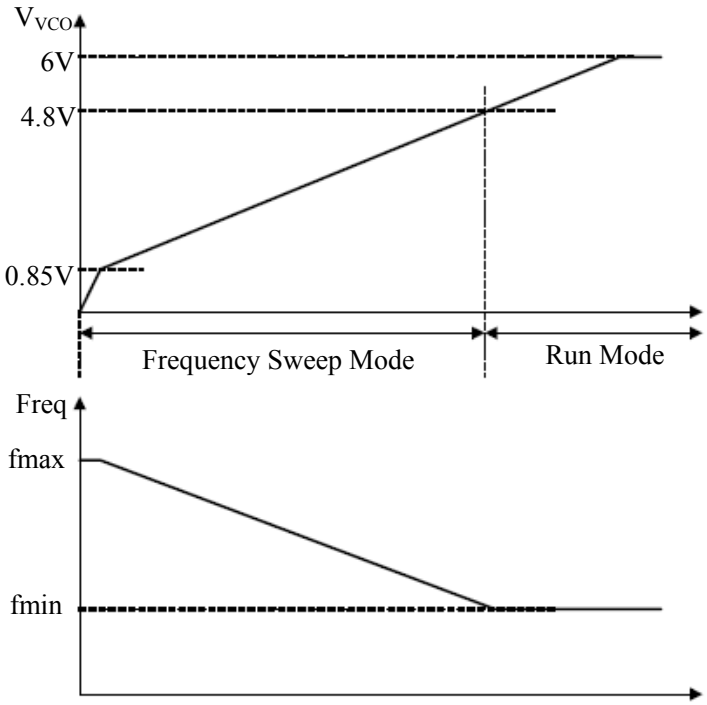


Fig. 3 3520D Frequency sweep mode timing diagram.

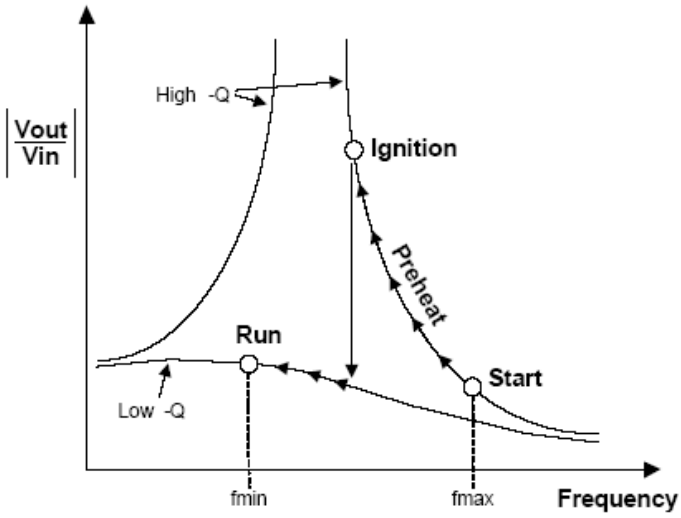


Fig. 4 Resonant tank Bode plot with lamp operating points.

Run Mode

The 3520D enters RUN mode when the voltage on pin VCO exceeds 4.8V (**VVCO_RUN**). The lamp has ignited and the ballast output stage becomes a low-Q, series-L, parallel- RC circuit. Also, the VS sensing and fault logic blocks (Figure 5) both become enabled for protection against non- ZVS and over-current fault conditions. The voltage on the VCO pin continues to increase and the frequency deceases further until the VCO pin voltage limits at 6V (VVCO_MAX) and the minimum frequency is reached. The resonant inductor, resonant capacitor, DC bus voltage and minimum frequency determine the running lamp power. The IC stays at this minimum frequency unless non-ZVS occurs at the VS pin, a crest factor over-current condition is detected at the VS pin, or VCC decreases below the UVLO- threshold (see State Diagram).

Electrical Characteristic (Continued)

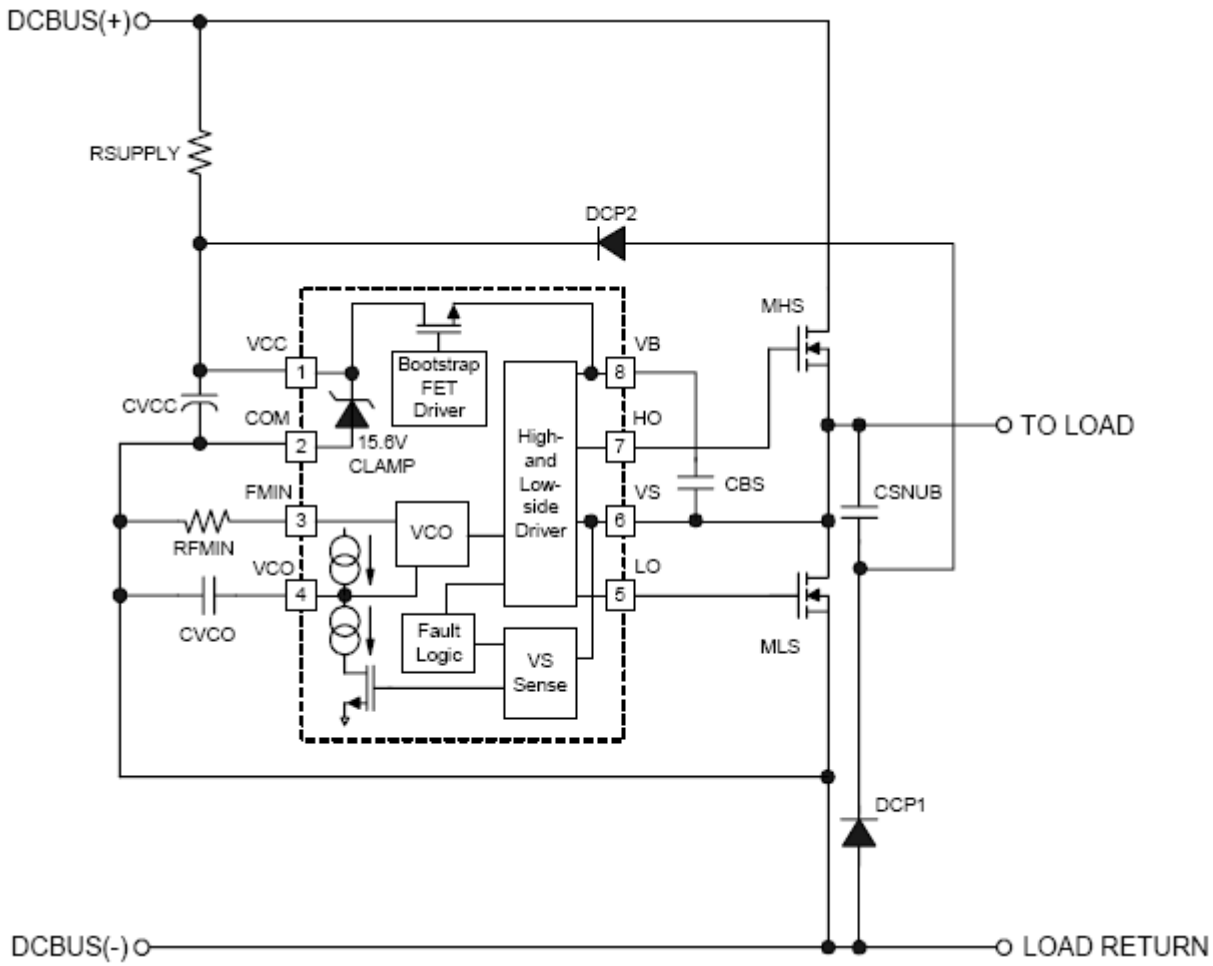


Fig. 5 3520D Run mode circuitry.

Non Zero-Voltage Switching (ZVS) Protection

During run mode, if the voltage at the VS pin has not slewed entirely to COM during the dead-time such that there is voltage between the drain and source of the external lowside half-bridge MOSFET when LO turns-on, then the system is operating too close to, or, on the capacitive side of, resonance. The result is non-ZVS capacitive-mode switching that causes high peak currents to flow in the half-bridge MOSFETs that can damage or destroy them(Figure 6). This can occur due to a lamp filament failure(s), lamp removal (open circuit), a dropping DC bus during a mains brown-out or mains interrupt, lamp variations over time, or component variations. To protect against this, an internal high-voltage MOSFET is turned on at the turn-off of HO and the VS-sensing circuit measures VS at each rising edge of LO. If the VS voltage is non-zero, a pulse of current is sinked from the VCO pin (Figures 5 and 6) to slightly discharge the external capacitor, CVCO, causing the frequency to increase slightly. The VCO capacitor then charges up during the rest of the cycle slowly due to the internal current source.

Electrical Characteristic (Continued)

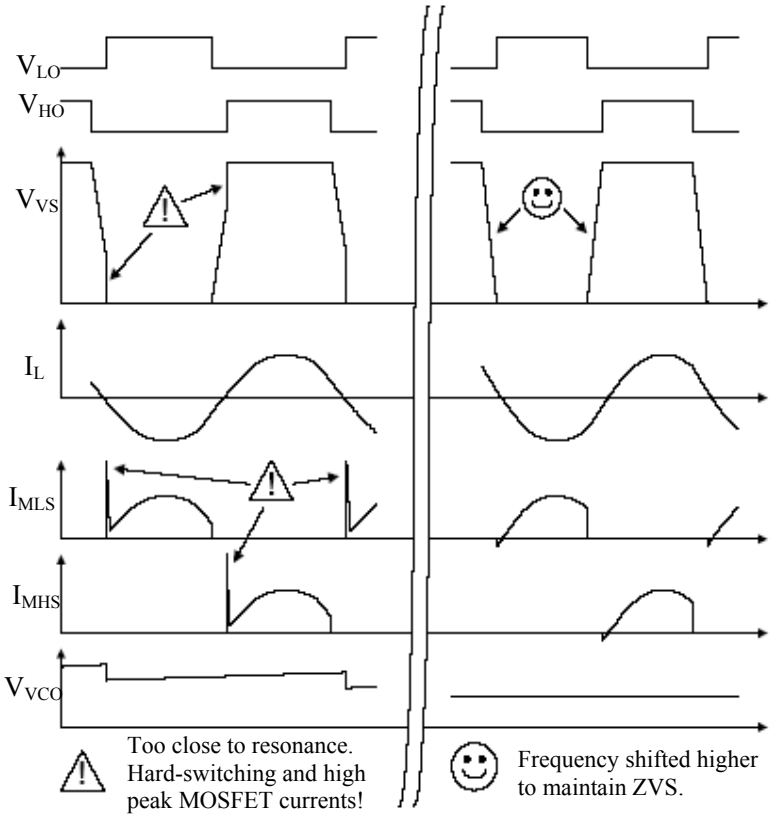


Fig. 6 3520D non-ZVS protection timing diagram.

The frequency is trying to decrease towards resonance by charging the VCO capacitor and the adaptive ZVS circuit "nudges" the frequency back up slightly above resonance each time non-ZVS is detected at the turn-on of LO.

The internal high-voltage MOSFET is then turned off at the turn-off of LO and it withstands the high-voltage when VS slews up to the DC bus potential. The circuit then remains in this closed-loop adaptive ZVS mode during running and maintains ZVS operation with changing line conditions, component tolerance variations and lamp/load variations. During a lamp removal or filament failure, the lamp resonant tank will be interrupted causing the half-bridge output to goopen circuit (Figure 7). This will cause capacitive switching (hard-switching) resulting in high peak MOSFET currents that can damage them. The 3520D will increase the frequency in attempt to satisfy ZVS until the VCO pin decreases below 0.82V (VVCOSD). The IC will enter Fault Mode and latch the LO and HO gate driver outputs 'low' for turning the half-bridge off safely before any damage can occur to the MOSFETs.

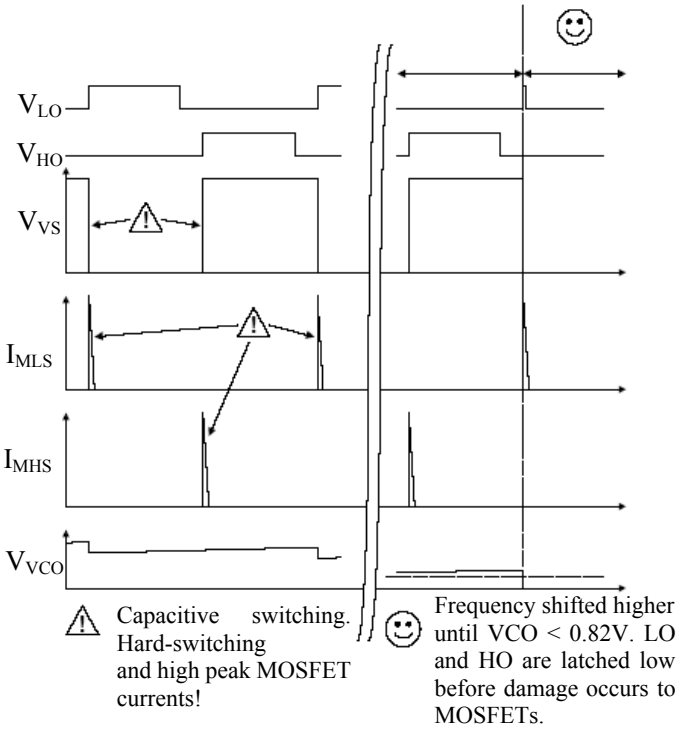


Fig. 7 Lamp removal or open filament fault condition timing diagram

During normal lamp ignition, the frequency sweeps through resonance and the output voltage increases across the resonant capacitor and lamp until the lamp ignites. If the lamp fails to ignite, the resonant capacitor voltage, the inductor voltage and inductor current will continue to increase until the inductor saturates or the output voltage exceeds the maximum voltage rating of the resonant capacitor or inductor.

The ballast must shutdown before damage occurs.

Electrical Characteristic (Continued)

To protect against a lamp non-strike fault condition, the 3520D uses the VS-sensing circuitry (Figure 5) to also measure the low-side half-bridge MOSFET current for detecting an over-current fault. By using the RDSon of the external lowside MOSFET for current sensing and the VS-sensing circuitry, the 3520D eliminates the need for an additional current sensing resistor, filter and current-sensing pin. To cancel changes in the RDSon value due to temperature and MOSFET variations, the 3520D performs a crest factor measurement that detects when the peak current exceeds the average current by a factor of 5 (CSCF). Measuring the crest factor is ideal for detecting when the inductor saturates due to excessive current that occurs in the resonant tank when the frequency sweeps through resonance and the lamp does not ignite. When the VCO voltage ramps up for the first time from zero, the resonant tank current and voltages increase as the frequency decreases towards resonance (Figure 8). If the lamp does not ignite, the inductor current will eventually saturate but the crest factor fault protection is not active until the VCO voltage exceeds 4.8V (VVCO_RUN) for the first time. The frequency will continue decreasing to the capacitive side of resonance towards the minimum frequency setting and the resonant tank current and voltages will decrease again. When the VCO voltage exceeds 4.8V (VVCO_RUN), the IC enters Run Mode and the non-ZVS protection and crest factor protection are both enabled. The non-ZVS protection will increase the frequency again cycle-by-cycle towards resonance from the capacitive side. The resonant tank current will increase again as the frequency nears resonance until the inductor saturates again.The crest factor protection is now enabled and measures the instantaneous voltage at the VS pin only during the time when LO is ‘high’ and after an initial 1us blank time from the rising edge of LO.

The blank time is necessary to prevent the crest factor protection circuit from reacting to a non- ZVS condition. An internal averaging circuit averages the instantaneous voltage at the VS pin over 10 to 20 switching cycles of LO. During Run Mode, the first time the inductor saturates when LO is ‘high’ (after the 1us blank time) and the peak current exceeds the average by 5 (CSCF), the 3520D will enter Fault Mode and both LO and HO outputs will be latched ‘low’. The half-bridge will be safely disabled before any damage can occur to the ballast components.

The crest factor peak-to-average fault factor varies as a function of the internal average (Figure 20). The maximum internal average should be below 3.0 volts. Should the average exceed this amount, the multiplied average voltage can exceed the maximum limit of the VS sensing circuit and the VS sensing circuit will no longer detect crest factorfaults. This can occur when a half-bridge MOSFET is selected that has an RDSon that is too large for the application causing the internal average to exceed the maximum limit.

FAULT MODE

During Run Mode, should the VCO voltage decrease below 0.82V (VVCOSD) or a crest factor fault occur, the 3520D will enter Fault Mode (see State Diagram). The LO and HO gate driver outputs are both latched ‘low’ so that the halfbridge is disabled. The VCO pin is pulled low to COM and the FMIN pin decreases from 5V to COM. VCC draws micro-power current (ICCFLT) so that VCC stays at the clamp voltage and the IC remains in Fault Mode without the need for the charge-pump auxiliary supply. To exit Fault Mode and return to Frequency Sweep Mode, VCC must be cycled below the UVLO- threshold and back above the UVLO+ threshold.

Electrical Characteristic (Continued)

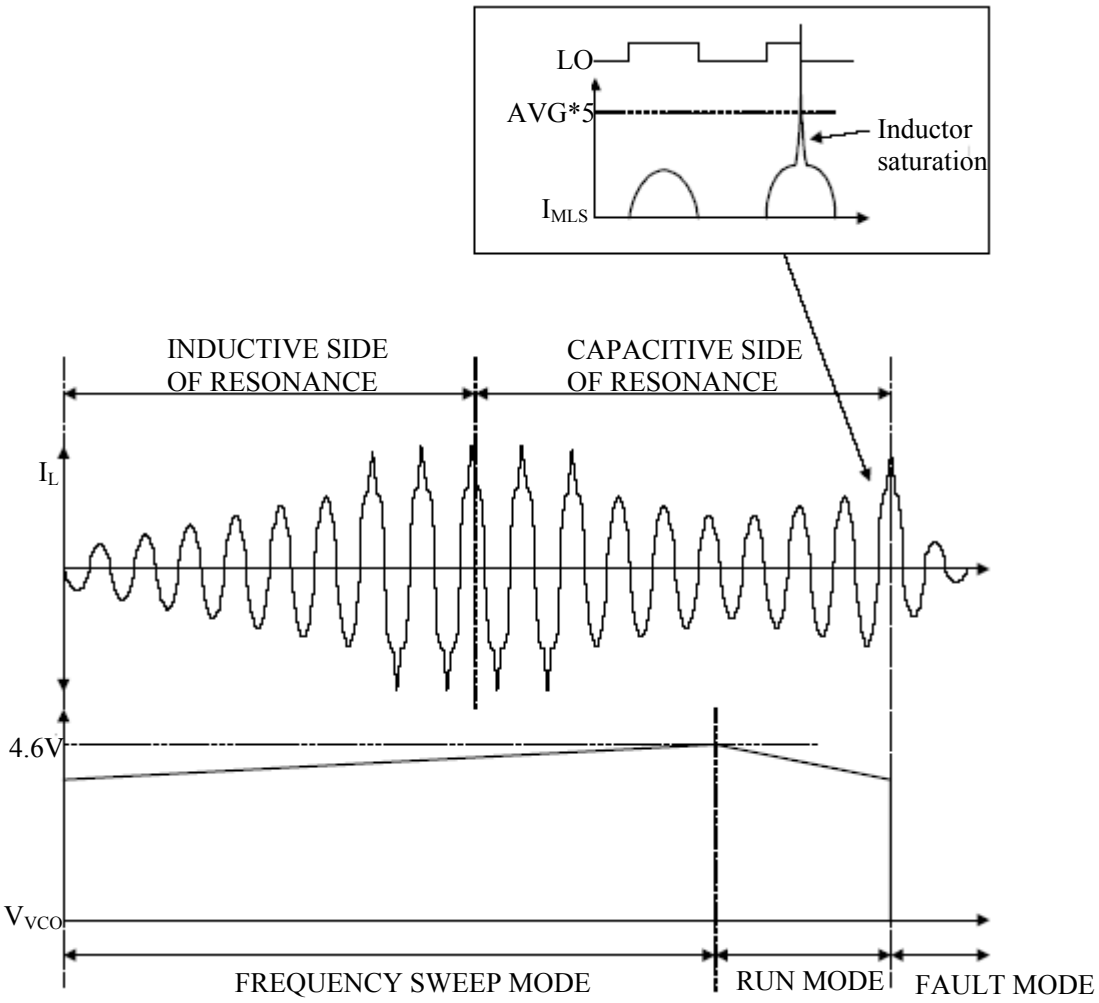
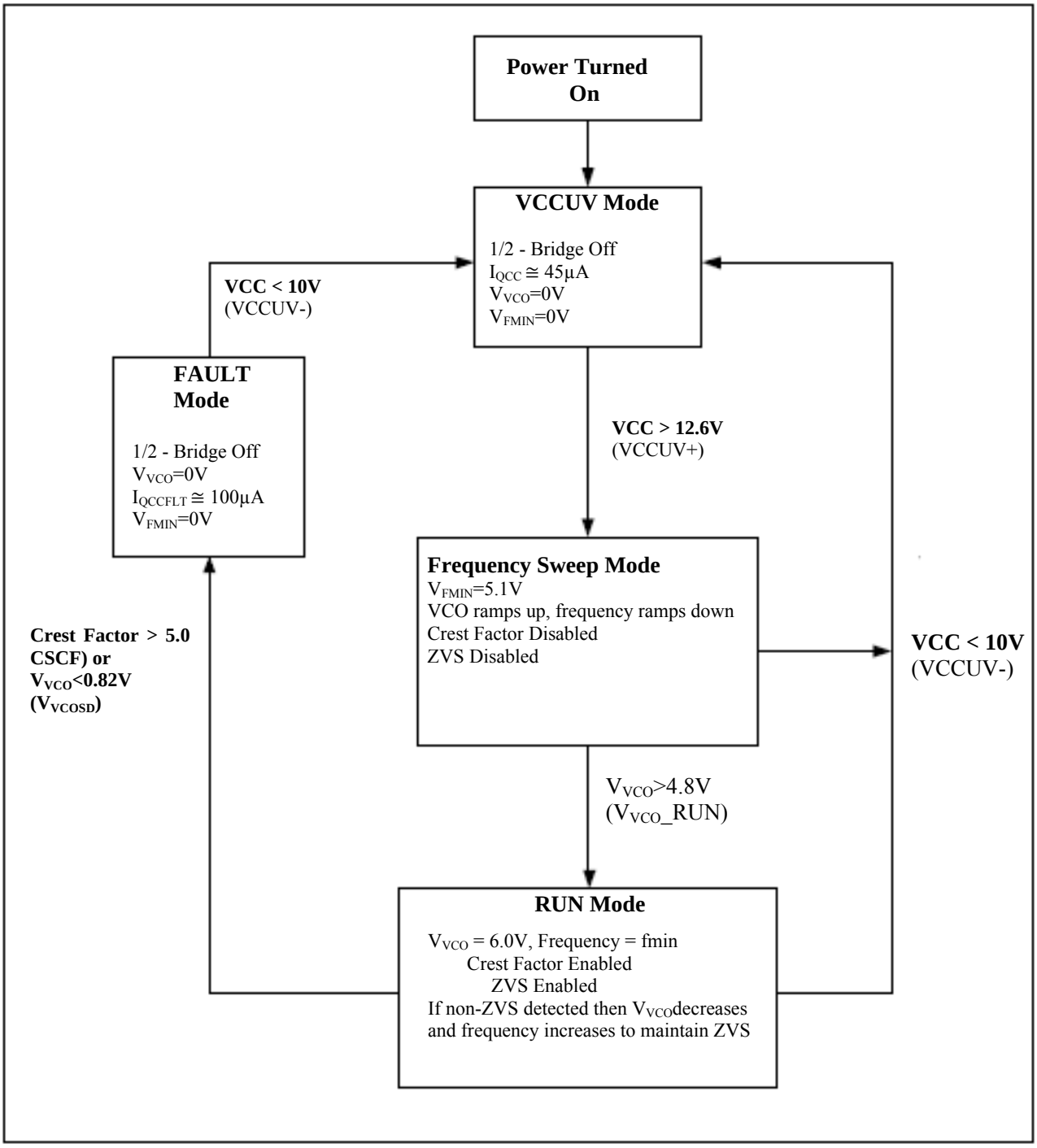


Fig. 8 Crest factor protection timing diagram

State Diagram



Typical Performance Characteristics

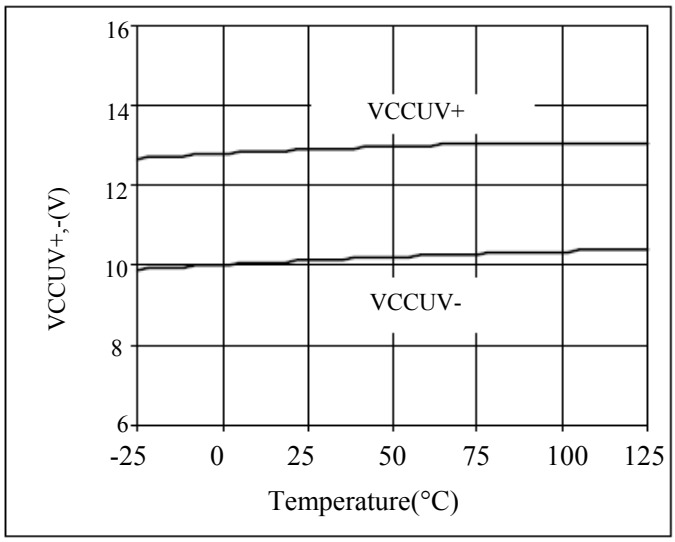


Fig. 9 VCCUV+/- vs TEMP

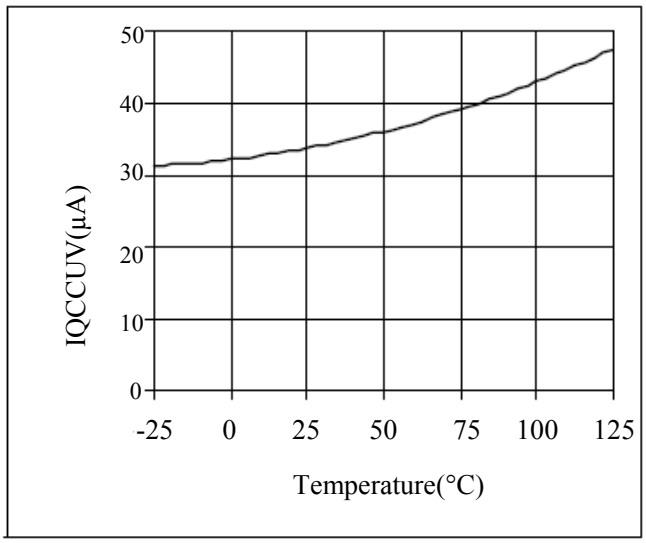


Fig. 10 IQCCUV vs TEMP
VCC=10V, VCO=0V

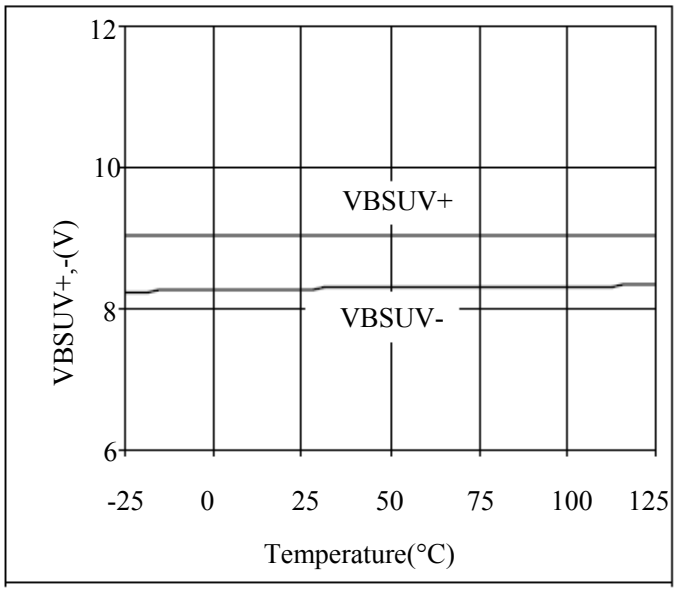


Fig. 11 VBSUV+/- vs TEMP

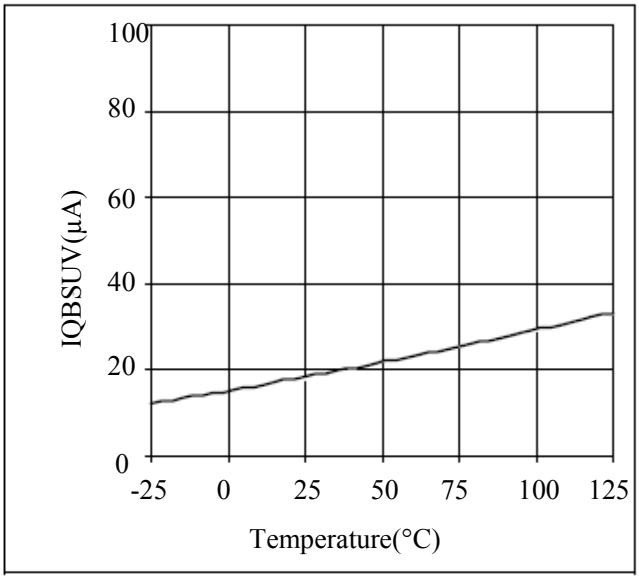


Fig. 12 IQBSUV vs TEMP

Typical Performance Characteristics

(Continued)

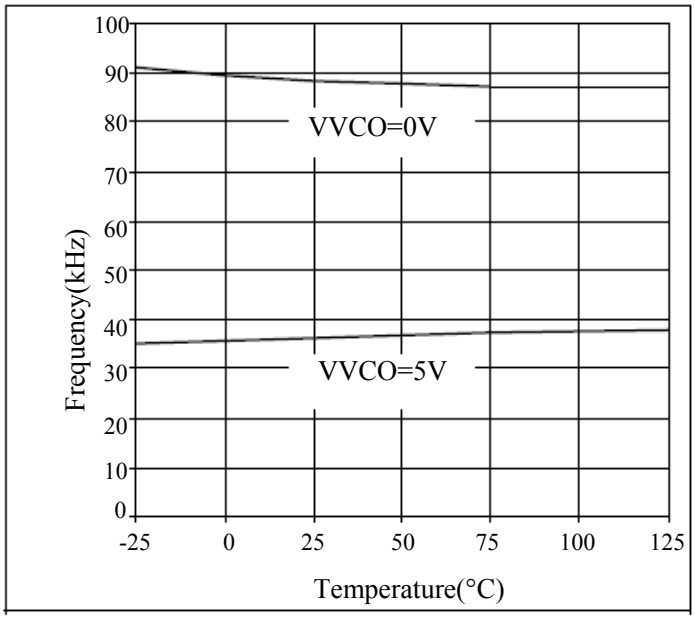


Fig. 13 Frequency vs TEMP
REMIN=82K

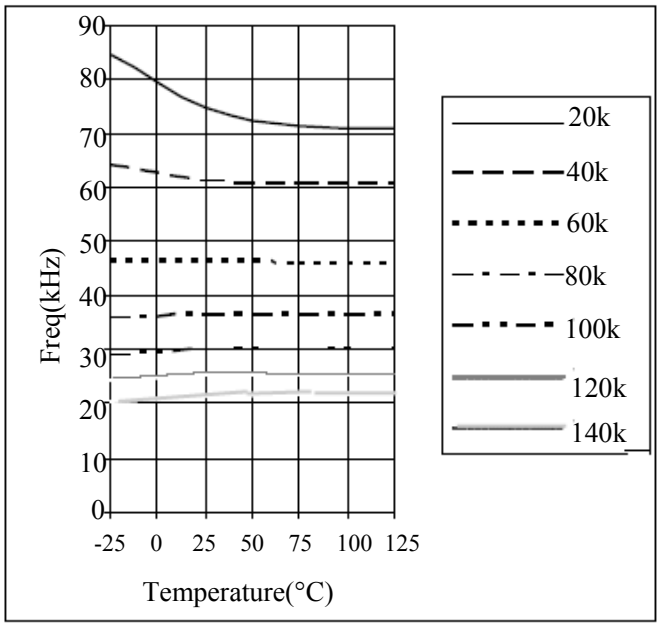


Fig. 14 Frequency vs RFMIN vs TEMP
VVCO=6V

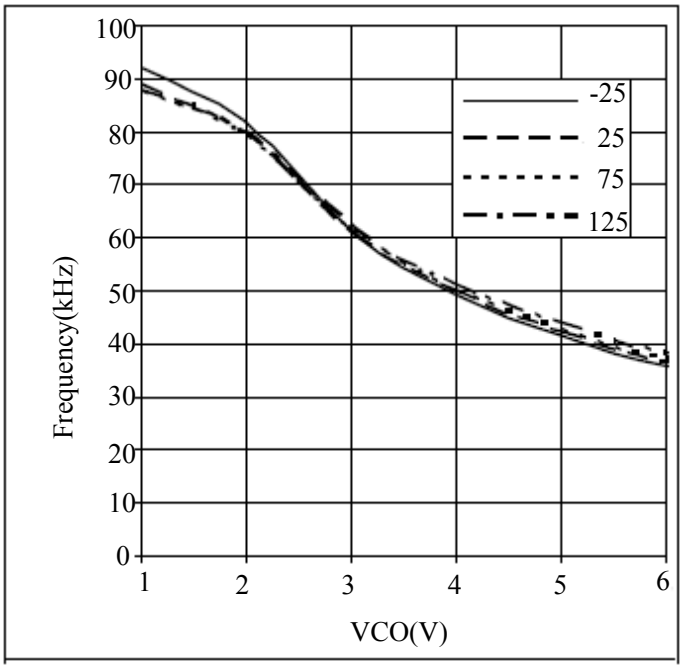


Fig. 15 FREQ VS VVCO vs TEMP
VCC=14V

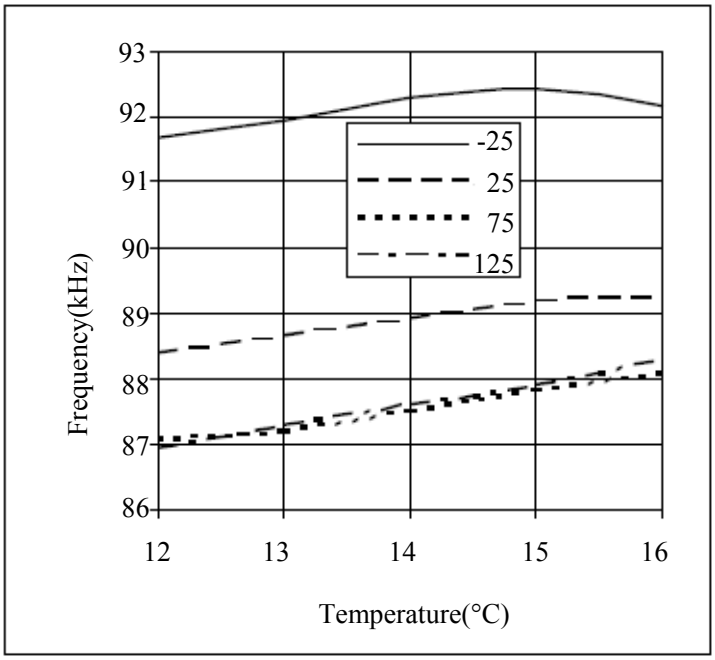


Fig. 16 FREQ VS VCC vs TEMP
VVCO=0V

Typical Performance Characteristics

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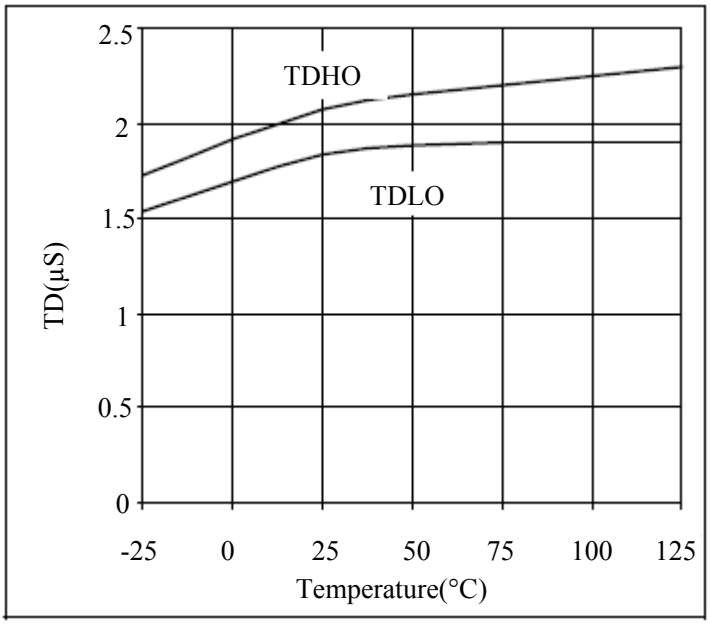


Fig. 17 DTHO, DTLO vs TEMP
VCO=0V

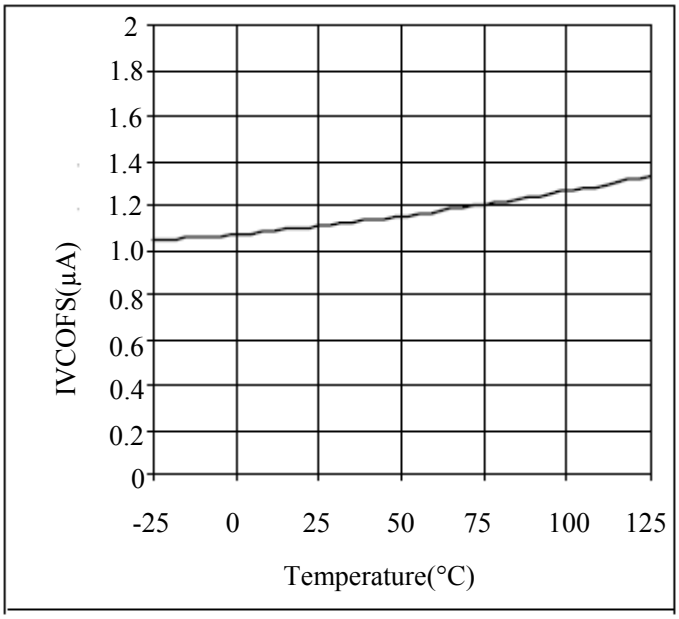


Fig. 18 IVCO_FS vs TEMP

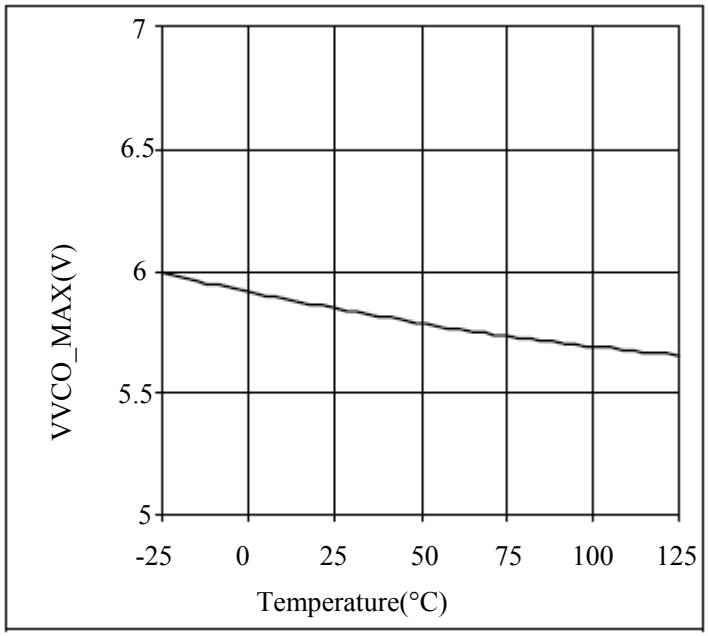


Fig. 19 VVCOMAX vs TEMP

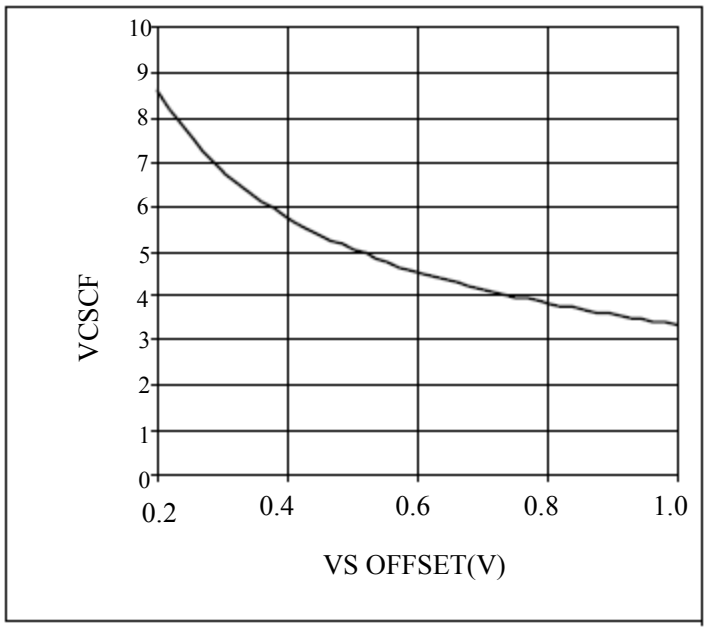


Fig. 20 CSCF vs OFFSET

Typical Performance Characteristics (Continued)

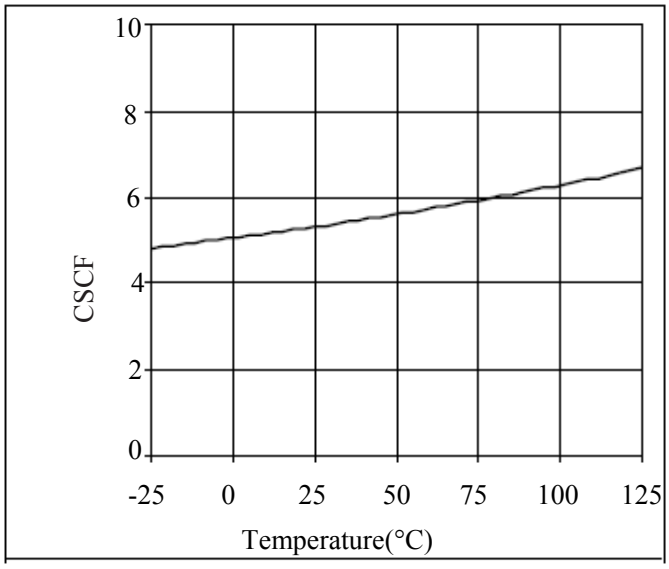


Fig. 21 CSCF vs TEMP
VS_OFFSET=0.5V

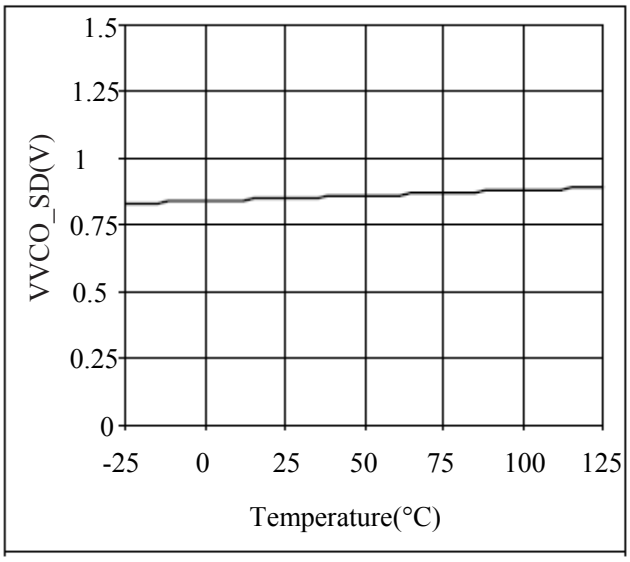


Fig. 22 VVCO_SD vs TEMP

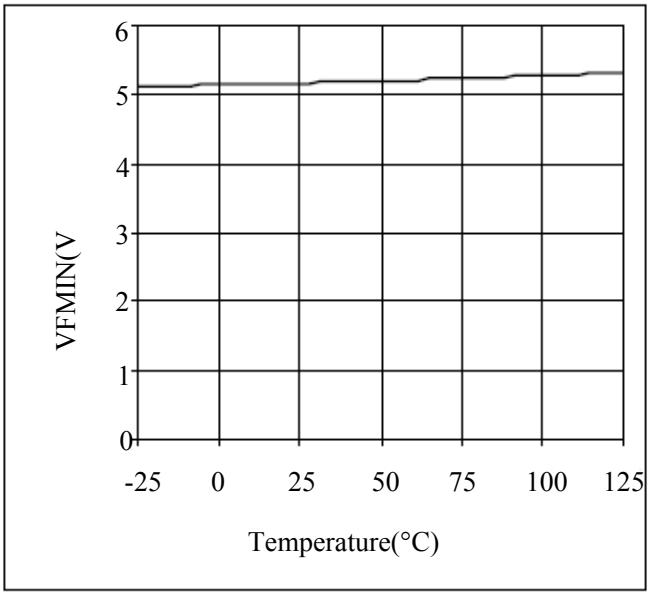


Fig. 23 VFMIN vs TEMP
VCO=0V, RFMIN=82K

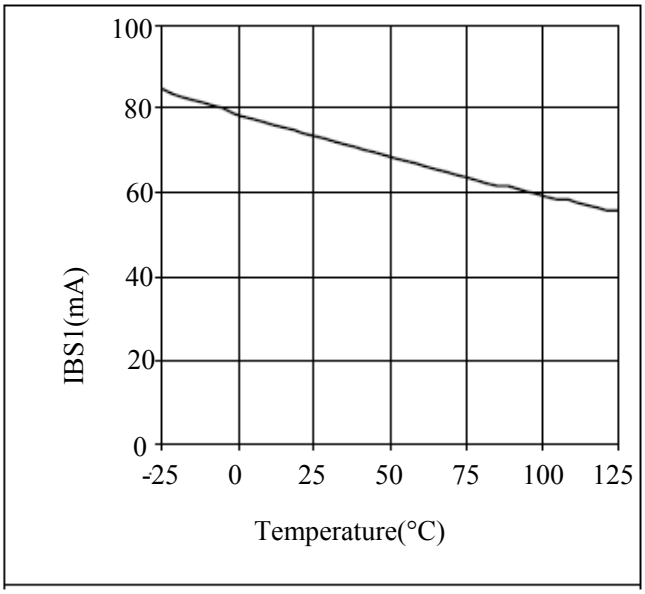


Fig. 24 IBS1 vs TEMP

Typical Performance Characteristics (Continued)

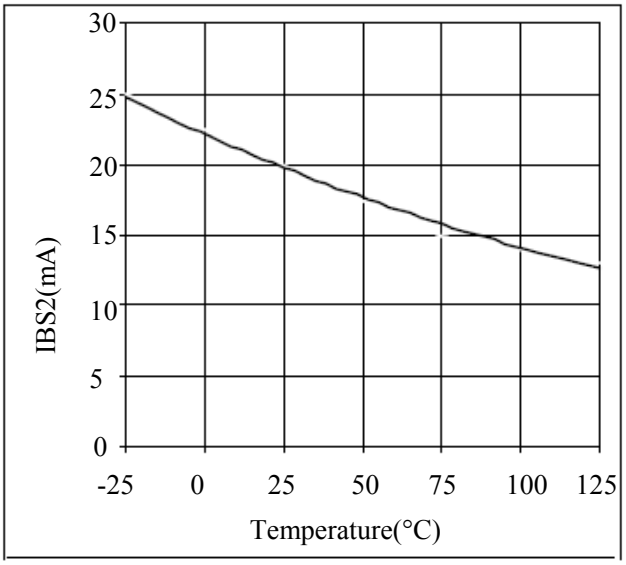
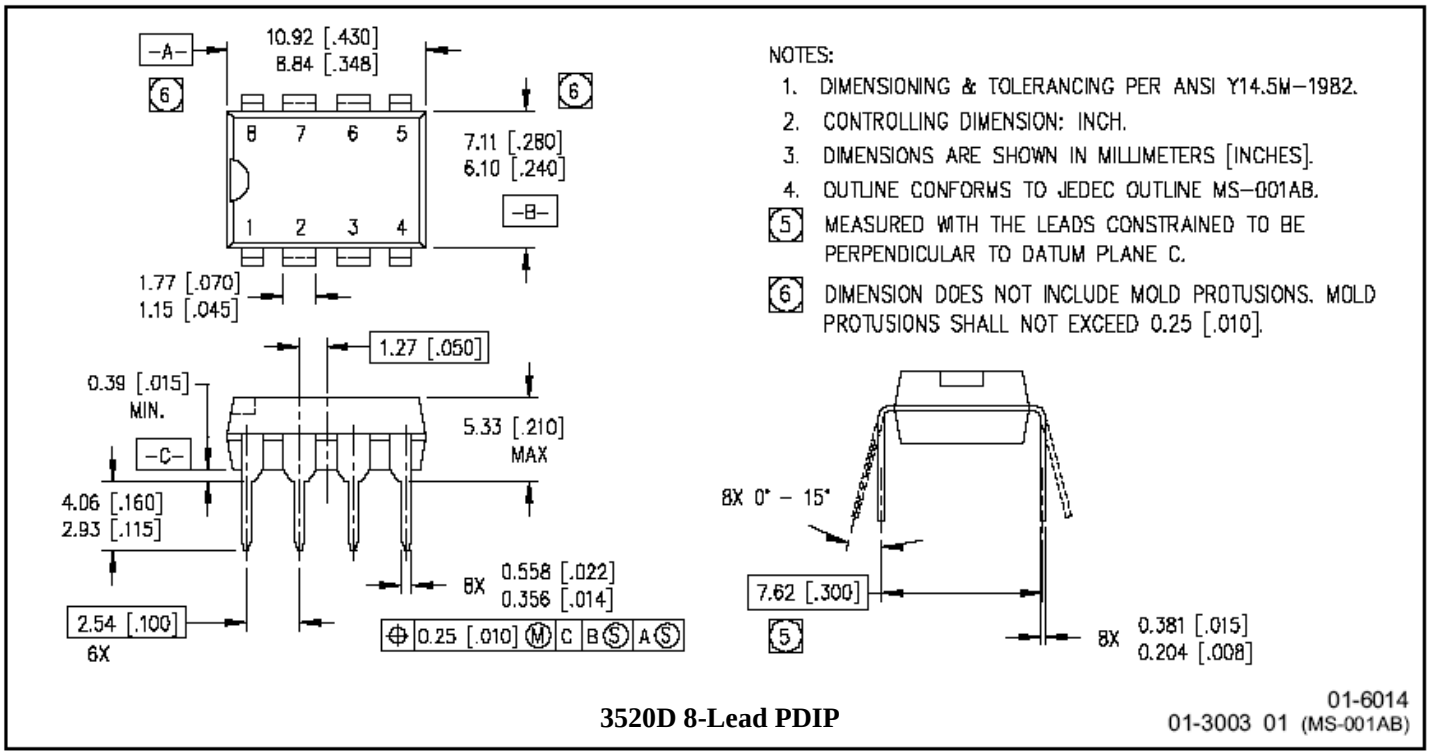


Fig. 25 IBS2 vs TEMP

Mechanical Dimensions

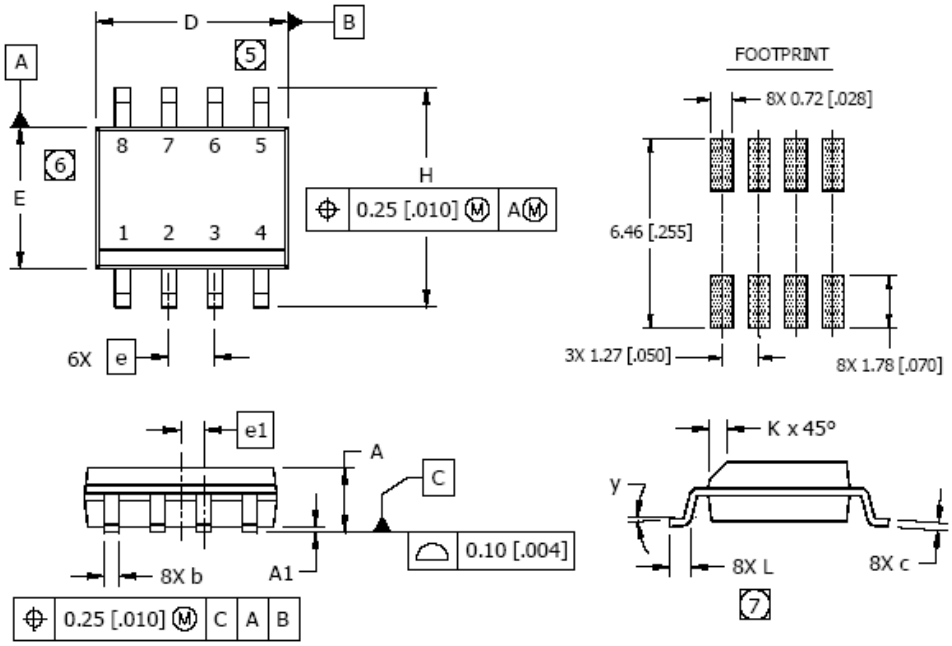


3520D 8-Lead PDIP

ADAPTIVE BALLAST CONTROL IC

Mechanical Dimensions

(Continued)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

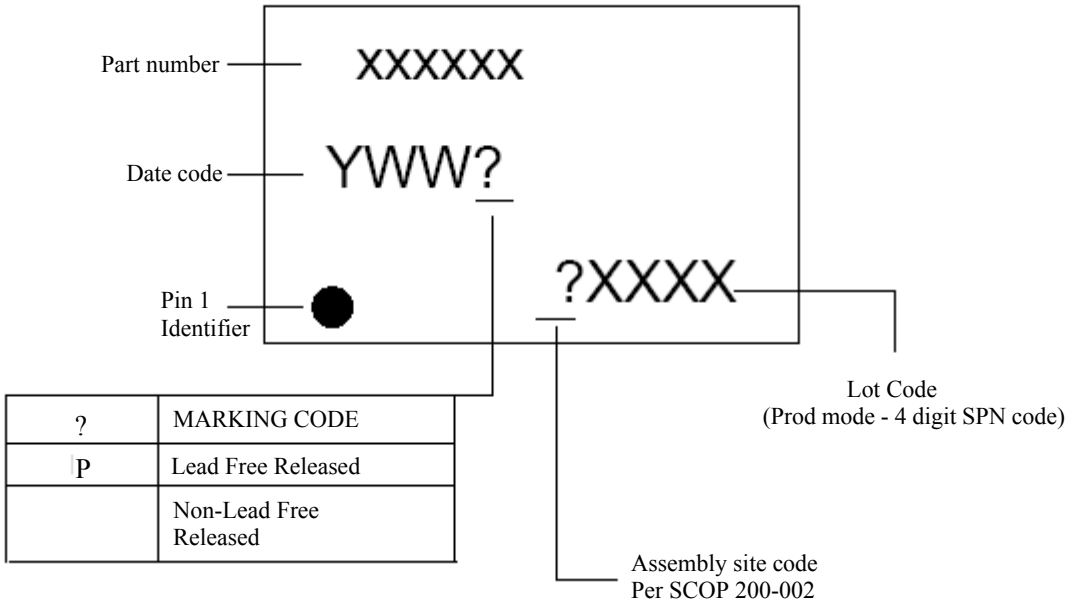
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

3520DS 8-Lead SOIC

Leadfree part marking information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP 3520D order 3520D

8-Lead SOIC 3520DS order 3520DS

Leadfree Part

8-Lead PDIP 3520D order 3520DPbF

8-Lead SOIC 3520DS order 3520DSPbF