AND8394/D

A 48 V, 2 A High Efficiency, Single Stage, Isolated Power Factor Corrected Power Supply for LED Drivers and Telecom Power

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Introduction

This application note describes a relatively novel and simple way to produce an off−line, power factor corrected 15 Vdc and higher output power supply using an isolated, single stage conversion topology. The power topology is essentially a buck−boost derived flyback converter operating in continuous conduction mode (CCM) and utilizing ON Semiconductor's NCP1652A controller which was designed specifically for this implementation. The power supply described in this application note is a 48 Vdc, 2 A supply with universal AC input and is intended for general purpose supplies, telecom distributed power "front−ends" and constant voltage LED drivers such as those used in area lighting and distributed lighting applications such as refrigerator case lighting and cove lighting. Efficiencies approaching 90% were achieved with a power factor exceeding 0.95 for most typical loads. The supply includes overcurrent protection, overvoltage protection, brownout detection, and an input EMI filter.

Background

Applications that require an isolated, regulated output voltage along with input power factor correction typically involve a two stage conversion process as depicted in Figure 1. This scheme is composed of an input boost power factor corrector stage which converts and pre−regulates the input line into a 400 Vdc bus. This bus then provides the voltage for a conventional dc−to−dc converter which can be of any appropriate topology. For lower power applications of 150 W and less, this is usually a flyback converter.

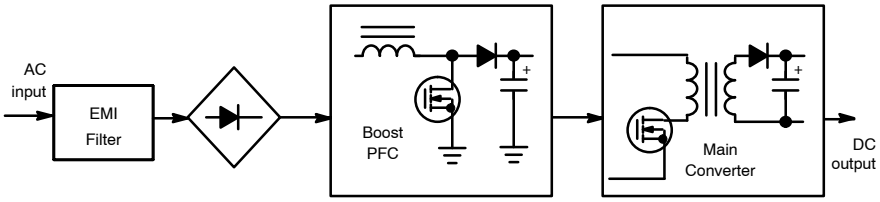

Figure 1. Conventional 2−Stage Conversion

With a few minor performance compromises, a simpler technique can be used in which the power factor and main converter sections are combined into one conversion stage. This has significant advantages as it eliminates the need for the bulky boost inductor, High Voltage MOSFET, power rectifier and bulk capacitor. This is illustrated in Figure 2.

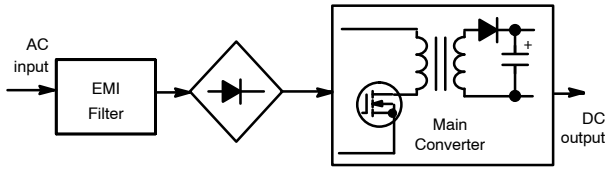

Figure 2. Single Stage Conversion with NCP1652A

The difference here is that the flyback conversion stage not only handles the voltage regulation and input to output isolation functions, but provides power factor correction as well. The circuit essentially functions as a conventional PFC converter with the output being derived from a secondary winding on what would be the boost choke in the "normal" type of non−isolated PFC circuit. The dc input to the converter is a 100/120 Hz haversine instead of a pure dc voltage because the normal input "bulk" capacitor following the bridge rectifier is reduced to a value of a microfarad or less. The full schematic of the single stage converter is shown in Figure 3.

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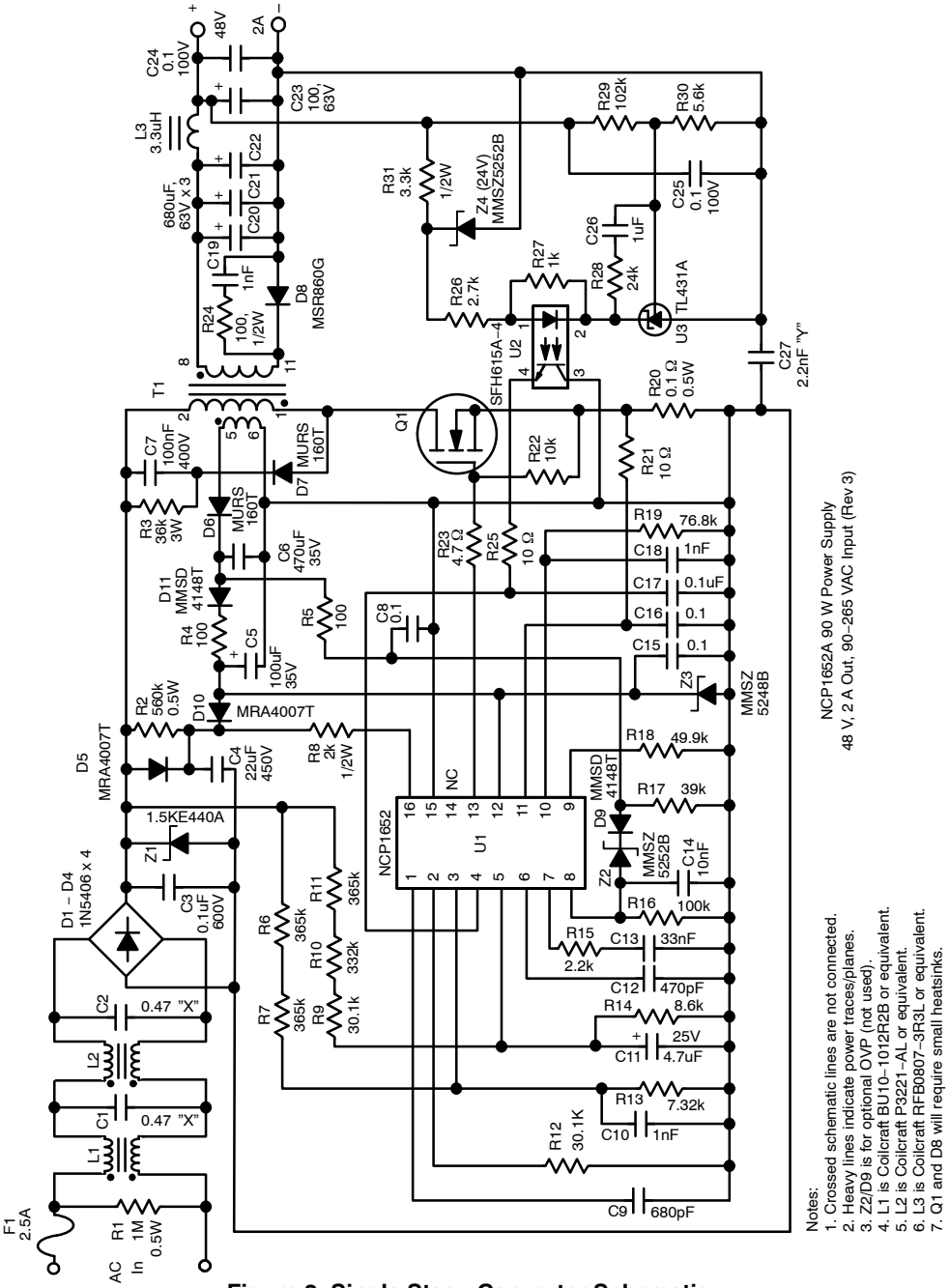


Figure 3. Single Stage Converter Schematic

Single Stage Converter Characteristics

The single stage, isolated PFC converter can be derived from a conventional buck−boost flyback topology. The operational mode can be in discontinuous conduction mode (DCM), critical conduction mode (CRM), or continuous mode (CCM). While the most common operational mode for lower power circuits is CRM, CCM offers significant advantages for applications that require fixed frequency operation with output voltages of 15 V dc or higher where the use of synchronous rectification yields marginal efficiency improvements. In CCM, the peak MOSFET current can be significantly less than in CRM resulting in lower switching losses, particularly at power levels above 50 watts. CCM also reduces the high frequency output capacitor ripple current thus improving the overall power supply reliability. The NCP1652A controller is designed particularly for CCM operation and also provides a second gate drive output for the implementation of an active clamp snubber for higher power applications where voltage spikes caused by the flyback transformer's leakage inductance energy can become a significant issue. The 48 V, 2 A adapter circuit of Figure 3 achieved an average efficiency approaching 90% for typical operation loads. The flyback transformer T1 was designed to effectively operate in "deep" CCM with a relatively low magnetizing current component (see Figure 8 for the transformer design details).

This resulted in significantly reduced switching losses in MOSFET Q1 over a similar CRM based design.

The single stage PFC conversion process, regardless of the operational mode, has several compromises over the traditional 2−stage conversion scheme of Figure 1. They are as follows:

- As with any power factor corrector circuit, the gain bandwidth of the control loop is very low, typically in the 10 Hz to 30 Hz range. This is necessary, otherwise the control loop would attempt to regulate off the 100/120 Hz line variations of the input and this would result in a very poor power factor. As a consequence of the low bandwidth, transient response to load step changes will be poor although dc regulation will be excellent. For most applications where point−of−load regulation (POL) is utilized and/or the load is constant (e.g. LED load), the slow transient response is inconsequential. Figure 7 shows the output voltage profile at supply turn−on with no load and with full load indicating a controlled voltage rise with no overshoot that is sometimes typical with slow control loops.
- Because the loop cannot regulate away the 100/120 Hz line ripple, it will appear as a ripple component on the output. For this circuit, the output ripple was in the order of $\pm 3\%$ of the output voltage for full load using with three 680 μF output capacitors (see Figure 4). Additional output capacitance will reduce this further. Again, for most analog or POL applications, this magnitude of ripple should not be a problem.
- Due to the lack of a large input bulk capacitor (C3), which would preclude high power factor, the converter has no significant inherent hold−up time other than that provided by the stored energy in T1 and the output capacitors. Long hold up time is typically not a requirement for an LED power supply.
- The power factor for the single stage converter tends to degrade with increasing line and decreasing load due to factors related to the D/(1−D) transfer function and CCM operation, however, for most typical line and load conditions the PF will be above 0.95.

Despite these tradeoffs, the single stage, isolated PFC converter is an efficient and very cost effective solution to many applications where the load is relatively constant and/or point of load (POL) regulators are used downstream.

Circuit Technical Information

NCP1652A components selection: The logic level circuit components immediately associated with the NCP1652A shown in the Figure 3 schematic should work well with just about any design implementation. Changes for different output voltages involve modifying the voltage sense divider for the TL431 (R29, R30. Zener Z4 and resistor R31 will be required for output voltages over 32 V dc. The value of R20 will determine the peak limit of the MOSFET current and the sub sequential maximum output current. R12 sets the ramp compensation for CCM operation and can be adjusted depending on the primary inductance and level of the CCM transformer magnetizing ramp. The switching frequency is set to approximately 70 kHz with C9 and should be adequate for most applications. R5, R16, R17, D9, Z2 and C14 form a simple OVP circuit (optional) that monitors the V_{CC} derived from T1's auxiliary winding. Since this voltage will track the output voltage, it provides a simple primary side means of OVP sensing. R2, D5 and C4 form a DC startup circuit for the NCP1652A which uses a peak detector to sample the input haversine. This circuit, along with optional TVS Z1, also doubles as a transient suppression circuit in the event of short duration, high amplitude line transients that input capacitor C3 would be unable to suppress.

Input EMI filter design: The EMI filter consists of two stages of off−the−shelf common mode inductors (L1 and L2) which are manufactured by Coilcraft. The common mode inductors have a high leakage inductance so a single inductor can be used for both common mode and differential mode filtering. The differential LC low pass filter is formed with the leakage inductance and the X capacitors from line−to−line. The first stage of filtering is with L1 and C1, and the second stage is with L2 and C2. L1 has a leakage inductance of 15 μH and L2 has a leakage inductance of 22 μH.

$$f_{c1} = \frac{1}{2\pi\sqrt{L3C18}} = \frac{1}{2\pi\sqrt{15\ \mu H \cdot 0.47\ \mu F}} = 59.97\ kHz \quad \text{(eq. 1)}$$

$$f_{c2} = \frac{1}{2\pi\sqrt{L2C17}} = \frac{1}{2\pi\sqrt{22\ \mu H \cdot 0.47\ \mu F}} = 49.52\ kHz \quad \text{(eq. 2)}$$

When testing in accordance with the IEC 61000−4−6 limits (0.15 MHz to 80 MHz) there should be at least −24 dB of attenuation of the 70 kHz switching frequency with these EMI filter component values.

On the ac input side of the filter is a fuse, F1 for safety. The fuse is rated for 2.5 amps of continuous current, where the average input current for 90 watts output is:

$$I_{avg} = \frac{P_{out}\sqrt{2}}{\eta V_{inLL}} = \frac{90\ W\sqrt{2}}{0.88 \cdot 90\ Vac} = 1.61\ A \quad \text{(eq. 3)}$$

Where η is the estimated efficiency (0.88)

The input line voltage is full wave rectified and there is a small bulk film capacitor (C3) across the output of the bridge rectifiers (D1, D2, D3, and D4). The capacitor is there to decouple the high frequency switching and provide a low impedance source for the flyback converter. A typical range for the capacitor is 0.1 μF to 1.0 μF. For this application, a 0.1 μF capacitor was selected to minimize residual power factor effects at light load.

T1 Flyback Transformer Design: The transformer design for a single stage PFC converter is more complex than a standard flyback converter and requires an iterative process, especially when operation is in continuous conduction mode. There are several ways to mathematically approach this, however, treating the transformer as an energy storage

choke initially is probably the most straight forward way. Achieving the correct design on the first try is largely a matter of experience with realizing what core volumes and structures will support the desired power level and accommodate the necessary coil turns. A PQ3230 ferrite core was chosen for this design based on previous experience and the following facts:

- The PQ core has a fairly large cross sectional area parameter (Ae) for its overall volume. This will minimize primary turns which contribute to unwanted leakage inductance. The shape of the core also has a good shielding effect on radiated emissions, particularly if the required core gap is entirely in the center pole.
- The core window area has a good length to width aspect ratio which helps minimize turn layers and thus reduce leakage inductance and magnetic flux proximity effects.
- For minimal leakage inductance, this core will accommodate a “sandwiched” secondary winding configuration where the secondary is in between two primary windings which are connected in series.

Since the peak primary current in the inductor will determine the output power, the peak magnitude of the current can be obtained from the following relationship:

$Ipk = 2\ P_{out} / n \times f \times V_{in}$ (min) x ton(max)

Where η is the estimated efficiency, f is the switching frequency, $V_{in(min)}$ is the minimum average input voltage at lowest line voltage, and $t_{on(max)}$ is the maximum on time. This results in a value of:

I_{pk} = (2 x 95 W)/(0.88 x 70,000 x 83 V x 10 μs) = 3.7 A (pk)

Note that the average line voltage was used and not the rms value (90 Vac) for low line. This results from the fact that the input is a 100/120 Hz haversine and the energy storage will be a function of the average voltage and not rms.

Now, for wire sizing purposes we need to know the rms value of this peak primary current. If we assume an average duty cycle of D = 0.5 V at 120 V ac input and assume an almost rectangular CCM waveform (the magnetizing component will actually be about 30% of the peak, but this should give a worst case estimate), the rms value of the switching frequency component for a pure dc input would be:

$$I_{rms} = I_{pk} \times \sqrt{D} = 3.7 \times 0.707 = 2.6\ A \quad \text{(eq. 4)}$$

Now we must divide this by 0.707 again to account for the fact that the input to the converter is a 100/120 Hz haversine envelope and not pure dc. This results in an rms primary current of about 1.8 A. Looking at wire tables we can effectively choose #24 magnet wire for the primary since it will handle this current and should have minimal skin effect loss at 70 kHz.

The minimum primary inductance required is given by the following:

Lmin = Vdc pk (min) x ton(max) / Ipk = (120 V dc x 10 μs)/ 3.7 A = 324 μH

Where Vdc pk min is the low line value of the peak input voltage (85 Vac x 1.414). Now we make an assumption: In order to be in CCM for most of the typical loading of the supply, let’s double this inductance value to 650 μH. The minimum number of primary turns required for this core can now be calculated:

$$N_p = \frac{L \times I_{pk} \times 10^8}{Ae \times B_{max}} = \frac{650\ \mu H \times 4\ A \times 10^8}{1.6\ cm^2 \times 2800\ g} = 5 \quad \text{(eq. 5)}$$

Where the peak current was rounded off to 4 amps and the maximum flux density (B_{max}) was chosen to be 2.8 kilogauss to give a saturation safety margin for over−current conditions.

Noting that the PQ3230 bobbin winding width for the PQ3230 core is about 0.73 inches, we can comfortably get about 30 turns of number 24 wire (dia. = 0.022”) on one layer of the bobbin and a total of 60 turns for the entire series primary, so 60 turns total is a good number to go with.

The next step will be to decide the primary to secondary turns ratio. This will determine the reflected flyback voltage on MOSFET Q1 and also the peak reverse voltage seen by the output rectifier D8. Let’s try 2.5:1 where the secondary will have 25 turns (120 V ac divided by 48 V dc.) With this selection we can comfortably get 24 or 25 turns of # 24 wound over 1 layer with margins to handle the secondary current which will be about 4 A rms worst case. The reflected primary flyback voltage and maximum PRV output diode voltage will occur at high line. Let’s assume an input voltage of 270 Vac which translates to peak voltage of 378 Vdc. The reflected flyback voltage will be the peak secondary voltage of 48 Vdc plus the output rectifier forward drop times the turns ratio:

$V_{flyback}$ = (48 V + 1 V) x 2.5 = 123 V

Adding this to the peak primary voltage of 378 V dc gives 378 + 123 = 501 V dc plus any leakage inductance spike which will probably be in the order of 100 V. The selected 800 V MOSFET should be adequate for this. The primary of T1 is bypassed with the voltage clamping snubber network of D7, C7 and R3 to clamp residual spikes caused by T1’s leakage inductance. The output rectifier’s PRV voltage will be the peak input voltage divided by the turns ratio plus the output voltage and output diode drop:

Diode PRV = (378 / 2.5) + 49 V = 200 Vpk (plus probable diode recovery spike)

So, the 600 V rated ultra−fast device is more than sufficient to handle this. Notice that a small R/C snubber composed of R24 and C19 is across D9 to attenuate any parasitic voltage spikes for EMI reduction. The final transformer design is detailed in Figure 8.

Test Results

Power factor and efficiency measurements were taken at loads of 25%, 50%, 75% and 100% at both US and Euro mains voltages. The efficiencies were averaged and the results are shown in the table below.

	Load	100%	75%	50%	25%	Overall Efficiency
Vin = 120 Vac	PF	0.98	0.97	0.96	0.95	
	η	87.0	87.2	87.1	86.1	87%
Vin = 230 Vac	PF	0.98	0.96	0.95	0.92	
	η	88.6	88.2	87.1	85	87.2%

Output Ripple: The 120 Hz output ripple with a 2 A load and 2000 μF (3 x 680 μF) of output capacitance is shown in Figure 4 for 120 V ac input. The ripple amplitude is strictly a function of the output capacity and load on the power supply since the regulation loop bandwidth is necessarily less than the ripple frequency to assure high power factor. Doubling the amount of output capacitance will halve the ripple amplitude.

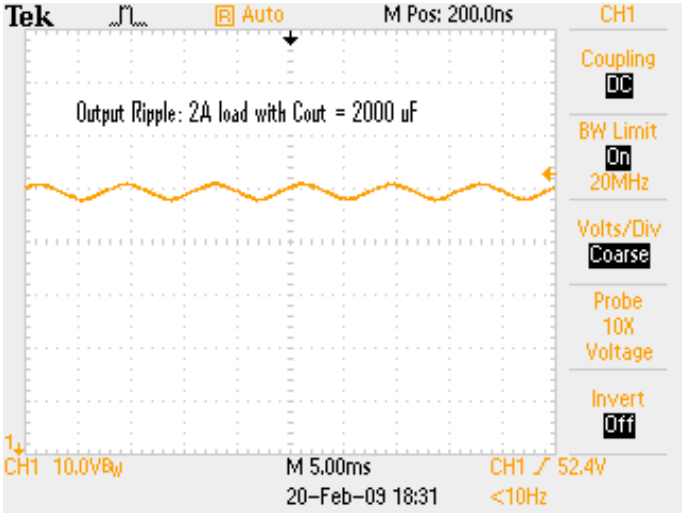
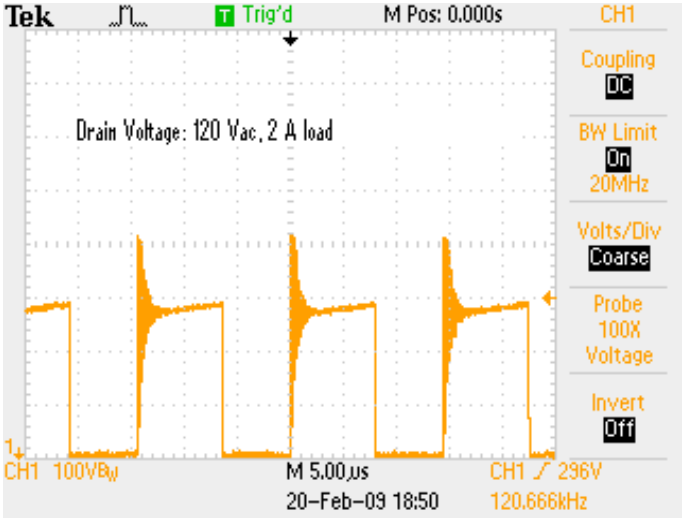
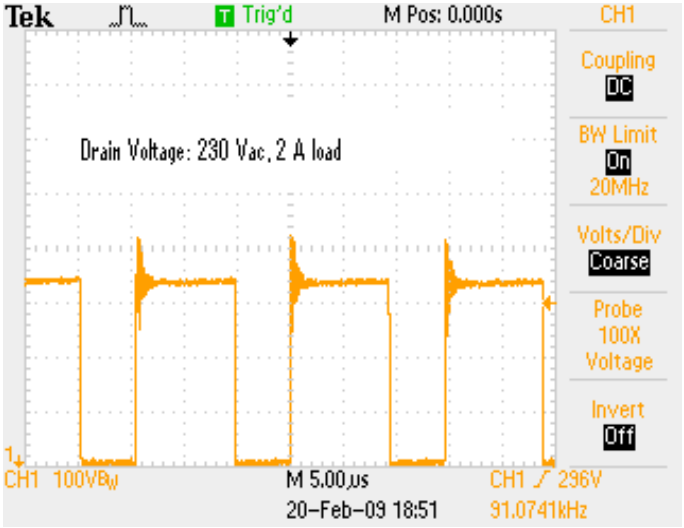


Figure 4. Output Ripple



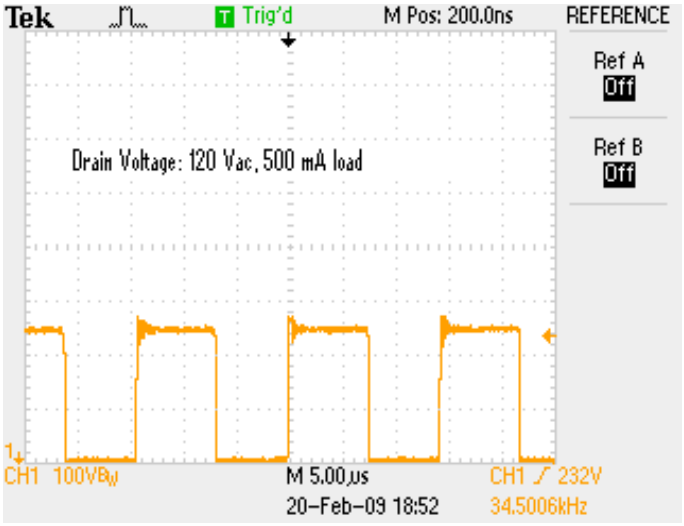
(a)



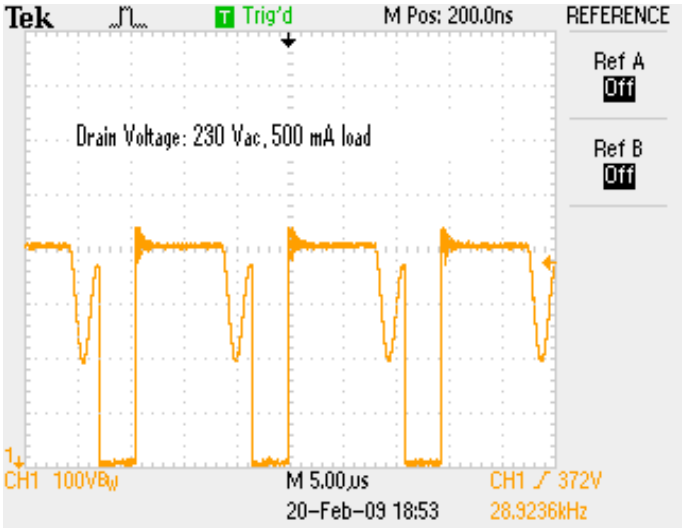
(b)

Figure 5. Q1 Drain Waveforms at Full Load at 120 Vac and 230 Vac

Flyback Waveforms: The waveforms of Figures 5a and 5b shows the drain voltage profile on MOSFET Q1 with full output load (2 A) for 120 Vac and 230 Vac inputs. The leading edge voltage spike is caused by the leakage inductance of transformer T1 and is largely damped by the snubber network of D7, C7 and R3.



(a)

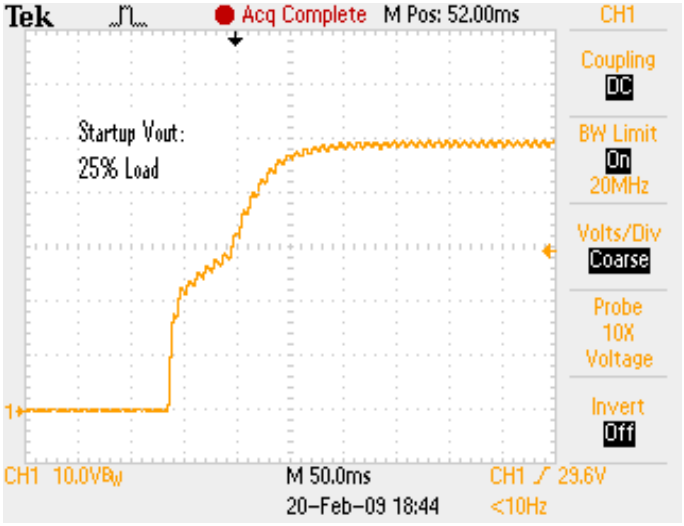


(b)

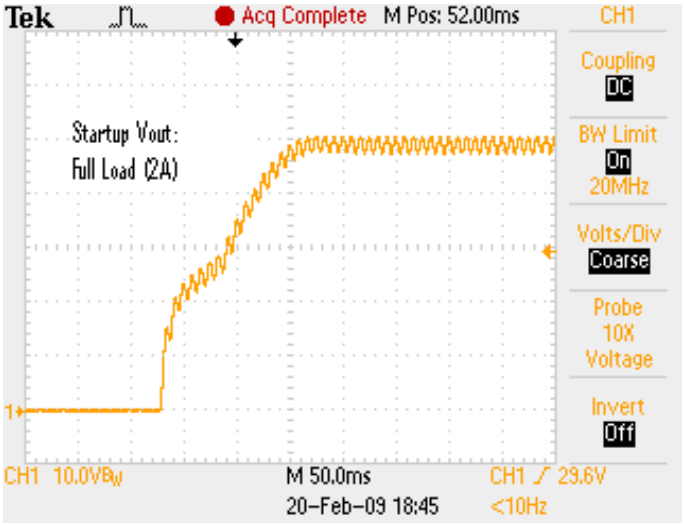
Figure 6. Q1 Drain Waveforms at 25% Load at 120 Vac and 230 Vac

The waveforms of Figures 6a and 6b display Q1's drain waveform at 25% output load (1.25 A). Note that operation is clearly in DCM at this load for both line input levels. Note that when the flyback energy is depleted, the drain voltage will ring prior to Q1's next turn−on due to the resonant circuit formed by the transformer's primary inductance and the MOSFET's parasitic capacitance. This is a characteristic of DCM operation.

The drain waveforms in the prototype were typical of a relatively low leakage inductance transformer. Use of proper PC board layout techniques with minimal power loop traces, liberal ground planes, and clad "pours" where possible to lower trace inductance will assure proper switching waveform profiles and lowest EMI generation. Very low flyback transformer leakage inductance is also extremely important as previously mentioned. In higher power applications and in cases were mechanical constraints limit optimum core structure and/or winding techniques, the use of an active clamp to suppress the primary voltage spikes may be necessary. The optional auxiliary gate drive output of pin 14 on the NCP1652A is provided for this function.



(a)



(b)

Figure 7. Output Turn−on Profiles 25% Load and at Full Load

The output turn on profiles of Figures 7a and 7b clearly indicate that no output overshoot exists for either load condition, particularly at light load where it is not uncommon to exhibit overshoot with narrow bandwidth control loops. At full load the 120 Hz throughput ripple is clearly visible. The selection of the component values for R28 and C26 will have a significant impact on the turn on profile and response to load changes.

BILL OF MATERIALS FOR 48 V, 90 W NCP1652A ADAPTER DEMONSTRATION BOARD

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
D5, D10	2	Diode			SMA	ON Semiconductor	MRA4007T	No	Yes
D1, D2, D3, D4	4	Diode			Axial Lead	ON Semiconductor	1N5406	No	Yes
D6, D7	2	Ultrafast Diode			SMB	ON Semiconductor	MURS160	No	Yes
D9, D11	2	Signal Diode			SOD123	ON Semiconductor	MMSD4148A	No	Yes
D8	1	UFR "soft" Diode			TO−220AB	ON Semiconductor	MSR860G	No	Yes
Z1	1	TVS	Input Transient Option		Axial Lead		1.5KE440A	Yes	Yes
Z3	1	Zener Diode	18 V	5%	SOD123	ON Semiconductor	MMSZ5248B	No	Yes
Z2, Z4	2	Zener Diode	24 V	5%	SOD123	ON Semiconductor	MMSZ5252B	No	Yes
Q1	1	MOSFET	11 A, 800 V		TO−220	Infineon	SPP11N80C3	No	Yes
U1	1	PFC Controller			SOIC16	ON Semiconductor	NCP1652A	No	Yes
U2	1	Optocoupler			4 Pin SMD	Vishay	H11A817 or SFH6156A−4	Yes	Yes
U3	1	Progam. Zener	2.5 V	1%	SOIC−8	ON Semiconductor	TL431A	No	Yes
C1, C2	2	X Caps	0.22 μF, 305 Vac	10%	LS = 15 mm	Rifa, Wima, Vishay,Epcos	Box Cap − X2	Yes	
C27	1	Y2 Cap	2.2 nF, 1 kV	10%	LS = 10 mm	Rifa, Wima, Vishay	Box or Disc Y2 Cap	Yes	
C3	1	Polyprop. Film	0.1 to 0.22 μF, 600 V	10%	LS =24 mm	Rifa, Wima, Vishay	Polypropylene Film Cap	Yes (Must be Polyprop)	
C7	1	Disc Cap	68 to 100 nF, 400 V	10%	LS = 10 mm	Vishay	Ceramic Disc Cap, 400 V Min	High Quality Ceramic	
C8, 15, 16, 17, 25	5	Ceramic Cap	0.1 μF, 50 V	10%	1206	Anybody	100 nF, 50 V Ceramic SMD Cap	Yes	
C24, C25	2	Ceramic Cap	0.1 μF, 100 V	10%	1206/1210	Anybody	100 nF, 100 V Ceramic SMD Cap	Yes	
C26	1	Ceramic Cap	1.0 μF, 16 V	10%	1206	Anybody	1 μF, 16 V Ceramic SMD Cap	Yes	
C19	1	Ceramic Disc Cap	1 nF, 1 kV	10%	LS = 8 mm	Anybody	1 nF pF Ceramic Disc Cap	Yes	
C12	1	Ceramic Cap	470 pF, 50 V	10%	1206	Anybody	Ceramic SMD Cap	Yes	
C9	1	Ceramic Cap	680 pF, 50 V	10%	1206	Anybody	Ceramic SMD Cap	Yes	
C10, C18	2	Ceramic Cap	1 nF, 100 V	10%	1206	Anybody	Ceramic SMD Cap	Yes	
C14	1	Ceramic Cap	10 nF, 50 V	10%	1206	Anybody	Ceramic SMD Cap	Yes	
C13	1	Ceramic Cap	33 nF, 50 V	10%	1206	Anybody	Ceramic SMD Cap	Yes	
C5	1	Electrolytic Cap	100 μF, 35 V	10%	LS = 2.5 mm	Rubycon, UCC, Nich.	Radial Lead, Dia = 5 mm	Yes	
C11	1	Electrolytic Cap	4.7 μF, 25 V	10%	LS = 2.5 mm	Rubycon, UCC, Nich.	Radial Lead, D= 5 mm	Yes	
C6	1	Electrolytic Cap	470 μF, 35 V	10%	LS = 5mm	Rubycon, UCC, Nich.	Radial Lead	Yes	
C23	1	Electrolytic Cap	100 μF, 63 V	10%	LS = 5 mm	Rubycon, UCC, Nich.	Radial Lead Electrolytic	Yes	
C20, 21, 22	3	Electrolytic Cap	1000 μF, 63 V	10%	LS = 8 mm	Rubycon, UCC, Nich.	Radial Lead, D = 16 − 18 mm	Recommended Value	
C4	1	Electrolytic Cap	22 μF, 450 V	10%	LS = 5 mm	Rubycon, UCC, Nich.	Radial Lead, D = 12 − 15 mm	Yes	
R4	1	0.25 W Resistor	100 Ω	10%	Axial Lead	Anybody	1/4 W Metal Film Resistor	Yes	
R1	1	0.5 W Resistor	1M, 0.5 W	10%	Axial Lead	Anybody	1/2 W Metal Film Resistor	Yes	
R31	1	0.5 W Resistor	3.3k, 0.5 W	10%	Axial Lead	Anybody	1/2 W Metal Film Resistor	Yes	

BILL OF MATERIALS FOR 48 V, 90 W NCP1652A ADAPTER DEMONSTRATION BOARD

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
R8	1	0.5 W Resistor	2k, 0.5 W	10%	Axial Lead	Anybody	1/2 W Metal Film Resistor	Yes	
R2	1	0.5 W Resistor	560k	10%	Axial Lead	Anybody	1/2 W Metal Film Resistor	Yes	
R24	1	0.5 W Resistor	100 Ω	10%	Axial Lead	Anybody	1/2 W Metal Film Resistor	Yes	
R20	1	0.5 W Resistor	0.1 Ω	5%	LS = 18 mm	Anybody	Axial Lead, Non−Inductive	Yes	
R3	1	3 W or 5 W Resistor	36k to 39k	10%	LS = 30 mm	Ohmite	Axial Lead Metal Film or WW Resistor	Yes	
R23	1	0.25 W Resistor	4.7 Ω	5%	1206	Anybody	1206 SMD Resistor	Yes	
R5	1	0.25 W Resistor	100 Ω	5%	1206	Anybody	1206 SMD Resistor	Yes	
R21, R25	2	0.25 W Resistor	10 Ω	5%	1206	Anybody	1206 SMD Resistor	Yes	
R27	1	0.25 W Resistor	1k	5%	1206	Anybody	1206 SMD Resistor	Yes	
R15	1	0.25 W Resistor	2.2k	5%	1206	Anybody	1206 SMD Resistor	Yes	
R26	1	0.25 W Resistor	2.7k	5%	1206	Anybody	1206 SMD Resistor	Yes	
R28	1	0.25 W Resistor	24k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R30	1	0.25 W Resistor	5.6k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R29	1	0.25 W Resistor	102k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R22	1	0.25 W Resistor	10k	5%	1206	Anybody	1206 SMD Resistor	Yes	
R13	1	0.25 W Resistor	7.32k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R14	1	0.25 W Resistor	8.6k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R9, R12	2	0.25 W Resistor	30.1k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R17	1	0.25 W Resistor	39k	5%	1206	Anybody	1206 SMD Resistor	Yes	
R18	1	0.25 W Resistor	49.9k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R19	1	0.25 W Resistor	76.8k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R16	1	0.25 W Resistor	100k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R10	1	0.25 W Resistor	332k	1%	1206	Anybody	1206 SMD Resistor	Yes	
R6, 7, 11	3	0.25 W Resistor	365k	1%	1206	Anybody	1206 SMD Resistor	Yes	
F1	1	Fuse	2.5 A, 250 Vac		TR−5	Anybody	Minifuse − TR−5 Package	Yes	
L1	1	EMI Inductor			E/E Core	Coilcraft	BU10−1012R2B	No	
L2	1	EMI Inductor			Toroid	Coilcraft	P3221−AL	No	
L3	1	3.3 μH Choke	3.3 μH, 5 A		LS = 0.2”	Coilcraft	RFB0807−3R3L	Yes	
T1	1	Flyback xfmr	48 V, 90 W CCM		Custom	Mesa Power Systems	13−1407 (600 μH Primary)	No	
J1, J2	2	I/O Connectors			LS = 5 mm	DigiKey	# 281−1435−ND (LS = 0.2”)		
(for Q1, D8)	2	Heatsink Q1, D8			LS = 25.4 mm	Aavid	531102B02500G (or Similar)		

MAGNETICS DESIGN DATA SHEET

Project: NCP1652A, 90 W, 48 Vout, isolated, single stage PFC

Part Description: CCM Flyback transformer, 70 kHz, 48 Vout

Schematic ID: T1

Core Type: PQ3230, 3C94 (Ferroxcube) or P material (Mag Inc.)

Core Gap: Gap core for 600 to 650 uH across pins 1 to 2.

Inductance: 625 uH nominal measured across primary (pins 1 to 2)

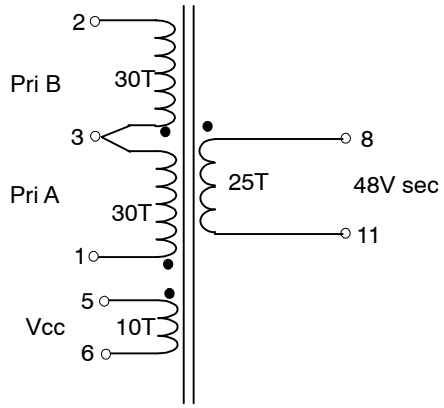
Bobbin Type: 12 pin pc mount (Mag Inc PC−B3230−12 or equivalent)

Windings (in order):

Winding # / type	Turns / Material / Gauge / Insulation Data
Primary A: (1 − 3)	30 turns of #24HN over one layer (no margins). Self−leads to pins. Insulate for 3 kV to next winding.
48V Secondary (8 − 11)	25 turns of #24HN close wound over one layer and centered with 2 mm end margins. Insulate with tape for 3 kV to next winding.
Primary B: (3 − 2)	Same as primary A. Insulate for 1.5 kV to Vcc/Aux.
Vcc/Aux (5 − 6)	10 turns of #24HN spiral wound and centered with 8 mm end margins. Insulate with tape and terminate self−leads to pins.

Hipot: 3 kV from primary/Vcc to 48V secondary winding.

Schematic



Lead Breakout / Pinout

(bottom view)

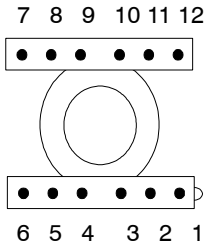


Figure 8. Flyback Transformer Design

Conclusions

For single stage, isolated PFC converters where the output voltage is 15 V and less, the efficiency can be enhanced with the use of synchronous output rectifiers instead of convention PN or Schottky diodes. Synchronous output rectifiers are not, however, wholly compatible with continuous conduction mode (CCM) operation. This is because CCM or DCM operation will almost always transition into the other depending on the load situation. At light load a CCM oriented design will transition to DCM and with DCM operation, the startup and over−current mode usually operate in CCM. As a result of these two modes of operation, the required gate drive signal to the synchronous MOSFET must be based on different sensing criteria for each mode which causes additional circuit complexity. The "problem mode" is CCM because there has to be a delayed timing sequence to the sync MOSFET to prevent simultaneous conduction overlap with the main primary side MOSFET. Even though the necessary timing sequence can be achieved, one critical issue still remains. When the sync MOSFET is turned off just prior to the main primary MOSFET coming on, the intrinsic body diode of the sync MOSFET must carry the still flowing continuous flyback current. This parasitic body diode has very poor recovery characteristics and when the main MOSFET turns on, this body diode is force commutated off and significant reverse current will flow in the body diode during the recovery process. This current along with the associated circuit reactive parasitic components generates large voltage spikes and ringing on the sync MOSFET and main MOSFET during this transition. This usually necessitates the addition of larger snubbers and/or TVS clamping circuits to avoid MOSFET failure. The added circuit cost and dissipative issues are generally not worth it.

As illustrated in this application note, the NCP1652A when optimized for CCM operation can achieve high efficiency across wide load variation. The use of a single stage topology significantly reduces the overall component bill of material cost while still achieving high power factor in a compact form factor and well behaved startup characteristics. Multiple protection schemes have been implemented in this design to address ensure robust and reliable operation.

References

- Data sheet NCP1652
- Application note AND8124: 90 W, Universal Input, Single Stage, PFC Converter
- Application note AND8147: An Innovative Approach to Achieving Single Stage PFC and Step−Down Conversion for Distributive Systems
- Application note AND8209: 90 W, Single Stage, Notebook Adaptor
- Reference design TND317: 90 W Notebook AC−DC Adapter GreenPoint® Reference Design

All the above documentation is available for download from ON Semiconductor's website (www.onsemi.com).

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