

Burst Triple-Mode PWM Flyback Controller

General Description

The R7731A is a high-performance, low cost, low start-up current and current mode PWM controller with burst triple-mode to support green mode power saving operation. The R7731A integrates functions of soft start, Under Voltage LockOut (UVLO), Leading Edge Blanking (LEB), Over Temperature Protection (OTP) and internal slope compensation. It provides the users a superior AC/DC power application of higher efficiency, low external component counts and lower cost solution.

To protect the external power MOSFET from being damaged by supply over voltage, the R7731A output driver is clamped at 12V. Furthermore, R7731A features fruitful protections like Over Load Protection (OLP) and Over Voltage Protection (OVP) to eliminate the external protection circuits and provide reliable operation. R7731A is available in SOT-23-6 and DIP-8 packages.

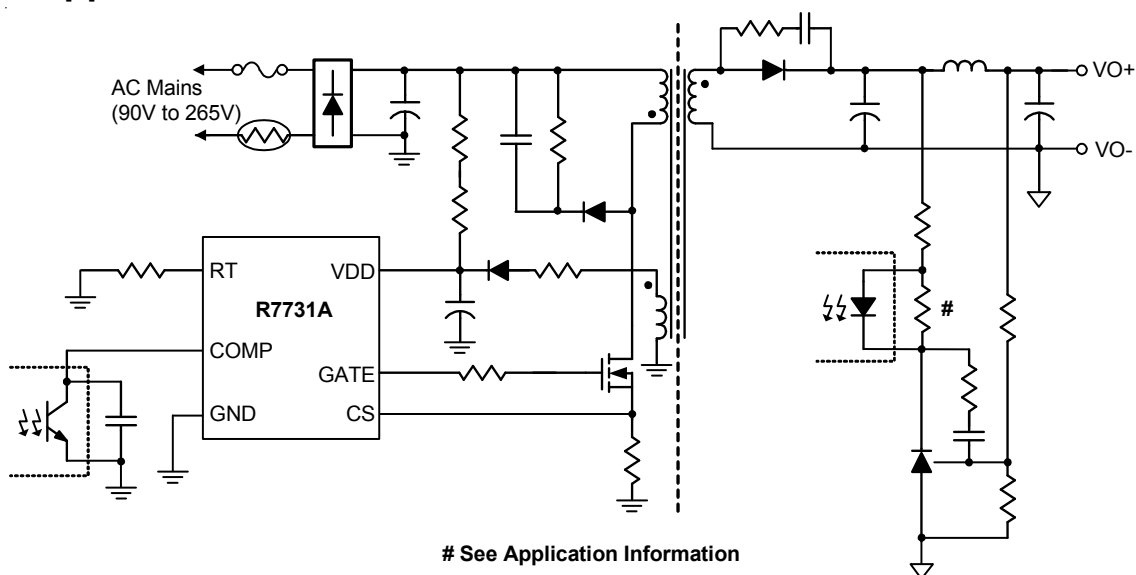
Features

- Very Low Start-up Current (<30uA)
- 10/14V UVLO
- Soft Start Function
- Current Mode Control
- Jittering Switching Frequency
- Internal Leading Edge Blanking
- Built-in Slope Compensation
- Burst Triple-Mode PWM for Green-Mode
- Cycle-by-Cycle Current Limit
- Feedback Open Protection
- Output Over Voltage Protection
- Over Temperature Protection
- Over Load Protection
- Soft Driving for Reducing EMI
- High Noise Immunity
- Opto-Coupler Short Protection
- RoHS Compliant and Halogen Free

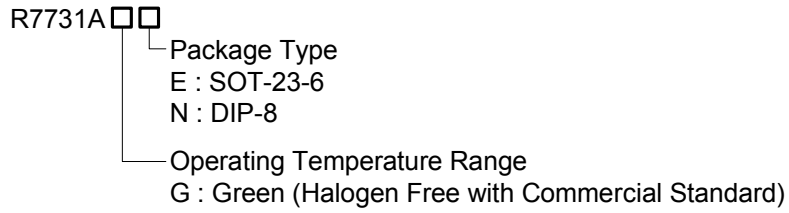
Applications

- Adaptor and Battery Charger
- ATX Standby Power
- Set-Top Box (STB)
- DVD and CD(R)
- TV/Monitor Standby Power
- PC Peripherals

Typical Application Circuit



Ordering Information



Note :

Richpower Green products are :

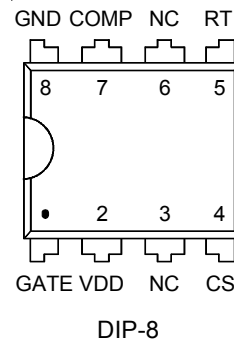
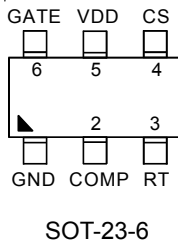
- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

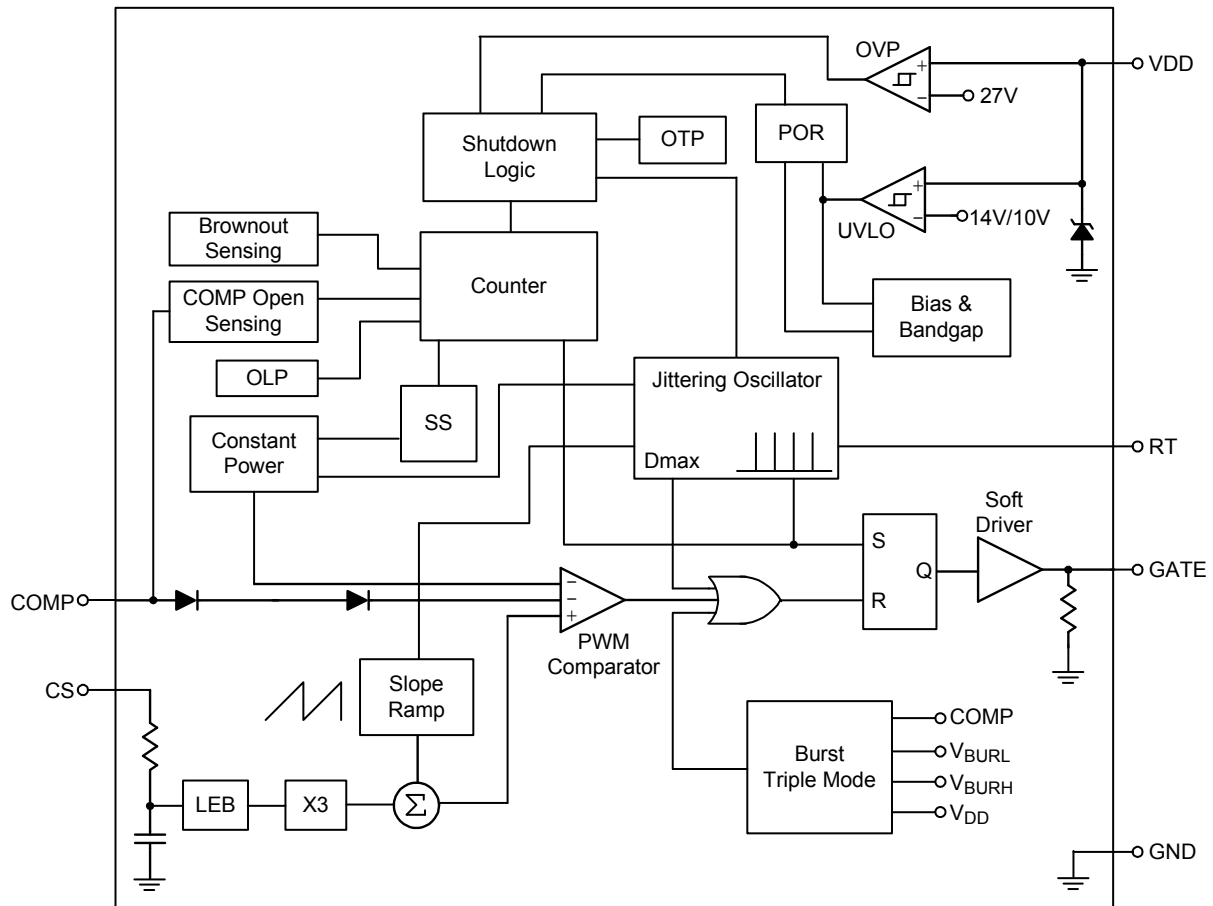
For marking information, contact our sales representative directly or through a Richpower distributor located in your area, otherwise visit our website for detail.

Pin Configurations

(TOP VIEW)



Function Block Diagram



Functional Pin Description

| Pin No. | | Pin Name | Pin Function |
|----------|------|----------|---|
| SOT-23-6 | DIP8 | | |
| 1 | 8 | GND | Ground. |
| 2 | 7 | COMP | Comparator input pin. By connecting a opto-coupler to this pin, the peak current set point is adjusted accordingly to the output power requirement. |
| 3 | 5 | RT | Set the switching frequency by connecting a resistor to GND. |
| 4 | 4 | CS | Primary current sense pin. |
| 5 | 2 | VDD | IC power supply pin. |
| 6 | 1 | GATE | Gate driver output to drive the external MOSFET. |
| -- | 3, 6 | NC | No internal connection. |

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{DD} ----- -0.3V to 30V
- GATE Pin ----- -0.3V to 20V
- RT, COMP, CS Pin ----- -0.3V to 6.5V
- I_{DD} ----- 10mA
- Power Dissipation, P_D @ $T_A = 25^\circ C$
 - SOT-23-6 ----- 0.4W
 - DIP-8 ----- 0.714W
- Package Thermal Resistance (Note 2)
 - SOT-23-6, θ_{JA} ----- $250^\circ C/W$
 - DIP-8, θ_{JA} ----- $140^\circ C/W$
- Junction Temperature ----- $150^\circ C$
- Lead Temperature (Soldering, 10 sec.) ----- $260^\circ C$
- Storage Temperature Range ----- $-65^\circ C$ to $150^\circ C$
- ESD Susceptibility (Note 3)
 - HBM (Human Body Mode) ----- 4kV
 - MM (Machine Mode) ----- 250V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{DD} ----- 12V to 25V
- Operating Frequency ----- 50k to 130kHz
- Junction Temperature Range ----- $-40^\circ C$ to $125^\circ C$
- Ambient Temperature Range ----- $-40^\circ C$ to $85^\circ C$

Electrical Characteristics

($V_{DD} = 15V$, $R_T = 100k\Omega$, $T_A = 25^\circ C$, unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|-----------------|---|------|------|------|---------|
| VDD Section | | | | | | |
| VDD Over Voltage Protection Level | V_{OVP} | | 25.5 | 27 | 28.5 | V |
| On Threshold Voltage | V_{TH_ON} | | 13 | 14 | 15 | V |
| VDD On/Off Hysteresis | V_{DD_HYS} | | 3 | 4 | 5 | V |
| Start-up Current | I_{DD_ST} | $V_{DD} = V_{TH_ON} - 0.1V$ | -- | 20 | 30 | μA |
| Operating Current | I_{DD_OP} | $V_{DD} = 15V$, $R_T = 100k\Omega$, GATE = Open, $V_{COMP} = 2.5V$ | -- | 1.1 | 2.2 | mA |
| VDD Holdup Mode Hysteresis Ending Level | V_{DD_HYS} | $V_{COMP} < 1.6V$ | -- | 11.5 | -- | V |
| VDD Holdup Mode Entry Level | V_{DD_LOW} | $V_{COMP} < 1.6V$ | -- | 11 | -- | V |
| VDD Clamp Voltage | V_{DD_CLAMP} | | -- | 29 | -- | V |
| Oscillator Section (RT pin) | | | | | | |
| Normal PWM Frequency | f_{OSC} | $R_T = 100k\Omega$ | 60 | 65 | 70 | kHz |

To be continued

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|----------------------|---|-----|------|-----|------|
| Frequency Jittering Range | | | -- | ±6 | -- | % |
| PWM Frequency Jitter Period | T _{JIT} | For 65 kHz | -- | 4 | -- | ms |
| Maximum Duty Cycle | D _{MAX} | | 70 | 75 | 80 | % |
| Frequency Variation Versus V _{DD} Deviation | f _{DV} | V _{DD} = 12V to 25V | -- | -- | 2 | % |
| Frequency Variation Versus Temperature Deviation | f _{DT} | T _A = -30°C to 105°C (Note 5) | -- | -- | 5 | % |
| COMP Input Section | | | | | | |
| Open Loop Voltage | V _{COMP_OP} | COMP pin open | 5.2 | 5.6 | 6 | V |
| COMP Open-loop Protection Delay Cycles | T _{OLP} | R _T = 100kΩ | -- | 60 | -- | ms |
| Short Circuit Current | I _{ZERO} | V _{COMP} = 0V | -- | 1.2 | 2.2 | mA |
| Current-Sense Section | | | | | | |
| Initial Peak Current Limit Offset | V _{CSTH} | | 0.8 | 0.85 | 0.9 | V |
| Leading Edge Blanking Time | T _{LEB} | | -- | 420 | 520 | ns |
| Propagation Delay Time | T _{PD} | | -- | 100 | -- | ns |
| GATE Section | | | | | | |
| Rising Time | T _R | V _{DD} = 15V, C _L = 1nF | -- | 250 | 350 | ns |
| Falling Time | T _F | V _{DD} = 15V, C _L = 1nF | -- | 150 | 250 | ns |
| Gate Output Clamping Voltage | V _{CLAMP} | V _{DD} = 22V | -- | 12 | -- | V |
| Over Temperature Protection | T _{OTP} | | 140 | -- | -- | °C |
| OTP Hysteresis | T _{OTP_HYS} | | -- | 30 | -- | °C |

Note 1. Stresses beyond those listed under “ Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

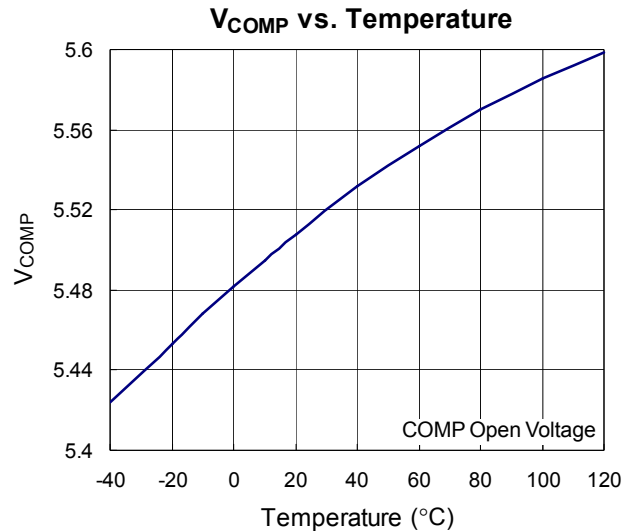
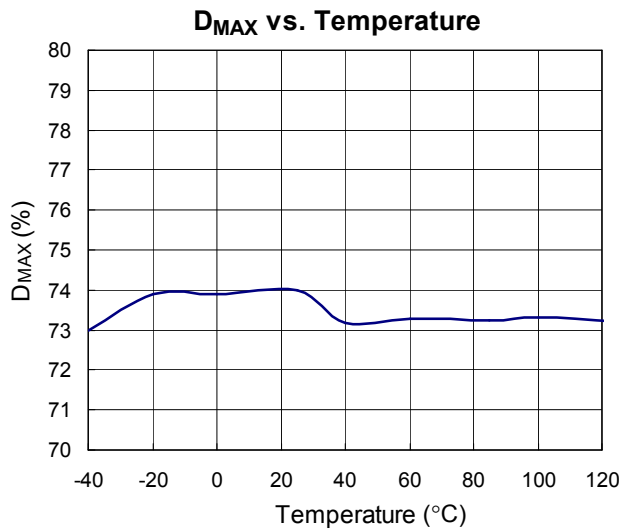
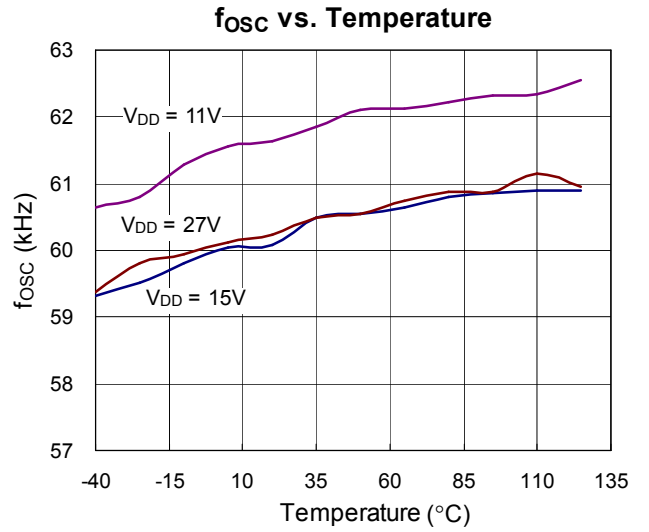
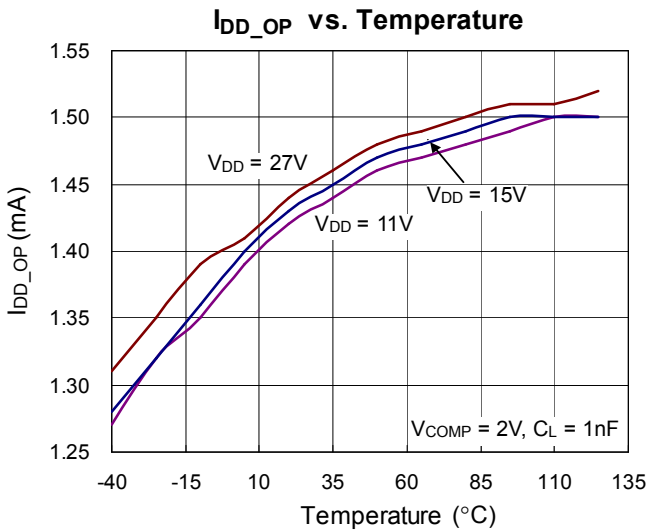
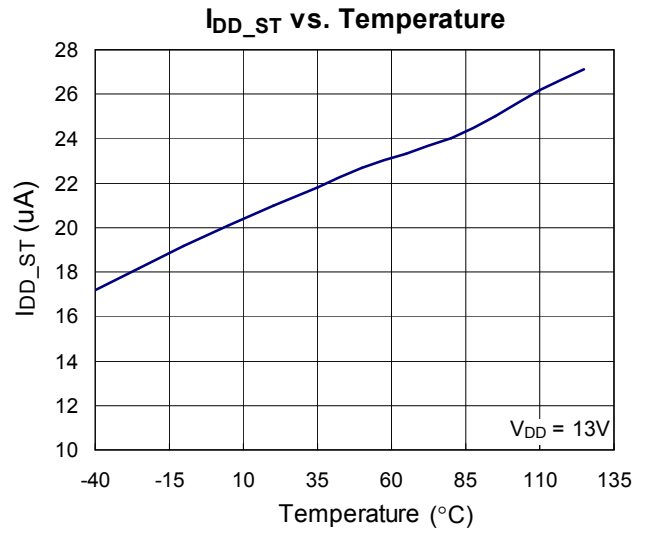
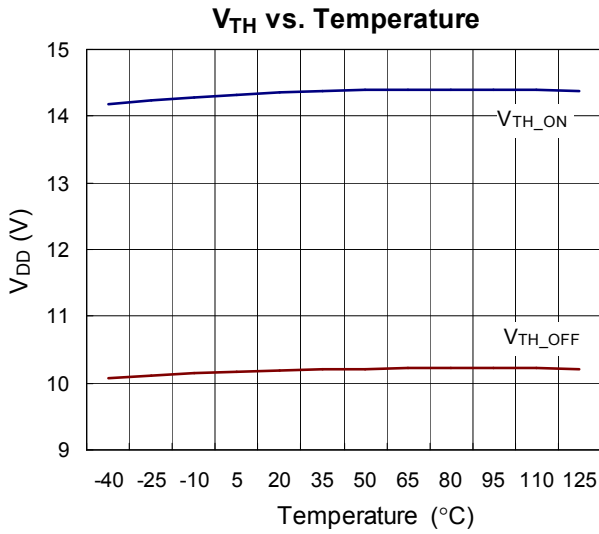
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

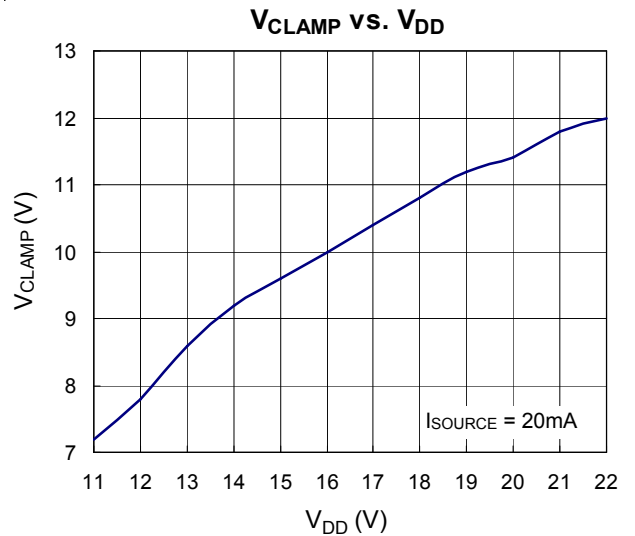
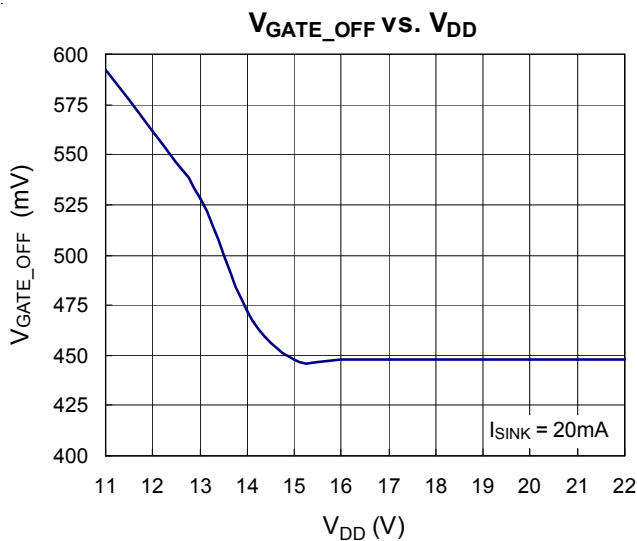
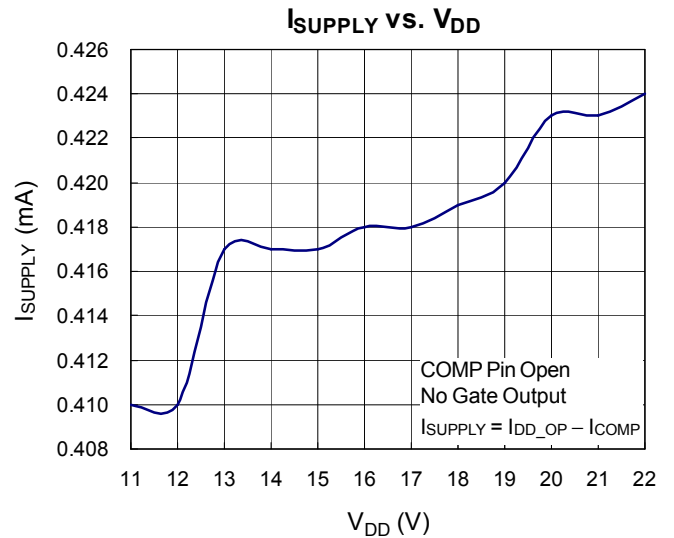
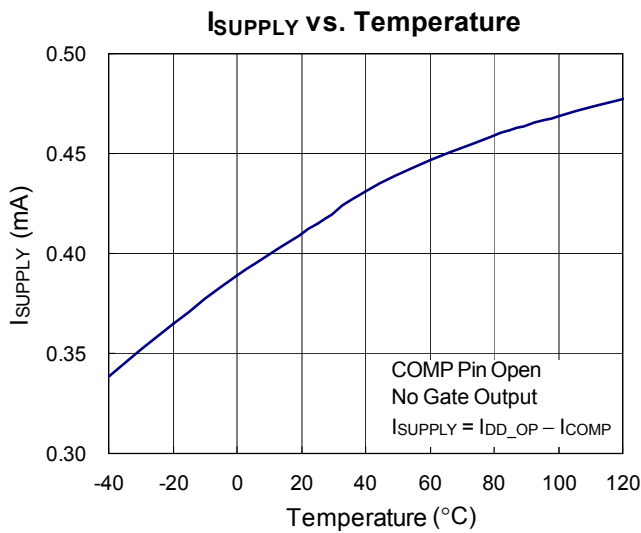
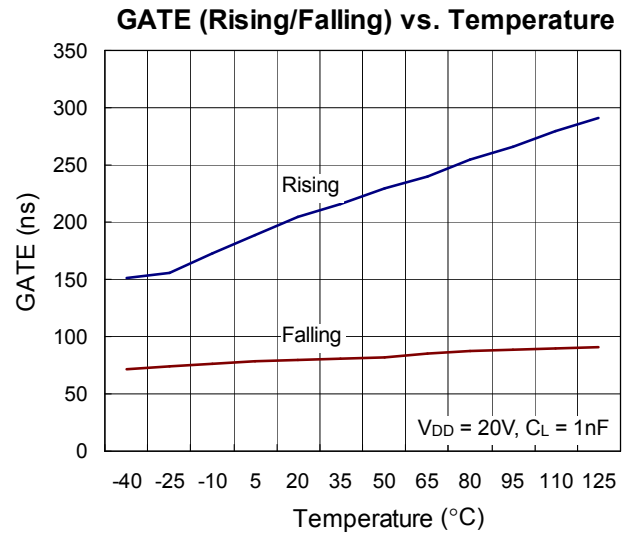
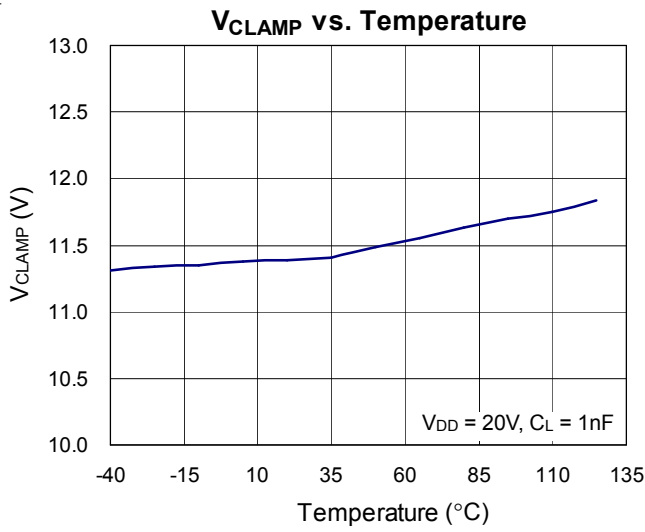
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Operating Characteristics





Application Information

UVLO

Under Voltage LockOut (UVLO) block is to ensure V_{DD} has reached proper operation voltage before we enable the whole IC blocks. To provide better temperature coefficient and precise UVLO threshold voltage, the reference voltage of hysteresis voltage (10V / 14V) is from band-gap block directly. By this way, R7731A can operate more reliable in different environments.

Jittering Oscillator

For better EMI performance, R7731A will operate the system with $\pm 6\%$ frequency deviation around setting frequency.

To guarantee precise frequency, it is trimmed to 5% tolerance. It also generates slope compensation saw-tooth, 75% maximum duty cycle pulse and overload protection slope. By adjusting resistor of R_T pin according to the following formula :

$$f_{OSC} \text{ (kHz)} = \frac{6500}{R_T \text{ (k}\Omega)}$$

It can typically operate between 50kHz to 130kHz. Note that R_T pin can't be short or open otherwise oscillator will not operate.

Built-in Slope Compensation

To reduce component counts, slope compensation is implemented by internal built-in saw-tooth. Since it's built-in, it's compromised between loop gain and sub-harmonic reduction. In general design, it can cancel sub-harmonic to 90Vac.

Leading Edge Blanking (LEB)

MOSFET C_{OSS} , secondary rectifier reverse recovery current and gate driver sourcing current comprise initial current spike. The spike will seriously disturb current mode operation especially at light load and high line. R7731A provides built-in 420ns LEB to guarantee proper operation in diverse design.

Noise Immunity

Current mode controller is very sensitive to noise. R7731A takes the advantages of Richpower long term experience in designing high noise immunity current mode circuit and

layout. Also, we amplify current sense signal to compare with feedback signal instead of dividing feedback signal. All the effort is to provide clean and reliable current mode operation.

Soft Start

During initial power on, especially at high line, current spike is kind of unlimited by current limit. Therefore, besides cycle-by-cycle current limiting, R7731A still provides soft start function. It effectively suppresses the start-up current spike. As shown in the Figure 1 and Figure 2, the start-up V_{CS} is about 0.3V lower than competitor. The typical soft start duration is 4ms ($R_T=100k\Omega$). Again, this will provide more reliable operation and possibility to use smaller current rating power MOSFET.

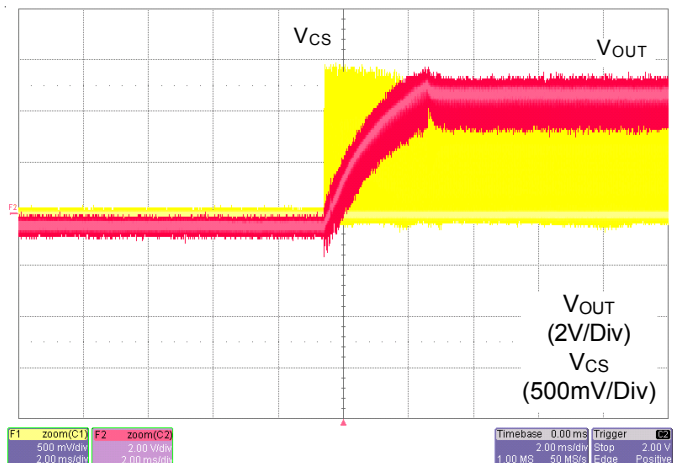


Figure 1. Competitor

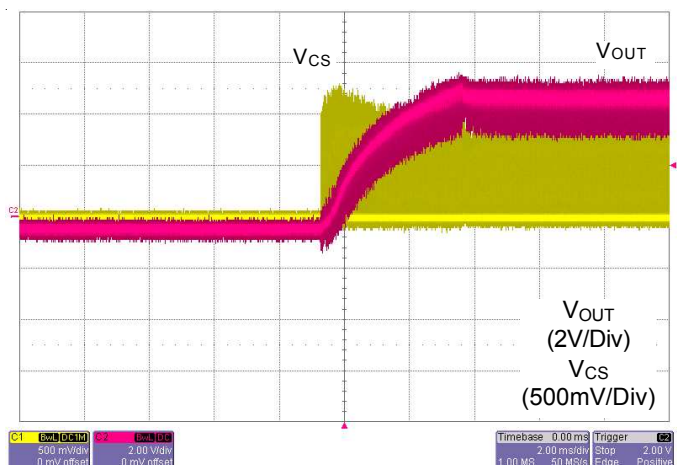


Figure 2. R7731A

Gate Driver

A totem pole gate driver is fine tuned to meet both EMI and efficiency requirement in low power application. An internal pull low circuit is activated after pretty low V_{DD} to prevent external MOSFET from accidentally turning on during UVLO.

Burst Triple-Mode

To fulfill green mode requirement, there are 3 operation modes in R7731A. Please also refer to Figure 3 for details.

- **PWM Mode** : For most of load condition, the circuit will run at traditional PWM current mode.
- **Burst Mode** : During light load, switching loss will dominate the power efficiency calculation. This mode is to cut switching loss. As shown in Figure 3, when the output load gets light, feedback signal drops and

touches V_{BURL} (Typical value is 1.75V). Clock signal will be blanked and system ceases to switching. After V_{OUT} drops and feedback signal goes back to V_{BURH} (1.8V, typically), switching will be resumed. Burst mode so far is widely used in low power application because it's simple, reliable and will not have any patent infringement issue.

- **VDD Holdup Mode** : When the V_{DD} drops down to V_{DD} turn off threshold voltage, the system will be shut down. During shut down period, controller does nothing to any load change and might cause V_{OUT} down. To avoid this, when V_{DD} drops to a setting threshold, 11V, the hysteresis comparator will bypass PWM and burst mode loop and force switching at a very low level to supply energy to V_{DD} pin. The designed value is 11.25V with 0.5V hysteresis band.

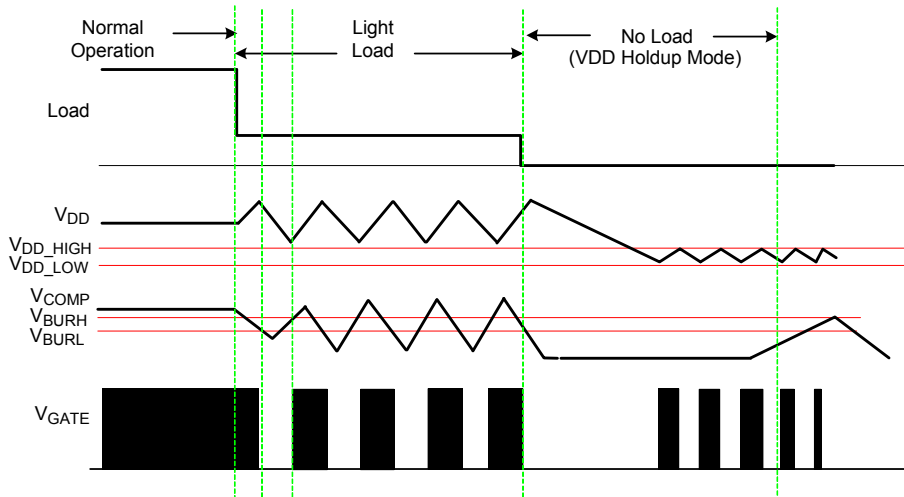


Figure 3. Burst Triple-Mode

Protection

R7731A provides fruitful protection functions that intend to protect system from being damaged. All the protection functions can be listed as below:

- **Cycle-by-Cycle Current Limit** : This is a basic but very useful function and it can be implemented easily in current mode controller.
- **Over Load Protection** : Long time cycle-by-cycle current limit will lead to system thermal stress. To further protect system, system will be shut down after about 4096 clock cycles. it's about 60ms delay in 67kHz operation. After shutdown, system will resume and behave as hiccup. By proper start-up resistor design,

thermal will be averaged to an acceptable level over the ON/OFF cycle of IC. This will last until fault is removed. #It's highly recommended to add a resistor in parallel with the opto-coupler. To provide sufficient bias current to make TL-431 regulate properly, 1.2kΩ resistor is suggested.

- **Brownout Protection** : During heavy load, this will trigger 60ms protection and shut down the system. If it's in light load condition, system will be shut down after V_{DD} is running low and triggers UVLO.
- **OVP** : Output voltage can be roughly sensed by V_{DD} pin. If the sensed voltage reaches 27V threshold, system will be shut down after 20us deglitch delay.

- **Feedback Open and Opto-Coupler Short** : This will trigger OVP or 60ms delay protection. It depends on which one occurs first.
- **OTP** : Internal OTP function will protect the controller itself from suffering thermal stress and permanent damage. It stops the system from switching until the temperature is under threshold level. Meanwhile, if V_{DD} reaches V_{DD} turn off threshold voltage, system will hiccup till over temperature condition is gone.

PCB Layout Guide

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply:

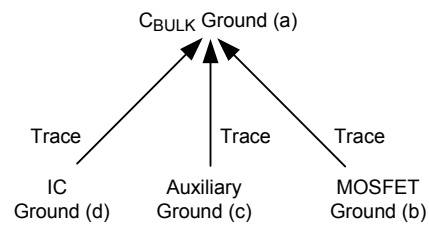
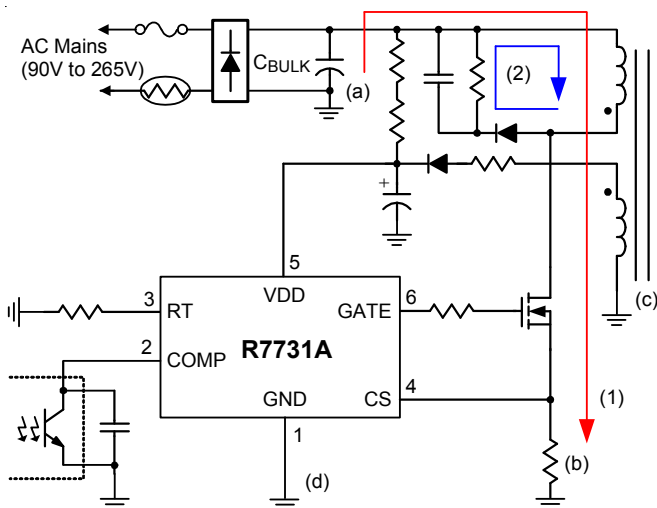
The current path (1) from bulk capacitor, transformer, MOSFET, Rcs return to bulk capacitor is a huge high frequency current loop. It must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(2) from RCD snubber circuit to MOSFET is also a high switching loop, too. So keep it as small as possible.

It is good for reducing noise, output ripple and EMI issue to separate ground traces of bulk capacitor(a),

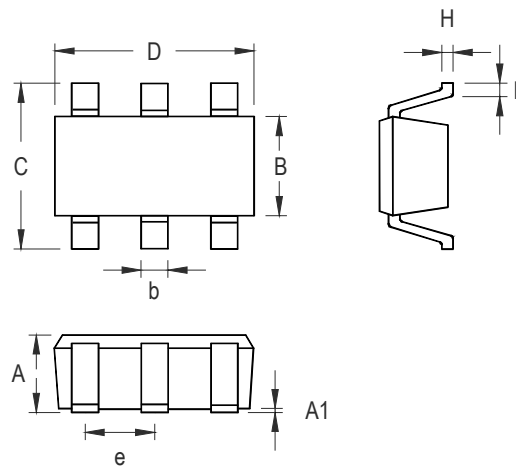
MOSFET(b), auxiliary winding(c) and IC control circuit (d). Finally, connect them together on bulk capacitor ground(a). The areas of these ground traces should be kept large.

Placing bypass capacitor for abating noise on IC is highly recommended. The bypass capacitor should be placed as close to controller as possible.

To minimize reflected trace inductance and EMI minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, provide sufficient copper area at the anode and cathode terminal of the diode for heatsinking. Provide a larger area at the quiet cathode terminal. A large anode area can increase high-frequency radiated EMI.

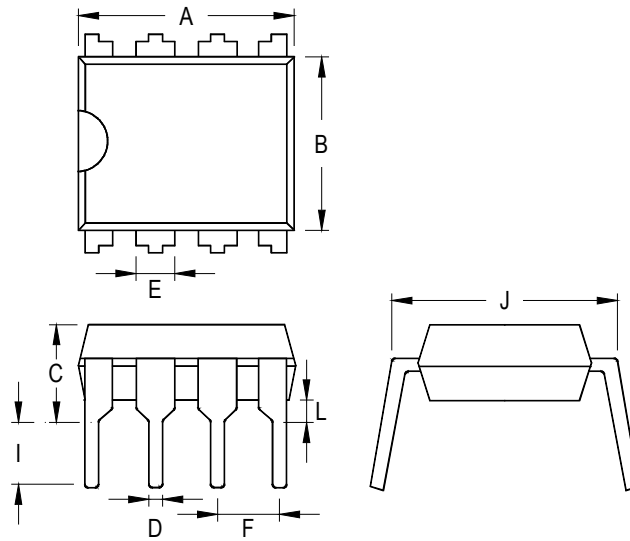


Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.889 | 1.295 | 0.031 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.250 | 0.560 | 0.010 | 0.022 |
| C | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

SOT-23-6 Surface Mount Package



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 9.068 | 9.627 | 0.357 | 0.379 |
| B | 6.198 | 6.604 | 0.244 | 0.260 |
| C | 3.556 | 4.318 | 0.140 | 0.170 |
| D | 0.356 | 0.559 | 0.014 | 0.022 |
| E | 1.397 | 1.651 | 0.055 | 0.065 |
| F | 2.337 | 2.743 | 0.092 | 0.108 |
| I | 3.048 | 3.556 | 0.120 | 0.140 |
| J | 7.366 | 8.255 | 0.290 | 0.325 |
| L | 0.381 | | 0.015 | |

8-Lead DIP Plastic Package

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