The Active Diode - Current-Driven Synchronous Rectifier

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Abstract- **A novel current-driven synchronous rectifier called the Active Diode is presented in this paper. This synchronous rectifier is independent of converter circuit topology and this is why it is called the Active Diode. The proposed current-driven synchronous rectifier can operate at high switching frequency with high efficiency thanks to the help of current sensing energy recovery circuit. Compared with conventional voltage-driven synchronous rectification solutions, the Active Diode has several outstanding characteristics. It can be easily applied to most switching topologies like an ideal diode. Constant gate drive voltage is obtained regardless of line and load fluctuation and makes it ideal in high input voltage range applications. Converters designed with the Active Diode are also capable of being connected in parallel without taking the risk of reverse power sinking. The principle of operation is given in the paper. A series of experiments verify the analysis and demonstrate the merits.**

I. INTRODUCTION

There is demand for low voltage high current power converters and synchronous rectification is a promising way to reduce losses on the high current secondary side.

Most synchronous rectification studies focus on conventional voltage-driven synchronous rectifier (SR)[5-7]. It makes use of the secondary winding to drive MOSFETs on the secondary side and produces low loss rectification.

Conventional SR is simple but there are many weaknesses as listed below.

1) Different switching topologies need different SR drive solutions [4-8]. Forward, flyback, half-bridge center tap or current doubler, each needs its specific drive method.

2) Gate drive voltage of voltage-driven SR is proportional to input voltage. In some wide input voltage range application, it's difficult to drive SR efficiently and safely in the whole input range. The MOSFET is never driven at an optimum gate drive voltage.

3) The gate drive voltage is prohibited by transformer leakage inductance in certain time period. This greatly jeopardizes efficiency at high switching frequencies.

4) Voltage-driven SR converter is not suitable to be connected in parallel [9]. Converters built with voltage-driven SR can either source or sink power. In particular, sinking power is not acceptable in parallel operation as power from the output goes back to the input through a sinking converter.

5) Discontinuous current mode (DCM) operation is lost because voltage-driven SR is theoretically a bi-directional switch. The control voltage signal contains no current information and continues to go negative at light load. This greatly reduces efficiency at light load.

6) Gate drive voltage is not always available to drive the SR. The gate voltage depends on the primary arrangement and may be lost after transformer reset. Active clamp circuit is needed which increases circuit complexity.

A current-driven synchronous rectifier seems to circumvent all the above-mentioned weaknesses. If the gate drive of the MOSFET depends on the current through itself rather than the voltage from somewhere and turns on when current flows in one direction and turns off when current attempts to flow in a reverse manner. All problems can be solved apparently.
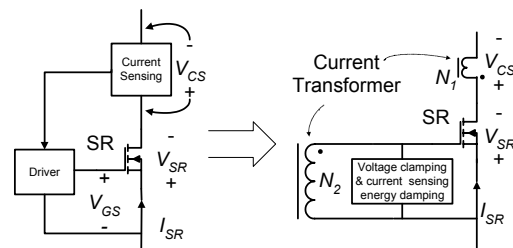

Fig.1 Conventional current-driven synchronous rectifier: block diagram & circuit implementation

The concept of current-driven synchronous rectifier was proposed more than ten years ago but it has never been popular. Feasible operation frequency reported is low, for example, 100kHz for a bipolar transistor SR [1] and 25kHz for a MOSFET SR [2]. The reported frequency range and SR performance obviously cannot meet the requirement of modern power conversion where efficiency and size are of primary concerns. Fig.1 shows the block diagram of a conventional current-driven SR. The current sensing circuit is dissipative and comparable to that of the MOSFET. To minimize this current sensing loss, voltage drop across current sensing part must be as small as possible. This immediately brings in problems because high gain high bandwidth amplification will be needed to produce the gate drive voltage. Such amplifier is too expensive to be implemented.

In this paper a novel current driven synchronous rectifier is presented. It solves the problem with amplification and produces operation near to an ideal diode. It recovers current sensing energy and relief the stringent requirement on amplification. It can be implemented to any topology and behaves like a diode. It is called the "Active Diode". The following sections explain the operation of this Active Diode followed by implementation to various topologies.
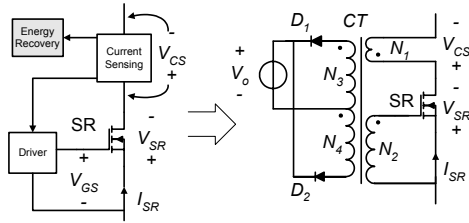
II. THE ACTIVE DIODE

Fig.2 Proposed current-driven synchronous rectifier: block diagram & circuit implementation

The novel Active Diode is shown in Fig.2. It consists of a circuit which recovers the current sensing energy. This circuit is implemented by a current transformer in series with a low loss MOSFET. There are 4 terminals. Two of them act as the anode and cathode of the Active Diode and the other two are connected to a voltage source to which the recovered energy is delivered.

Basic operation of this energy recovery current-driven synchronous rectifier is explained. When current I_{SR} flows through the source to drain of SR and N_1 winding of current transformer, current is induced in winding N_2 and turns on the SR. When the corresponding voltage in N_3 rises diode D_1 conducts and delivers energy to a DC voltage source. This DC source can be any DC voltage within a converter. Usually it is the converter DC output. As long as the SR current continues to flow in current transformer and the DC voltage is stable, the SR drive voltage is constant. When the SR forward current drops to zero and tends to go negative, Diode D_1 blocks and diode D_2 turns on to reset the core. Gate voltage of the SR goes negative and the SR shuts down. No reverse current is allowed to flow through SR. Characteristic of the proposed current-driven SR behaves like an ideal diode.

The circuit model in Fig 3 illustrates the behavior of this current-driven synchronous rectifier with waveforms. Some assumptions are made in the following analysis, trapezoidal waveform, typical in PWM converter, is assumed to flow through the SR. Later it will be demonstrated that this current-driven SR can actually work under almost all types of current waveforms in a switching converter. Current transformer is modeled as a perfectly coupled transformer with a magnetizing inductance L_M at N_2 winding. Leakage effect is omitted. SR MOSFET gate capacitance C_g is taken as a constant. Winding capacitance merges into gate capacitance as C_g. SR MOSFET is considered as an ideal switch with propagation delay omitted.
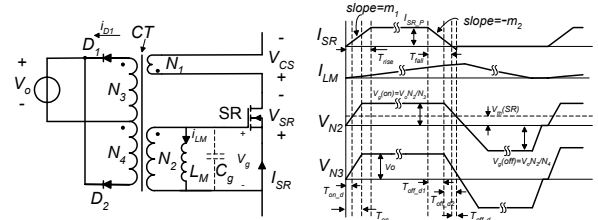
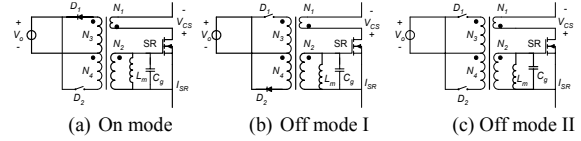Fig.3 Proposed current-driven SR: circuit model & critical waveforms

(a) On mode   (b) Off mode I   (c) Off mode II

Fig.4 Steady state operation of energy recovered current driven SR:

§2.1 STEADY STATE ANALYSIS

Steady state represents the operation period when the current-driven SR is driven fully on or fully off after switching transition period.

On Mode: This mode is shown in Fig.4(a). SR current flows into N_1 winding of current transformer and the reflected current flows out through two paths. One goes through N_3 winding and diode D_1 to DC voltage V_o. The other one goes through N_2 winding as magnetizing current. Winding N_1 and N_2 is clamped by DC source V_o. During this period, magnetizing current builds up linearly. The following equations can be obtained:

$$V_g(on) = V_o \times \frac{N_2}{N_3} \tag{1}$$

$$i_{Lm}(t) = \frac{V_g(on)}{L_m}t = \frac{V_o}{L_m} \times \frac{N_2}{N_3}t \quad ; \quad 0 \le t \le DT_S \tag{2}$$

$$I_{Lm\_max} = \frac{V_o}{L_m} \times \frac{N_2}{N_3}DT_S \tag{3}$$

$$i_{D1}(t) = \frac{N_2}{N_3}\left[I_{SR\_P} \times \frac{N_1}{N_2} - i_{Lm}(t)\right] \tag{4}$$

where I_{SR_P} is the peak forward SR current as illustrated in Fig.4(b), D is the equivalent duty cycle of this SR, T_s is the switching period, $N_1 \sim N_4$ are numbers of turn of four windings. Other parameters are in Fig.3.

The magnetizing current must be controlled. Gate drive voltage is represented by (1). The maximum magnetizing current can be found by (3). Current transformer should not saturate at this maximum current. To ensure SR safely turn on, current in diode D_1 should always conduct so as to clamp SR gate voltage. If magnetizing current goes so high so that it takes over the whole reflected current, diode D_1 will shut down and gate voltage will resonate back to zero. To avoid this,

$$I_{Lm\_max} \le I_{SR\_P} \frac{N_1}{N_2} \qquad (5)$$

From (3) and (5), we can find the minimal magnetizing inductance.

$$L_m \ge \frac{V_o \cdot DT_S \cdot N_2^2}{I_{SR\_P} \cdot N_1 \cdot N_3} \qquad (6)$$

In a practical design, the maximal magnetizing current is usually much smaller than the reflected winding current $I_{SR\_P} \times \frac{N_1}{N_2}$, so (4) can be simplified as:

$$i_{D1}(t) \approx I_{SR\_P} \times \frac{N_1}{N_3} \qquad (7)$$

OFF Mode I: This mode is shown in Fig.4(b). When current flows through SR drops to the point that is insufficient to sustain magnetizing current, reset winding N_4 and diode D_2 conducts and takes over magnetizing energy while diode D_1 and winding N_3 does not conduct. Again winding N_2 is clamped by V_o. SR drive voltage is now negative. Magnetizing current decreases linearly until it reaches zero. This is described by the following equations:

$$V_g(off) = -V_o \times \frac{N_2}{N_4} \qquad (8)$$

$$i_{Lm}(t) = I_{Lm\_max} - \frac{V_g(off)}{L_m}(t - DT_S) \qquad (9)$$

To ensure magnetic reset, magnetizing current should drop to zero before the next switching cycle. From (3), (8), (9), we can get the following constrain for winding turn ratio and duty cycle,

$$D \le \frac{N_3}{N_3 + N_4} \qquad (10)$$

OFF Stage II: This mode is shown in Fig.4(c). When magnetizing current resets to zero, diode D_2 blocks. In winding N_2, SR gate capacitance resonates with magnetizing inductance. The SR gate voltage drops to zero and then remains around zero. Some damping network should be added in practice to absorb the excessive resonant energy in case drive voltage goes beyond SR threshold voltage and falsely triggers the SR on.

Extra energy loss during steady state mainly comes from the current flowing through diode D_1. The current transformer can be designed with high efficiency due to magnetizing energy recovery. Loss due to current flowing thorough diode D_2 can be neglected because magnetizing energy is usually much smaller than the current sensing energy.

$$P_{Loss\_D1} = V_{F\_D1} \times I_{D1} \times D = V_{F\_D1} \times I_{SR\_P} \times \frac{N_1}{N_3} D \quad (11)$$

where V_{F_D1} is the forward voltage drop of diode D_1.

§2.2 TRANSIENT ANALYSIS

Transient analysis describes the SR operation during switching transition period. This period is short compared with the switching period but it more or less determines the overall performance of the SR. Any timing discrepancy between current and gate drive voltage will introduce either
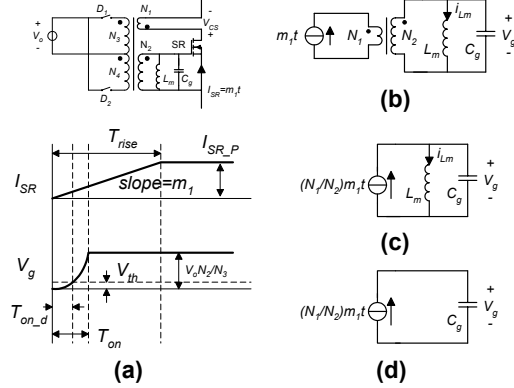
Fig.5 Turn on transient equivalent circuit (a) circuit model and critical waveforms (b) turn on circuit model (c) turn on equivalent circuit (d) simplified turn on equivalent circuit

SR body diode conduction loss or cross-conduction loss. Turn on and turn off transition is described as follows.

§2.2.1 TURN ON TRANSIENT

At the turn on transient, a rising current with slope m_1 flows into the SR and current transformer. This slope is usually determined by the external applied voltage and the parasitic inductance in the rectification loop. Fig.5(a)shows that when this SR current starts to build up, the coupled current in current transformer first flows out from N_2 winding and charges up the SR gate. N_3 and N_4 windings don't conduct. Equivalent circuit can be redrawn as Fig.5(b) and Fig.5(c). The turn on transient occupies only a small part of the switching period and magnetizing current cannot build up instantly within such a short period. The magnetizing inductance with zero initial current can be regarded as an open circuit. Equivalent circuit can be further simplified to Fig.5(d) with the following simplified expressions,

$$v_g(t) = \frac{1}{C_g} \int_0^t m_1 \frac{N_1}{N_2} t dt = \frac{1}{2C_g} m_1 \frac{N_1}{N_2} t^2 \qquad (12)$$

$$T_{on\_d} = \sqrt{\frac{2V_{th} C_g N_2}{m_1 N_1}} \qquad (13)$$

$$T_{on} = \sqrt{\frac{2V_o C_g N_2^2}{m_1 N_1 N_3}} \tag{14}$$

where V_{th} is threshold voltage of SR MOSFET, T_{on_d} is defined as the time period from the time when SR current starts to flow into current transformer to the time SR gate voltage reaches beyond SR threshold voltage V_{th}. Turn on time T_{on} is defined as the time when SR current starts to build up to the time gate voltage reaches the clamped voltage $V_o \frac{N_2}{N_3}$.

Usually the SR current rising time T_{rise} is much longer than T_{on}. So the case when T_{on} is shorter than T_{rise} is omitted in the analysis as it can be determined following the same procedure.

The analysis above shows that the SR gate capacitance C_g is a critical parameter that would influence turn on delay time. Smaller gate capacitance will speed up turn on process. Low SR MOSFET threshold voltage and high current slope rate can also help to decrease turn on delay time.

It should be noted here that this turn on process is always a zero-voltage-switching process because body diode of the SR conducts before the time gate drive voltage is applied.

Body diode conduction loss P_{BD_on} due to turn on delay can be expressed as (15). To address the extra loss caused by SR body diode conduction, SR resistive loss (16) during this turn on transient should be deducted. Then this extra loss becomes (17).

$$P_{BD\_on} = \frac{m_1 T_{on\_d}^2 V_{F\_BD}}{2T_S} \tag{15}$$

$$P_{SR\_on} = \frac{1}{T_S} \int_0^{T_{on\_d}} (m_1 t)^2 R_{ds\_on} dt = \frac{m_1^2}{3T_S} T_{on\_d}^3 R_{ds\_on} \tag{16}$$

$$P_{extra\_loss\_on} = P_{BD\_on} - P_{SR\_on} \tag{17}$$

where V_{F_BD} is the voltage drop of SR body diode, R_{ds_on} is the SR turn on resistance.

§2.2.2 TURN OFF TRANSIENT

Turn off transient analysis begins at the time when current flowing through SR starts to decline at a rate of $-m_2$ and ends at the time when gate voltage goes negative and is clamped by N_4 winding and V_o. Fig.6 shows that there are two operation modes during this transient.

Turn off mode I: The circuit diagram is shown in Fig.6(a). Diode D_1 is conducting and delivers energy to V_o. Gate drive voltage is clamped by winding N_3 and V_o. Current of Diode D_1 is dropping accordingly to the falling SR current.

Turn off mode II: When the current in diode D_1 drops to zero, D_1 blocks and the circuit model changes to Fig.6(b). Now N_1 reflected current is less than magnetizing current. There is a resonance in N_2 winding between the magnetizing inductance and gate capacitance.

Critical waveforms during this turn off transient is shown in Fig.6(c). T_{off_d1} is defined as the time period from SR current starts to drop until it drops to the reflected magnetizing current and diode D_1 blocks. T_{off_d2} is defined as the time period from this point to the time when SR voltage drops to its threshold voltage. T_{fall} is defined as the duration SR current drops from its steady state value to zero.
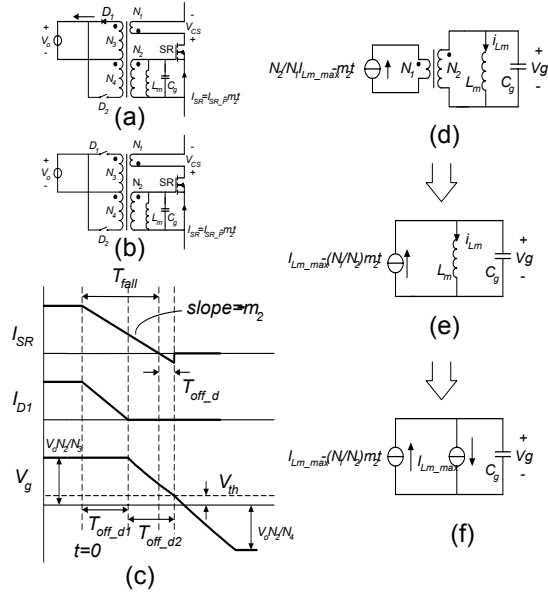

Fig.6 Circuit modes and waveforms at turn off transient (a) turn off mode I (b) turn off mode II (c) critical waveforms during turn off transient (d)-(f) equivalent models at turn off mode II

T_{off_d} is defined as the time duration from SR current reaches zero until SR voltage drops below its threshold voltage and SR shuts down. It can be shown that,

$$T_{off\_d} = T_{off\_d1} + T_{off\_d2} - T_{fall} \tag{18}$$

$$T_{fall} = \frac{I_{SR\_P}}{m_2} \tag{19}$$

$$T_{off\_d1} = \frac{I_{SR\_P} - \frac{N_2}{N_1} \cdot I_{Lm\_max}}{m_2} \tag{20}$$

To find T_{off_d2}, let's consider its equivalent circuit as shown in Fig.6(d) which is equivalent to Fig.6(e).

Analysis can be simplified when we consider the magnetizing inductance is large and magnetizing current keeps constant during this transient. Fig.6(f) represents the inductance as a current source. Then, we can get the following simplified expressions,

$$v_g(t) = V_g(on) - \frac{1}{2C_g} \frac{N_1}{N_2} m_2 t^2 \qquad (21)$$

$$T_{off\_d2} = \sqrt{2 \cdot \frac{V_g(on) - V_{th}}{m_2} \cdot \frac{N_2}{N_1} \cdot C_g} \qquad (22)$$

$$T_{off\_d} = \sqrt{2 \cdot \frac{V_g(on) - V_{th}}{m_2} \cdot \frac{N_2}{N_1} C_g} - \frac{N_2}{N_1} \cdot \frac{V_g(on)}{m_2 L_m} \cdot DT_S$$

$$(23)$$

$$P_{extra\_loss\_off} = \frac{1}{T_S} \int_0^{T_{off\_d}} (m_2 t)^2 R_{ds\_on} dt = \frac{m_2^2}{3T_S} T_{off\_d}^3 R_{ds\_on}$$

$$(24)$$

(24) represents the extra loss due to SR turn off delay.

It should be noted that turn off delay time T_{off_d} as calculated from (23) is not necessarily positive. When negative T_{off_d} is obtained, it means SR MOSFET channel switches off before the time SR current drops to zero. In this case, the remaining SR current is carried by its internal body diode. This may occur in discontinuous conduction mode operation where m_2, is much smaller than in continuous conduction mode.

§2.3 Performance Evaluation

The transient analysis above illustrates that the proposed current-driven synchronous rectifier introduces extra loss compared with a normal synchronous rectifier with precise drive timing signal due to the turn on delay, turn off delay and conduction loss of Diode D_1. This total extra loss is:

$$P_{extra} = P_{loss\_D1} + P_{extra\_loss\_on} + P_{extra\_loss\_off}$$
$$= P_{loss\_D1} + P_{BD\_on} - P_{SR\_on} + P_{extra\_loss\_off} \qquad (25)$$
$$\approx P_{loss\_D1} + P_{BD\_on}$$

where $-P_{SR\_on}$ and $P_{extra\_loss\_off}$ partly cancel out each other. Bear in mind that both of these two items are much smaller than the first and second items so the total extra loss can be simplified as the SR body diode conduction loss during turn on period plus the diode D_1 conduction loss. From (1), (11), (13) and (15), this total extra loss can be expressed by:

$$P_{extra} = \frac{N_3}{N_1} \cdot \frac{V_{th} \cdot V_g(on) \cdot C_g \cdot V_{F\_BD}}{V_o \cdot T_S} + \frac{N_1}{N_3} \cdot V_{F\_D1} \cdot I_{SR\_P} \cdot D$$

$$(26)$$

It can be seen that an optimal N_3/N_1 turn ratio exists to get the minimal extra loss. This optimal turn ratio can be found by differentiating (26),

$$\frac{N_3}{N_1}\bigg|_{optimal} = \sqrt{\frac{D \cdot V_{F\_D1} \cdot V_o \cdot I_{SR\_P} \cdot T_S}{V_{th} \cdot V_g(on) \cdot V_{F\_BD} \cdot C_g}} \qquad (27)$$

$$P_{extra}\big|_{min} = 2\sqrt{\frac{V_{th} \cdot V_g(on) \cdot V_{F\_BD} \cdot V_{F\_D1} \cdot I_{SR\_P} \cdot C_g \cdot D}{V_o T_S}} \quad (28)$$

N_3 can be determined from (27). N_2 is determined by (1). And N_4 winding is determined by (10). Winding N_4 and diode D_2 only carry magnetizing energy. So low power components can be used.

From (11), we can also know that the energy delivery diode D_1 also suffers from extra conduction loss if the SR current is relatively high. To minimize this conduction loss, low voltage drop Schottky diode is usually prefered. Another choice is to replace D_1 with a SR. Fig.7 is one of the possible methods to drive the replaced SR.
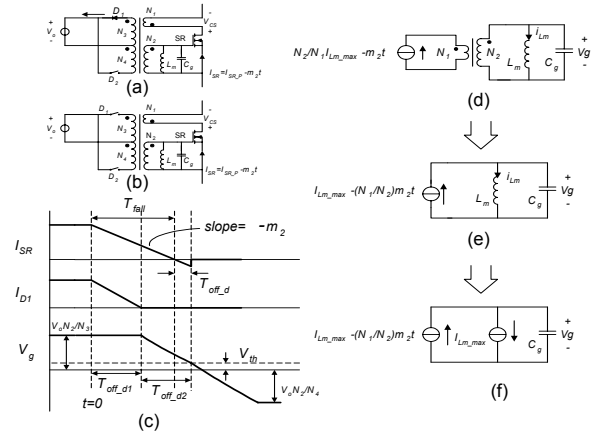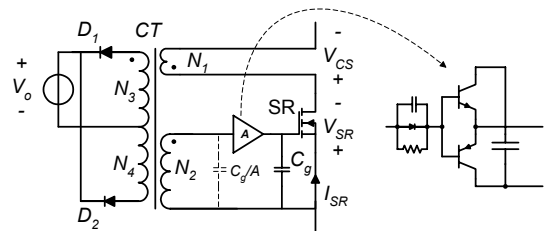

Fig.7 Replace D1 with a SR

Fig.8 Improve switching transition process with a driver

To further improve the performance of energy recovery current-driven synchronous rectifier so that it can be applied at high frequency, turn on and turn off delay time should be always kept as small as possible. A driver circuit as shown in Fig.8 can be added between the drive winding N_2 and SR gate capacitance to speed up the switching process. A simple *NPN-PNP* transistor totem pole driver can fulfill this task. As can be seen from (13) and (23), a critical parameter that affects both turn on and turn off delay time is the SR gate capacitance. Surely the smaller the gate capacitance is, the less the delay time. If the driver has current gain of A, effective input impedance of the driver is then C_g/A, hence turn on and turn off time can all be significantly reduced.

III. EXPERIMENTAL DEMONSTRATION

§3.1 Wide Input Range, CCM & DCM Operation

A flyback current-driven SR converter that operates at 80kHz switching frequency is built. Input voltage of this converter is from 90V to 315V (input range 3.5:1), the output is 5V with 3A maximal current. Current transformer is implemented with turn ratio of 3:80:40:8 ($N_1\sim N_4$). A driver circuit is added between N_2 winding and SR gate terminal to speed up turn on and turn off transient. SR MOSFET is implemented by HUF76113TST (30mΩ, 30V, Harris). Gate capacitance Cg of this MOSFET is measured through an impedance analyzer HP4194 under rated frequency and bias current. Current waveform is measured with Tektronix current probe TCP202. Fig.9 shows the waveforms captured when converter operates at 90V and 315V input, 5V/2.5A output. It can be seen clearly that the SR gate voltage properly builds up with respect to its current. A constant drive voltage of 10V is obtained at both low line and high line. At low line, the converter operates at continuous mode. At high line, the converter operates at discontinuous mode.

§3.2 Performance in Different Switching Topologies

The Active Diode module is implemented to different circuit topologies to demonstrate the fact that the proposed current-driven SR can be applied independent of topologies. Experiments are carried out with waveforms shown. Application of the Active Diode module into a switching topology is very easy. The module has four terminals. Two of which are just anode and cathode of SR. The left two terminals are energy recovery terminals to be connected to the DC output.
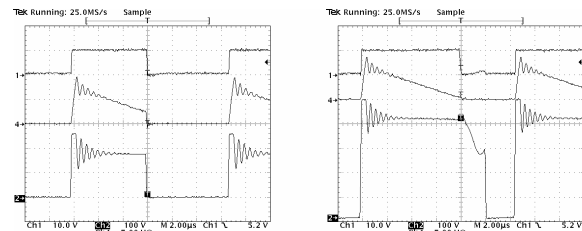
Ch1: SR gate drive voltage (10V/div)
Ch2: Primary drain voltage (100V/div)
Ch4: SR current (5A/div) Time: 2μs/div
Fig. 9   Flyback converter in CCM at low line & DCM at high line
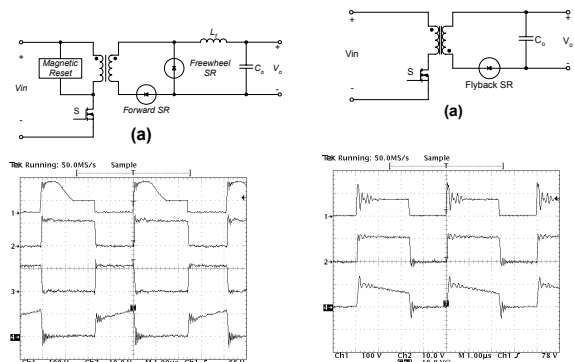
Ch1: Primary MOSFET Drain (100V/div)
Ch2: Freewheel SR gate voltage (10V/div)
Ch3: Forward SR gate voltage (10V/div)
Ch4: Forward SR current (10A/div)
Time: 1us/div

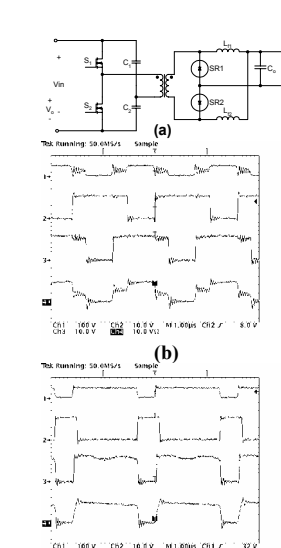Fig.10 48V input, 5V/10A output 250kHz Forward SR converter: (a) topology (b) waveforms
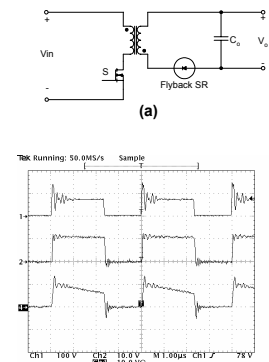
Ch1: Primary MOSFET Drain (100V/div)
Ch2: Flyback SR gate voltage (10V/div)
Ch4: Flyback SR current (10A/div)
Time: 1us/div

Fig.11 48V input, 5V/5A output, 250kHz Flyback SR converter: (a) topology (b) waveforms
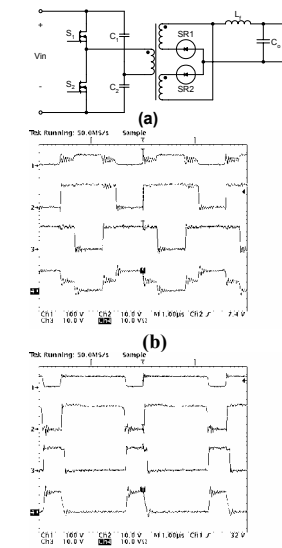
Ch1: Primary MOSFET Drain (100V/div)
Ch2: Gate voltage of SR1 (10V/div)
Ch3: Gate voltage of SR2 (10V/div)
Ch4: SR2 current (10A/div)
Time: 1us/div

Fig.12 48V input, 5V/10A output, 250kHz half-bridge center tap converter (a) topology (b) symmetric drive waveforms (c) asymmetric drive waveforms
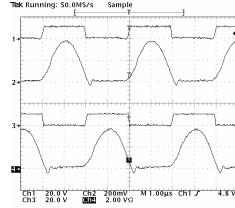
Ch1: Primary MOSFET Drain (100V/div)
Ch2: Gate voltage of SR1 (10V/div)
Ch3: Gate voltage of SR2 (10V/div)
Ch4: SR2 current (10A/div)
Time: 1us/div

Fig.13 48V input, 5V/10A output, 250kHz half-bridge current doubler converter (a) topology (b) symmetric drive waveforms (c) asymmetric drive waveforms
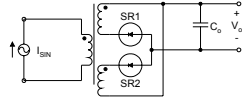
(a)

(b)
Ch1: Gate voltage of SR1 (20V/div)
Ch2: Current of SR1 (2A/div)
Ch3: Gate voltage of SR2 (20V/div)
Ch4: Current of SR2 (2A/div)
Time: (1us/div)
Fig.14 250kHz Sinusoidal full-wave
rectification (a) topology (b) waveforms

Five basic topologies, forward, flyback, half-bridge center-tapped, half-bridge current doubler, and sinusoidal full wave rectification as shown in Fig.10~Fig.14 are evaluated. All converters operate at the same switching frequency of 250kHz. Converters shown in Fig.10~Fig.13 all have 48V input, 5V/10A output except the flyback converter whose output is 5V/5A for fair comparison. The measured waveforms are shown. Fig.12(b) and Fig.13(b) should be especially highlighted. With conventional voltage-driven solution, it is difficult to drive the two SRs in symmetric drive half-bridge center tap and current doubler topologies. Waveforms of sinusoidal input full wave rectification converter are shown in Fig.14. Sinusoidal SR current is typical in various resonant topologies. SR gate drive voltage can also build up properly with respect to sinusoidal current.

In all these experiments, drive voltage is self-derived from the current signal. Current-driven SR module works very much like a diode rectifier. Measure efficiency of 5V/10A forward converter at typical line full load is around 91%[10].

§3.3 Paralleling of Active Diode Converters

A conventional voltage-driven SR converter is not suitable to be connected in parallel directly. The reason is that SR MOSFET is a bi-directional switch that allows both forward and reverse current flow. If two voltage-driven SR converters are paralleled together, in some extreme cases, one converter provides power while the other sinks the power. Usually it may cause destructive reverse current.

When the Active Diode is used in a converter design, no reverse power is allowed to flow into a converter because of its diode like characteristic.

Converter paralleling experiments is performed as follow. Two 5V output current-driven SR forward converters are paralleled as Fig. 15 (a). Each of them has its independent control loop. Their input terminals are connected in parallel to the 48V line voltage. Two current-driven SR forward converters are paralleled to supply a 10A constant current load. Ouput current of each converter is adjustable. Current of freewheeling SRs in the two converters are measured and shown in Fig.15 (b)-(f). In Fig.15(b) and (f), one converter provides all output power and the other completely shuts down. In Fig.15(c) and (e), one converter operates at discontinuous mode and the other provides most of the power. In Fig.15(d), each of the two converters provides around half of the total power. In all cases, no dangerous reverse power flows into a parallel connected Active Diode converter.

IV. CONCLUSION

A novel high frequency current-driven synchronous rectifier is proposed and analyzed. Compared with the existing synchronous rectification solutions, this proposed synchronous rectifier has several outstanding characteristics.

Firstly, it provides a universal approach to drive a synchronous rectifier in most switching topologies. It is a four-terminal device with two terminals of anode and cathode as a diode and the other two connected to DC output. It can be easily applied in various topologies such as forward, flyback, half-bridge center tap, half-bridge current doubler and resonant topologies.

Secondly, the proposed current-driven SR has constant drive voltage during line voltage variation. This makes it desirable in high input range application. The SR drive voltage is also easily programmable by adjusting winding turn ratio.

Thirdly, converters built with this current-driven SR can be connected in parallel without taking the risk of reverse power sinking.

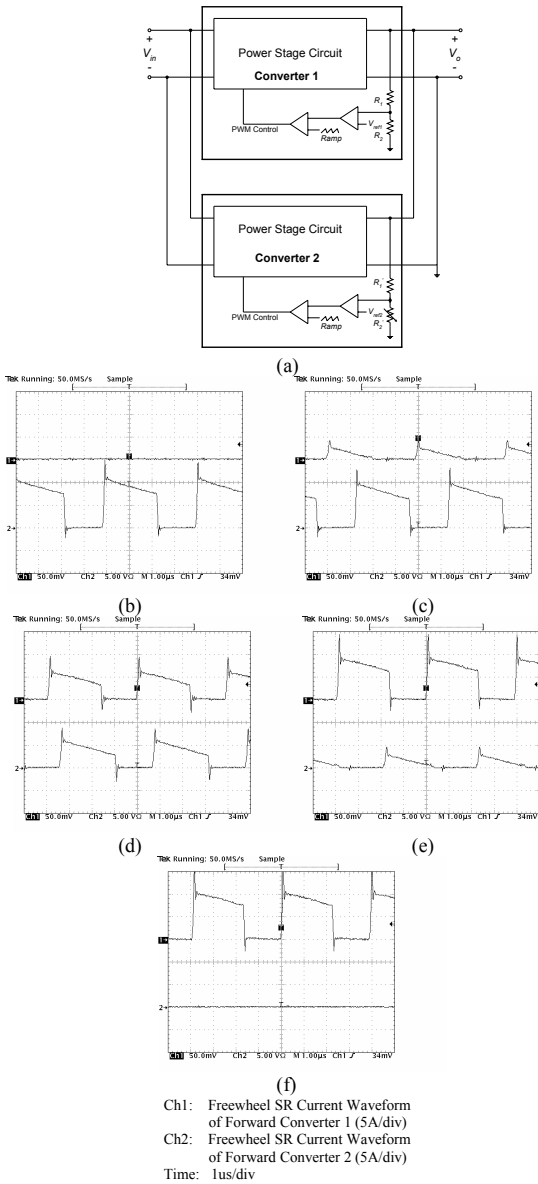These advantages are fully demonstrated through a series of experiments.

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(a)

(b)   (c)

(d)   (e)

(f)

Ch1:   Freewheel SR Current Waveform
       of Forward Converter 1 (5A/div)
Ch2:   Freewheel SR Current Waveform
       of Forward Converter 2 (5A/div)
Time: 1us/div

Fig.15   (a) Paralleling Two Current-Driven SR Converters
          (b)-(f) Measured current contribution of two converters

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