Digital Signal Detector Interface IC

PS202

General Description

The detector Integrated circuit is designed for interfacing Passive sensors with microcontrollers or processors. A single wire Data Out, Clock In (DOCI) interface is provided for interfacing with a micro-controller. Multiple devices can easily be operated at the same time. One element connect directly to the inputs. Pull down resistors and DC decoupling circuitry is integrated on chip. The signal is converted to a 14 bit digital value. A digital second order Butterworth low-pass filter removes unwanted higher frequency content. The 14 bit output signal from the filter is supplied to an external microcontroller through the DOCI interface.

Features

Digital Signal Processing (DSP)
Differential inputs
Single wire serial interface (DOCITM)
Operating voltage down to 3V
Low current consumption
High dynamic range
High supply rejection
High input impedance(
Direct connection to the MCU

Applications

Mobile Phone
CCTV Set
USB Alarm
Lan Camera
Lan Monitor
Personal Alarm
Super Car Alarm
Multi Sensor Detectors
Pyroelectric sensor

Device Pin out

Pin No.	Name	Description
1	Vdd	Positive supply
2	IN1	Sensor input 1
3	IN2	Sensor input 2
4	Vss	Supply ground
5	DOCI	Data Out Clock In, Serial interface
6	TEST	Reserved test mode, connect to VSS
7	TCLK	Chip test clock input, can be left open or tied to VSS
8	Vss	Supply ground

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage	V_{DD}	−0.3	5.5	V	
Operating Temp	T_{ST}	−20	70	˚C	
Storage Temp	T_{ST}	−40	125	˚C	

Stresses beyond those listed above may cause permanent damage to the device.

Exposure to absolute maximum ratings may affect the device reliability.

Operating Conditions (T=25˚C, VDD=5V, unless stated otherwise)

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Supply Voltage	V_{DD}	3.0	5	5.5	V	DC
Supply Current	I_{DD}		30	40	µA	V_{DD}=5V
Digital DOCI Interface						
Input low voltage	V_{IL}			20	%V_{DD}	
Input high voltage	V_{IH}	80			%V_{DD}	
Pull up / down current		220	280	350	µA	Input to V_{SS} / V_{DD}
Input capacitance *	C_I		5		pF	
Data setup time *	ts	2				1/FCLK
Data clock low time*	t_L	200			ns	
Data clock high time*	t_H	200			ns	
Data bit settling time*	tbit	1			µs	CLOAD = 10pF
Serial Interface update time	TREP		256		˚	1/FCLK
Analog Inputs IN1/IN2,						
Input leakage *	V_{IN} = -10mV .. +10mV		−1		1	fA
Input voltage range	Differential Common mode		−50 −100		50 100	mV mV
Digital converter						
ADC Resolution				14	Bits	Max Count = 2^14
ADC Sensitivity		6	6.5	7	µV/count	
ADC Temperature Coefficient **	Tc	-300		300	ppm/K	
RMS output noise referred to input **	@ 0.5Hz @ 1Hz @ 2Hz @ 5Hz		2.5 1.5 0.5 0.4		µV µV µV µV	
ADC Offset		6200	8250	11000		counts
Oscillator and Filter						
LPF cutoff frequency*			10		Hz	
A/D Conversion time	T_{REP}		256		1/F_{CLK}	
Internal clock	F_{CLK}	60	70	90	kHz	

frequency						

*) Guaranteed by Design, not tested within production.

**) Characterized and verified during evaluation/qualification, not tested within production.

All voltages are referred to Vss, unless otherwise specified.

Currents are positive when flowing into the node, unless otherwise specified.

T=25°C, unless stated otherwise

Parameters are guaranteed within the range of operating conditions unless otherwise specified.

Functional Description

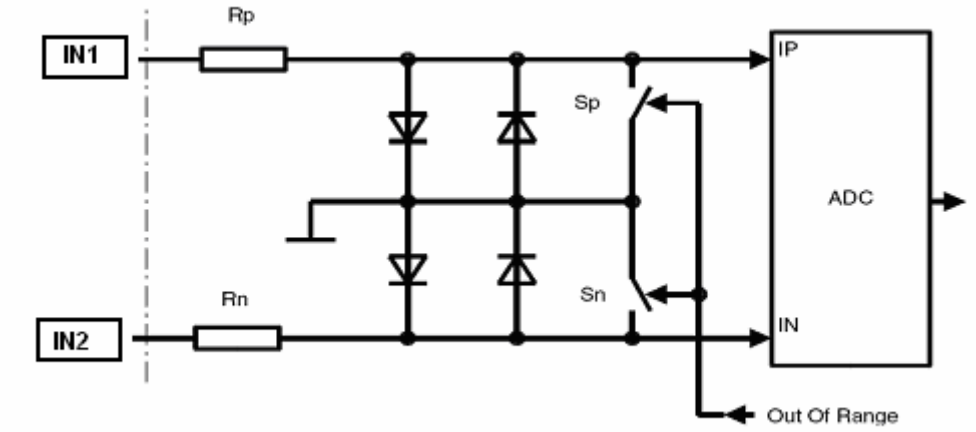

Fig .1 ADC Input Stage

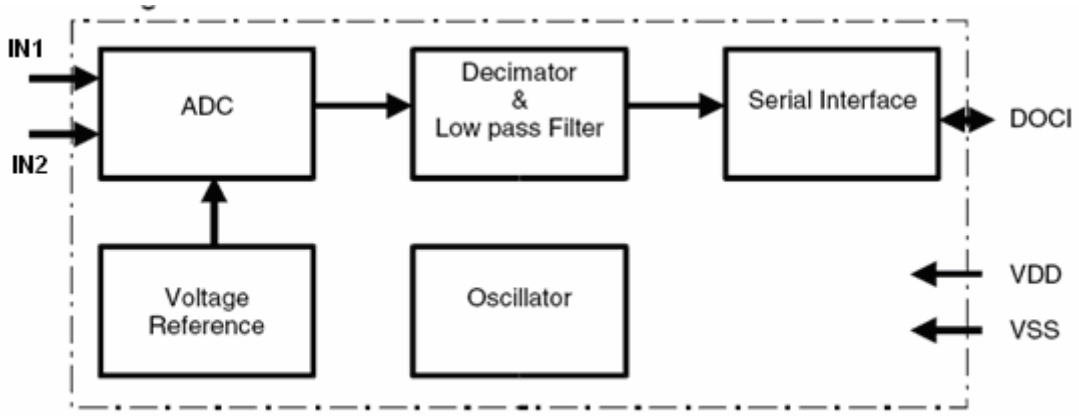

Fig. 2 PS202 Interior Function

1,Oscillator

The IC contains an on chip low power oscillator, with a frequency of 70kHz. All time related signals and the cutoff frequency of the digital filter are related to the oscillator's frequency.

2,Analog to Digital Conversion

The analog to digital converter (ADC) generates a digital signal from the voltage level measured between the human sensor terminals.

3, Decimator and Low Pass Filter

A second order Butterworth low pass filter removes unwanted higher frequency components and provides a 14 bit value. The MSB is usually “0” as the ADC ranges from 0 to 16384.

4, Serial Interface

Data is transferred from the filter to the output data latch whenever the filter has new data available and the output latch is not being read. If the micro controller reads the register faster than the update rate of the filter, the data read is ‘all zeros’. The start of a read cycle is indicated by the PS202 by pulling DOCI (Data Out, Clock In) high. The microcontroller must wait for 25µs. It then generates a low to high transition on the DOCI line, before it samples the data bit. The first bit read is the MSB, which is usually “0”. This process is repeated until all 14 bits have been read. After the last bit is read, the microcontroller must force low level and subsequently release DOCI. When a new filter value is generated, the PS202 will pull the DOCI line high and a new data byte can be read. If reading is interrupted for more than 256 system clocks with the DOCI interface at low level, the output data latch is updated with a new filter value. Reading can be interrupted, while the DOCI interface is forced high. The output latch is not updated in this condition.

5,Out Of Range Detection

The dynamic range of the ADC Input stage is approx. +/- 50mV. To avoid saturation, the PS202 contains an out of range detection logic, which detects values above 15872 (97% of range) and below 511 (3% of range). If the values are outside this range, the switches SP and SN are closed for the duration of 512 system clocks. This ensures fast settling after disturbances. The input impedance of the actual ADC (IP / IN) is practically infinite.

6, DOCI Protocol

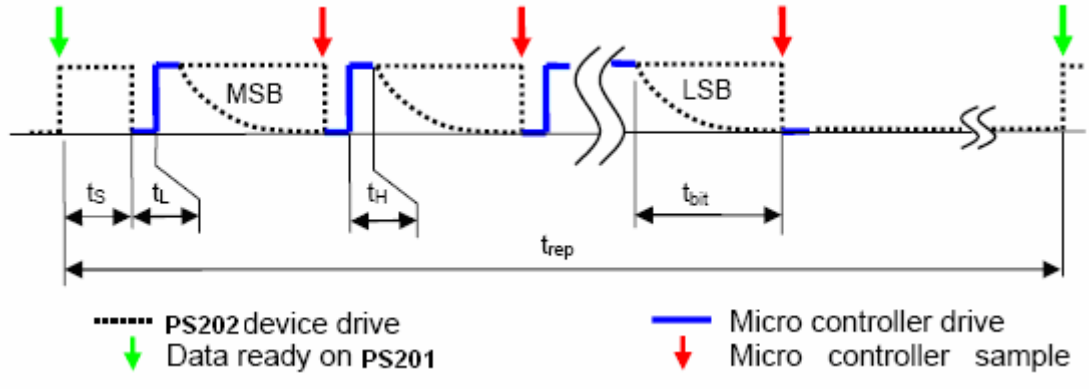

Fig. 3 PS202 DOCI Protocol

7,Out Of Range Detection

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Typical Output Curve

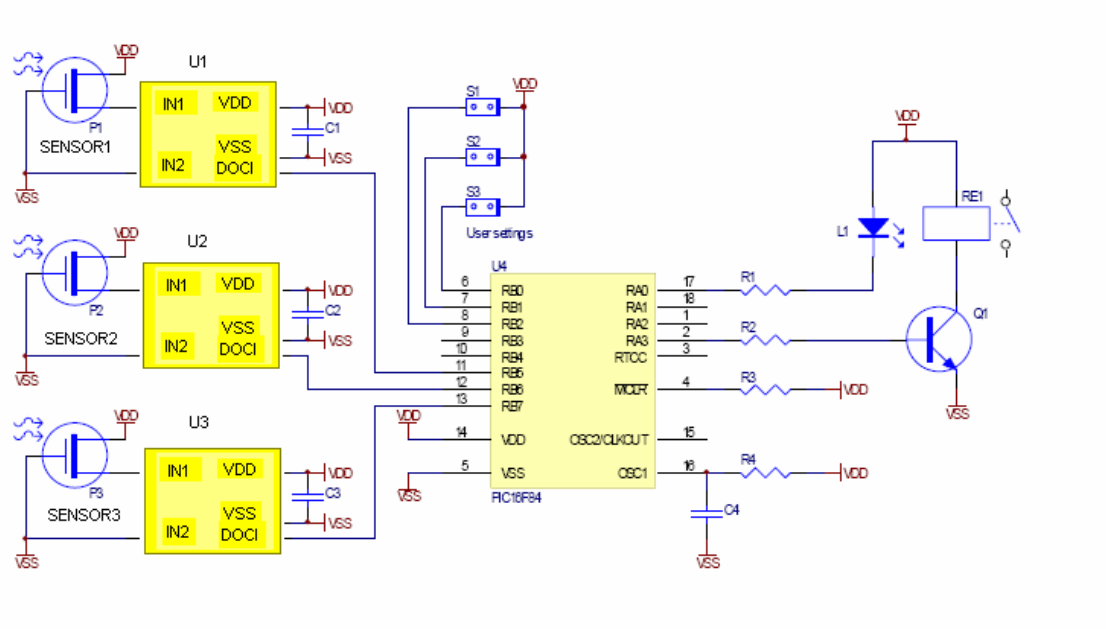

Fig. 4 PS202 Typical Output Curve

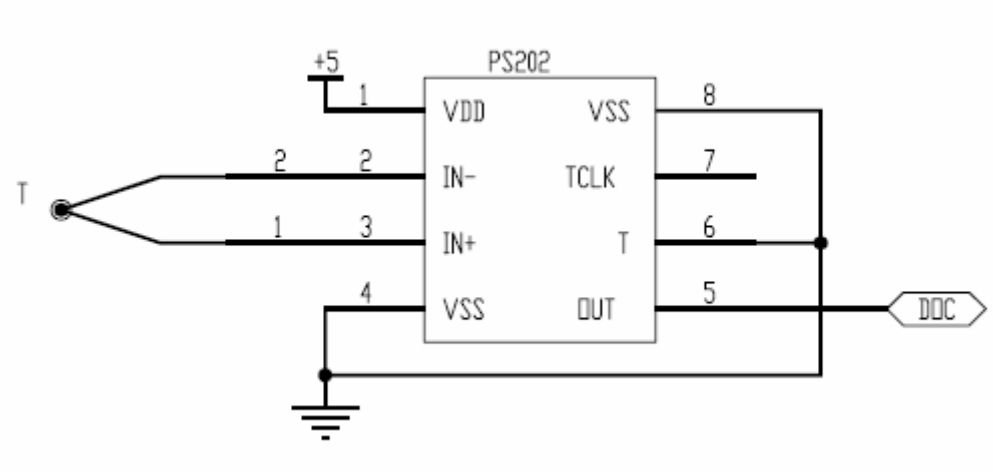

Fig. 5 PS202 Typical for Thermocouple Output Curve

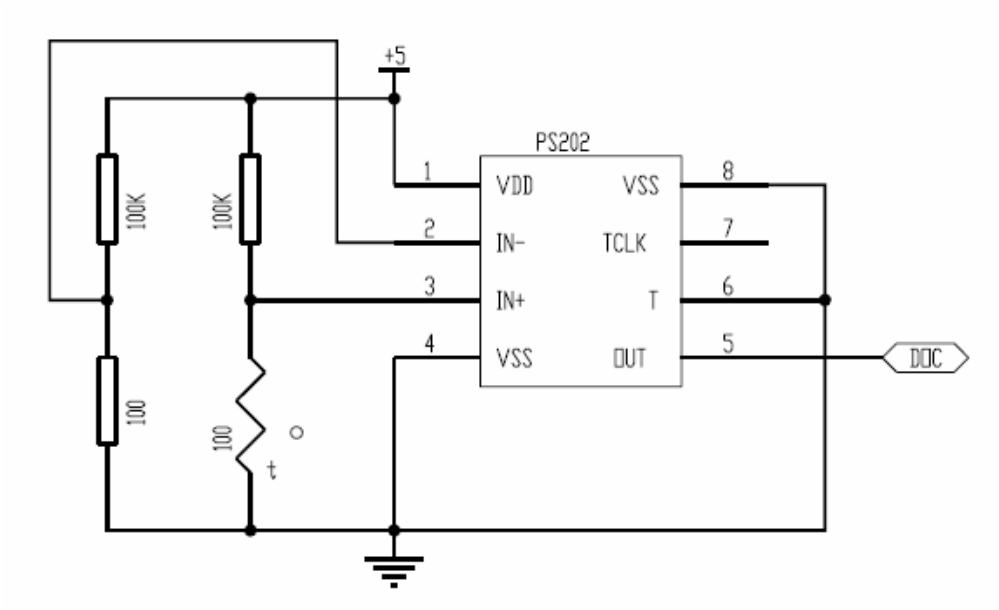

Fig. 6 PS202 Typical for Thermistor (PTC/NTC) Output Curve

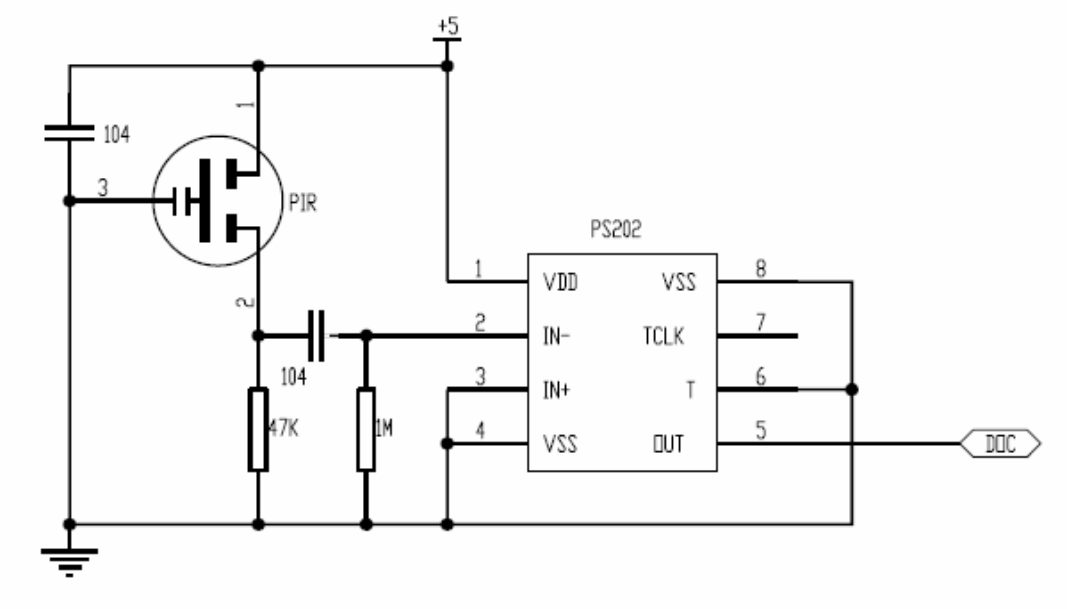

Fig. 7 PS202 Typical for PIR Sensor Output Curve

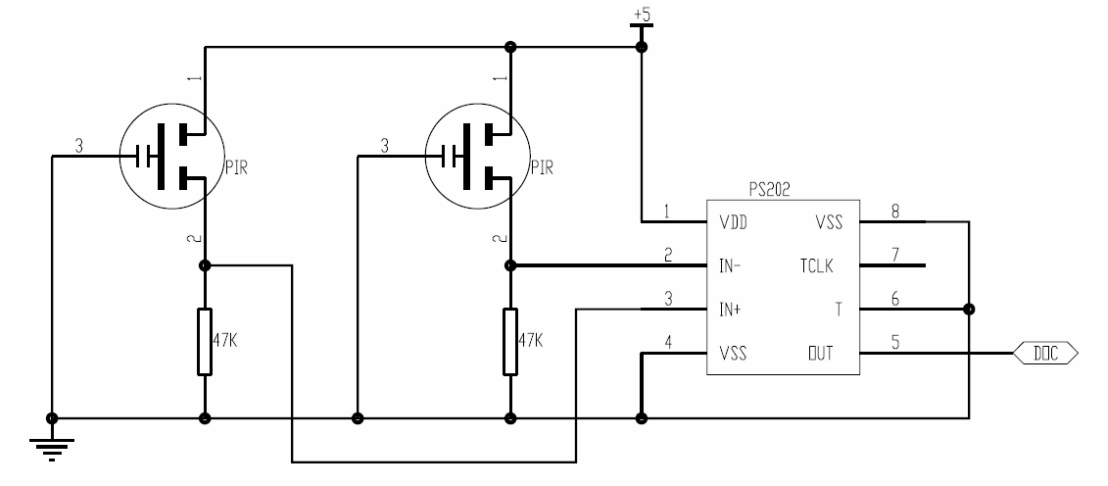

Fig. 8 PS202 Typical for Double PIR Sensor Output Curve

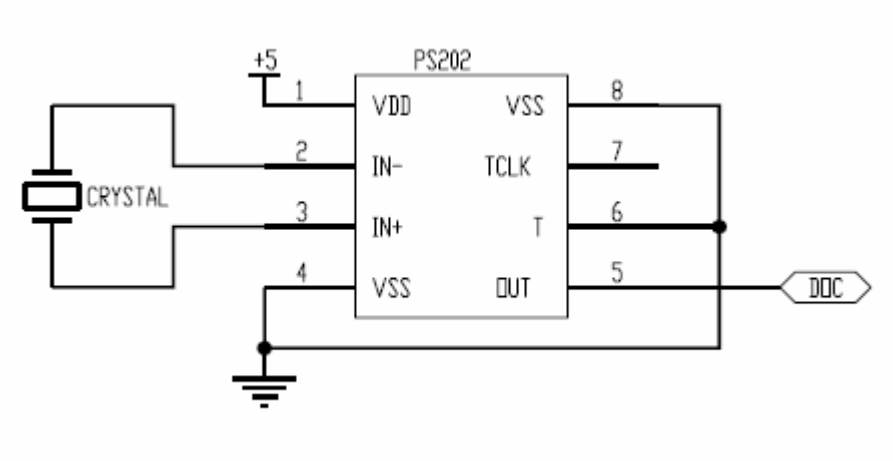

Fig. 9 PS202 Typical for Crysta l(Piezoelectric Ceramic)material Output Curve

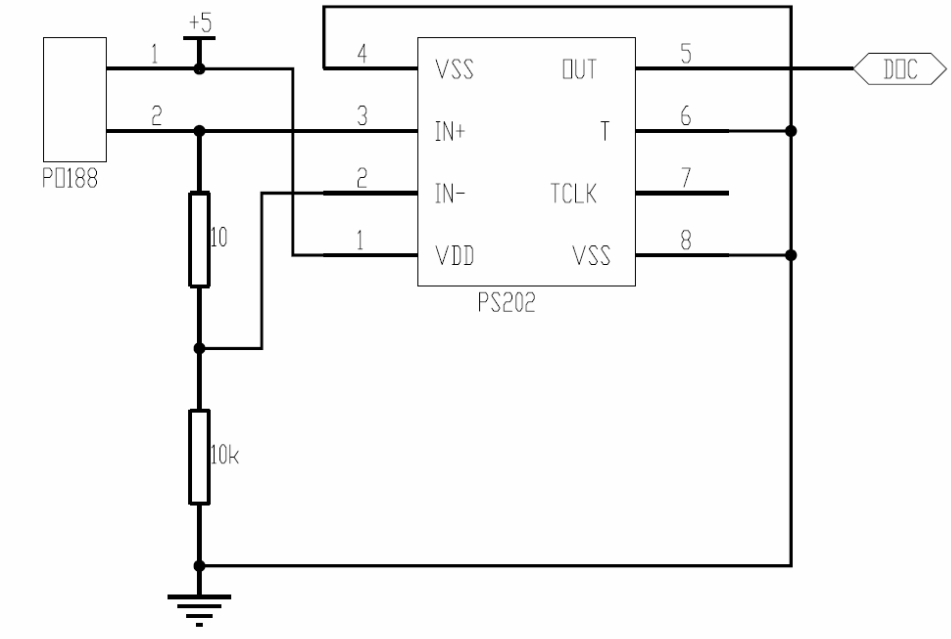

Fig. 10 PS202 Typical for Po188 light sensor Output Curve

Package Size

SOP 8 type packaga

Announce

1.All kinds of disturb from circumstance engender misinformation, and there out bring economy loss, detector manufacturer don't assume responsibility.

2.This detector can't be used in lawless situation and privacy situation.

The detector manufacture isn't charged with using the detector in these situations.

3. All the materials are compatible with RoHS.

4. If the specification is modified in future, forgive us not to inform you.