FAIRCHILD SEMICONDUCTOR®

August 2010

FAN103
Primary-Side-Regulation PWM Controller (PWM-PSR)

Features

- Low Standby Power Under 30mW
- High Voltage Startup
- Fewest External Component Counts
- Constant-Voltage (CV) and Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Green-Mode Function: Linearly-Decreasing PWM Frequency
- Fixed PWM Frequency at 50kHz with Frequency Hopping to Solve EMI Problem
- Cable Compensation in CV Mode
- Peak-Current-Mode Control in CV Mode
- Cycle-by-Cycle Current Limiting
- V_{DD} Over-Voltage Protection with Auto Restart
- V_{DD} Under-Voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 15V
- Fixed Over-Temperature Protection with Auto Restart
- Available in the 8-Lead SOP Package

Applications

- Battery chargers for cellular phones, cordless phones, PDA, digital cameras, power tools, etc.
- Replaces linear transformer and RCC SMPS

Description

This third-generation Primary-Side-Regulation (PSR) and highly integrated PWM controller provides several features to enhance the performance of low-power flyback converters. The proprietary topology, TRUECURRENT™, of FAN103 enables precise CC regulation and simplified circuit for battery charger applications. A low-cost, smaller and lighter charger results as compared to a conventional design or a linear transformer.

To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease PWM frequency under light-load conditions. This green mode assists the power supply in meeting the power conservation requirement.

By using the FAN103, a charger can be implemented with few external components and minimized cost. A typical output CV/CC characteristic envelope is shown in Figure 1.

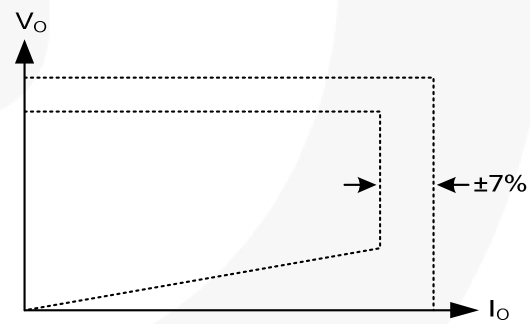


Figure 1. Typical Output V-I Characteristic

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN103MY	-40°C to +105°C	8-Lead, Small Outline Package (SOP-8)	Tape & Reel

Application Diagram

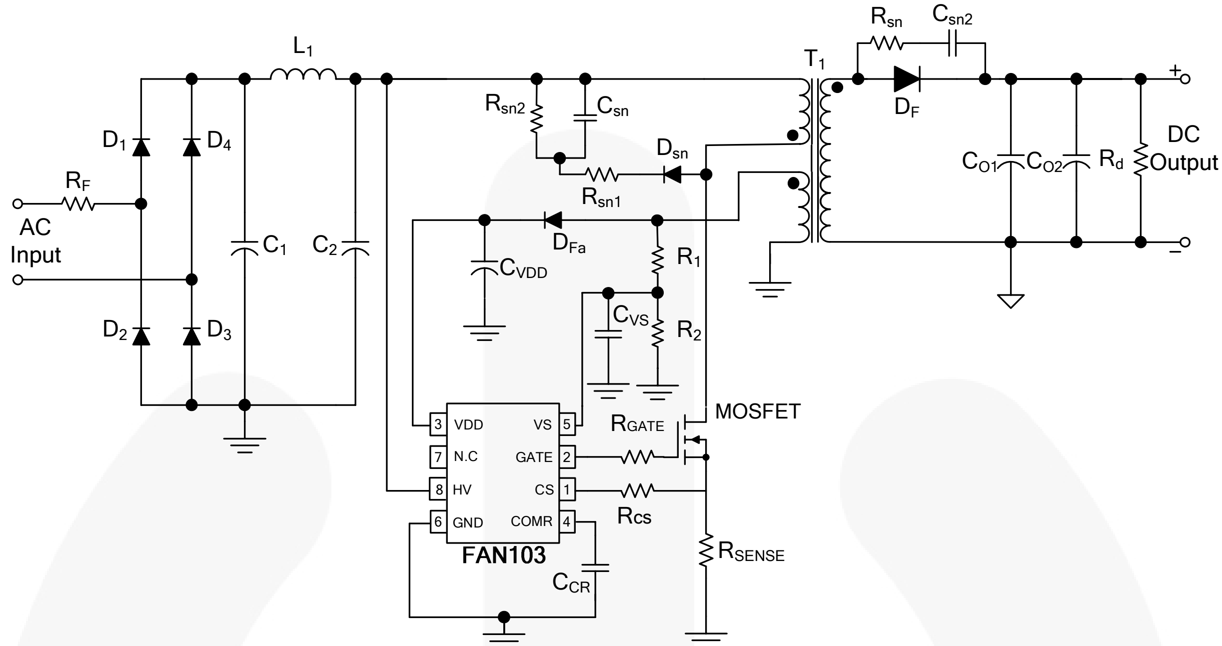


Figure 2. Typical Application

Internal Block Diagram

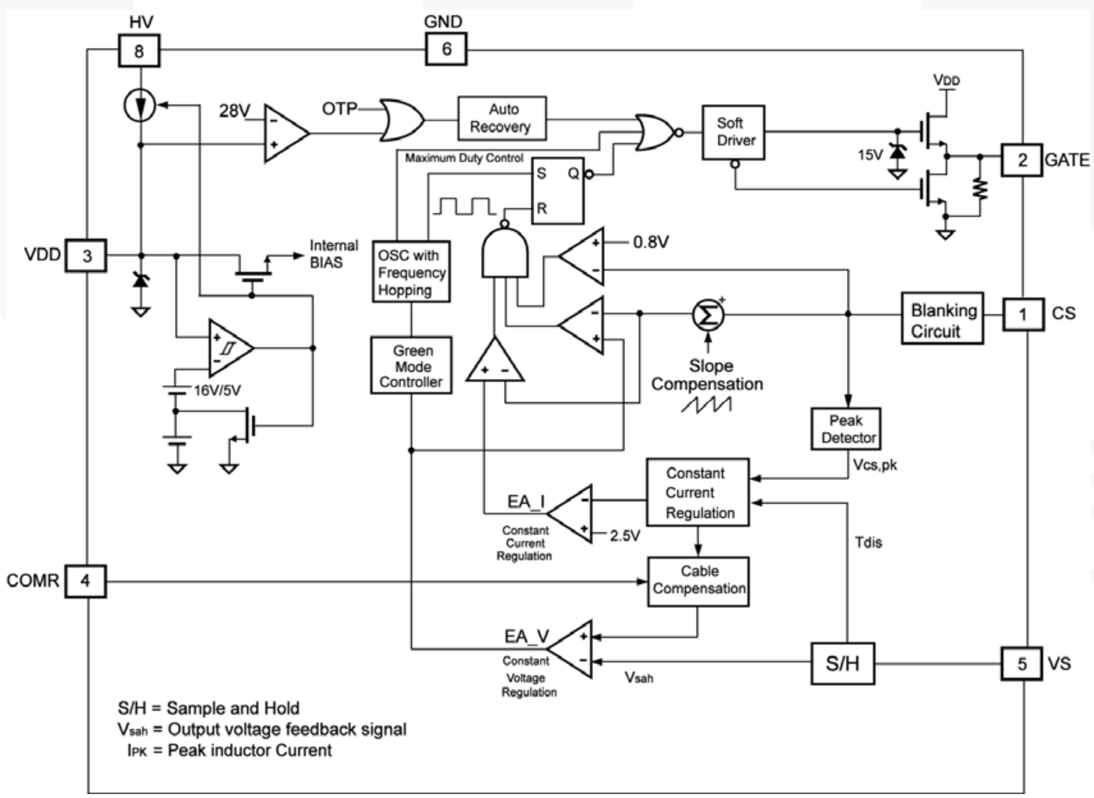
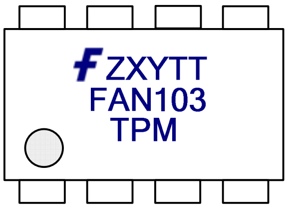


Figure 3. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die-Run Code
T: Package Type (M=SOP)
P: Y=Green Package
M: Manufacture Flow Code

Figure 4. Top Mark

Pin Configuration

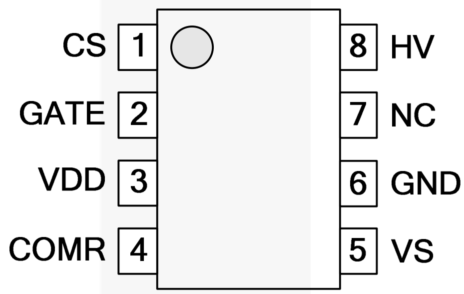


Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects a current sense resistor, to detect the MOSFET current for peak-current-mode control in CV mode, and provides the output-current regulation in CC mode.
2	GATE	**PWM Signal Output**. This pin uses the internal totem-pole output driver to drive the power MOSFET. It is internally clamped below 15V.
3	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external V_{DD} capacitor of typically 10µF. The threshold voltages for startup and turn-off are 16V and 5V, respectively. The operating current is lower than 5mA.
4	COMR	**Cable Compensation**. This pin connects a capacitance between the COMR and GND pins for compensation voltage drop due to output cable loss in CV mode.
5	VS	**Voltage Sense**. This pin detects the output voltage information and discharge time based on voltage of auxiliary winding.
6	GND	**Ground**
7	NC	**No Connect**
8	HV	**High Voltage**. This pin connects to bulk capacitor for high-voltage startup.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage(1)(2)			30	V
V_{VS}	VS Pin Input Voltage		-0.3	7.0	V
V_{CS}	CS Pin Input Voltage		-0.3	7.0	V
V_{COMV}	Voltage Error Amplifier Output Voltage		-0.3	7.0	V
V_{COMI}	Current Error Amplifier Output Voltage		-0.3	7.0	V
P_D	Power Dissipation (T_A<50°C)			660	mW
θ_{JA}	Thermal Resistance (Junction-to-Air)			150	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)			39	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model (Except HV Pin), JEDEC-JESD22_A114		4.50	kV
		Charged Device Model (Except HV Pin), JEDEC-ESD22_C101		1.25	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

Unless otherwise specified, V_{DD}=15V and T_A=25°C.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{DD} Section							
V_{OP}	Continuously Operating Voltage					25	V
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Threshold Voltage			4.5	5.0	5.5	V
I_{DD-OP}	Operating Current				3.2	5.0	mA
$I_{DD-GREEN}$	Green-Mode Operating Supply Current				0.95	1.20	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection Level				28		V
$V_{DD-OVP-HYST}$	Hysteresis Voltage for V_{DD} OVP			1.5	2.0	2.5	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage-Protection Debounce Time			90	200	350	µs
HV Startup Current Source Section							
V_{HV-MIN}	Minimum Startup Voltage on HV Pin					50	V
I_{HV}	Supply Current Drawn from Pin HV		V_{DC}=100V		1.2	3.0	mA
I_{HV-LC}	Leakage Current after Startup		HV=500V, V_{DD}=V_{DD-OFF} +1V		0.5	3.0	µA
Oscillator Section							
f_{OSC}	Frequency	Center Frequency		47	50	53	kHz
		Frequency Hopping Range		±1.5	±2.0	±2.5	
t_{FHR}	Frequency Hopping Period				3		ms
$f_{OSC-N-MIN}$	Minimum Frequency at No-Load				370		Hz
$f_{OSC-CM-MIN}$	Minimum Frequency at CCM				13		kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=10~25V		1	2	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A=-40°C to +105°C			15	%
Voltage-Error-Amplifier Section							
V_{VR}	Reference Voltage			2.475	2.500	2.525	V
V_N	Green-Mode Starting Voltage on EA_V		f_{OSC}=-2kHz		2.5		V
V_G	Green-Mode Ending Voltage on EA_V		f_{OSC}=1kHz		0.5		V
Voltage-Sense Section							
$V_{BIAS-COMV}$	Adaptive Bias Voltage Dominated by V_{COMV}		R_{VS}=20kΩ		1.4		V
I_{tc}	IC Bias Current				10		µA
Current-Sense Section							
t_{PD}	Propagation Delay to GATE Output				90	200	ns
t_{MIN-N}	Minimum On Time at No-Load		V_{COMR}=1V		950		ns
V_{TH}	Threshold Voltage for Current Limit				0.8		V
V_{TL}	Threshold Voltage on VS Pin Smaller than 0.5V				0.25		V

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise specified, V_{DD}=15V and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Current-Error-Amplifier Section						
V_{IR}	Reference Voltage		2.475	2.500	2.525	V
Cable Compensation Section						
V_{COMR}	COMR Pin for Cable Compensation			0.85		V
Gate Section						
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
V_{OL}	Output Voltage Low	V_{DD}=20V, Gate Sinks 10mA			1.5	V
V_{OH}	Output Voltage High	V_{DD}=8V, Gate Sources 1mA	5			V
t_r	Rising Time	C_L=1nF		200	250	ns
t_f	Falling Time	C_L=1nF		60	100	ns
V_{CLAMP}	Output Clamp Voltage	V_{DD}=25V		15	18	V
Over-Temperature-Protection Section						
T_{OTP}	Threshold Temperature for OTP[3]			+140		°C

Note:
3. When the over-temperature protection is activated, the power system enters latch mode and output is disabled.

Typical Performance Characteristics

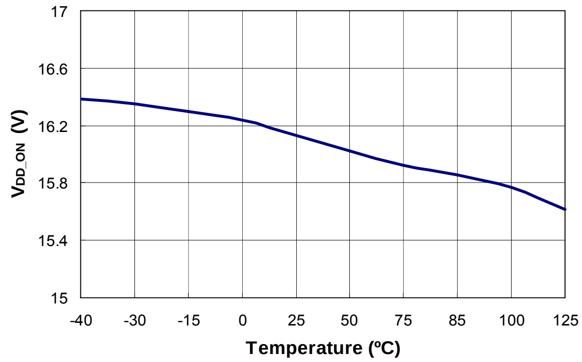


Figure 6. Turn-On Threshold Voltage ($V_{DD\text{-}ON}$) vs. Temperature

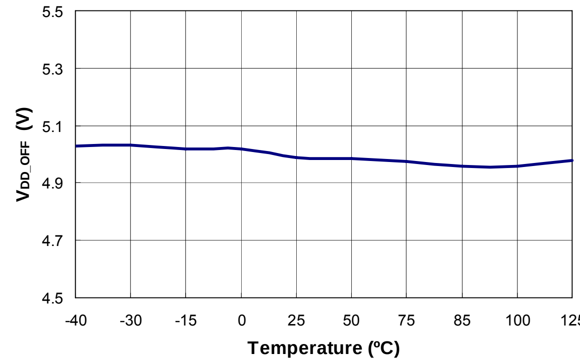


Figure 7. Turn-Off Threshold Voltage ($V_{DD\text{-}OFF}$) vs. Temperature

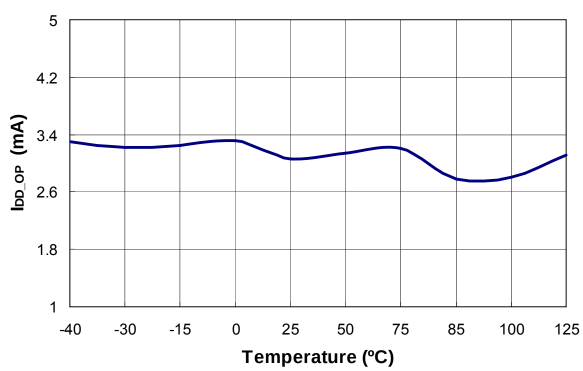


Figure 8. Operating Current ($I_{DD\text{-}OP}$) vs. Temperature

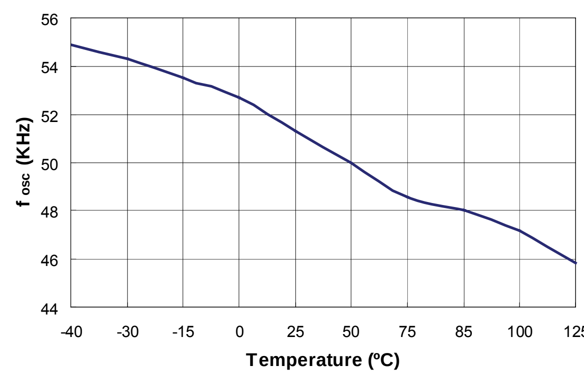


Figure 9. Center Frequency (f_{OSC}) vs. Temperature

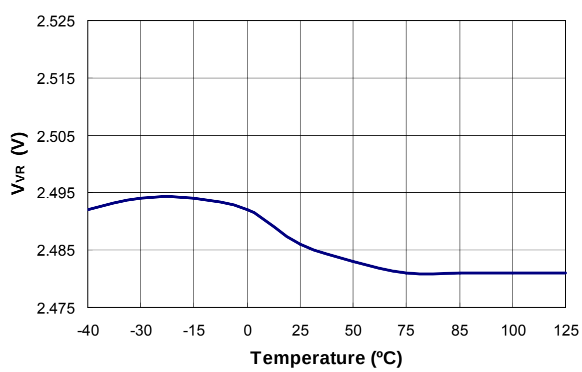


Figure 10. Reference Voltage (V_{VR}) vs. Temperature

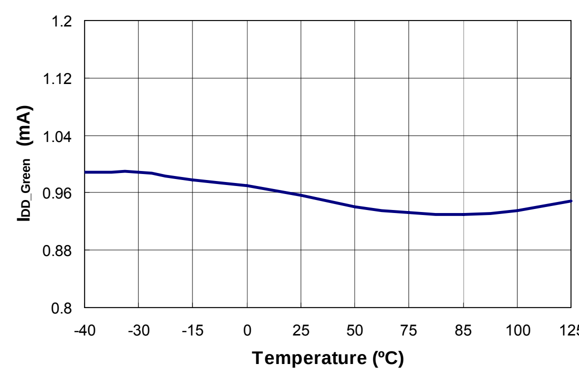


Figure 11. Green-Mode Operating Supply Current ($I_{DD\text{-}GREEN}$) vs. Temperature

Typical Performance Characteristics

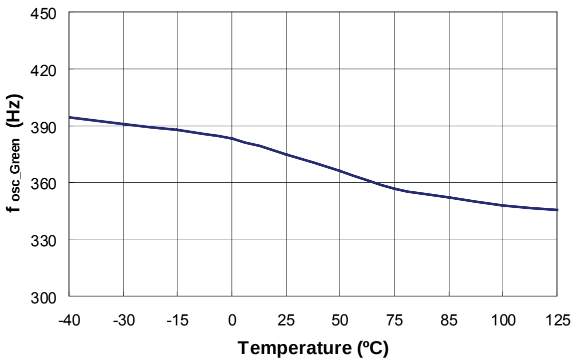


Figure 12. Minimum Frequency at No Load ($f_{OSC\text{-}N\text{-}MIN}$) vs. Temperature

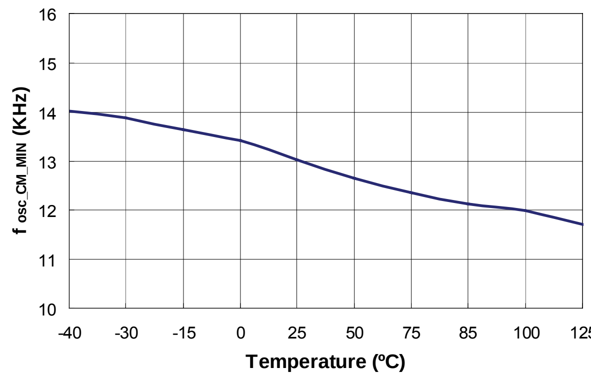


Figure 13. Minimum Frequency at CCM ($f_{OSC\text{-}CM\text{-}MIN}$) vs. Temperature

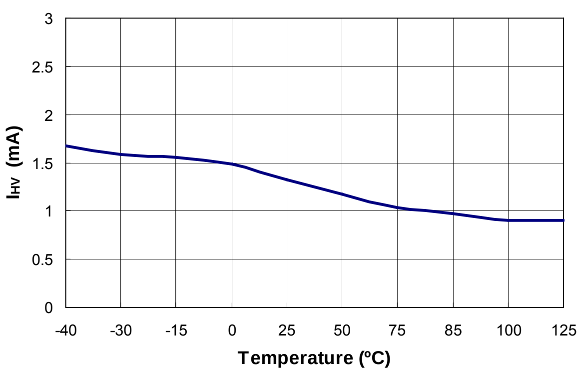


Figure 14. Supply Current Drawn from Pin HV (I_{HV}) vs. Temperature

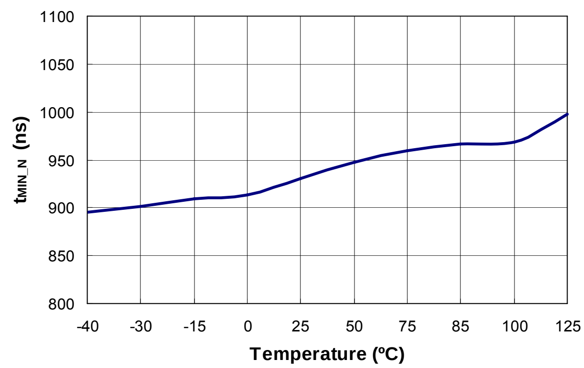


Figure 15. Minimum On Time at No Load ($t_{MIN\text{-}N}$) vs. Temperature

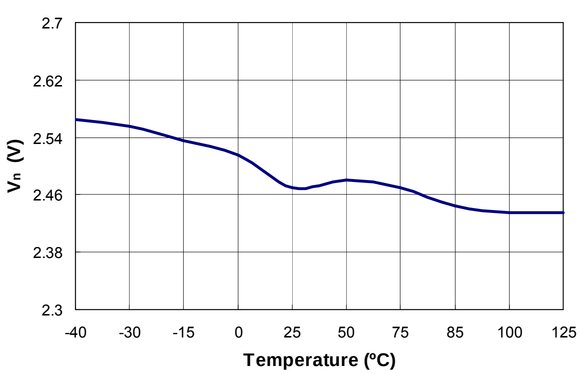


Figure 16. Green Mode Starting Voltage on EA_V (V_N) vs. Temperature

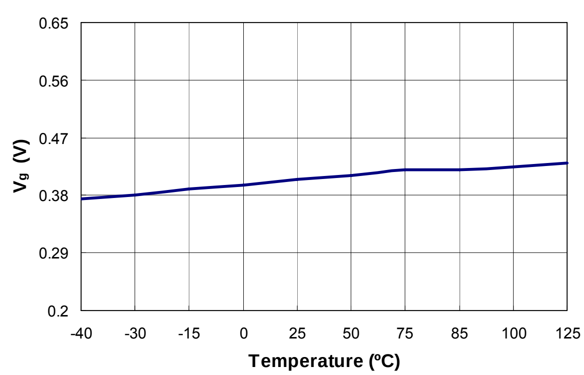


Figure 17. Green Mode Ending Voltage on EA_V (V_G) vs. Temperature

Typical Performance Characteristics

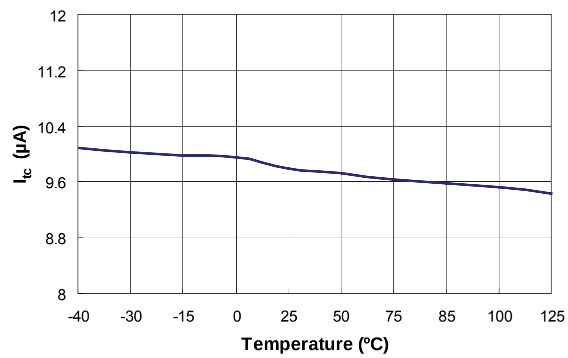


Figure 18. IC Bias Current (I_{tc}) vs. Temperature

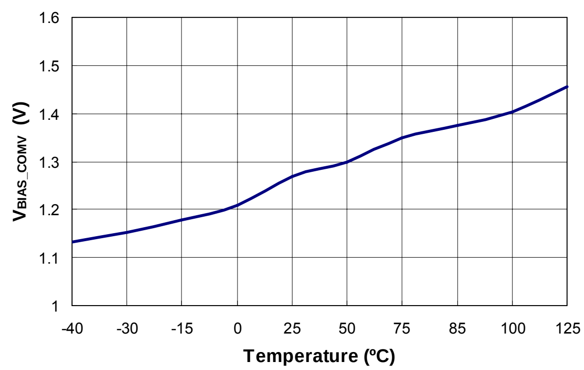


Figure 19. Output Clamp Voltage (V_{CLAMP}) vs. Temperature

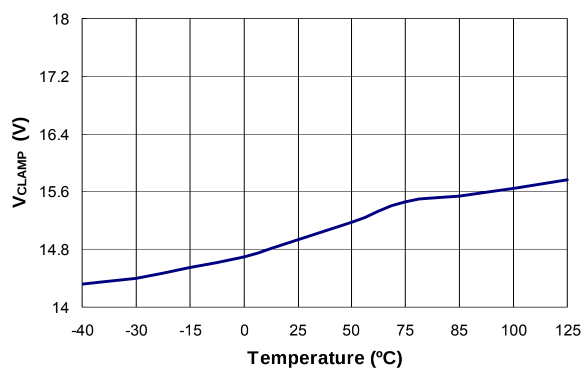


Figure 20. Variation Test Voltage on COMR Pin for Cable Compensation (V_{COMR}) vs. Temperature

Functional Description

Figure 21 shows the basic circuit diagram of a primary-side regulated flyback converter with typical waveforms shown in Figure 22. Generally, discontinuous conduction mode (DCM) operation is preferred for primary-side regulation since it allows better output regulation. The operation principles of DCM flyback converter are as follows:

During the MOSFET on time (t_{ON}), input voltage (V_{DL}) is applied across the primary-side inductor (L_m). Then, MOSFET current (I_{ds}) increases linearly from zero to the peak value (I_{pk}). During this time, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on. While the diode is conducting, the output voltage (V_o), together with diode forward voltage drop (V_F), are applied across the secondary-side inductor ($L_m \times N_s^2 / N_p^2$) and the diode current (I_D) decreases linearly from the peak value ($I_{pk} \times N_p/N_s$) to zero. At the end of inductor current discharge time (t_{DIS}), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero, the transformer auxiliary winding voltage (V_w) begins to oscillate by the resonance between the primary-side inductor (L_m) and the effective capacitor loaded across MOSFET.

During the inductor current discharge time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as $(V_o+V_F) \times N_a/N_s$. Since the diode forward-voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time, where the diode current diminishes to zero. Thus, by sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (EA_V) compares the sampled voltage with internal precise reference to generate error voltage (V_{COMV}), which determines the duty cycle of the MOSFET in CV mode.

Meanwhile, the output current can be estimated using the peak drain current and inductor current discharge time since output current is same as average of the diode current in steady state.

The output current estimator picks up the peak value of the drain current with a peak detection circuit and calculates the output current using the inductor discharge time (t_{DIS}) and switching period (t_s). This output information is compared with internal precise reference to generate error voltage (V_{COMI}), which determines the duty cycle of the MOSFET in CC mode. With Fairchild's innovative technique TRUECURRENT™, constant current (CC) output can be precisely controlled.

Among the two error voltages, V_{COMV} and V_{COMI}, the small one determines the duty cycle. Therefore, during constant voltage regulation mode, V_{COMV} determines the duty cycle while V_{COMI} is saturated to HIGH. During constant current regulation mode, V_{COMI} determines the duty cycle while V_{COMV} is saturated to HIGH.

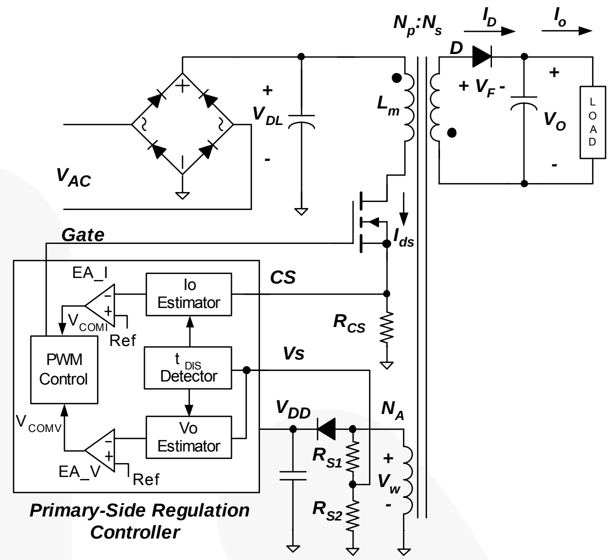


Figure 21. Simplified PSR Flyback Converter Circuit

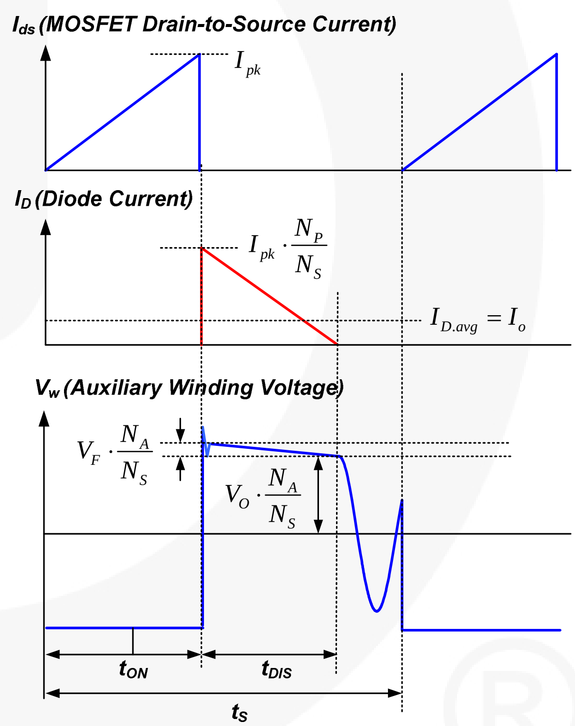


Figure 22. Key Waveforms of DCM Flyback Converter

Figure 23.

Cable Voltage Drop Compensation

When it comes to cellular phone charger applications, the battery is located at the end of cable, which causes, typically, several percentage of voltage drop on the actual battery voltage. FAN103 has a built-in cable voltage drop compensation, which provides a constant output voltage at the end of the cable over the entire load range in CV mode. As load increases, the voltage drop across the cable is compensated by increasing the reference voltage of voltage regulation error amplifier.

Operating Current

The operating current in FAN103 is as small as 3.2mA. The small operating current results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement. Once FAN103 enters deep-green mode, the operating current is reduced to 0.95mA, assisting the power supply in meeting power conservation requirements.

Green-Mode Operation

The FAN103 uses voltage regulation error amplifier output (V_{COMV}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 23. The switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is fixed at 50kHz. Once V_{COMV} decreases below 2.5V, the PWM frequency linearly decreases from 50kHz. When FAN103 enters into deep-green mode, the PWM frequency is reduced to a minimum frequency of 370Hz, gaining power saving to help meet international power conservation requirements.

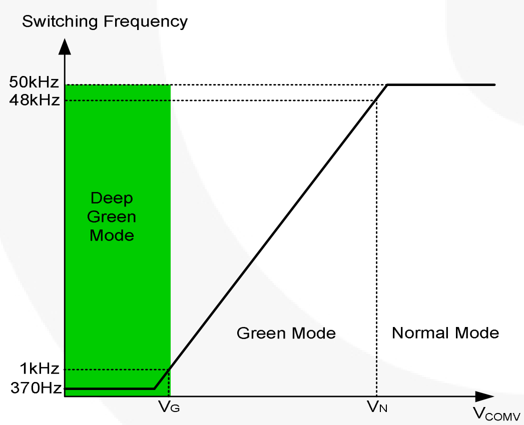


Figure 24. Switching Frequency in Green Mode

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. FAN103 has an internal frequency hopping circuit that changes the switching frequency between 47kHz and 53kHz with a period, as shown in Figure 24.

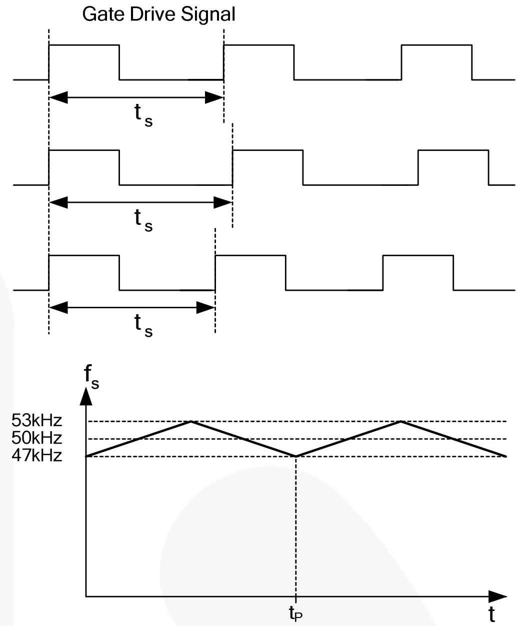


Figure 25. Frequency Hopping

High-Voltage Startup

Figure 25 shows the HV-startup circuit for FAN103 applications. The HV pin is connected to the line input or bulk capacitor through a resistor, R_{START} (100kΩ is recommended). During startup, the internal startup circuit in FAN103 is enabled. Meanwhile, line input supplies the current, $I_{STARTUP}$, to charge the hold-up capacitor, C_{DD}, through R_{START}. When the V_{DD} voltage reaches $V_{DD\text{-}ON}$, the internal startup circuit is disabled, blocking $I_{STARTUP}$ from flowing into the HV pin. Once the IC turns on, C_{DD} is the only energy source to supply the IC consumption current before the PWM starts to switch. Thus, C_{DD} must be large enough to prevent V_{DD} from dropping to $V_{DD\text{-}OFF}$ before the power can be delivered from the auxiliary winding.

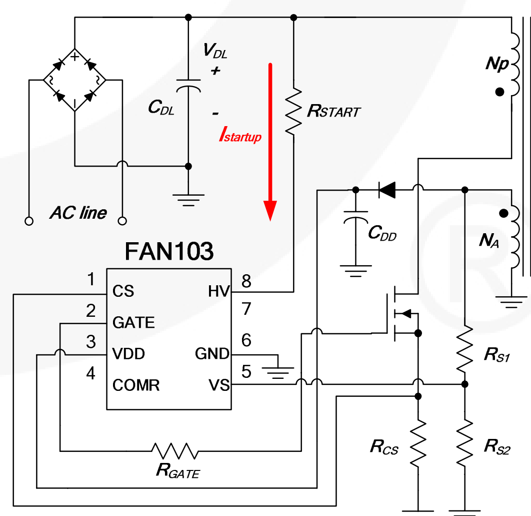


Figure 26. HV Startup Circuit

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16V and 5V, respectively. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable the FAN103. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} is not allowed to drop below 5V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor properly supplies V_{DD} during startup.

Protections

The FAN103 has several self-protection functions, such as Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and Pulse-by-Pulse Current limit. All the protections are implemented as auto-restart mode. Once an abnormal condition occurs, switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5V, the internal startup circuit is enabled again, then the supply current drawn from HV pin charges the hold-up capacitor. When V_{DD} reaches the turn-on voltage of 16V, FAN103 resumes normal operation. In this manner, the auto-restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated *(see Figure 26)*.

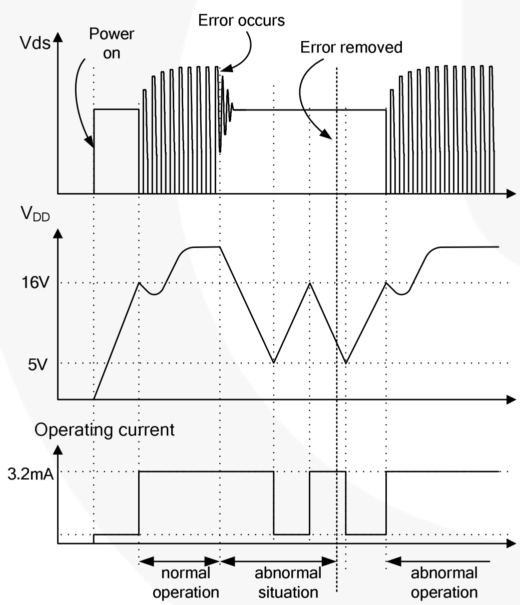


Figure 27. Auto Restart Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents damage from over-voltage conditions. If the V_{DD} voltage exceeds 28V at open-loop feedback condition, OVP is triggered and the PWM switching is disabled. The OVP has a de-bounce time (typically 200μs) to prevent false triggering due to switching noises.

Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C.

Pulse-by-pulse Current Limit

When the sensing voltage across the current sense resistor exceeds the internal threshold of 0.8V, the MOSFET is turned off for the remainder of switching cycle. In normal operation, the pulse-by-pulse current limit is not triggered since the peak current is limited by the control loop.

Leading-Edge Blanking (LEB)

Each time the power MOSFET switches on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. Conventional RC filtering can be omitted. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Gate Output

The FAN103 output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

Built-in Slope Compensation

The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current mode control. The FAN103 has a synchronized, positive-slope ramp built-in at each switching cycle.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN103, and increasing the power MOS gate resistance is advised.

Typical Application Circuit (Primary-Side-Regulated Flyback Charger)

Application	Fairchild Devices	Input Voltage Range	Output	Output DC Cable
Cell Phone Charger	FAN103	90~265V_{AC}	5V/1A (5W)	AWG26, 1.8 Meter

Features

- High efficiency (>68.17% at Full Load) Meeting EPS 2.0 Regulation with Enough Margin
- Low standby (Pin <30mW at No Load Condition)
- Tight output regulation (CV: ±5%, CC: ±7%)

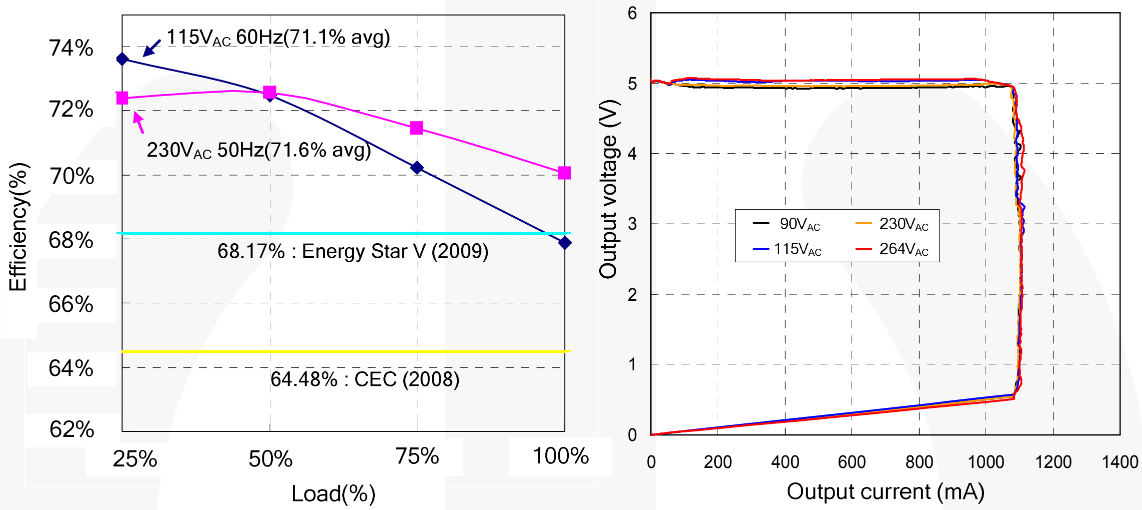


Figure 28. Measured Efficiency and Output Regulation

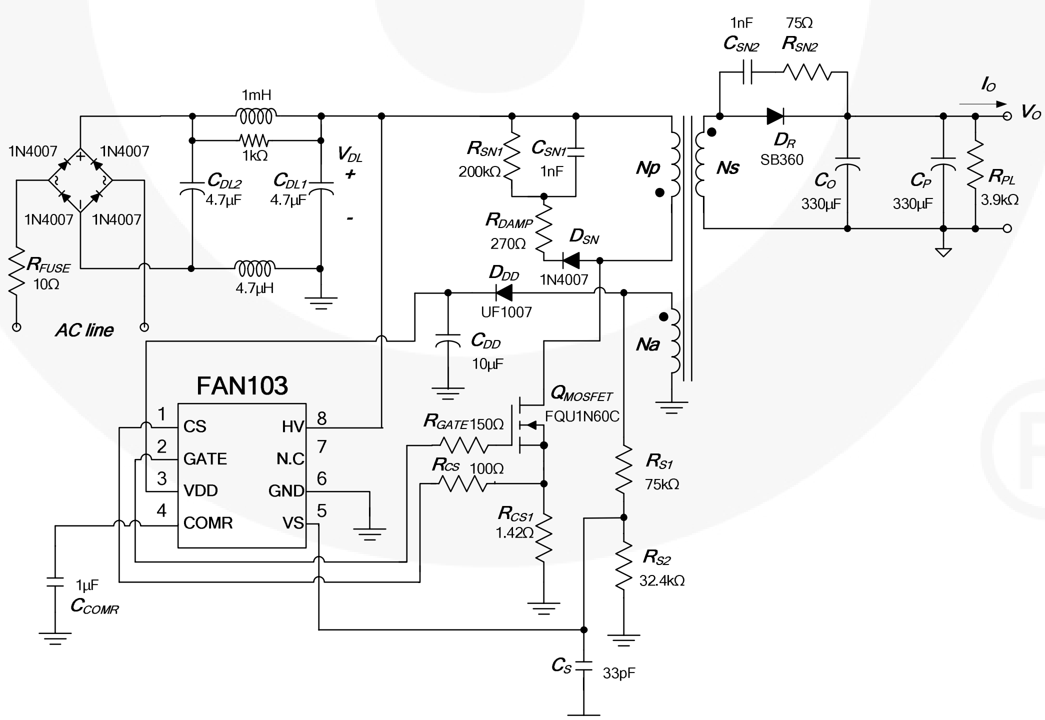


Figure 29. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: EE16
- Bobbin: EE16

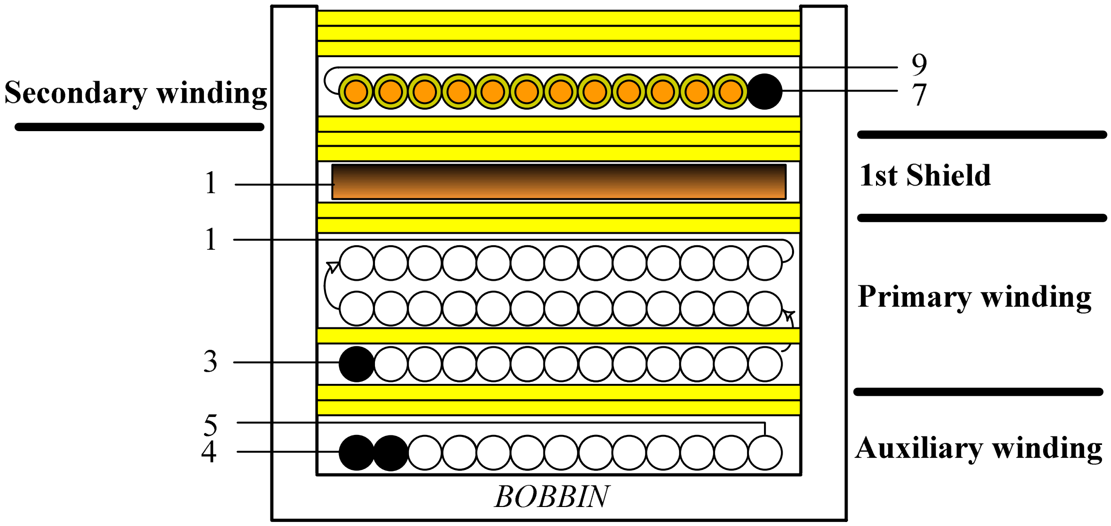


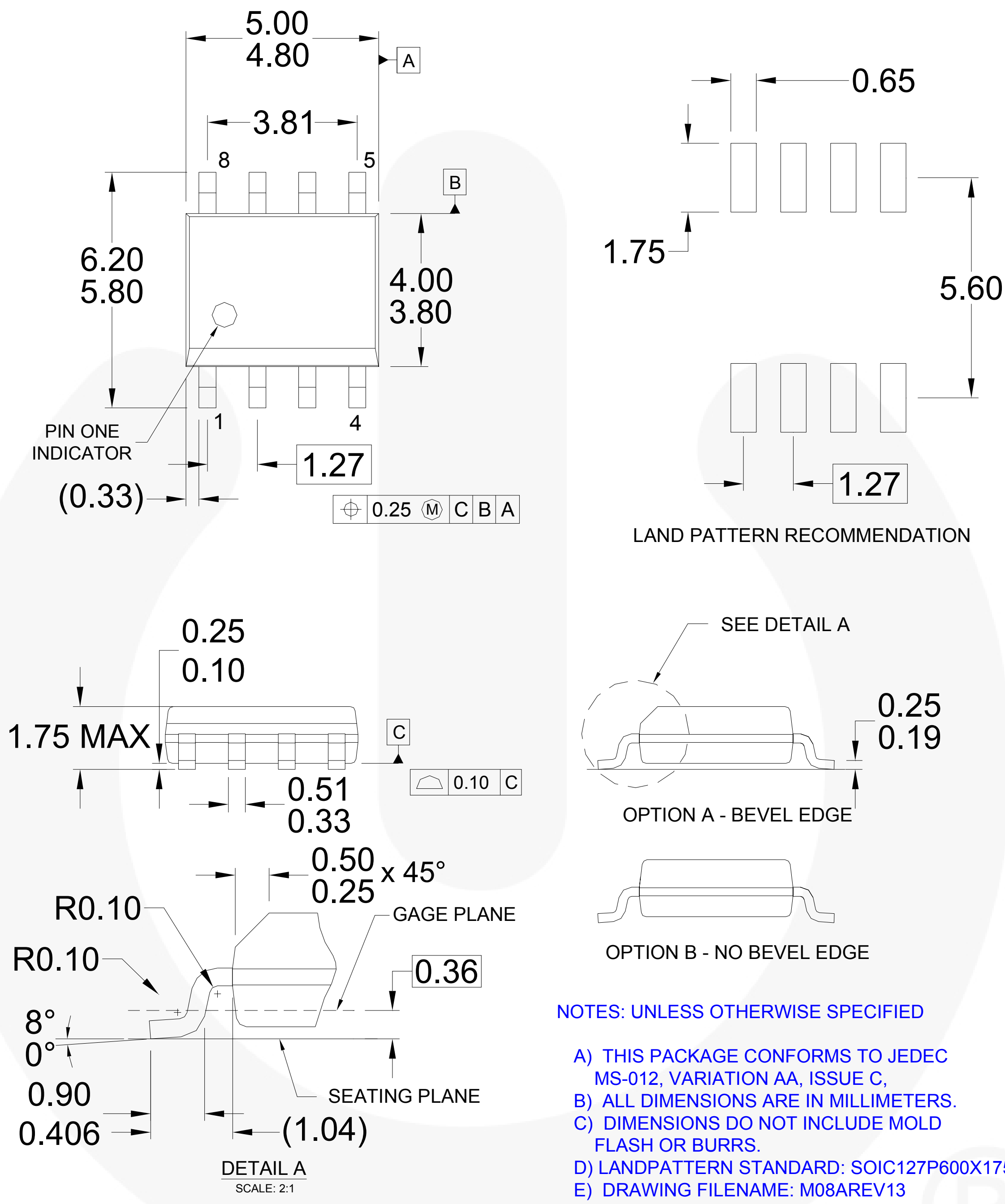
Figure 30. Bobbin Winding Diagram

Notes:
4. When W4R's winding is reversed winding, it must wind one layer.
5. When W2 is winding, put 1 layer tape after wind first layer.

NO	TERMINAL		WIRE	Ts	INSULATION	BARRIER	
	S	F			Ts	Primary	Seconds
W1	4	5	2UEW 0.23*2	15	2		
W2	3	1	2UEW 0.17*1	40	1		
				40	0		
				37	2		
W3	1		COPPER SHIELD	1.2	3		
W4R	7	9	TEX-E 0.6*1	9	3		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	1 – 3	1.75mH ± 5%	100kHz, 1V
Primary-Side Effective Leakage	1 – 3	80µH ± 5%	Short one of the secondary windings

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 31. 8-Lead, Small Outline Package (SOP-8)

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