ON Semiconductor®

Design and Implementation of a fixed-frequency Adapter with Very Low Power Consumption

Agenda

- New ENERGY STAR® requirements
- Needed features to meet the new specification
- New controller family NCP1237/38/87/88
- Design step 1: Power stage
- Design step 2: Set the compensations
- Design step 3: No Load Input Power
- Design step 4: Magnetics
- Design step 5: EMI
- Preliminary demo board example
- Conclusion

EPA 2.0 (External Power Supplies)

EPA ENERGY STAR Version 2.0 EPS Voluntary Specification
(Effective November 1, 2008)

Energy-Efficiency Criteria for Ac-Ac and Ac-Dc External Power Supplies in Active Mode: Standard Models

Nameplate Output Power (P_{no})	Minimum Average Efficiency in Active Mode (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.480 * P_{no} + 0.140
> 1 to ≤ 49 watts	≥ [0.0626 * Ln (P_{no})] + 0.622
> 49 watts	≥ 0.870

(was > 0.84 in previous version 1.1)

Energy-Efficiency Criteria for Ac-Ac and Ac-Dc External Power Supplies

Energy Consumption Criteria for No-Load

Nameplate Output Power (P_{no})	Maximum Power in No-Load		
	AC-AC EPS	AC-DC EPS	
0 to < 50 watts	≤ 0.5 watts	≤ 0.3 watts	***(< 0.5 W in 1.1)***
≥ 50 to ≤ 250 watts	≤ 0.5 watts	≤ 0.5 watts	***(< 0.75 W in 1.1)***

EPS 5.0 (ENERGY STAR® Program Requirements for Computers)

- Defines E_{TEC} for different types of products as a Typical Energy Consumption
- For the desktop and notebook product categories TEC will be determined by the following formula:

$$E_{TEC} = (8760/1000) * (P_{off} * T_{off} + P_{sleep} * T_{sleep} + P_{idle} * T_{idle})$$

- where all Px are power values in watts, all Tx are Time values in % of year, and the TEC E_{TEC} is in units of kWh and represents annual energy consumption based on mode weightings

- **The light load efficiency and no load consumption is more important**

E_{TEC} requirement desktops and notebooks

	Desktops and Integrated Computers (kWh)	Notebook Computers (kWh)
TEC (kWh)	**Category A**: ≤ 148.0 **Category B**: ≤ 175.0 **Category C**: ≤ 209.0 **Category D**: ≤ 234.0	**Category A**: ≤ 40.0 **Category B**: ≤ 53.0 **Category C**: ≤ 88.5

- Effective from July 1, 2009 (except: game consoles from July 1, 2010)

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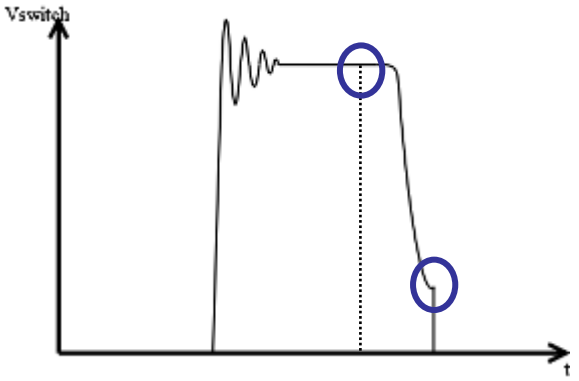
Improving Efficiency

- Sources of loss:
  - Switching losses:

$$P_{loss(switching)} = \frac{1}{2} \cdot C_{DRAIN} \cdot V_{DRAIN(turn-off)}^{2} \cdot F_{SW}$$

  - Losses caused by leakage inductance:

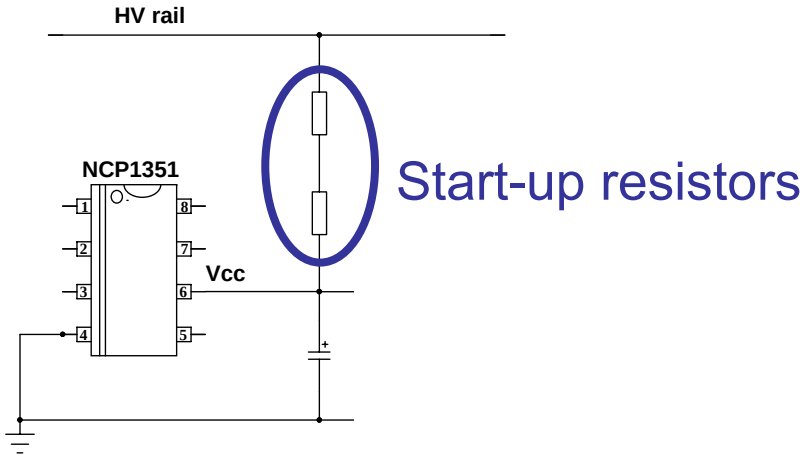
$$P_{loss(leak)} = \frac{1}{2} \cdot L_{leak} \cdot I_{peak}^{2} \cdot F_{SW}$$



- Ways to improve efficiency:
  - Lower the switching frequency F_{SW} ➔ frequency foldback at light loads
  - Lower the Drain voltage at turn-off ➔ valley switching

Reducing No-load Input Power

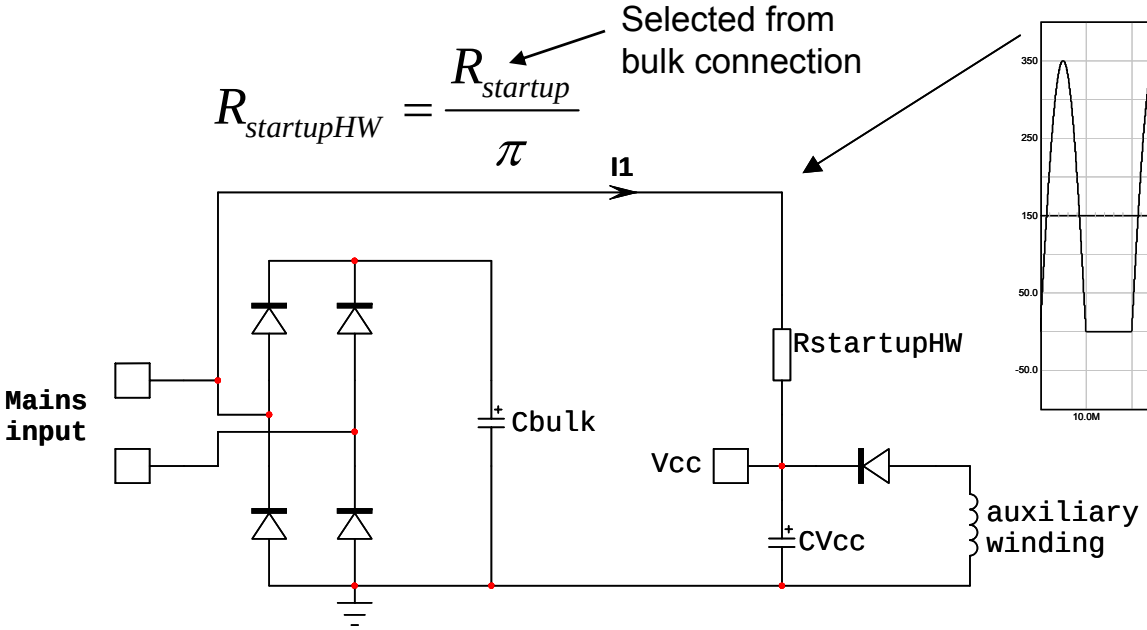
- Static losses in the start-up circuit:
  - Start-up resistor permanently drawing current from the bulk capacitor
- Ways to lower the start-up circuit losses
  - With external start-up resistor ➔ Extremely low start-up current
  - Integrated start-up current source ➔ Extremely low leakage when off
  - Connect the start-up circuit to the half-wave rectified ac input

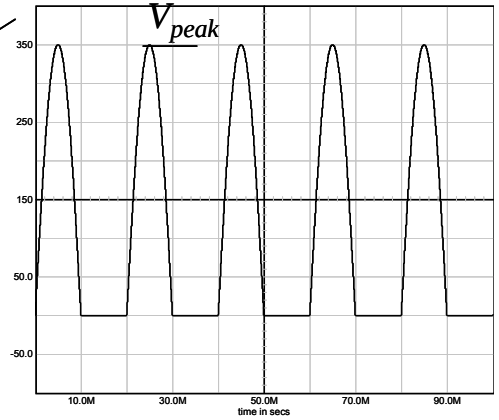


Reducing No-load Input Power

$$R_{startupHW} = \frac{R_{startup}}{\pi}$$

Selected from bulk connection





$$P_{R_{startupHW}} = \frac{P_{R_{startup}}\,\pi}{4} \longrightarrow \text{Brings a 21\% reduction in power}$$

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NCP1237/38/87/88

Avail. in Q1 2010

Value Proposition

The NCP1237/38/87/88 series represents the next generation of fixed frequency PWM controllers. It targets applications where cost-effectiveness, reliability, design flexibility and low standby power are compulsory.

Unique Features

- High-voltage current source with built-in Brown-out and mains OVP
- Freq. reduction in light load conditions and skip mode
- Adjustable Over Power Protection

Benefits

- Fewer components and rugged design
- Extremely low no-load standby power
- Simple option to alter the max. peak current set point at high line

Others Features

- Latch-off input for severe fault conditions, allowing direct connection of NTC
- Timer-based protection: auto-recovery or latched
- Dual OCP option available
- Built-in ramp compensation
- Frequency jittering for a softened EMI signature
- Vcc operation up to 30 V

Market & Applications

- AC-DC adapters for notebooks, LCD monitor, game console, printers
- CE applications (DVD, STB)

Application Data



	DSS	Dual OCP	Latch	Auto Recovery
NCP1237A	Yes	Yes	Yes	
NCP1237B	Yes	Yes		Yes
NCP1238A	Yes	No	Yes	
NCP1238B	Yes	No		Yes
NCP1287A	HV only	Yes	Yes	
NCP1287B	HV only	Yes		Yes
NCP1288A	HV only	No	Yes	
NCP1288B	HV only	No		Yes

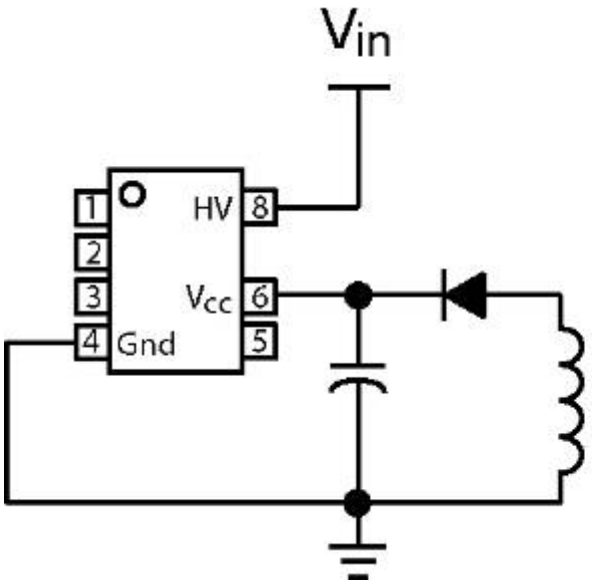
Various options available depending upon end applications needs

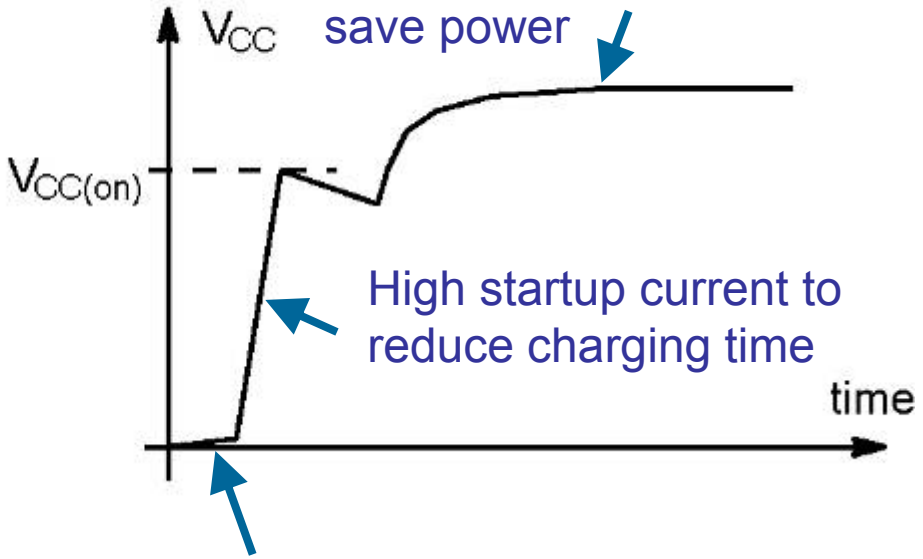
Ordering & Package Information

- NCP1237/38xDR2G - NCP1287/88xDR2G
- SOIC-7 2500p per reel

Pb O, DW

NCP1237/38/87/88 – Built-in Startup FET



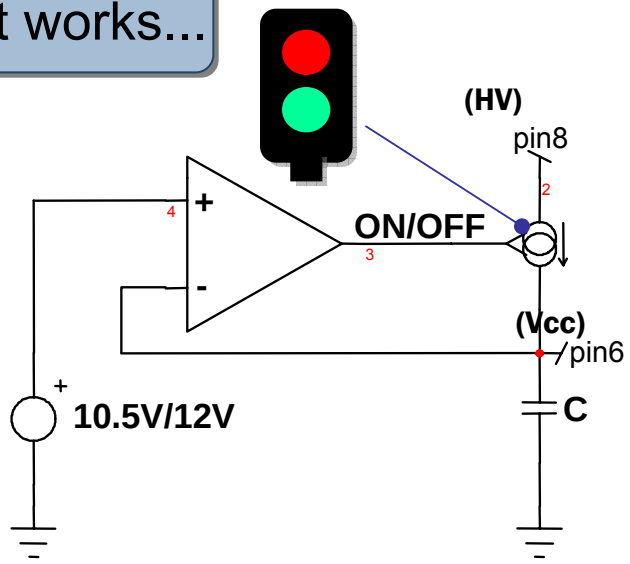


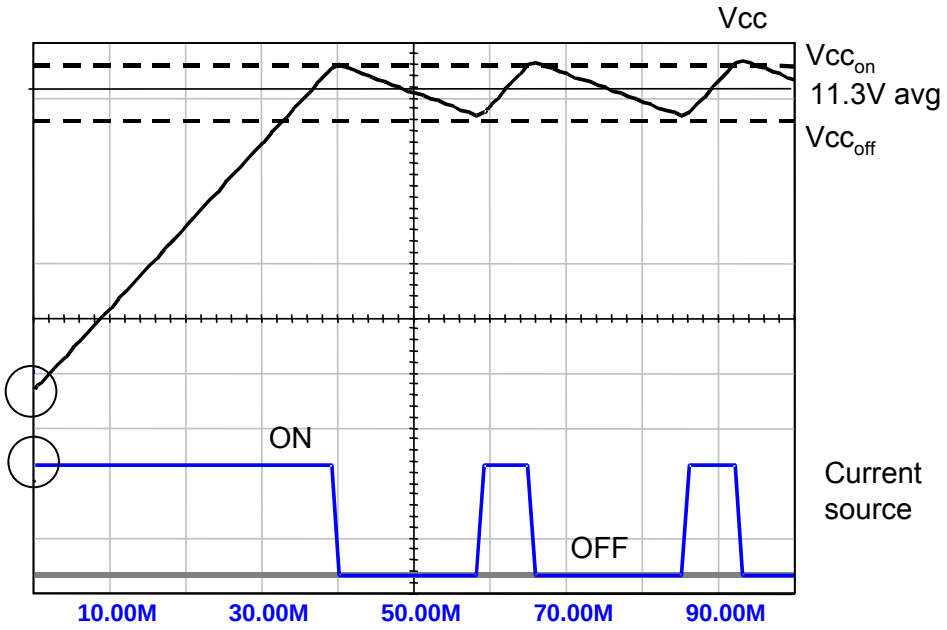
No startup resistor!

Saves PCB area
& saves power

NCP1237/38/87/88 – Dynamic Self Supply (Optional)

How it works...





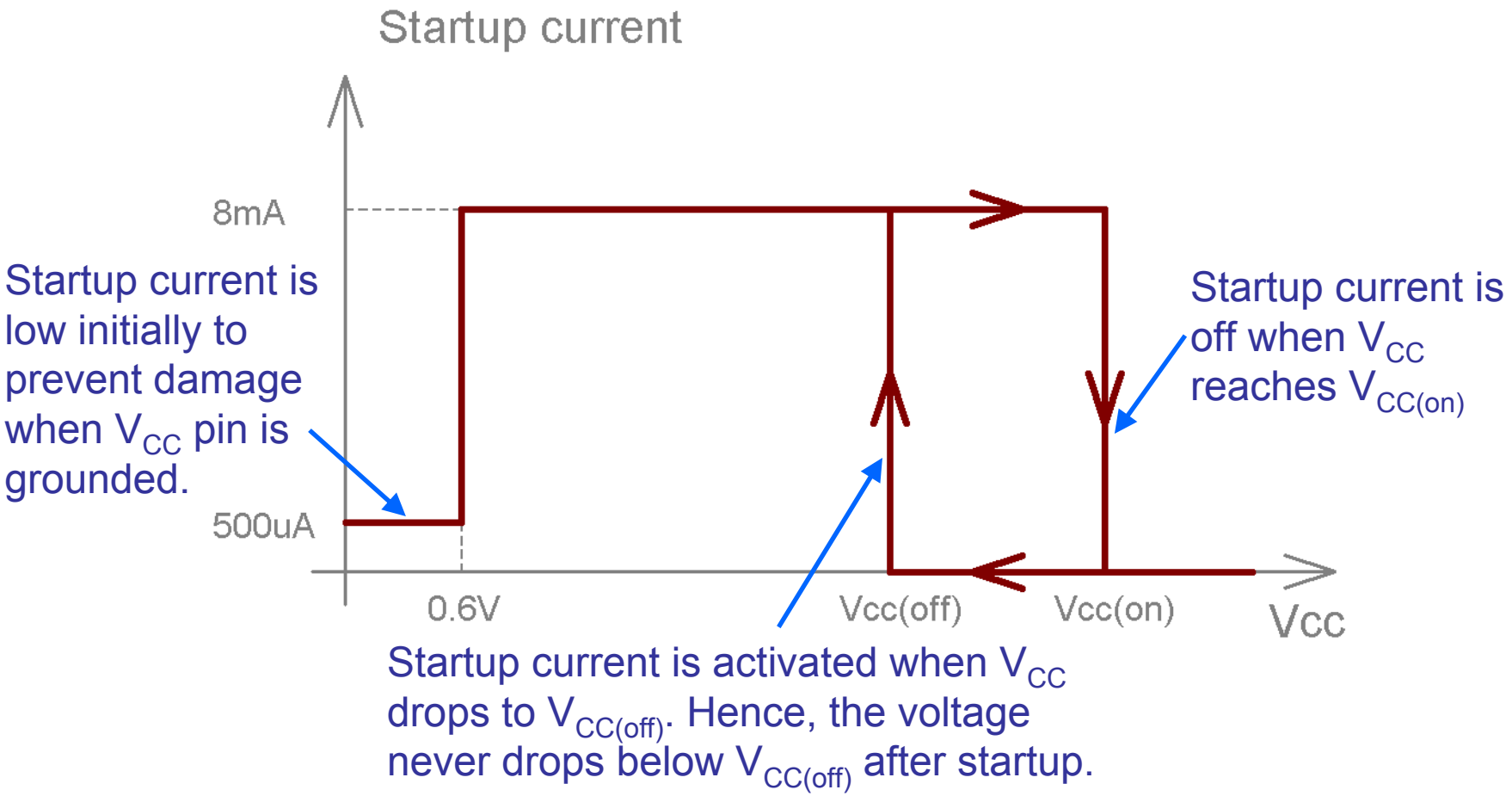
Power ON → Current Source turns ON → V_{cc} is rising; no output pulses

V_{cc} reaches $Vcc_{(on)}$ → Current Source turns OFF → V_{cc} is falling; output is pulsing

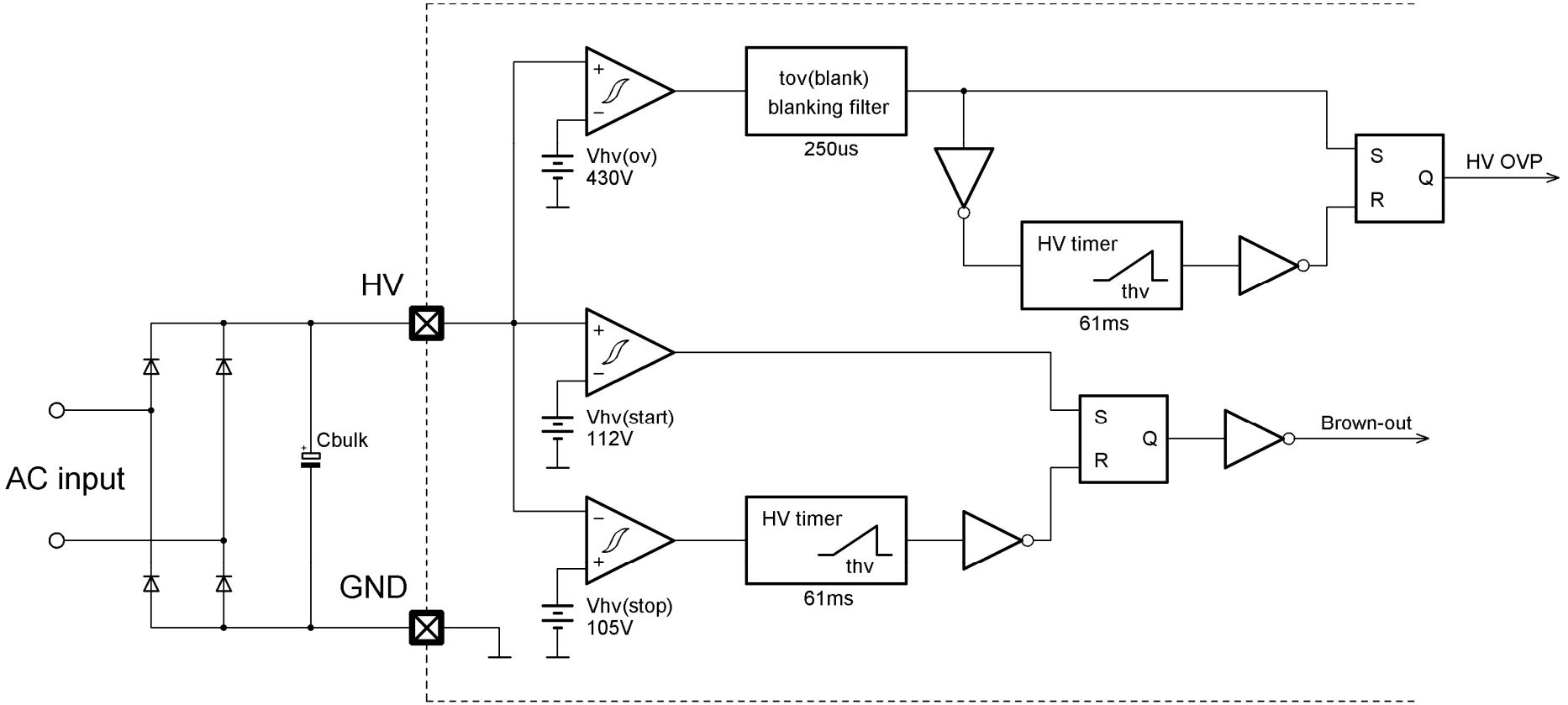
V_{cc} falls to $Vcc_{(off)}$ → Current Source turns ON → V_{cc} is rising; output is pulsing

Dynamic Self-Supply ⇒ No need of auxiliary winding!

NCP1237/38/87/88 – Dual Startup Current Level



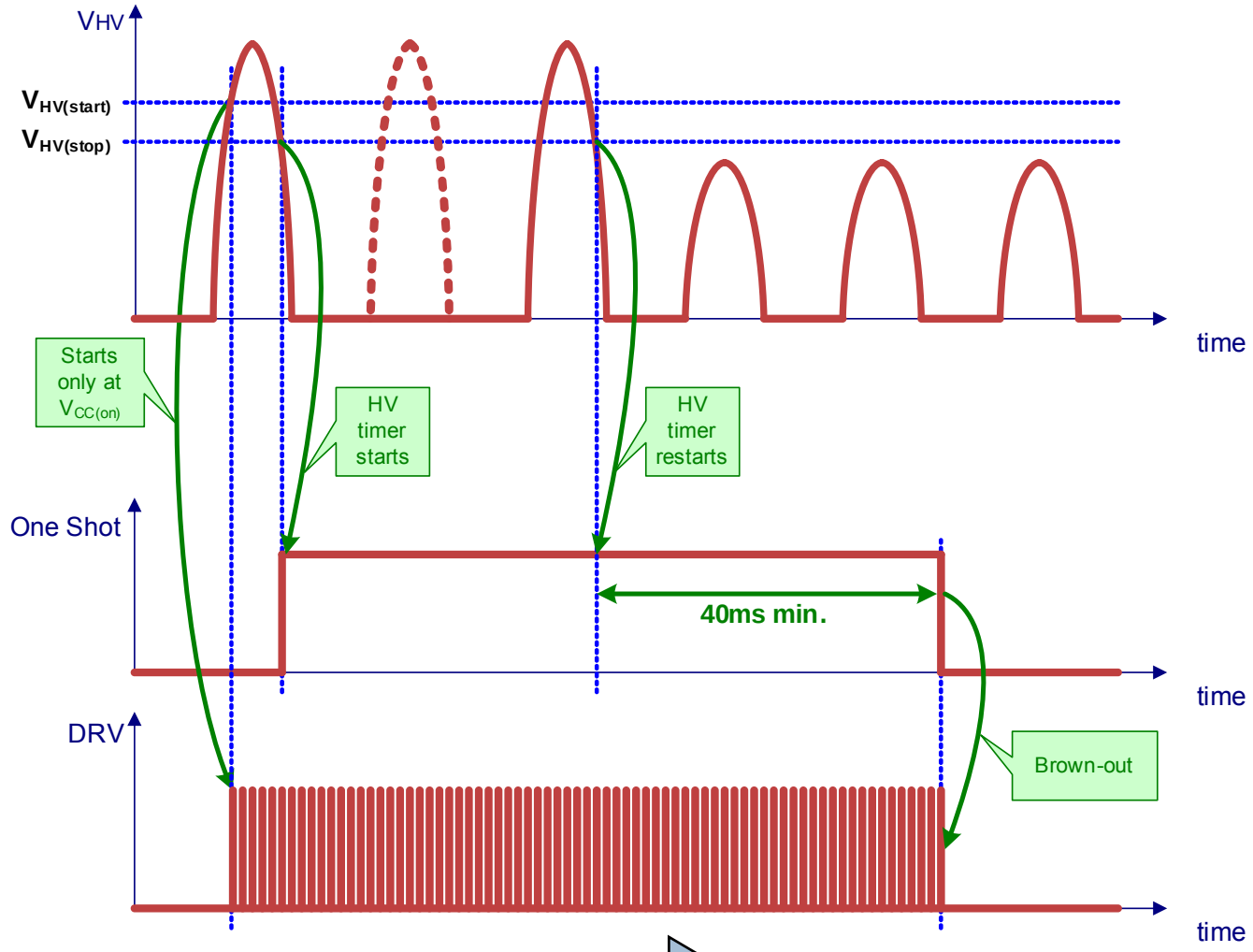
NCP1237/38/87/88 – Brown-out and Mains OVP



Detection independent of Ripple on HV pin

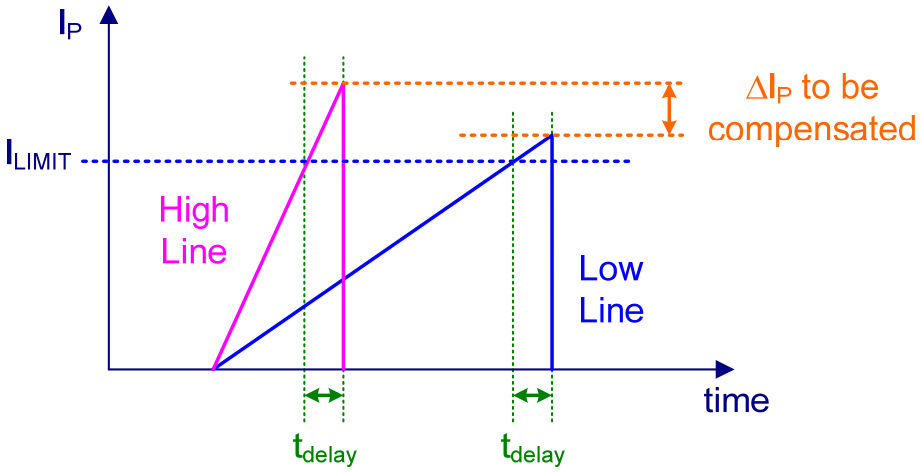
Can be connected to the half-wave rectified ac line

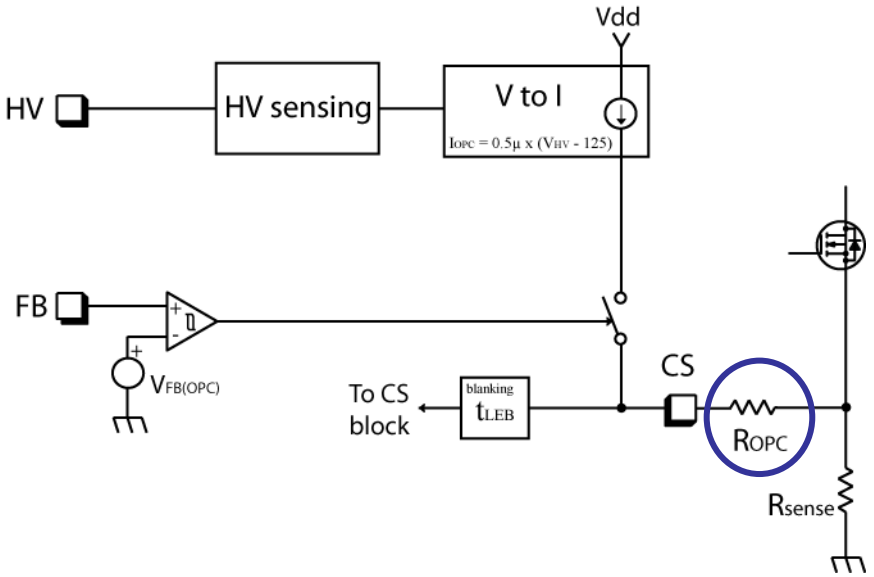
NCP1237/38/87/88 – Brown-out and Mains OVP



Timer-based detection ⇒ Passes full line cycle drop-out

NCP1237/38/87/88 – Over Power Protection



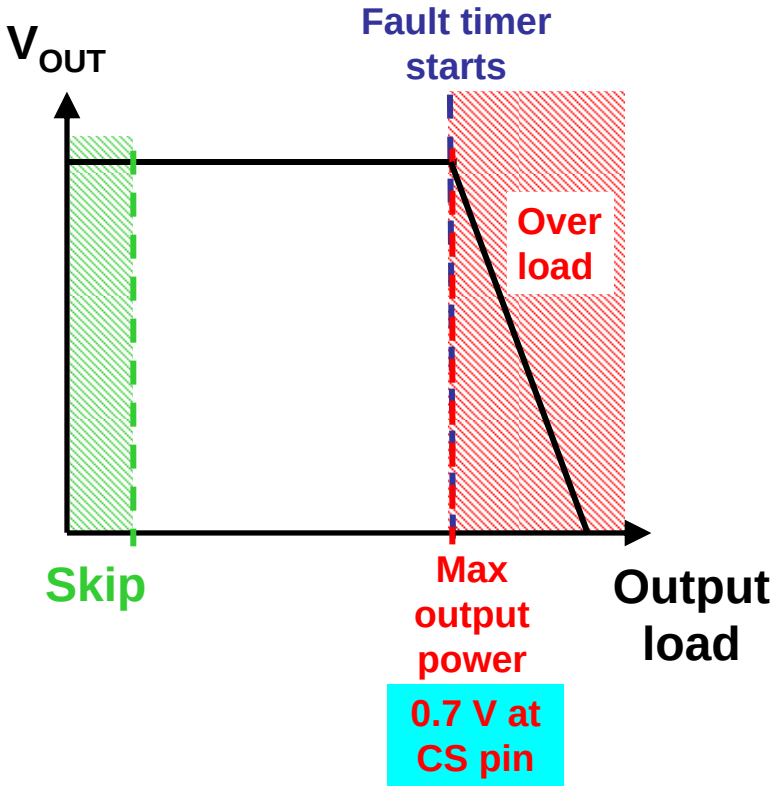


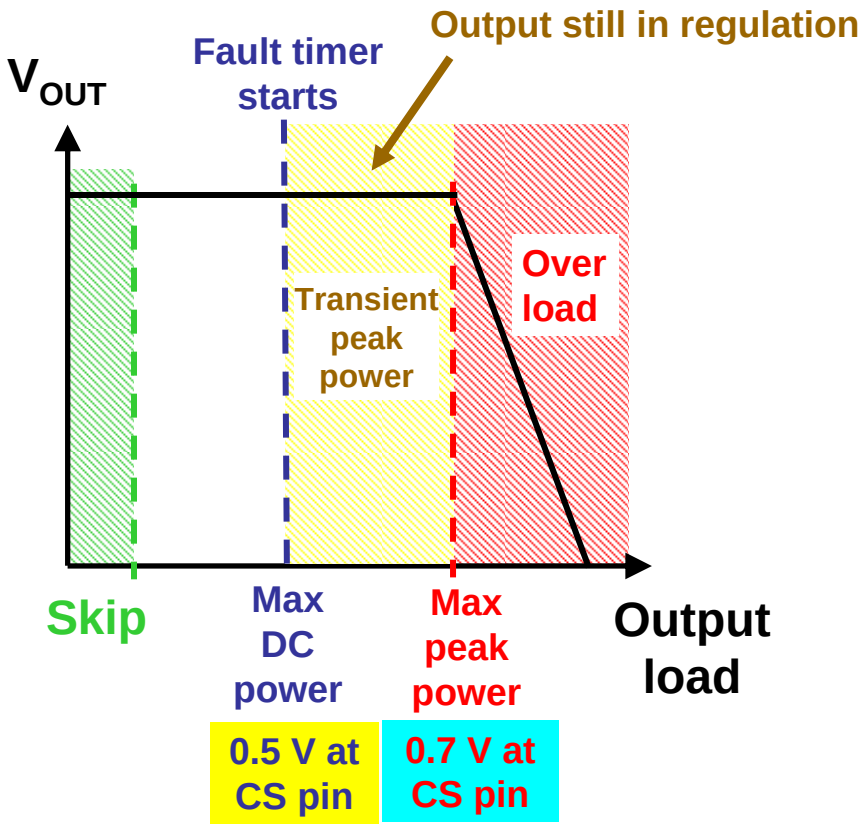
Need to compensate for the effect of the propagation delay

The compensation current creates an offset on the Current Sense signal

Over Power Protection ⇒ Maximum output power clamped

NCP1237/38/87/88 – Dual OCP Threshold



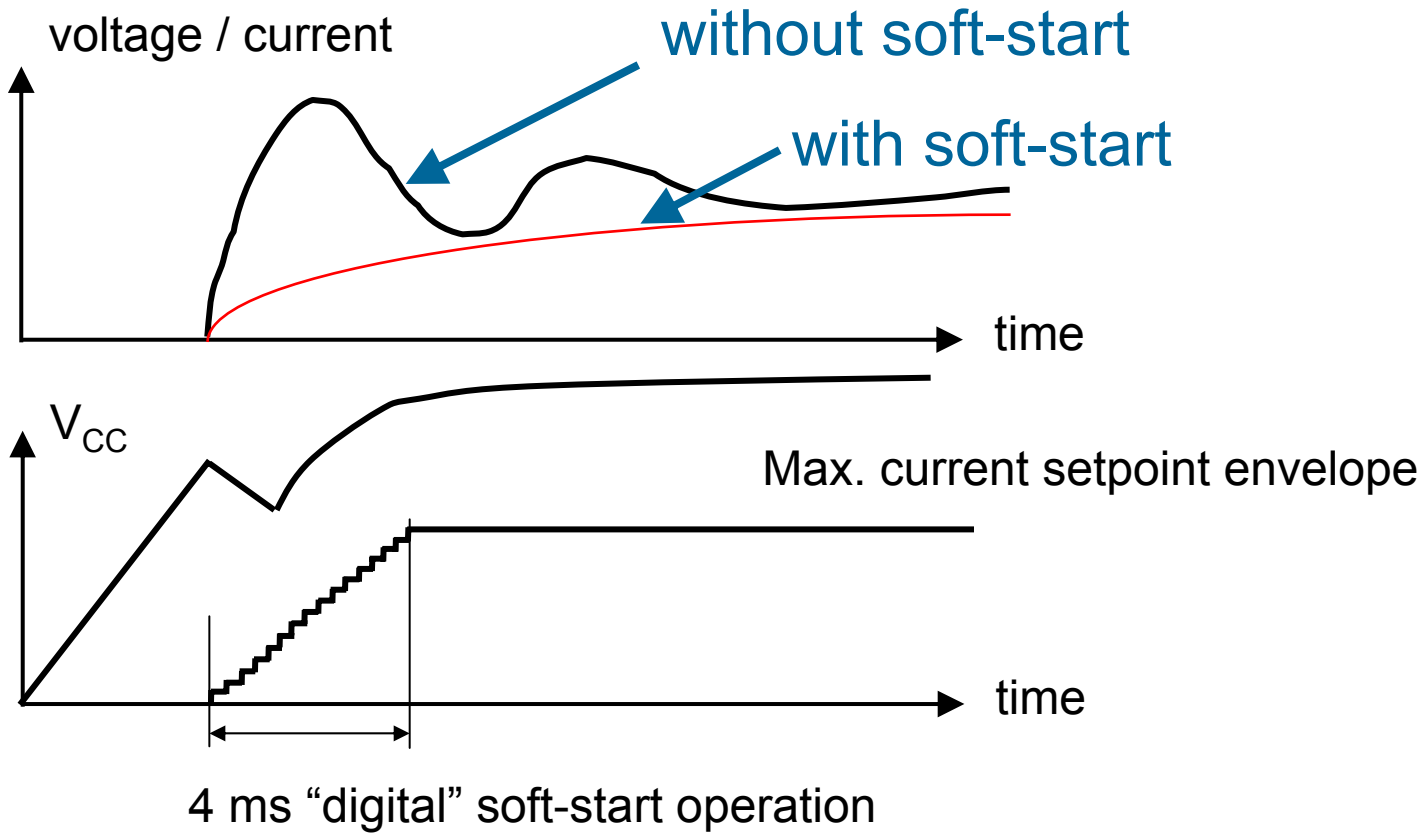


Accommodates large output power transients

Suitable for printers

These protections use the Up/Down counters, like classical analog integration.

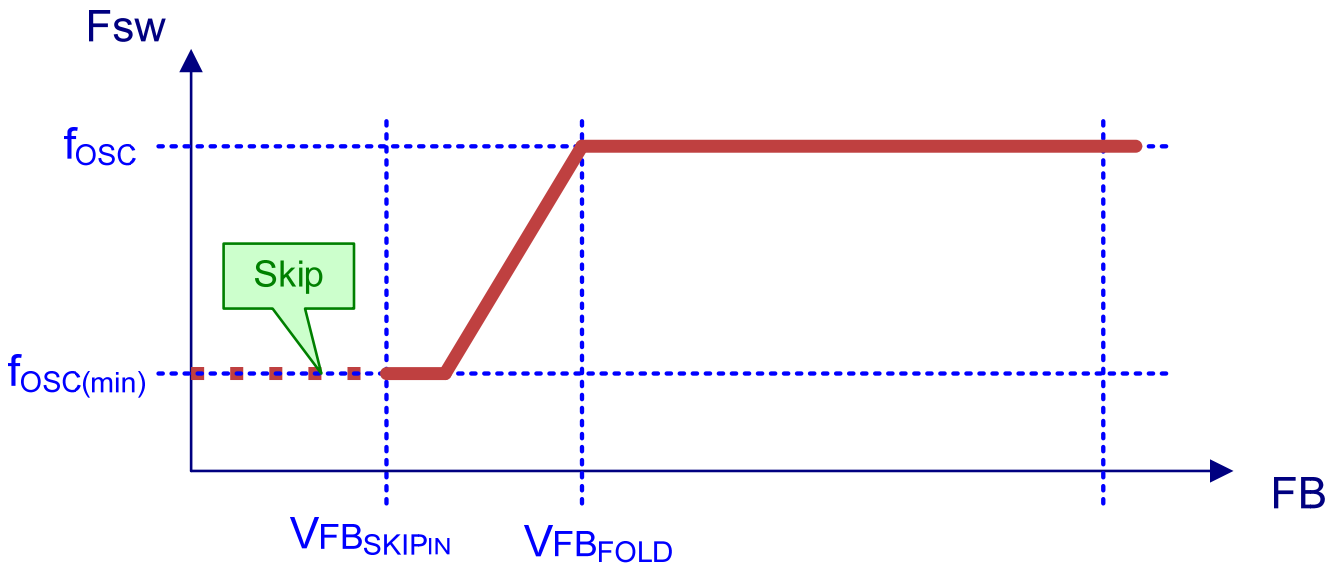
NCP1237/38/87/88 – 4 ms Soft Start



4 ms “digital” soft-start operation

4 ms Soft Start ⇒ Stressless start-up phase

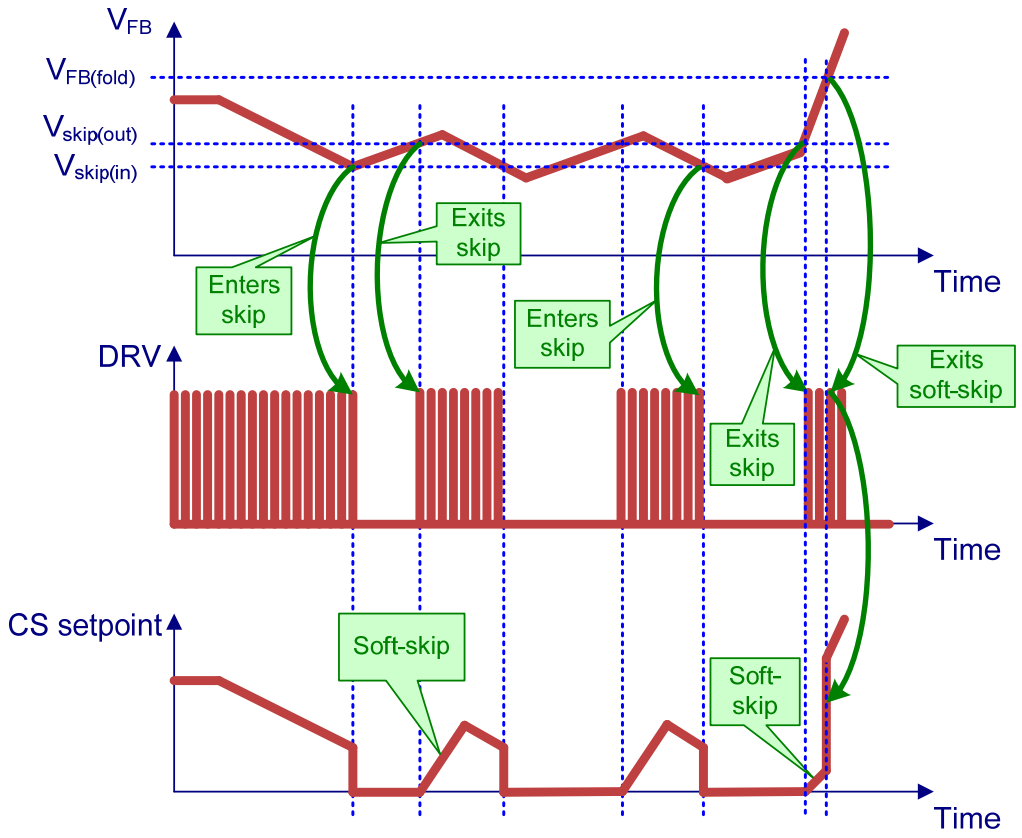
NCP1237/38/87/88 – Frequency Foldback



Switching frequency lowered at light load → Increased efficiency

Switching frequency clamped at 25 kHz → No audible noise

NCP1237/38/87/88 – Recover from Standby

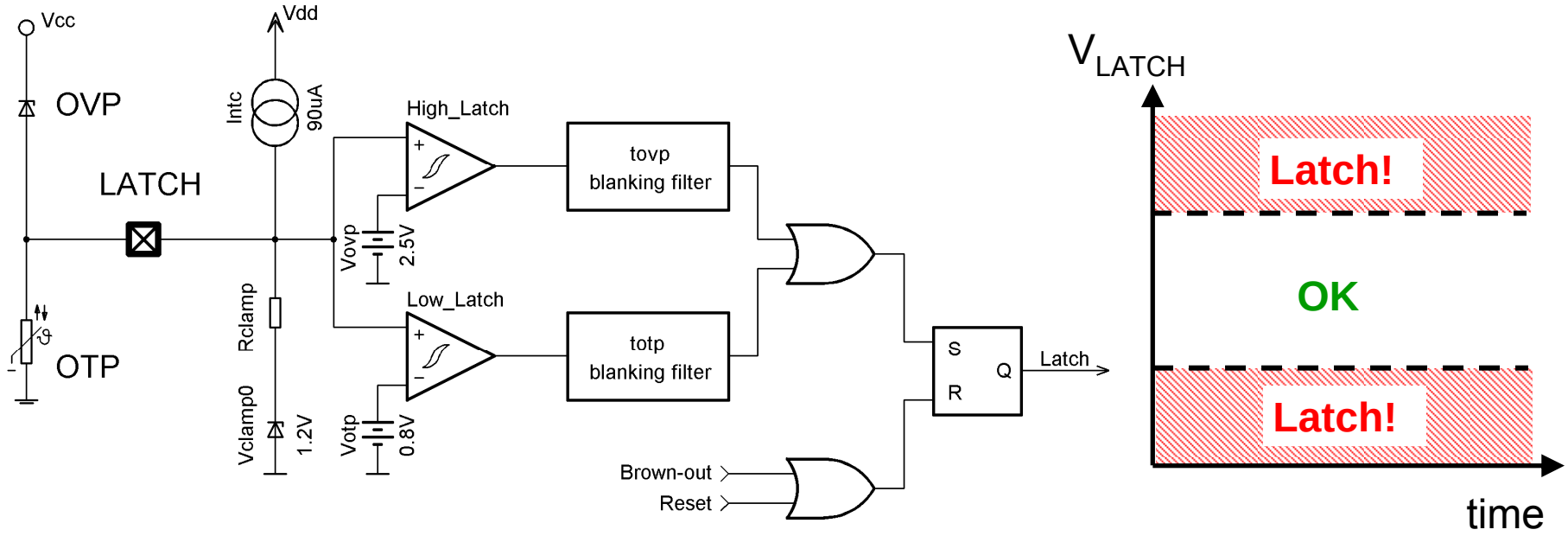


Soft-Skip mode is left as soon as the voltage on the feedback pin reaches the TLD threshold

Transient Load Detect Function (TLD)

Improved Load Transient response time

NCP1237/38/87/88 – Latch-off Protection

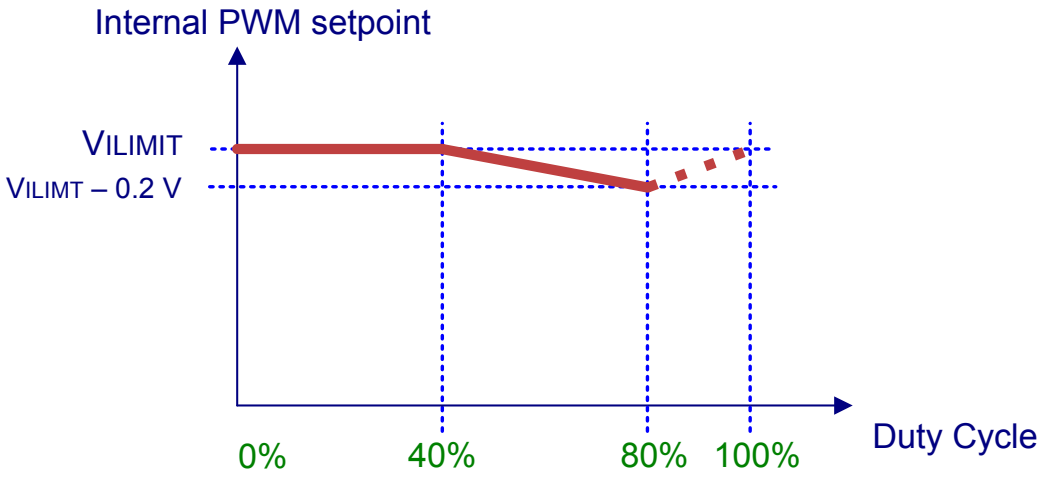


An NTC thermistor can be directly connected to the IC

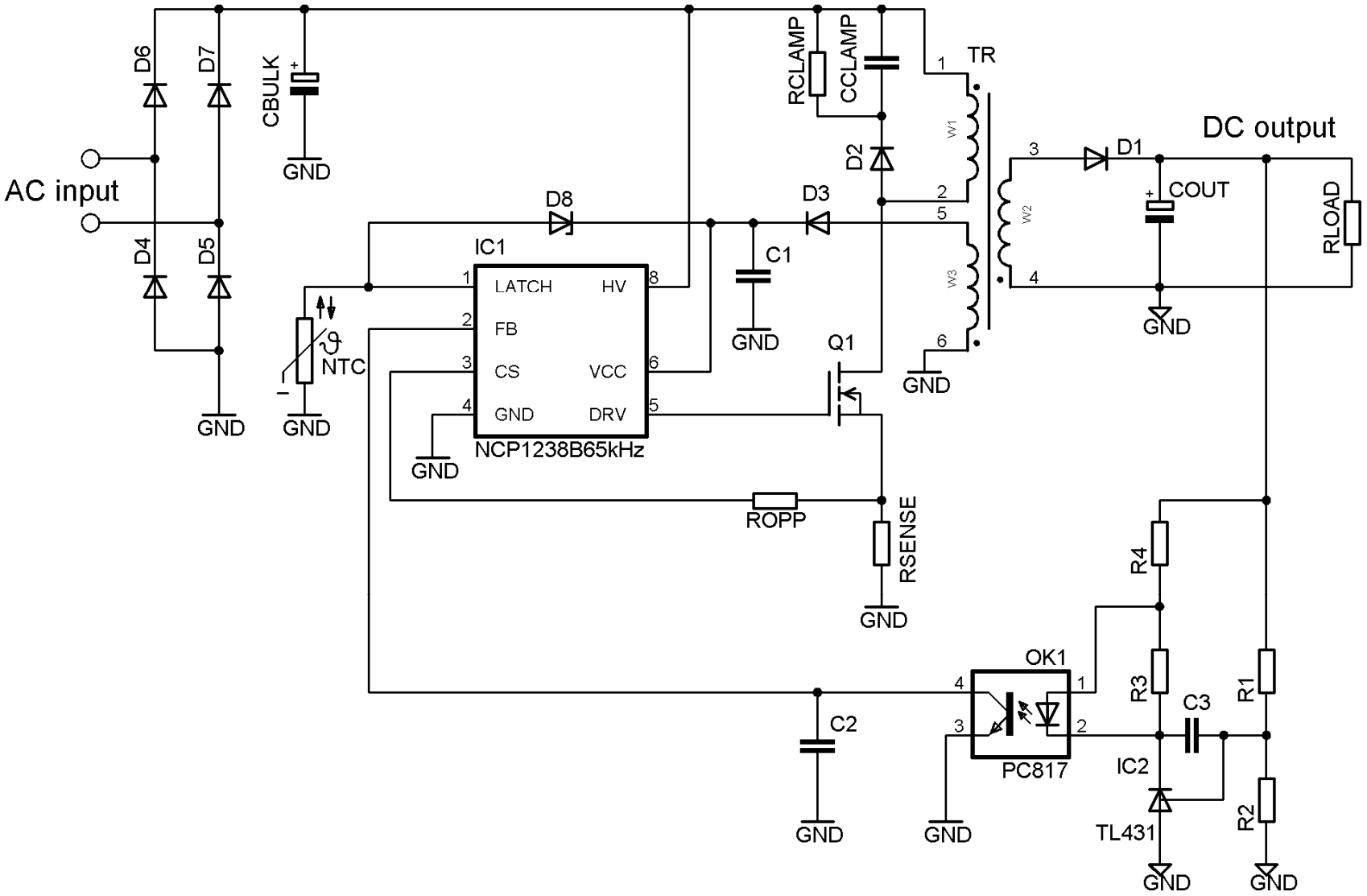
Less external components needed

NCP1237/38/87/88 – Slope Compensation

- There is a built in slope compensation with no external setting
- The internal slope compensation is activated if the duty cycle is higher than 40%
- The amount of slope compensation is 5mV/% observed at CS pin



Application Schematic



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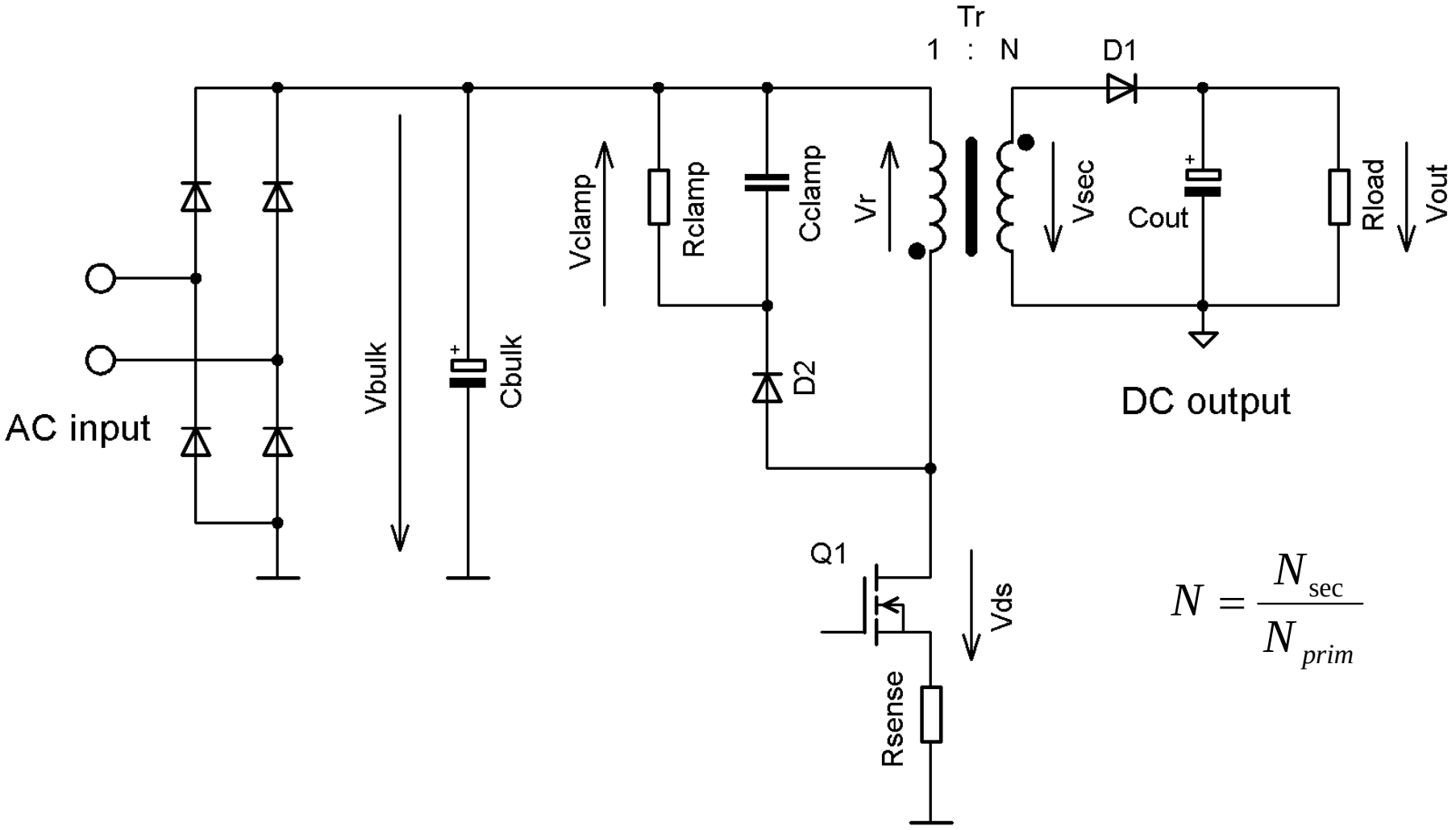
Power stage: Schematic of Flyback Converter



$$N = \frac{N_{sec}}{N_{prim}}$$

Power Stage Design: Bulk Capacitor

- Output power P_{out}

$$P_{out} = V_{out} \cdot I_{out}$$

- Average input current $I_{in,avg}$

$$I_{in,avg} = \frac{P_{in}}{V_{bulk,\min}}$$

- Estimation of input power P_{in}

$$P_{in} = \frac{P_{out}}{\eta}$$

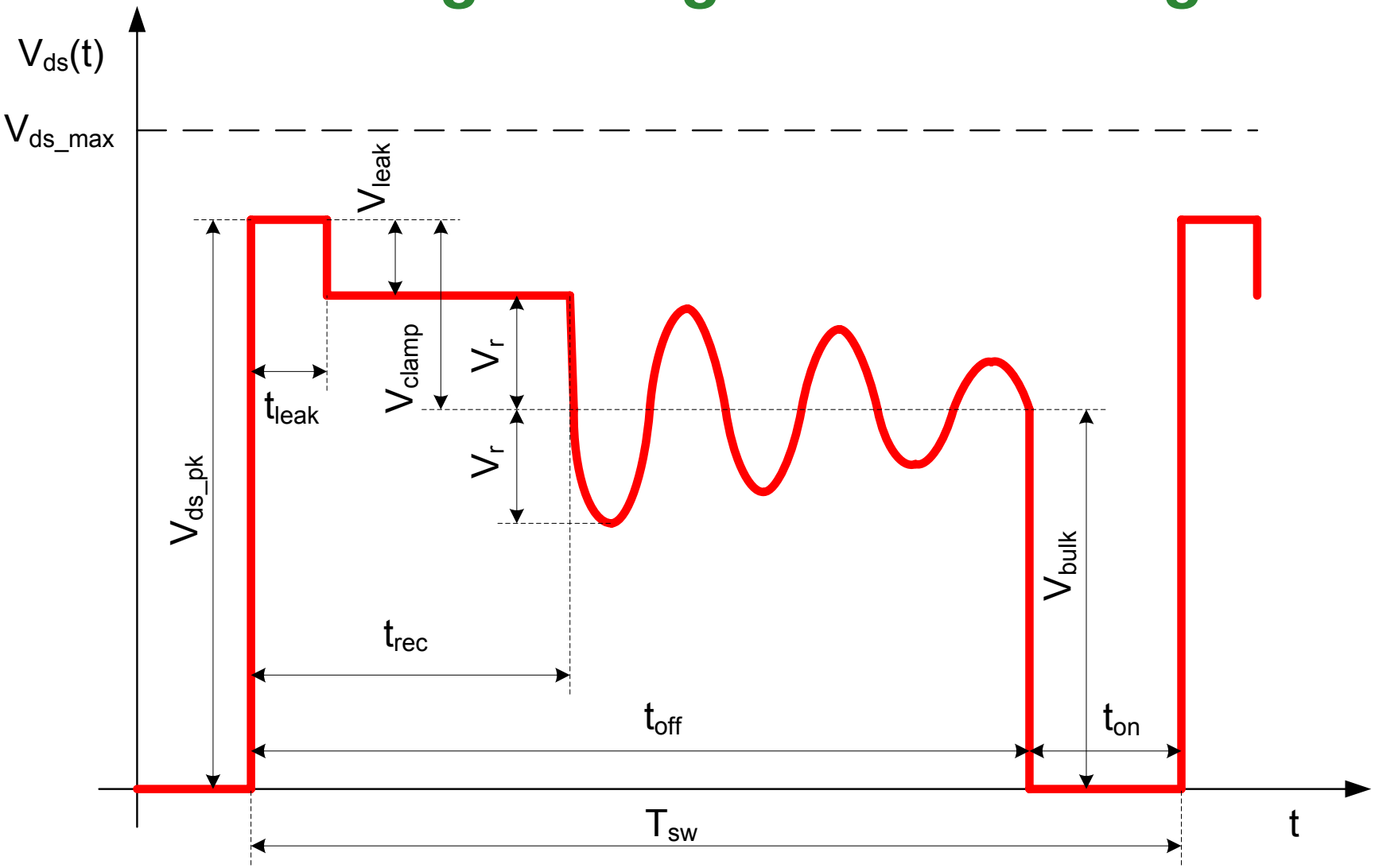
Estimate the η based on the EPA standard

- Bulk capacitor value C_{bulk}

$$C_{bulk} = \frac{I_{in,avg} \cdot t_{dis}}{\Delta V_{bulk}}$$

Use t_{dis}=8.5ms

Power Stage Design: Drain Voltage



Power Stage Design: Transformer Ratio

Transformer ratio – consideration of the V_{DSS} of used Q1

$$N = \frac{k_C \cdot \left(V_{out} + V_{f,diode}\right)}{0.85 \cdot V_{DS,\max} - 20V - V_{bulk,\max}} \qquad k_C = \frac{V_{clamp}}{V_r}$$

The 20V means margin for clamping diode turning-on overshoot.

Reflected voltage V_r at primary from secondary

$$V_r = \frac{V_{out} + V_{f,diode}}{N} \qquad N = \frac{N_{\sec}}{N_{prim}}$$

Maximum duty cycle DC_{max}

In CCM operation:

$$DC_{\max} = \frac{V_r}{V_r + V_{bulk,\min}}$$

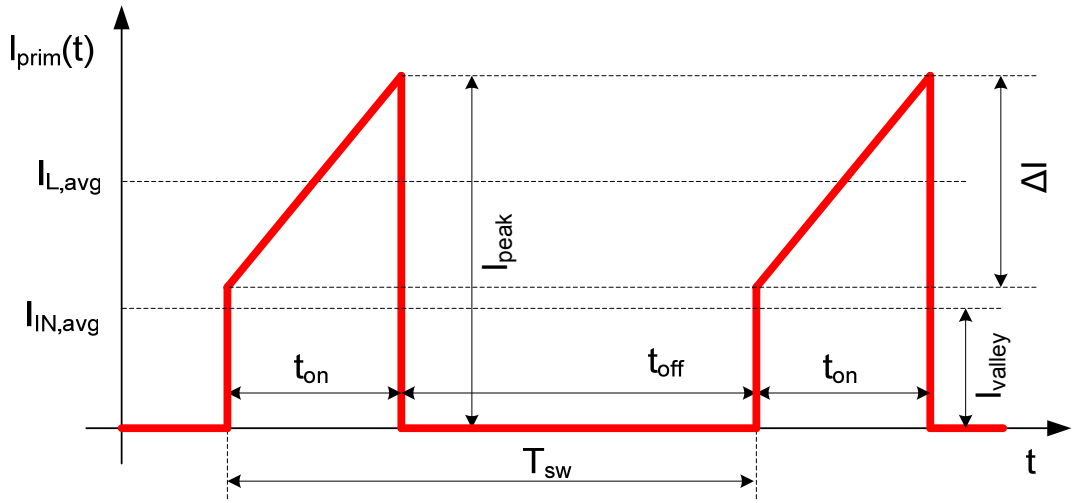
In DCM operation doesn't depend on N:

$$DC_{\max} = \frac{V_{out}}{V_{bulk,\min}} \cdot \sqrt{\frac{2 \cdot L_{prim} \cdot F_{sw}}{R_{load,\min}}}$$

Power Stage Design: Current Ripple

The average shared transformer current reflected to primary winding $I_{L,avg}$

$$I_{L,avg} = \frac{I_{in,avg}}{DC_{\max}}$$



Choose the relative ripple δI_r: it affects the operation in the CCM or DCM

- For universal AC input design use the δ Ir in range 0.5 to 1.0
- For European AC input use the δ Ir in range 0.8 to 1.6

$$\delta I_r = \frac{\Delta I}{I_{L,avg}}$$

$$\Delta I = \delta I_r \cdot I_{L,avg}$$

$$\Delta I = I_{peak} - I_{valley}$$

$$I_{peak} = I_{L,avg} \cdot \left(1 + \frac{\delta I_r}{2}\right)$$

$$I_{valley} = I_{L,avg} \cdot \left(1 - \frac{\delta I_r}{2}\right)$$

Power Stage Design: Primary Inductance

Transformer primary winding inductance L_{prim}

$$L_{prim} = \frac{V_{bulk,\min} \cdot DC_{\max}}{F_{sw} \cdot \Delta I}$$

Maximum RMS value of the current flowing through primary winding $I_{prim,RMS}$

$$I_{primRMS} = \sqrt{DC_{\max} \cdot \left(I_{peak}{}^2 - I_{peak} \cdot \Delta I + \frac{\Delta I^2}{3} \right)}$$

Maximum RMS value of the current flowing through secondary winding $I_{sec,RMS}$

$$I_{sec,peak} = \frac{I_{peak}}{N} \qquad \Delta I_{sec} = \frac{\Delta I}{N}$$

$$I_{sec\,RMS} = \sqrt{(1 - DC_{\max}) \cdot \left(I_{sec,peak}{}^2 - I_{sec,peak} \cdot \Delta I_{sec} + \frac{\Delta I_{sec}{}^2}{3} \right)}$$

Power Stage Design: Q1 Selection

Conduction loss at Q1 should be approx. 1% of the Pout

$$R_{DSon} \le \frac{P_{out}}{100 \cdot I_{prim,RMS}^{\ 2}}$$

Then the right device is chosen by parameters V_{DSmax}, I_{peak}, t_{on}, t_{off}

Current sensing resistor R_{sense} selection

$$R_{sense} = \frac{V_{ILIM}}{1.1 \cdot I_{peak}} \qquad P_{sense} = I_{primRMS}^{\ 2} \cdot R_{sense}$$

The 1.1 factor means 10% margin for L_{prim} and other parameters spread, to be able to deliver maximum power.

Power Stage Design: Secondary Rectification

D1 selection:

Reflected voltage across D1

$$PIV = V_{bulk,\max} \cdot N + V_{out}$$

The next important parameters for D1 selection are $I_{sec,peak}$, I_{out} and the fast and soft recovery

Cout selection:

Minimum C_{out} value

$$C_{out} \geq \frac{I_{out} \cdot DC_{\max}}{V_{out,ripple} \cdot F_{sw}}$$

The maximum allowed ESR of C_{out}

$$ESR \leq \frac{V_{out,ripple}}{I_{\sec,peak}}$$ Dominant part

$$I_{Cout,rms} = \sqrt{I_{\sec,rms}^{\ 2} - I_{out}^{\ 2}}$$

it is recommended to use more parallel C_{out} for lowering the output voltage ripple.

Power Stage Design: Clamping Network

TVS – losses in the suppressor: better at no load conditions

$$P_{clamp} = E_{clamp} \cdot F_{sw} = \frac{1}{2} \cdot L_{leak} \cdot I_{peak}^{2} \cdot F_{sw} \cdot \frac{V_{clamp}}{V_{clamp} - V_r}$$

RCD clamp – 1st iteration: better EMI response

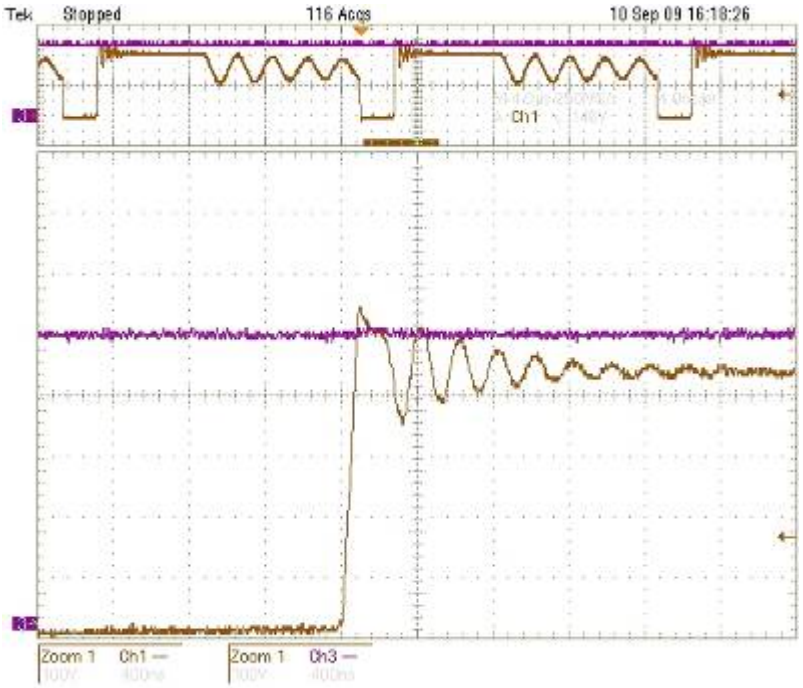
$$R_{clamp} = \frac{2 \cdot V_{leak} \cdot V_{clamp}}{L_{leak} \cdot I_{peak}^{2} \cdot F_{sw}}$$

$$P_{clamp} = \frac{V_{clamp}^{2}}{R_{clamp}}$$

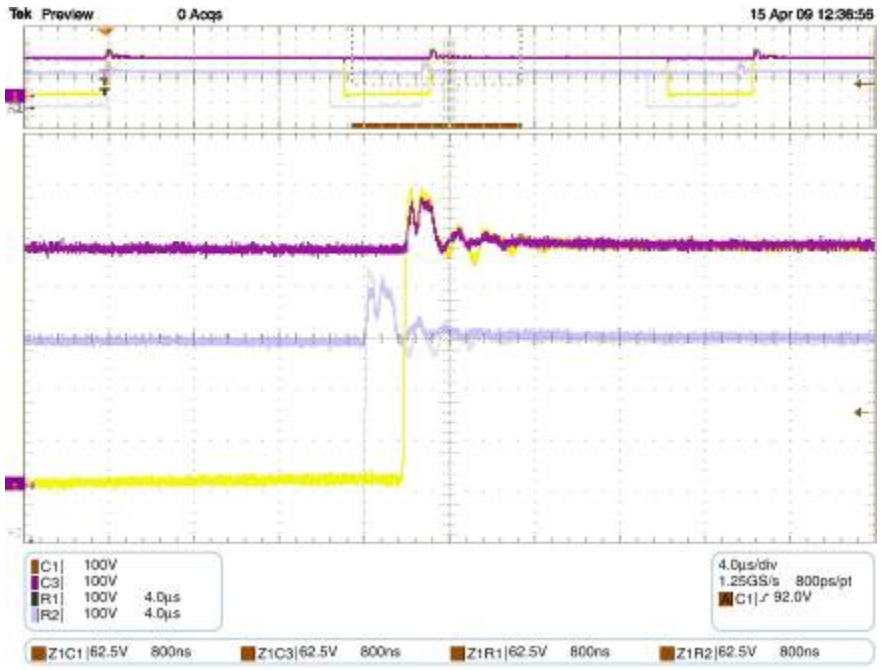
$$C_{clamp} > \frac{V_{clamp}}{V_{ripple} \cdot R_{clamp} \cdot F_{sw}}$$

These values need to be optimized for the no load consumption and losses in slow clamping diode D2

TVS vs RCD Clamp Comparison



Drain voltage ringing with TVS as clamp

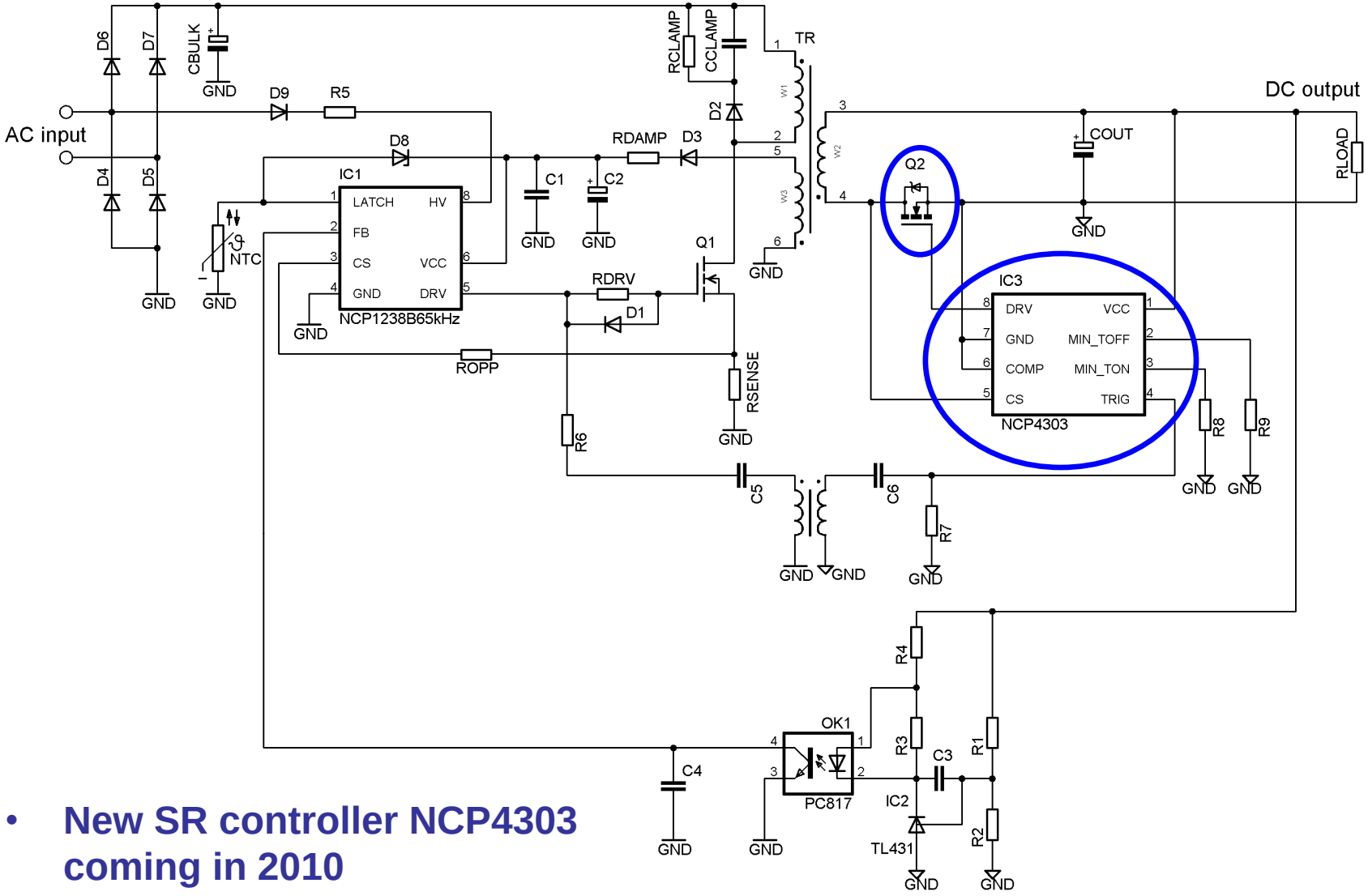


Drain voltage ringing with RCD as clamp

Different R_{damp} used in clamp

Ch1 – Drain, Ch3 – Clamp node

Synchronous Rectification



- **New SR controller NCP4303 coming in 2010**

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Over Power Compensation

The overpower compensation affects the primary peak current, by the following formula:

$$I_{PEAK} = \frac{V_{CS\,\mathrm{int}}}{R_{sense}} + V_{bulk} \cdot \left(\frac{t_{PROP}}{L_P} - g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}} \right) + V_{off} \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}}$$

Then the overpower compensation resistor can be calculated:

$$R_{OPP} = \frac{t_{PROP} \cdot R_{sense}}{L_P \cdot g_{OPP}}$$

The over power compensating resistor affects only the I_{peak} value, but in CCM the output power is given by the following formula, where I_{valley} plays a role:

$$P_{out} = \frac{1}{2} \cdot \eta \cdot L_{prim} \cdot F_{sw} \cdot \left(I_{peak}^{\,2} - I_{valley}^{\,2} \right)$$

2nd Level Over Power Protection

The overpower compensation affects the 2nd level over power protection by the addition of bulk voltage feed forward.

$$I_{TRAN} = \frac{V_{CStran}}{R_{sense}} - \left(V_{bulk} - V_{off}\right) \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}}$$

The overpower compensation can be used for reducing the transformer size to ½ and keeping the peak power capability.

Spread Sheet Design of OPC

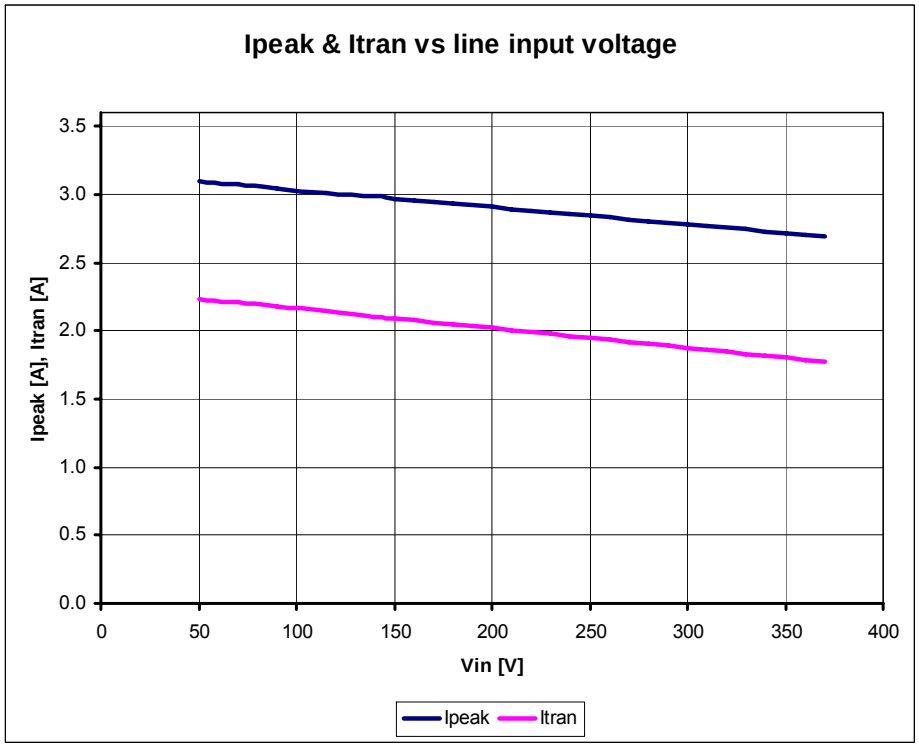
OPC design spread sheet was created and the user can choose the right R_{OPP} and it's effect to I_{peak}, I_{tran}, P_{out} and P_{tran}:

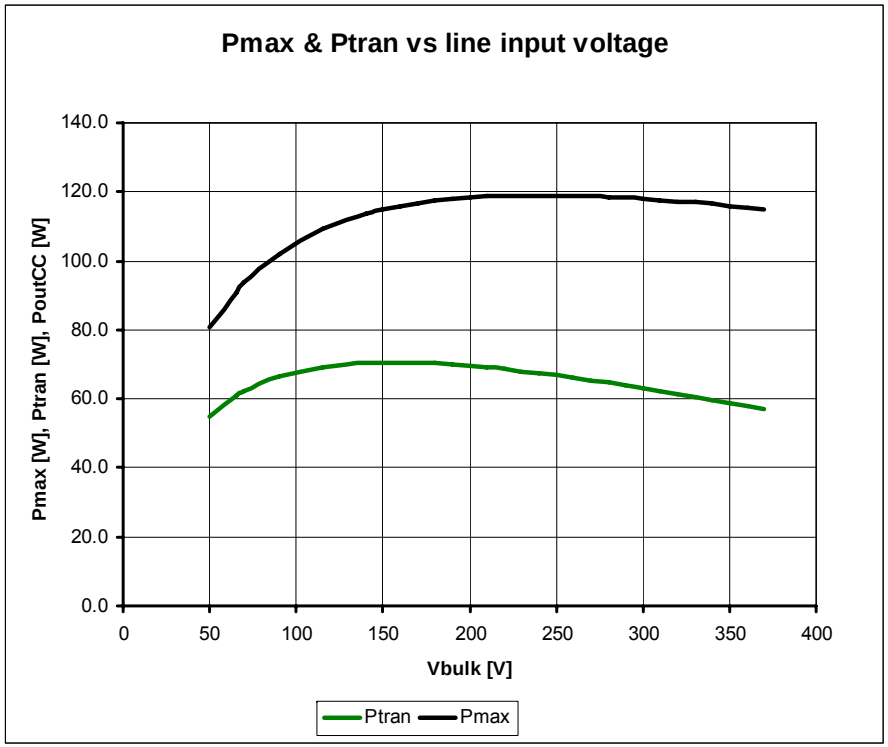
Inputs:

Output voltage	Vout [V]	19
Primary turns	N1 [-]	100
Secondary turns	N2 [-]	25
Ramp Comp at CS	RaCo [mV/%]	5
Maximum int set point	Vilimit [V]	0.7
Sensing resistor	Rsense [Ohm]	0.235
Propagation delay	tprop [ns]	100
Primary inductance	Lp [uH]	560
Vin to Iopp ratio	gopp [uS]	0.5
Over power comp resistor	Ropp [Ohm]	680
Switching frequency	Fsw [kHz]	65
2nd level overcurrent prot	Vcstran [V]	0.5

Will be available soon, while NCP1237/38/87/88 will be released

Spread Sheet Design of OPC





Keeping constant I_{peak} in CCM mode tends to I_{valley} decreasing with increasing the Vin. That's why the maximum output deliverable power P_{out} increases with increasing Vin. **Choose the right compensation.**

Loop Compensation

Download the work sheet at:

http://www.onsemi.com/pub/Collateral/FLYBACK DWS.XLS.ZIP

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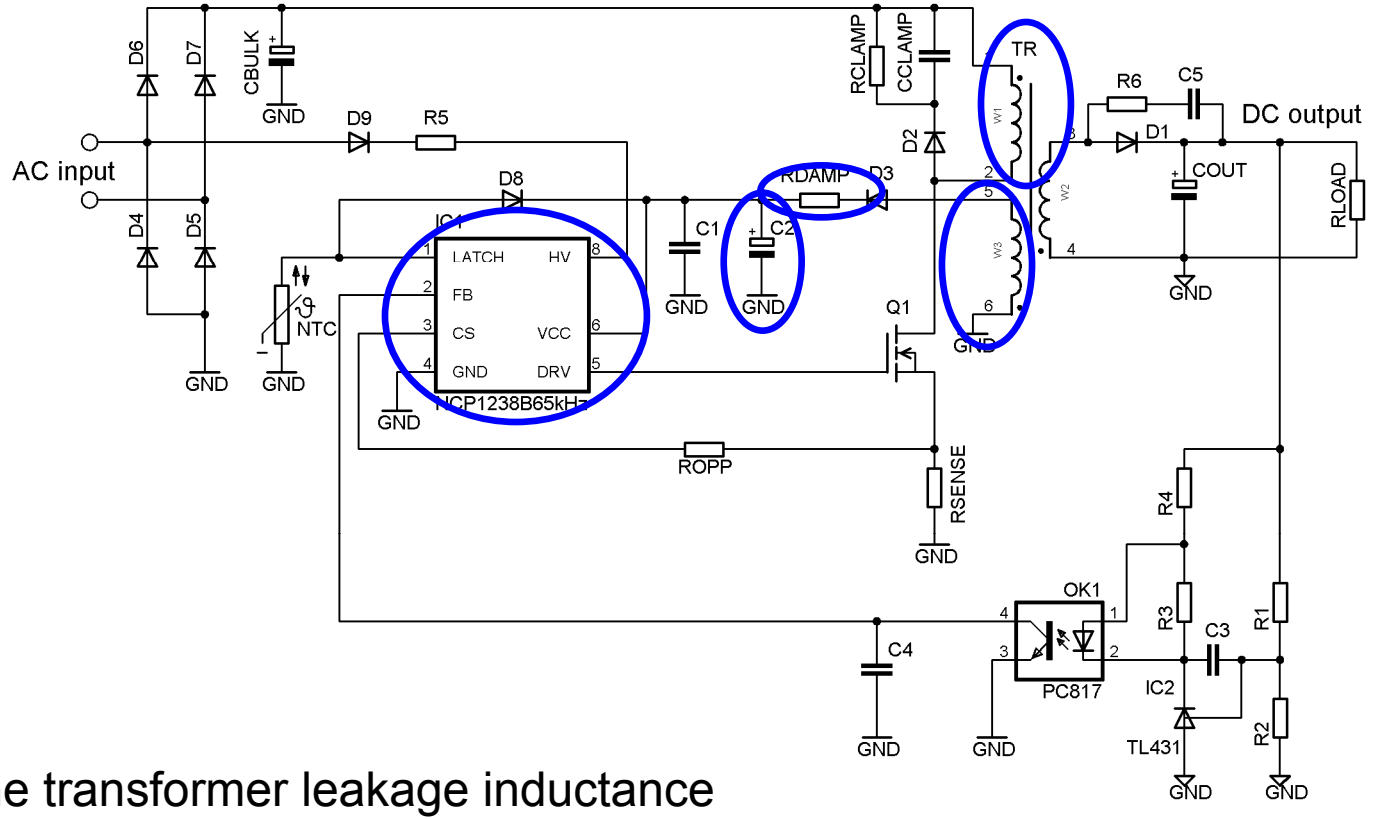
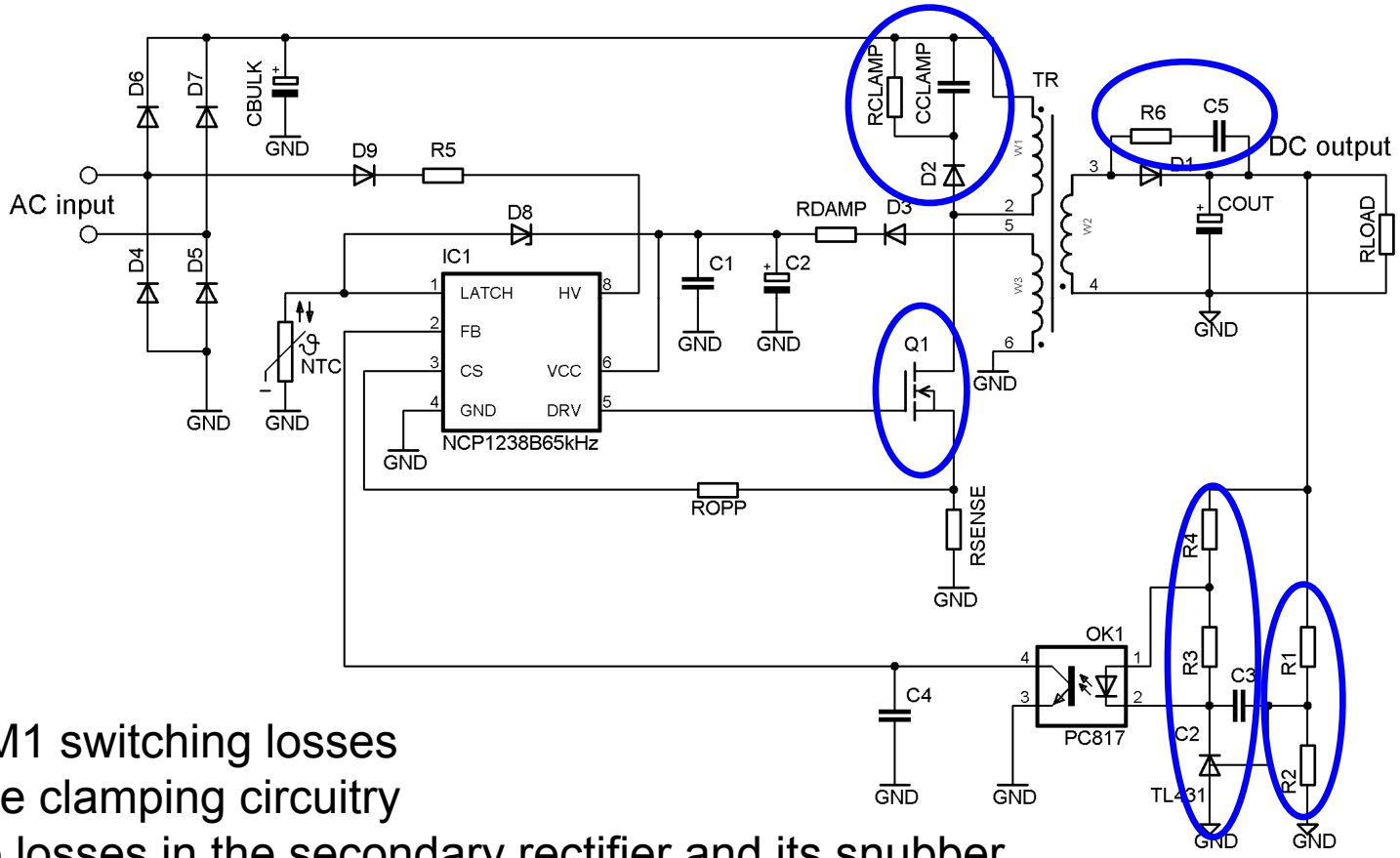
No Load Input Power Reducing Approach



- Decrease the transformer leakage inductance
- Use the controller IC with the frequency foldback and skip mode features
- Do not allow the DSS operation (Vcc cap increase)
- In case of low Vcc and high aux winding leakage increase the aux number of turns to disable the DSS
- Decrease the value of the Vcc damping resistor (may affect the EMI)

No Load Input Power Reducing Approach



- Lower the M1 switching losses
- Optimize the clamping circuitry
- Reduce the losses in the secondary rectifier and its snubber
- Decrease the TL431 biasing
- Decrease the cross current through the feedback resistor divider
- Set a stable operation for all loading currents
- Do not use the output voltage indication LED

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Area Product A_P

- There is defined the area product A_P [m^4]
- Product of effective window area W_a [m^2] and iron cross section area A_c [m^2]

$$A_P = W_a \cdot A_c$$

- Allows fast, effective and optimal magnetic design
- Should be published in core datasheet

Window Utilization Factor Ku

Ku is a measure of the amount of copper that appears in the window area of transformer. This window utilization factor is affected by:

1) Wire insulation
2) Wire lay (fill factor)
3) Bobbin area
4) Insulation required for multilayer windings or between windings

Typical values lay in range 0.35 to 0.48

The Load Coefficient K_{load}

- Flux density in magnetic should be designed at I_{peak} with some margin (5%) to avoid saturation
- Do you really need 100% Iout for 100% time??

If not, decrease core size!!

$$K_{load} = \frac{I_{out,RMS}}{I_{out,RMS,\max}}$$

Example:

- Maximum DC output current is 3.5 A, but it's only needed for transients
- The long term RMS value is only 1.75 A (at least 10 min.)
- Loading coefficient is only 0.5 (not 1) → core size is smaller → losses in core and in copper are smaller

Flyback Transformer Core Sizing

The core size can be calculated by the A_P factor in case of these inputs:

1. Converter parameters: L_{prim}, I_{peak}, K_{load}, δI_r, DC_{max}
2. Core maximum flux density B_{max} considered with the hysteresis and eddy current losses at switching frequency F_{sw}
3. Winding parameters (utilization factors for primary and secondary windings Ku_{prim}, Ku_{sec}), (current densities in primary and secondary windings J_{prim}, J_{sec}

$$A_P = \frac{L_{prim} \cdot I_{peak}^{\,2}}{B_{max}} \cdot K_{load} \cdot \left(\frac{\sqrt{DC_{max}}}{J_{prim} \cdot Ku_{prim}} + \frac{\sqrt{1 - DC_{max}}}{J_{sec} \cdot Ku_{sec}} \right) \cdot \sqrt{\frac{\delta I_r^{\,2} + 12}{3 \cdot (\delta I_r + 2)^2}}$$

Now the appropriate core can be selected from the vendor products list by the A_P factor .

Windings Design

- Number of turns of primary winding

$$NT_{prim} = \frac{L_{prim} \cdot I_{peak}}{B_{\max} \cdot A_c}$$

- Number of turns of secondary winding

$$NT_{\sec} = N \cdot NT_{prim}$$

- Number of turns of auxiliary winding

$$NT_{aux} = \frac{V_{CC} + V_{f,Vcc}}{V_{out} + V_{f,diode}} \cdot NT_{\sec}$$

Air Gap Length l_g

$$l_g = \frac{N \cdot \mu_0 \cdot I_{peak}}{B_{max}} - \frac{MPL}{\mu_r}$$

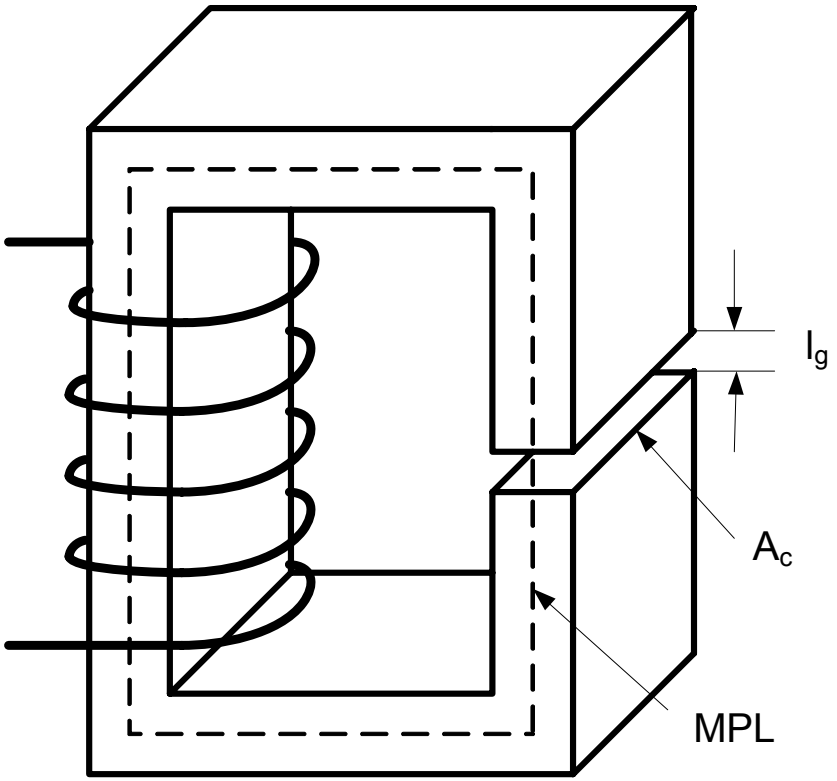
in case of $l_g << MPL$

MPL – core magnetic path length

μ_0 - permeability of vacuum

μ_r - permeability of core

In case an EE, RM or pot core is used, divide the calculated l_g by factor 2, because your core has 2 air gaps in magnetic path



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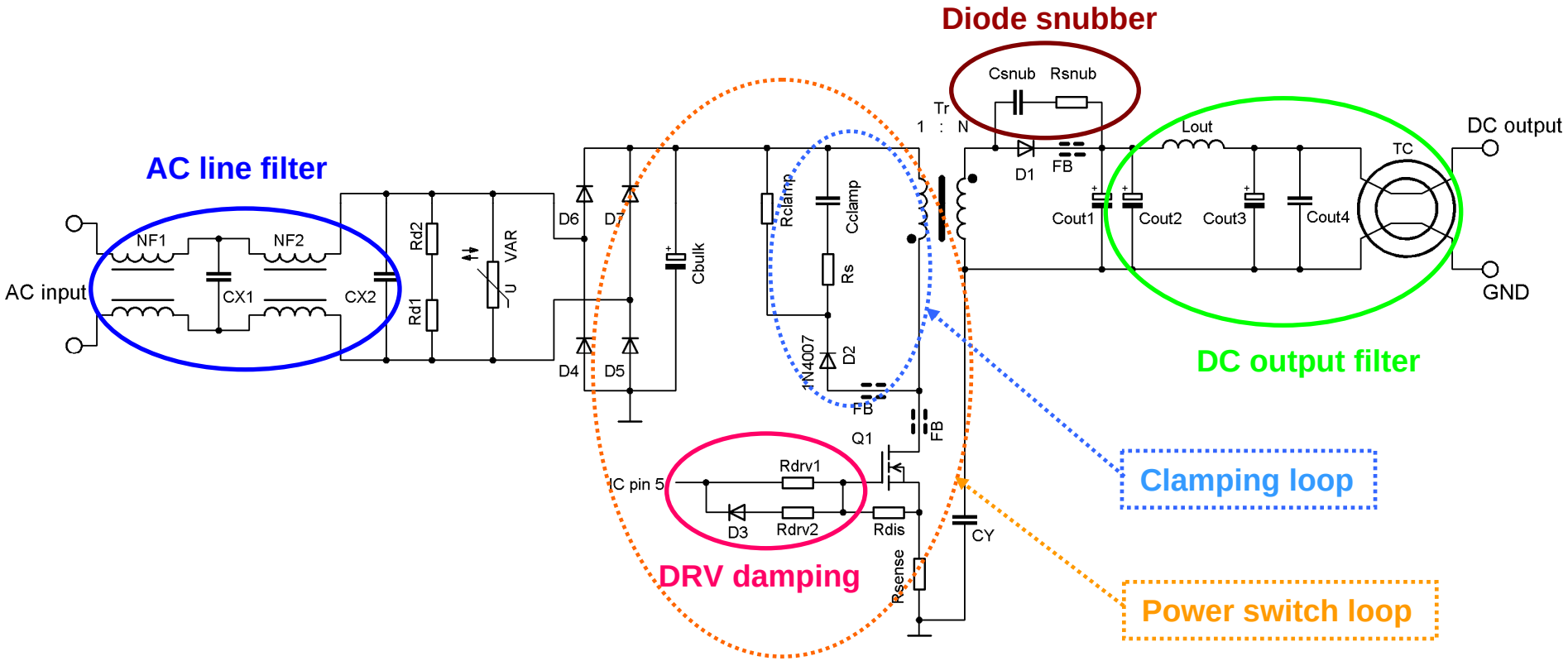
How to improve EMI of my design?



- All switching loops with RF currents should have small area
- Divide input AC filter at two chokes to decrease the parasitic capacitance coupling
- CY – closes the current loop for the RF currents injected via transformer

Diode Snubber Design

- Snubber resistance value should be close to the characteristic impedance of ringing circuitry

$$R_{snubber} = \sqrt{\frac{L_{leak,SEC}}{C_d}}$$

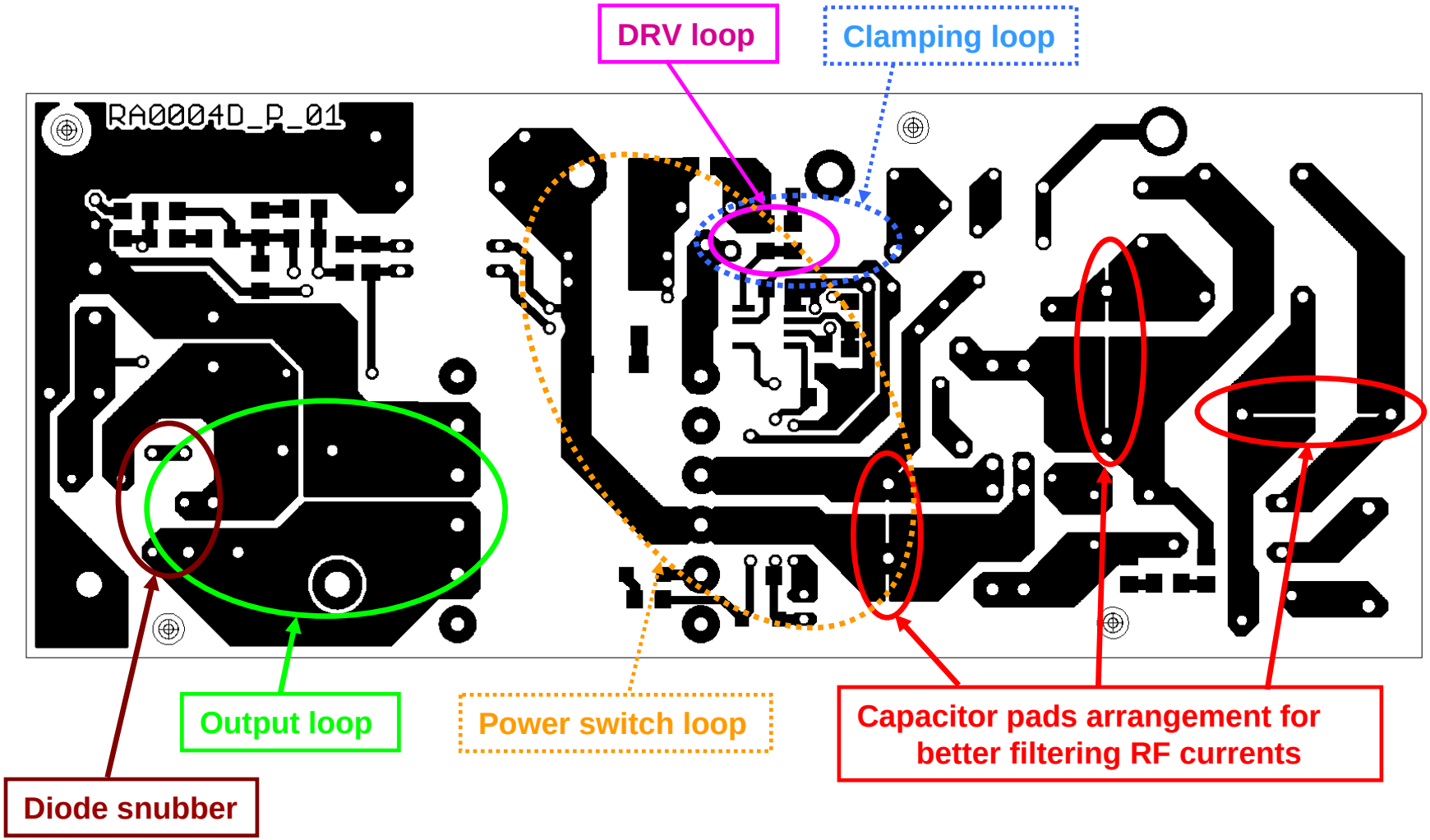
$L_{leak,SEC}$ –the transformer leakage inductance observed from secondary side

C_d – reverse direction diode capacitance

- RC time constant of the snubber should be small compared to the switching period but long compared to the voltage rise time

$$C_{snubber} \approx 3 \div 4 \cdot C_d$$

PCB Layout Tips



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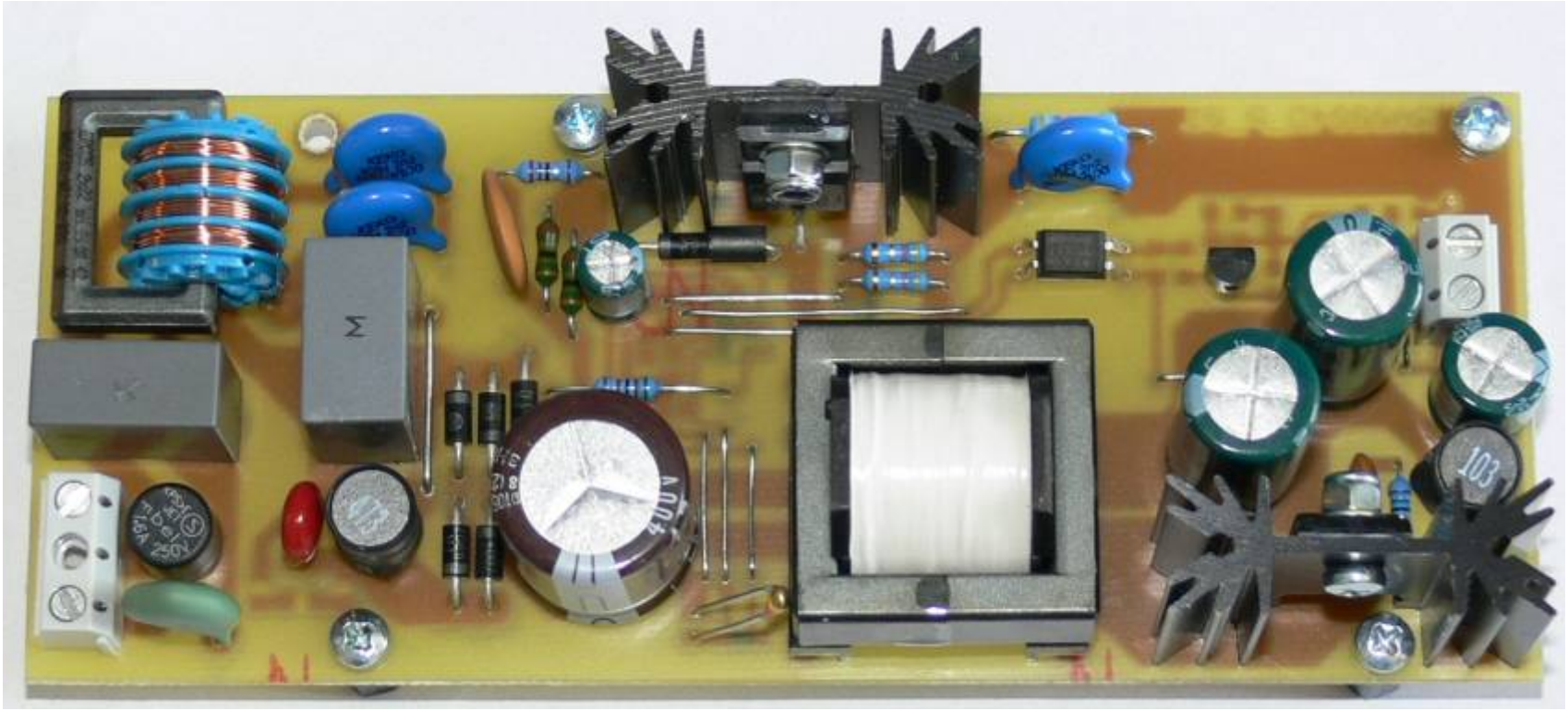
Preliminary Demonstration Board

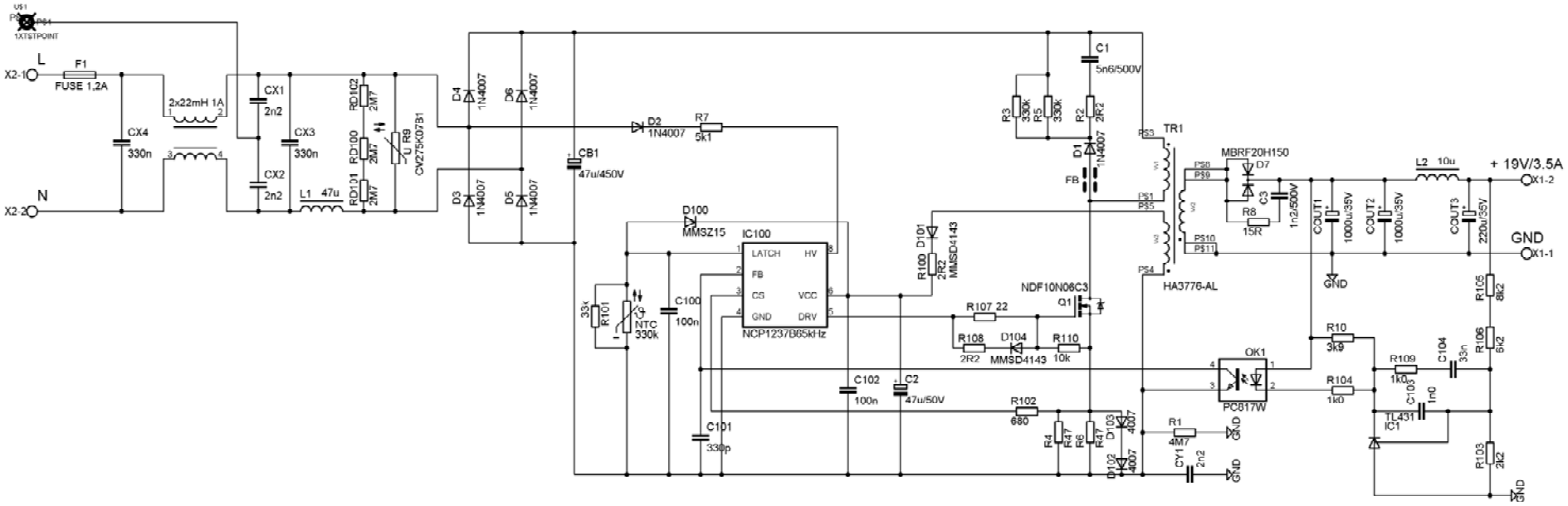
A typical 65 W notebook adapter (19 V output)



(optimized for EPS 2.0)

Schematic of Preliminary Demonstration Board

A typical 65 W notebook adapter (19 V output)



(optimized for EPS 2.0)

Demonstration Board Efficiency (Measured with DC Cord)

The DC cord length is 1.05m and copper cross sec. is 0.75mm^2

V_{IN} % of P_{OUTnom}	115 Vac/60Hz	230 Vac/60Hz
100 % (65 W)	87.10 %	87.37 %
75 % (49 W)	87.52 %	87.63 %
50 % (32 W)	87.54 %	87.88 %
25 % (16 W)	87.79 %	85.96 %

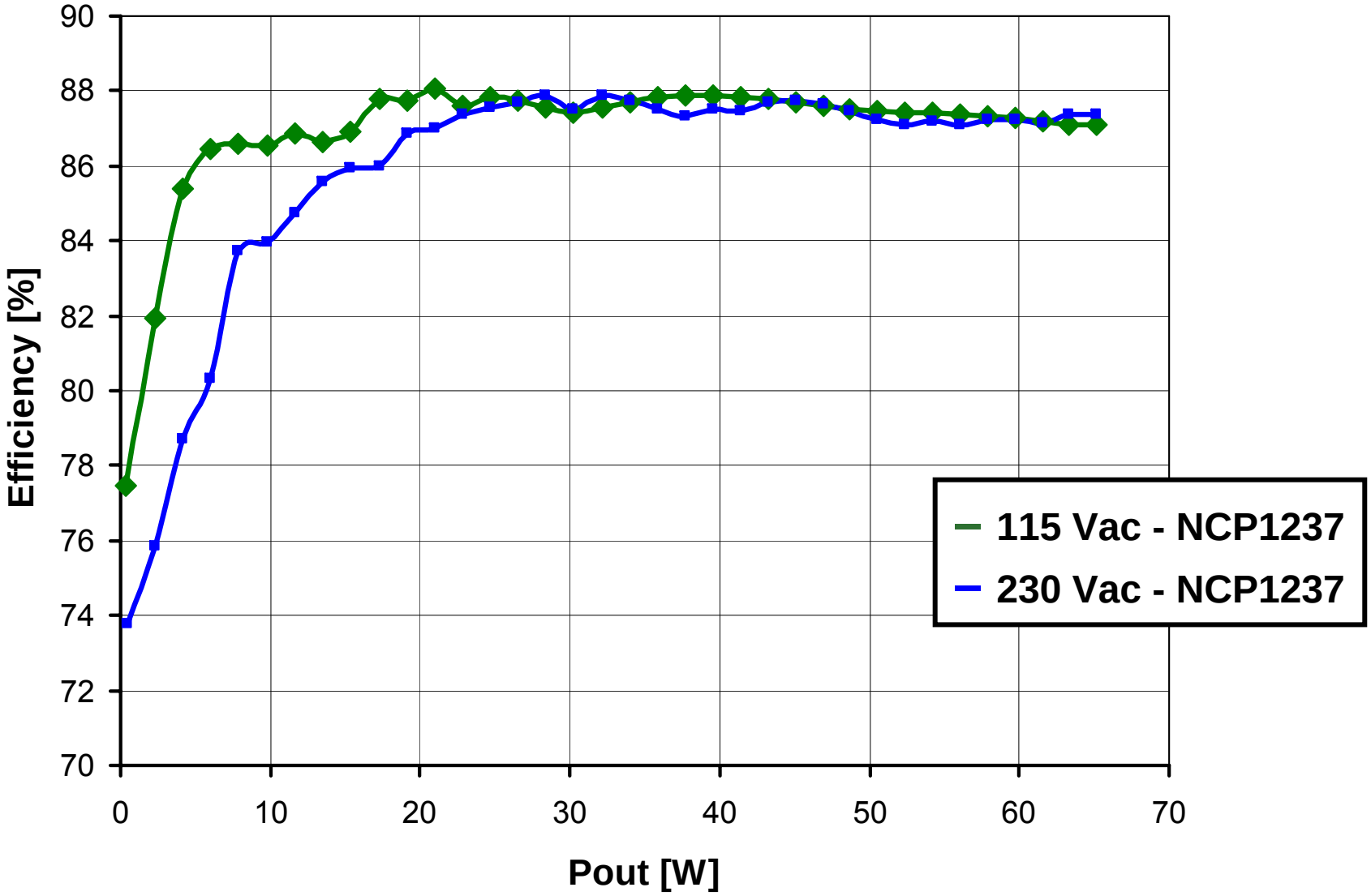
Average at 115Vac is 87.32% and at 230 Vac is 87.21 %

Demonstration Board Standby Power

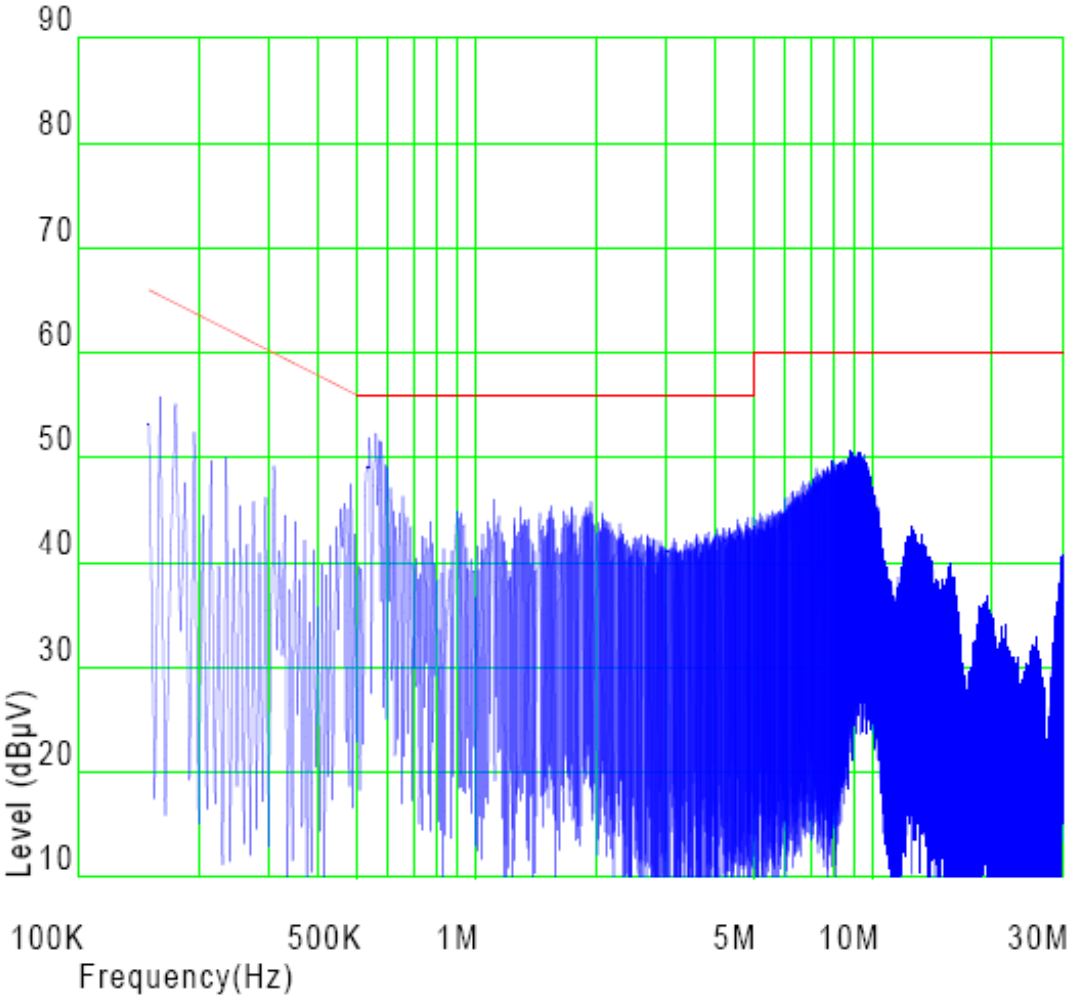
Light load and no load input power with the NCP1237

P_{OUT} \ V_{IN}	115 Vac/60 Hz	230 Vac/50 Hz
10 % (6.5 W)	86.55 %	83.74 %
5 % (3.3 W)	85.40 %	78.72 %
1 % (0.65 W)	77.49 %	73.77 %
No load	51.1 mW	73.5 mW

Demonstration Board Efficiency

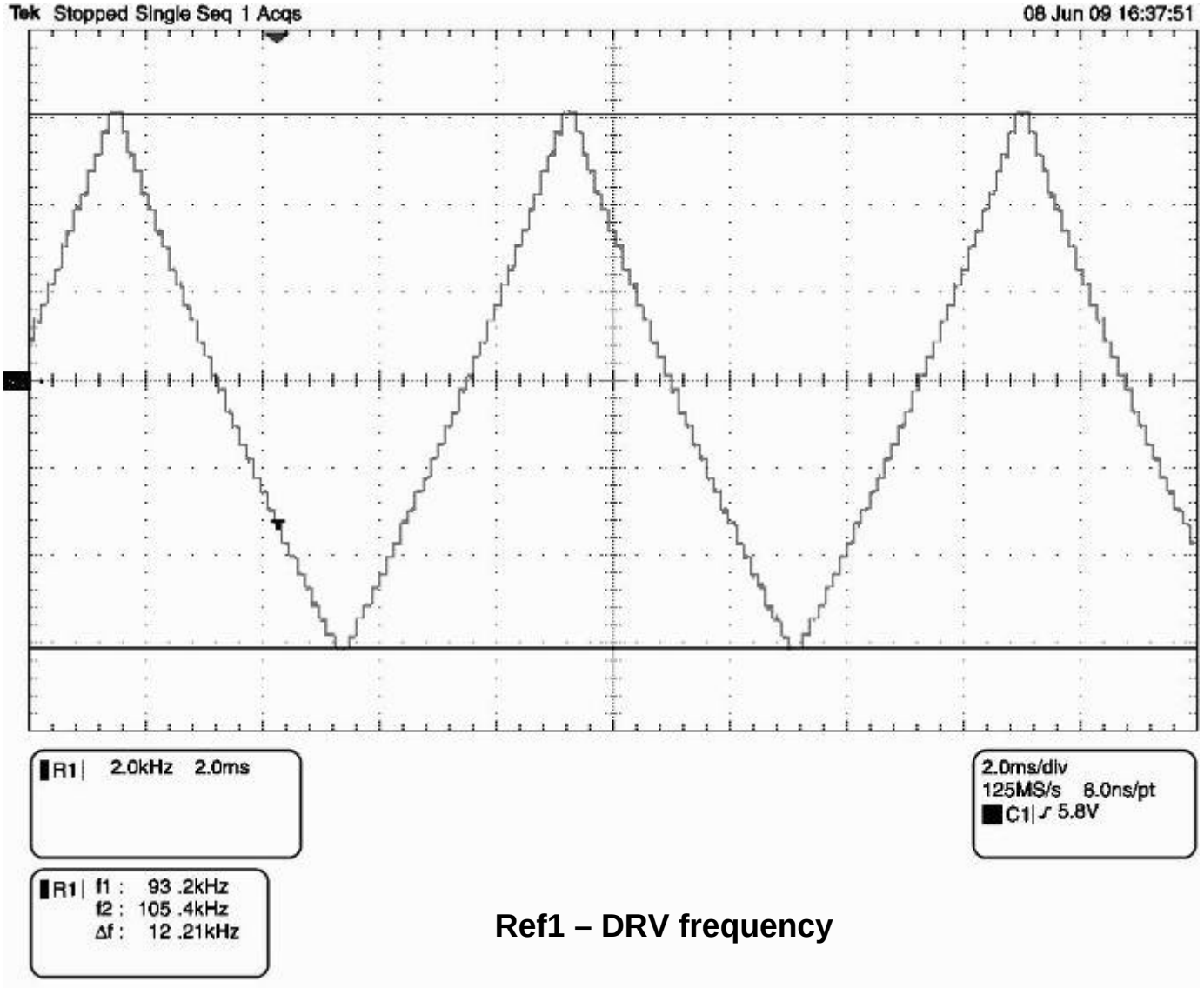


Demonstration Board Conducted EMI



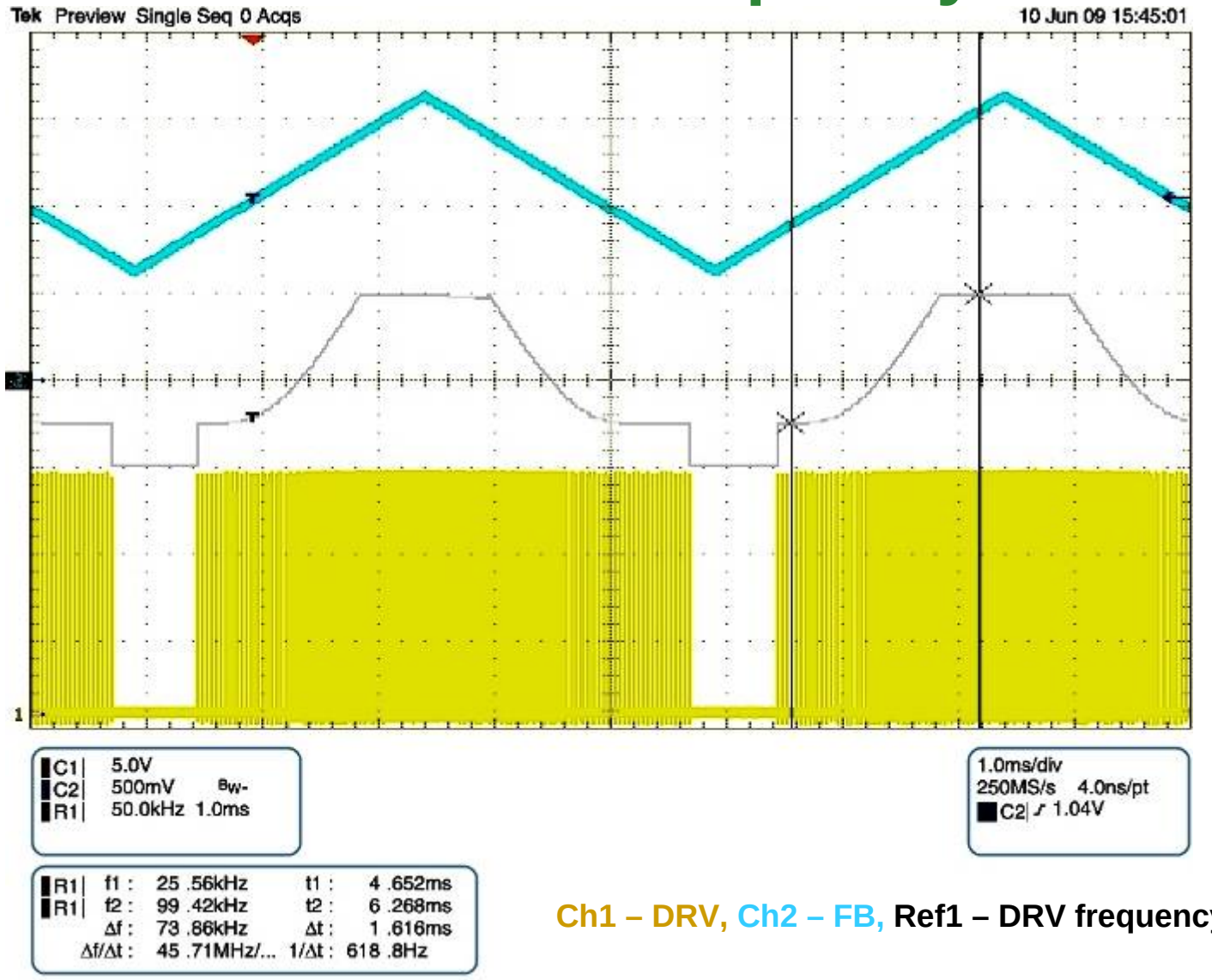
80% of full load (2.72 A) at 230 V/50 Hz NCP1237B 65 kHz

NCP1237B 100 kHz Frequency Jittering



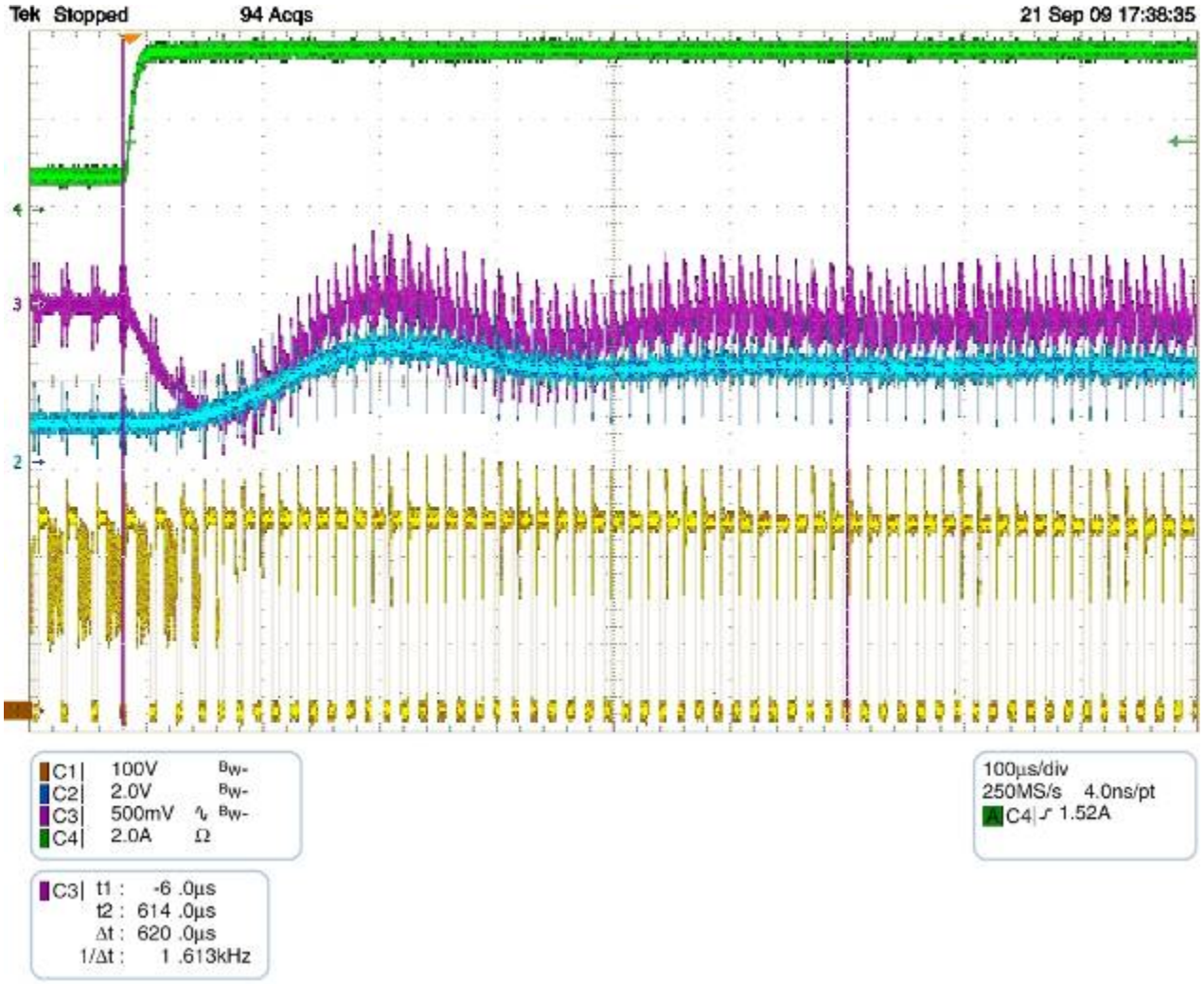
Ref1 – DRV frequency

NCP1237B 100 kHz Frequency Foldback



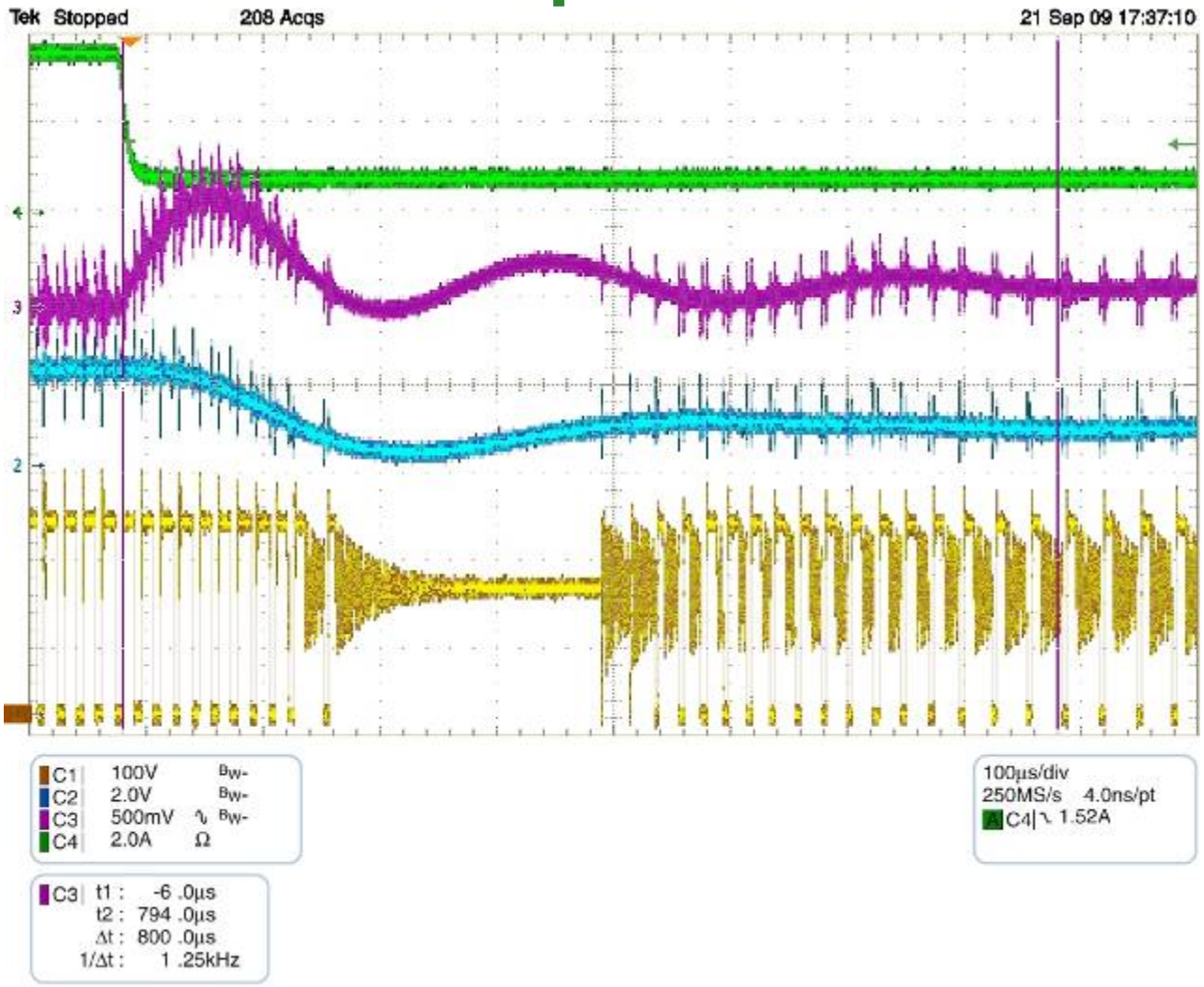
Ch1 – DRV, Ch2 – FB, Ref1 – DRV frequency

Load Transient Response from 20% to 100%



Ch1 – Drain, Ch2 – FB, Ch3 – Vout (AC coupling), Ch4 - Iout

Load Transient Response from 100% to 20%



Ch1 – Drain, Ch2 – FB, Ch3 – Vout (AC coupling), Ch4 - Iout

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Conclusion

- Meeting the most recent requirements from ENERGY STAR® or IEC is possible with the classical **Flyback** converter
- The new controller NCP1237/37/87/88 with frequency foldback and skip-mode at light load makes it possible
- Average efficiencies above **87%** are possible
- No-load input power below **300 mW** is possible
- No-load input power below **100 mW** is achievable, although the controller alone cannot ensure this. The whole power supply must be designed to reduce power waste.

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies