Design Example Report

Title	***75 W Single Output, Power-factor Corrected LED Driver Using TOP250YN***
Specification	208 VAC – 277 VAC Input 24 V, 3.1 A Output
Application	LED Driver
Author	Power Integrations Applications Department
Document Number	DER-136
Date	April 1, 2008
Revision	1.6

Summary and Features

- Single stage PFC based constant voltage, constant current output power supply
- 208 to 277 VAC input range.
- Average efficiency (over input range) at full load >85%
- Meets ENERGY STAR minimum PF requirement of 0.9 for commercial environment (0.9 worst case at 277 VAC)
- Meets harmonic content limits as specified in IEC 61000-3-2 for Class C
- Meets EN55015 B conducted EMI limits with >10 dBµV margin
- Fully fault protected
  - Auto-restart withstands shorted output indefinitely
  - Integrated thermal shutdown protects the entire supply
  - Operates with no-load indefinitely
- Full load: 6 rows of 4 diodes part# LW W5SG/GYHY-5K8L-Z

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

1 Introduction

The document presents a power supply design for LED Lighting applications. The design input voltage range is 208 to 277 VAC. The supply employs a single stage power-factor corrected circuit to generate a 24 V, 3 A output and meets the Energy Star minimum pf requirement of 0.9 for commercial applications with a high efficiency of 84%.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data for this design.

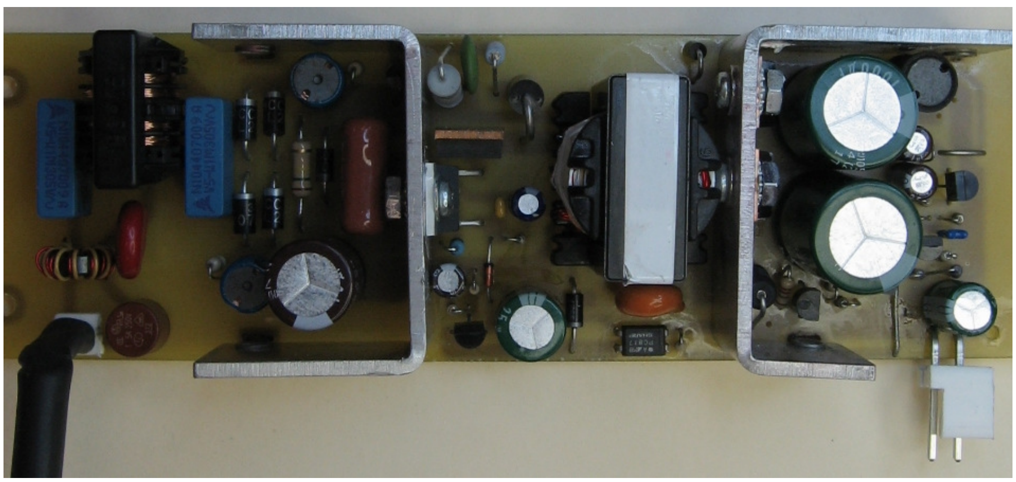


Figure 1 – Populated Circuit Board Photograph.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	208		277	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}		24	28	V	20 MHz Bandwidth
Output Current 1	I_{OUT1}		3.1		A	
Total Output Power						
Continuous Output Power	P_{OUT}			75	W	
Environmental						
Conducted EMI		Meets EN55015B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge		1			kV	1.2/50 µs Surge, IEC 61000-4-5, Series Impedance: Common Mode: 12 Ω
Surge		0.5			kV	1.2/50 µs Surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring-wave		2.5			kV	0.5 µs-100KHz Ring-wave IEEE C.62.41-1991, Class A, Differential and Common Mode
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

3 Schematic

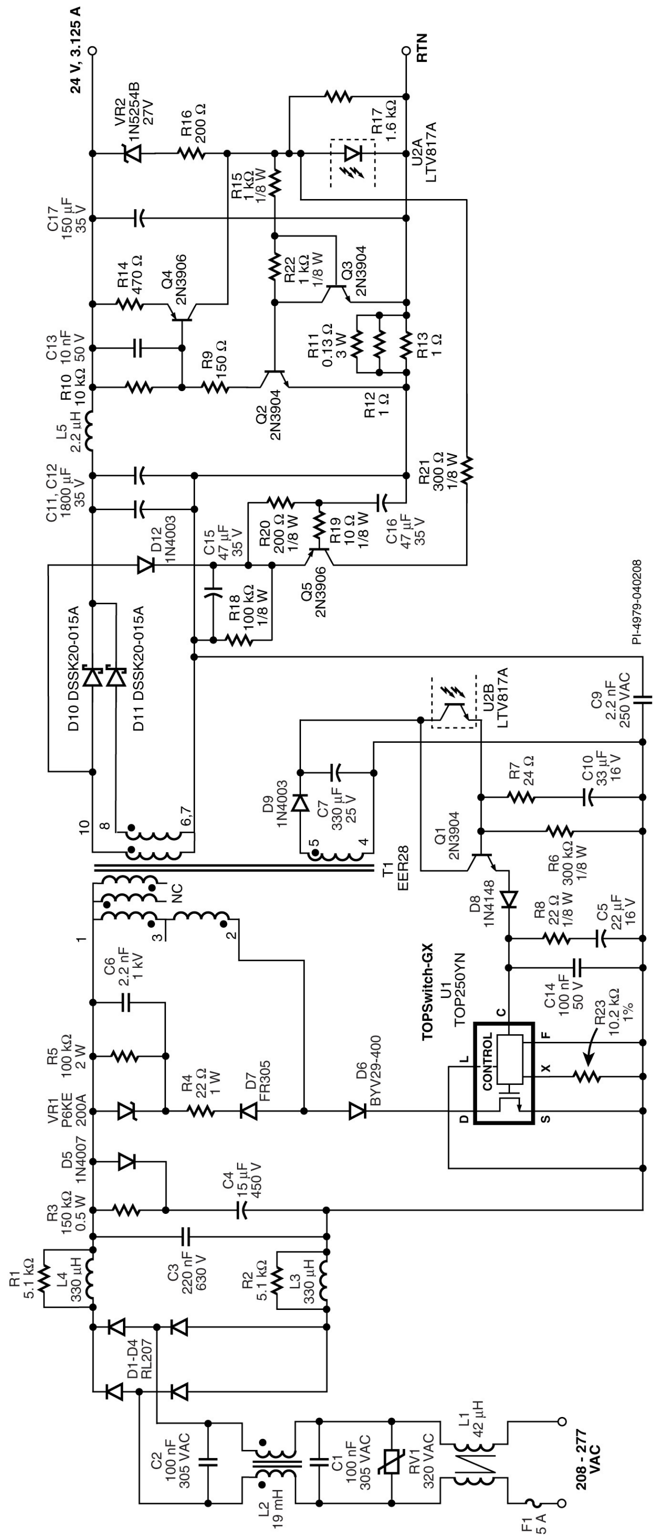


Figure 2 – Schematic.

4 PCB Layout

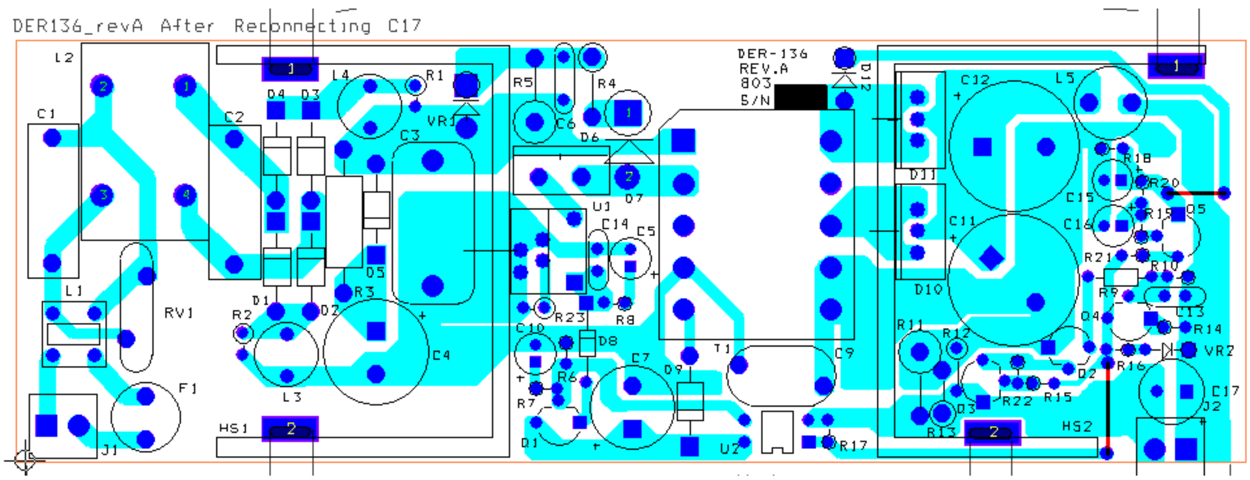


Figure 3 – PCB Layout.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

5 Circuit Description

This design uses a discontinuous mode flyback power supply configuration, fed with minimum capacitance at the input. Using a fixed duty-cycle over an AC line cycle allows the peak drain current envelope, and therefore the input current, to follow the input AC voltage waveform to give high power factor and low harmonic content. Although this simple configuration gives both output regulation and power factor correction in a single stage converter, it does require higher peak drain currents compared to a standard power supply with substantiation input capacitance.

Detailed descriptions of each functional block are given below.

5.1 Input EMI Filtering

In addition to the standard filtering (X capacitors C1 and C2 and common-mode inductor L2), L3 and L4 were added to provide increased differential-mode filtering and surge immunity. This was required due to the small value of input capacitance (C3) and the associated increase in switching currents seen by the AC input. Resistors R1 and R2 reduce high-frequency conducted and radiated EMI. Common-mode inductor L1 filters very high frequency common-mode noise.

Common-mode filtering is provided by L1, L2 and Y-capacitor C9. Together with transformer E-Shields (that reduce the source of common mode EMI currents), this allows the design to pass EN55015 B limits with greater than 10 dB of margin.

5.2 TOPSwitch Primary

On application of the AC input, the combination of the in-rush current to charge C1, C2 and C3, together with the parasitic inductance in the AC line, causes a voltage spike that appears across C3. In a design with a large input capacitance, this voltage rise is negligible; however, in this case the voltage spike on C3 is sufficiently large to exceed the BV_{DSS} rating of the MOSFET within TOP250YN (U1). To prevent this, capacitor C4 and diode D5 limit the maximum voltage across the DC bus while R3 is the bleeder to discharge capacitor C4 on AC removal.

The discontinuous mode of operation needed for high power factor increases the primary RMS current for a given output power. Selecting a larger TOPSwitch device (TOP250YN) than needed for power delivery offsets increases in RMS current (due to DCM operation) by reducing the R_{DSON} related conduction losses thereby giving higher efficiency and reduced dissipation.

As the DC input voltage across C3 falls to zero during normal operation, D6 was added in series with the drain to prevent the DRAIN ringing below SOURCE and reverse biasing the device. As reverse biasing of the device is not permitted, this diode must be used.

To provide a high power factor using a single-stage flyback converter, the MOSFET's duty cycle must be kept constant over a single AC line cycle (low bandwidth).

In the TOPSwitch-GX the operating duty cycle is a function of the control pin current. This requires that the current into the C pin be held constant to achieve power factor correction. The simplest way to achieve this would be to use a very large value for the CONTROL pin capacitance (C5). However, a large value of C5 causes a large startup time and a large startup overshoot.

To overcome this difficulty, an emitter follower (Q1) was used as an impedance transformer with a capacitor C10 in its base. Looking into the emitter of Q1, C10 appears to be larger (C10 x $Q1_{hfe}$), and R6 appears to be smaller (R6 / $Q1_{hfe}$). Capacitor C10, together with R6, sets the dominant pole of the circuit at approximately 0.02 Hz. Resistor R7 provides loop compensation, creating a zero at approximately 200 Hz, which gives additional phase starting at 20 Hz to improve phase margin at gain crossover. Gain crossover occurred in this design at approximately 35 – 40 Hz. Higher bandwidth is undesirable as this degrades power factor by increasing the third harmonic content in the input current waveform. Diode D8 prevents reverse current through Q1 during startup.

Feedback is provided from the secondary via optocoupler U2B, which in turn modulates the base voltage of Q1 and changes the current into the CONTROL pin.

The primary clamp circuit is formed by D7, R4, R5, C6, and VR1. During normal operation R5 and C6 set the clamping voltage. Zener VR1 sets a defined upper clamping voltage and conducts only during startup and load transients. A fast recovery (250 ns) blocking diode, D7, was used to recover some of the leakage energy, thereby improving efficiency. Resistor R4 dampens high frequency ringing and improves EMI performance.

5.3 Output Rectification

To reduce power dissipation and increase efficiency, two output diodes were used (D10 and D11). These are connected to separate secondary windings to improve current sharing between the two diodes. Filtering is provided by C11 and C12. Relatively large values are necessary to reduce line frequency ripple present in the output due to the low loop bandwidth required to achieve a high power factor. These values may be reduced depending on the acceptable current ripple through the LED load.

5.4 Output Feedback

The output feedback is split into two functional blocks: constant-voltage (CV) operation and constant-current (CC) operation.

5.4.1 Constant-Voltage Operation

Voltage feedback is provided by VR2 and optocoupler U2A. Once the output exceeds the voltage defined by the forward drop of U2A, VR2 and R16, current flows through the optocoupler and provides feedback to the primary. As the line and load change, the

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

magnitude of current changes to reduce or increase the MOSFET duty cycle which maintains output regulation. Resistor R16 sets the loop gain in the constant-voltage region.

The nominal output voltage regulation is set at 28 V, which is above the expected LED load voltage (when operated at its rated current). Under normal operation, the supply operates in constant-current mode, and voltage feedback is used only when the output is unloaded.

5.4.2 Constant-Current Operation

Transistor Q3 and the forward drop of the LED in U2A are used to create a bias voltage on the base on Q2. The additional drop across R11, R12, and R13 needed to turn on Q2 is equal to the difference between the bias voltage and the V_{BE} of Q2 (~0.5 V). Once Q2 begins to conduct, Q4 also conducts, supplying current through U2A and providing feedback. Resistor R9 limits the base current from Q4, and R14 sets the gain of the CC loop. Resistor R10 keeps Q4 off until Q2 is on, while C13 provides loop compensation. This arrangement gave an average output current in CC operation of 3.1 A.

5.5 Soft-Start

The very low loop bandwidth presents a problem at startup. Once the loop closes and feedback is provided via U2A, it takes significant time for the loop to respond and therefore allows significant output overshoot. This is because C10 must charge above 5.8 V before current is supplied into the CONTROL pin of U1.

The standard solution to output overshoot is to provide a soft-finish circuit. Typically this consists of a capacitor that allows current to flow in the feedback loop before the output has reached regulation. Here such a passive approach is not practical because of the capacitor size required.

To overcome this, the circuit formed around transistor Q5 is used to overdrive the feedback loop during startup. Using an element with gain (Q5) allows enough feedback current to pre-charge C10 before the output reaches regulation.

A separate auxiliary supply is created by D12 and C15 so that the voltage across C15 rises faster than the main output across C11 and C12. While C16 charges, Q5 is on, supplying current to charge C10 via the optocoupler, with resistor R21 limiting the maximum current. Once the voltage across C16 reaches V_O-$V_{BE\ (Q5)}$, Q5 turns off and the circuit becomes inactive. At power down, C16 is discharged via R18, resetting the circuit for the next power-up. The time constant of C16 and R18 appears very long; however, in practice, C10 also takes a significant time to discharge on power down, and even momentary AC drop outs do not result in any output overshoot.

5.6 Post Filter

A post filter consisting of L5 and C17 was added to reduce switching frequency ripple on the output. This also improves noise immunity and improves the reliability of the CC set-point.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

6 Bill of Materials

Item	Qty	Part Ref.	Description	Mfg Part Number	Mfg
1	2	C1 C2	100 nF, 305 VAC, X2	B32922A2104M	Epcos
2	1	C3	220 nF, 630 V, Film	ECQ-E6224KF	Panasonic
3	1	C4	15 µF, 450 V, Electrolytic, (12.5 x 25)	EKXG451ELL150MK25S	Nippon Chemi-Con
4	1	C5	22 µF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	ECA-1CM220	Panasonic
5	1	C6	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC Components Corp
6	1	C7	330 µF, 25 V, Electrolytic, Very Low ESR, 53 m, (10 x 12.5)	EKZE250ELL331MJC5S	Nippon Chemi-Con
7	1	C9	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
8	1	C10	33 µF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	ECA-1CM330	Panasonic
9	2	C11 C12	1800 uF, 35 V, Electrolytic, Very Low ESR, 16 mΩ, (16 x 25)	EKZE350ELL182ML25S	Nippon Chemi-Con
10	1	C13	10 nF, 50 V, Ceramic, Z5U	B37982N5103M000	Epcos
11	1	C14	100 nF, 50 V, Ceramic, Z5U	SR205E104MAR	AVX Corp
12	2	C15 C16	47 µF, 35 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG350ELL470ME11D	Nippon Chemi-Con
13	1	C17	150 µF, 35 V, Electrolytic, Very Low ESR, 72 Ω, (8 x 11.5)	EKZE350ELL151MHB5D	Nippon Chemi-Con
14	4	D1 D2 D3 D4	1000 V, 2 A, Rectifier, DO-15	RL207	Rectron
15	1	D5	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
16	1	D6	400 V, 9 A, Ultrafast Recovery, 60 ns, TO-220AC	BYV29-400	NXP Semiconductors
17	1	D7	600 V, 3 A, Fast Recovery Diode, DO-201AD	FR305-T	Diodes Inc.
18	1	D8	75 V, 300 mA, Fast Switching, DO-35	1N4148	Vishay
19	2	D9 D12	200 V, 1 A, Rectifier, DO-41	1N4003RLG	OnSemi
20	2	D10 D11	150 V, 20 A, Schottky, TO-220AB	DSSK 20-015A	IXYS
21	1	F1	5 A, 250V, Slow, TR5	3721500041	Wickman
22	2	HS1 HS2	HEATSINK, Alum, TO-220 2 hole, 2 mtg pins		Custom
23	2	J1 J2	2 Position (1 x 2) header, 0.156 pitch, Vertical	26-48-1021	Molex
24	1	L1	42 uH, Common Mode Inductor, 4 Pins, Toroid	5943000201	Fair-Rite Toroid
25	1	L2	19 mH, 0.5 A, Common Mode Choke	ELF15N005A	Panasonic
26	2	L3 L4	330 uH, 0.55 A, 9 x 11.5 mm	SBC3-331-551	Tokin
27	1	L5	2.2 uH, 6.0 A	RFB0807-2R2L	Coilcraft
28	3	Q1 Q2 Q3	NPN, Small Signal BJT, 40 V, 0.2 A, TO-92	2N3904RLRAG	On Semiconductor
29	2	Q4 Q5	PNP, Small Signal BJT, 40 V, 0.2 A, TO-92	2N3906	Fairchild

30	2	R1 R2	5.1 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-5K1	Yageo
31	1	R3	150 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-150K	Yageo
32	1	R4	22 Ω, 5%, 1 W, Metal Oxide	RSF100JB-22R	Yageo
33	1	R5	100 kΩ, 5%, 2 W, Metal Oxide	RSF200JB-100K	Yageo
34	1	R6	300 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-300K	Yageo
35	1	R7	24 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-24R	Yageo
36	1	R8	22 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-22R	Yageo
37	1	R9	150 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-150R	Yageo
38	1	R10	10 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-10K	Yageo
39	1	R11	0.13 Ω, 1%, 3 W	ALSR-3F-.13-1%	Huntington Electric
40	2	R12 R13	1 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-1R0	Yageo
41	1	R14	470 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-470R	Yageo
42	2	R15 R22	1 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-1K0	Yageo
43	2	R16 R20	200 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-200R	Yageo
44	1	R17	1.6 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-1K6	Yageo
45	1	R18	100 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-100K	Yageo
46	1	R19	10 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-10R	Yageo
47	1	R21	300 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-300R	Yageo
48	1	R23	10.2 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-10K2	Yageo
49	1	RV1	320 V, 48 J, 10 mm, RADIAL	V320LA10	Littlefuse
50	1	T1	Bobbin, EER28, Vertical, 10 pins	BEER-28-111-CP	TDK
51	1	U1	TOPSwitch-GX, TOP250YN, TO220-7C	TOP250YN	Power Integrations
52	1	U2	Opto coupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
53	1	VR1	200 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE200ARLG	OnSemi
54	1	VR2	27 V, 5%, 500 mW, DO-35	1N5254B	Microsemi

All parts are RoHS compliant.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

7 Transformer Specification

7.1 Electrical Diagram

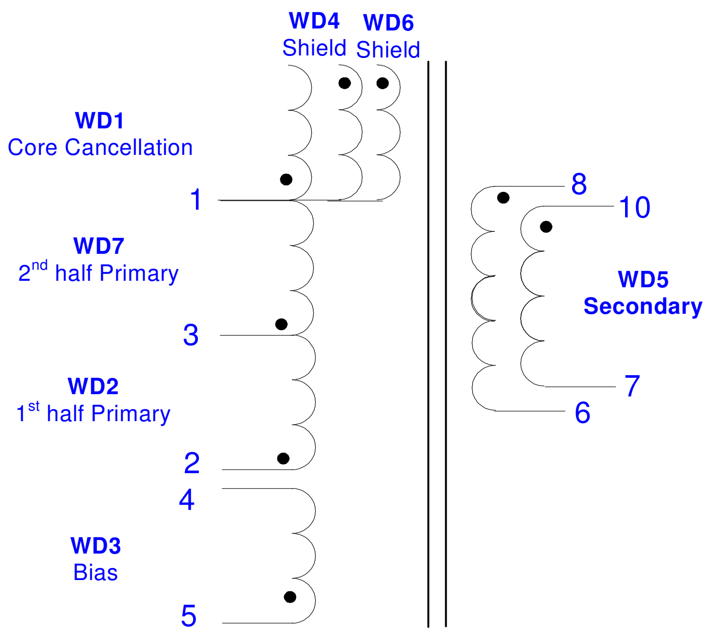


Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 second, 60 Hz, from Pins 1-5 to Pins 6-10.	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz.	171 µH, -0/+10%
Resonant Frequency	Pins 1-2, all other windings open.	1290 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with Pins 6-7-8-9-10 shorted, measured at 100 kHz.	3 µH (Max.)

7.3 Materials

Item	Description
[1]	Core: EER28 PC40 or equivalent gapped for 248 nH/T^2
[2]	Bobbin: Vertical EER28 10 pins, safety rated
[3]	Magnet Wire: 26AWG
[4]	Magnet Wire: 25AWG
[5]	Magnet Wire: 28AWG
[6]	Copper foil: 14 mm wide
[7]	Triple Insulated Wire: 28AWG
[8]	Tape: 14.7 mm
[9]	Tape: 16.7mm
[10]	Varnish
[11]	2 mm Polyester web tape

7.4 Transformer Build Diagram

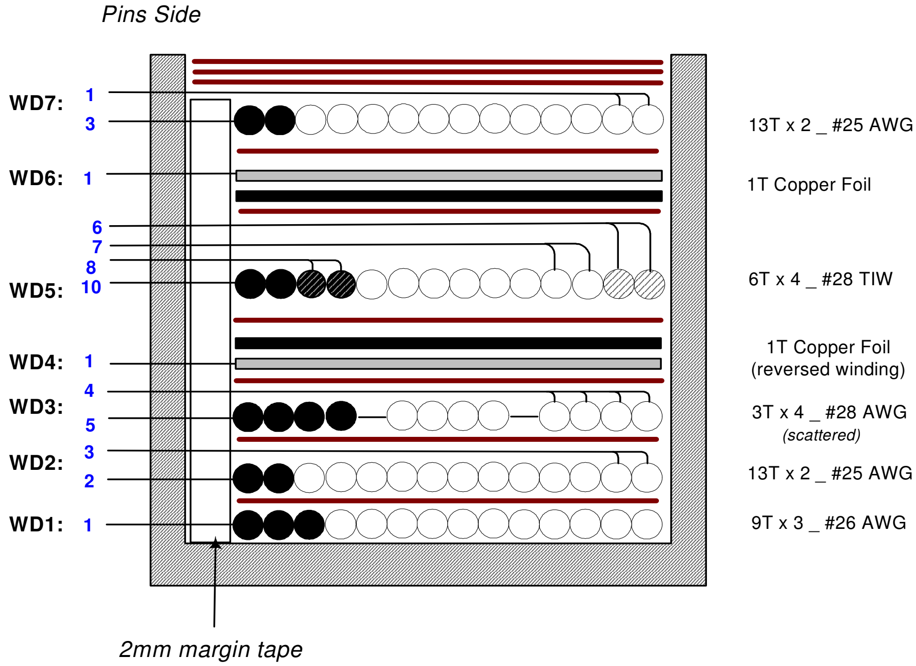


Figure 5 – Transformer Build Diagram.

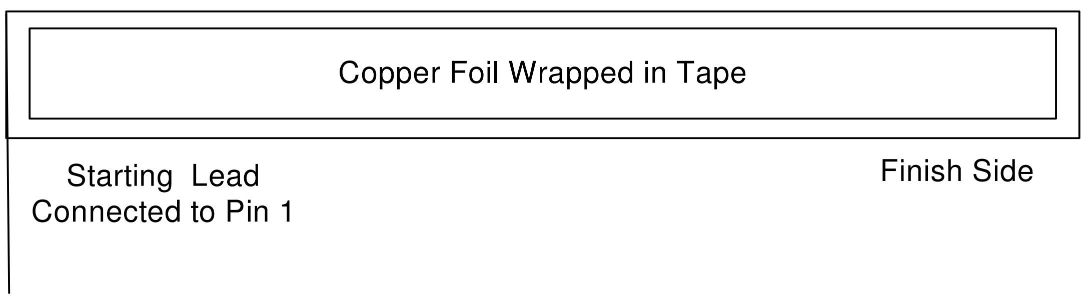


Figure 6 – Copper Tape Preparation for Winding 4.

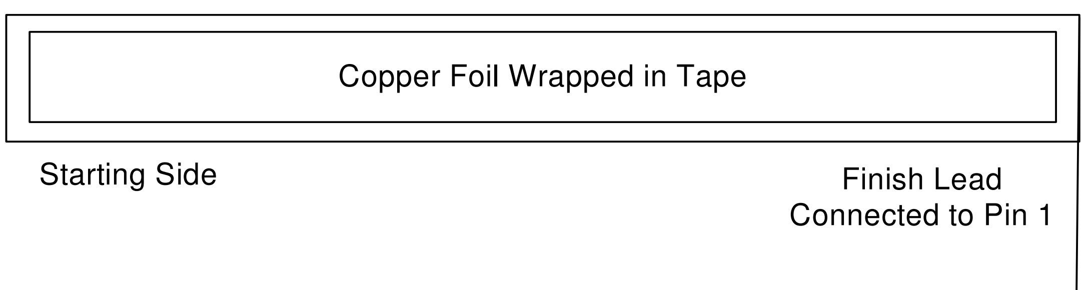


Figure 7 – Copper Tape Preparation for Winding 6.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

7.5 Transformer Construction

Bobbin Preparation	Place bobbin, item [2], on the winding machine with pins side oriented to the left hand side. Use 2 mm Polyester web tape [11] on left hand side to meet safety creepage distances.
WD1 Core Cancellation	Start at pin 1, wind from left to right 9 trifilar turns of item [3] in a uniform, tightly wound layer. Cut finish lead at the end of the winding.
Tape	Use 1 layer of tape, item [8], to hold the winding.
WD2 First Half Primary	Start at pin 2, wind from left to right 13 bifilar turns of item [4] in a uniform, tightly wound layer. Finish at pin 3.
Tape	Use 1 layer of tape, item [8], to hold the winding.
WD3 Bias	Start at pin 5, wind 3 quad-filar turns of item [5] from left to right in a single scattered layer. Finish at pin 4.
Tape	Use 1 layer of tape, item [8], to hold the winding.
WD4 Shield	Prepare copper tape, item [6], as shown in figure 6. Connect starting lead to pin 1. Wind 1 turn in ***reverse winding direction***. The finish lead is left unconnected.
Tape	Use 1 layer of tape, item [8], to hold the winding.
WD5 Secondary	Start at pins 10 and 8, Wind from left to right 6 turns of 4 wires in parallel, item [7], in a uniform layer. Finish on pins 7 and 6.
Tape	Use 1 layer of tape, item [8], to hold the winding.
WD6 Shield	Prepare copper tape, item [6], as shown in figure 7. Starting lead is left unconnected. Wind 1 turn and connect finish lead to pin 1.
Tape	Use 1 layer of tape, item [8], to hold the winding.
WD7 Second Half Primary	Start at pin 3, wind from left to right 13 bifilar turns of item [4] in a uniform, tightly wound layer. Finish at pin 1.
Tape	Use 3 layers item, [9] as insulation.
Final Assembly	Assemble and secure core halves with bobbin. Varnish impregnate item [10].

8 Transformer Spreadsheets

The standard flyback transformer design approach was modified due to the minimal input capacitance for high power-factor (PF). A very high capacitance value was entered for C_{IN} so the design uses the transformer at the peak of the AC line voltage (at low line). The output power entered was increased from the 75 W specified to 119 W. This was to compensate for the under-delivery of output power when the AC input voltage waveform is low.

ACDC_TOPSwitchGX_043007; Rev.2.15; Copyright Power Integrations 2007	INPUT	INFO	OUTPUT	UNIT	TOP_GX_FX_043007: TOPSwitch-GX/FX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					LED DRIVER XFR
VACMIN	208			Volts	Minimum AC Input Voltage
VACMAX	277			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	26.00			Volts	Output Voltage (main)
PO	119.00			Watts	Output Power
n	0.78				Efficiency Estimate
Z	0.50				Loss Allocation Factor
VB	12			Volts	Bias Voltage
tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	99999.00			uFarads	Input Filter Capacitor

ENTER TOPSWITCH-GX VARIABLES					
TOP-GX	TOP250			*Universal*	*115 Doubled/230V*
Chosen Device		*TOP250*	*Power Out*	*210W*	*290W*
KI	0.70				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN			*3.969*	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX			*4.851*	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	F				Full (F) frequency option – 132kHz
fS			*132000*	Hertz	TOPSwitch-GX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			*124000*	Hertz	TOPSwitch-GX Minimum Switching Frequency
fSmax			*140000*	Hertz	TOPSwitch-GX Maximum Switching Frequency
VOR	116.00			Volts	Reflected Output Voltage
VDS	10.00			Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	1.00				Ripple to Peak Current Ratio (0.4 < KRP < 1.0 : 1.0< KDP<6.0)

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EER28				
Core		*EER28*		*P/N:*	PC40EER28-Z
Bobbin		*EER28_BOBBIN*		*P/N:*	BEER-28-1112CPH
AE			0.821	cm^2	Core Effective Cross Sectional Area

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

LE		6.4	cm	Core Effective Path Length
AL		2870	nH/T^2	Ungapped Core Effective Inductance
BW		16.7	mm	Bobbin Physical Winding Width
M	1.50		mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00			Number of Primary Layers
NS	6			Number of Secondary Turns

DC INPUT VOLTAGE PARAMETERS				
VMIN		294	Volts	Minimum DC Input Voltage
VMAX		392	Volts	Maximum DC Input Voltage

CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.29		Maximum Duty Cycle
IAVG		0.52	Amps	Average Primary Current
IP		3.58	Amps	Peak Primary Current
IR		3.58	Amps	Primary Ripple Current
IRMS		1.11	Amps	Primary RMS Current

TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP		171	uHenries	Primary Inductance
NP		26		Primary Winding Number of Turns
NB		3		Bias Winding Number of Turns
ALG		248	nH/T^2	Gapped Core Effective Inductance
BM		2838	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP		3848	Gauss	Peak Flux Density (BP<4200)
BAC		1419	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1780		Relative Permeability of Ungapped Core
LG		0.38	mm	Gap Length (Lg > 0.1 mm)
BWE		27.4	mm	Effective Bobbin Width
OD		1.04	mm	Maximum Primary Wire Diameter including insulation
INS		0.08	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.96	mm	Bare conductor diameter
AWG		19	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		1290	Cmils	Bare conductor effective area in circular mils
CMA		1160	Cmils/Amp	!!! DECREASE CMA (200 < CMA < 500) Decrease L(primary layers),increase NS,smaller Core

TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)				
Lumped parameters				
ISP		15.66	Amps	Peak Secondary Current
ISRMS		7.62	Amps	Secondary RMS Current
IO		4.58	Amps	Power Supply Output Current
IRIPPLE		6.09	Amps	Output Capacitor RMS Ripple Current
CMS		1524	Cmils	Secondary Bare Conductor minimum circular mils

AWGS	18	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS	1.03	mm	Secondary Minimum Bare Conductor Diameter
ODS	2.28	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS	0.63	mm	Maximum Secondary Insulation Wall Thickness

VOLTAGE STRESS PARAMETERS			
VDRAIN	655	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS	115	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB	55	Volts	Bias Rectifier Maximum Peak Inverse Voltage

9 Specifications For Common Mode Inductor L1

9.1 Electrical Diagram

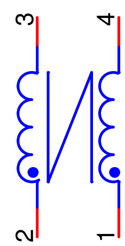


Figure 8 – L1 Electrical Diagram.

9.2 Inductance

Inductance	42 uH

9.3 Material

Item	Description
1	Fair-Rite Toroid 5943000201
2	Magnetic wire 26AWG
3	Triple Insulated wire 26AWG

9.4 Winding Instructions

Wind 12 parallel turns using item [2] and item [3]. Wind tightly and uniformly as shown in figure 9.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

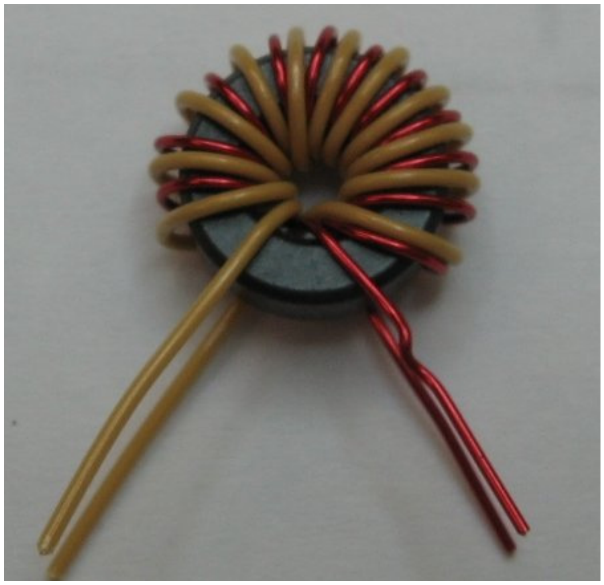


Figure 9 – Picture of L1.

10 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

10.1 Efficiency

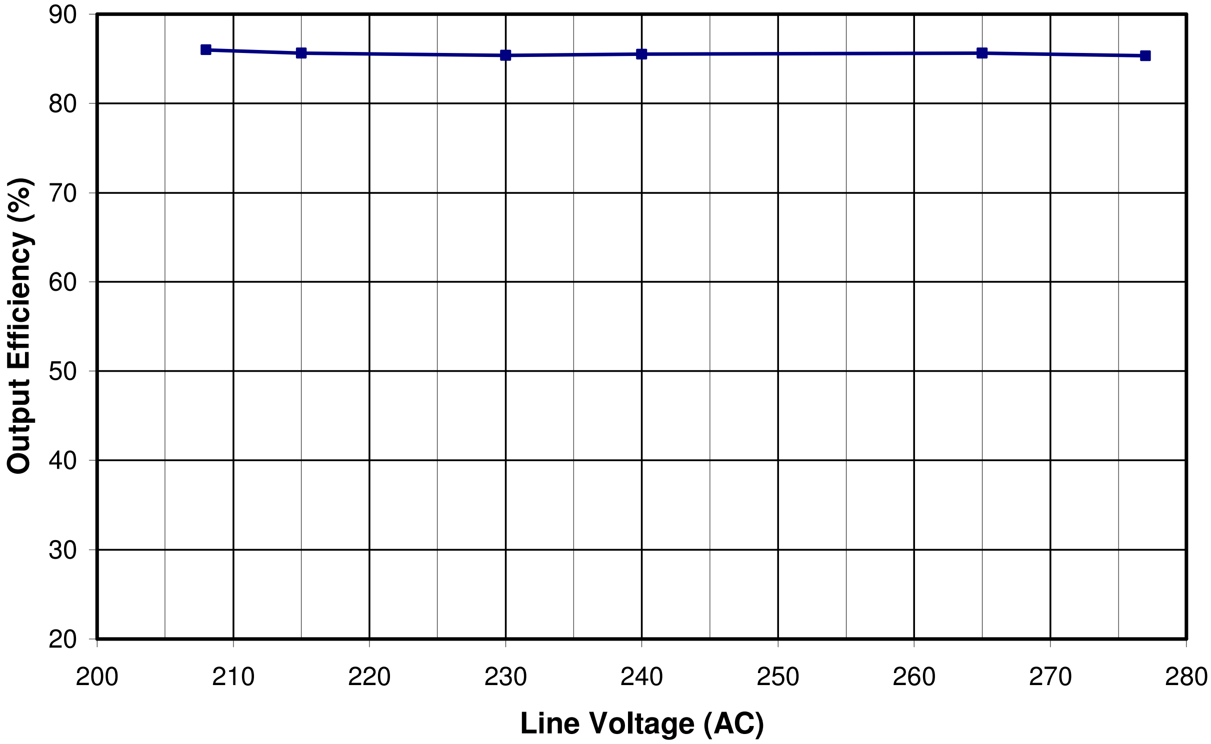


Figure 10 – Efficiency vs Input Voltage. Full Load, Room Temperature, 60 Hz.

INPUT VOLTAGE (AC)	OUTPUT EFFICIENCY (%)
208	86.01
215	85.64
230	85.39
240	85.51
265	85.62
277	85.32

Table 1: Measurements of Efficiency vs Line Voltage at Full Load.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

10.2 Output Characteristic

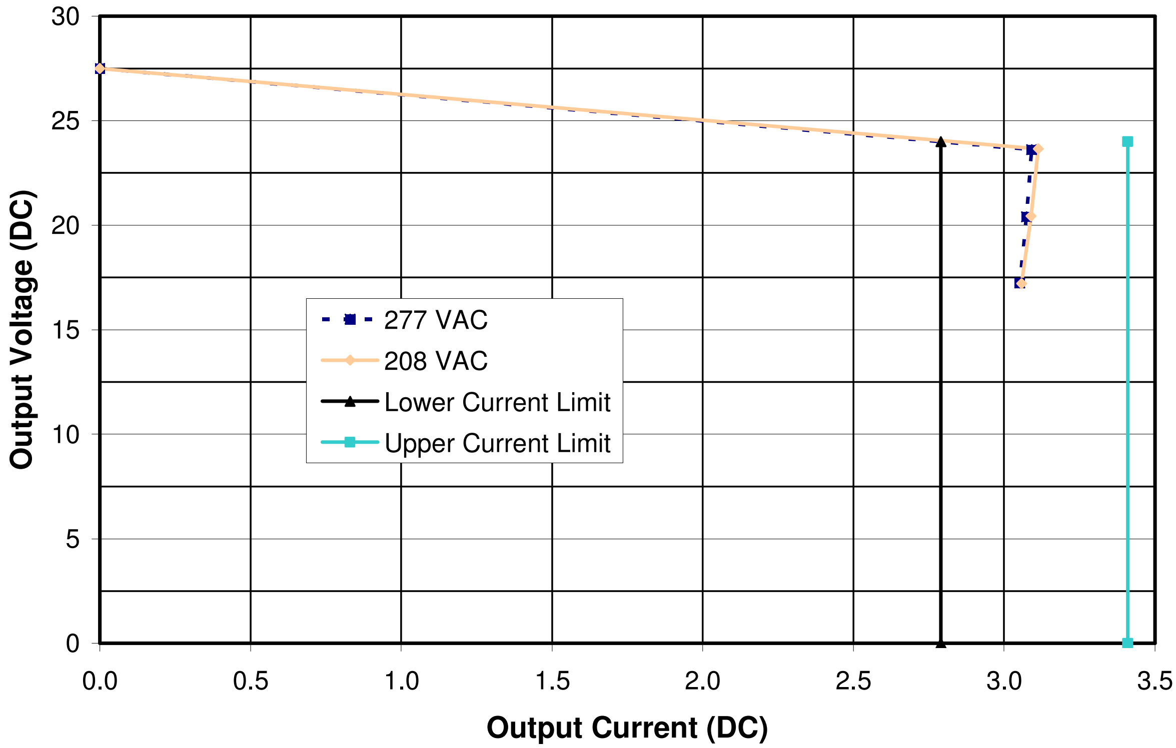


Figure 11 – Output Characteristic Showing Line and Load Regulation, Room Temperature.

10.3 Harmonic Content

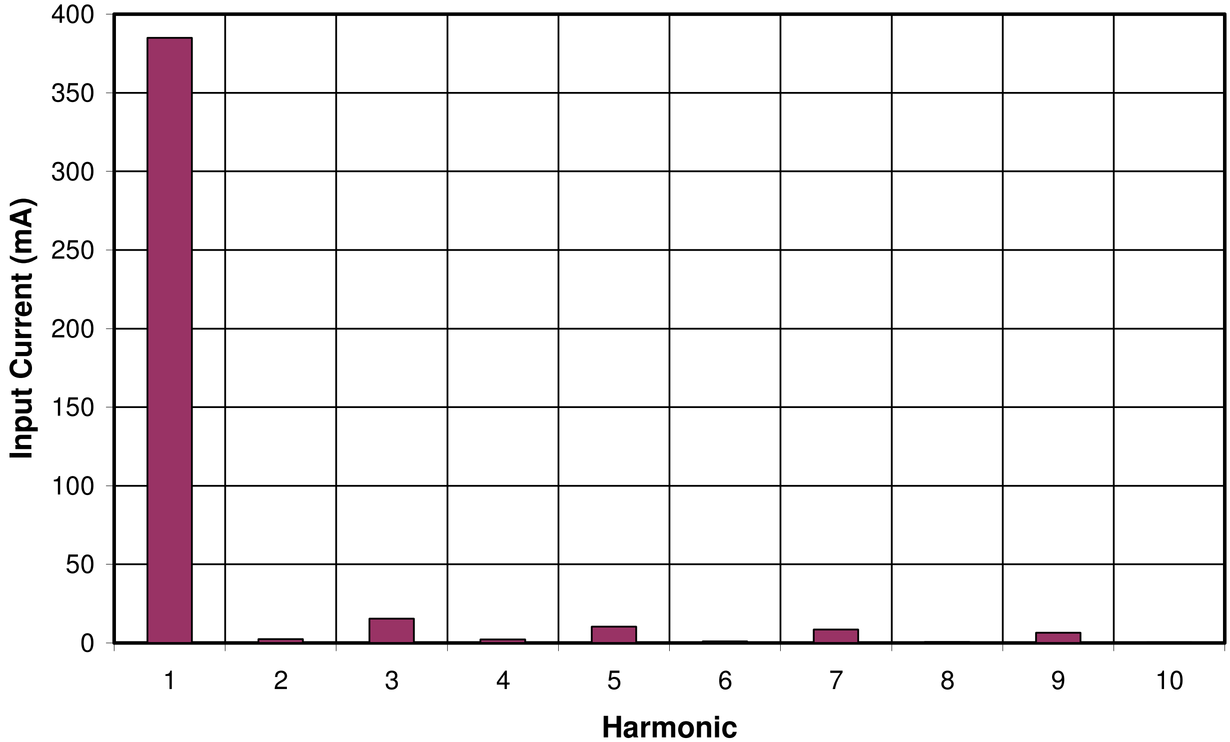


Figure 12 – Input Current Harmonic Content. Full Load, V_{IN} = 230 VAC.

10.4 Harmonic Content in Percentage of Fundamental

Harmonic	Iin(mA) At 230VAC	% of Fundamental	Maximum % Allowed By IEC 61000-3-2. Class C
1	385		
2	2.4	0.62	2.0
3	15.6	4.05	29.7
4	2.3	0.60	
5	10.5	2.73	10.0
6	1	0.26	
7	8.6	2.23	7.0
8	0.5	0.13	
9	6.5	1.69	5.0
10	0.4	0.10	

Table 2: Harmonic Content in Percentage of Fundamental and IEC 61000-3-2 Limits for C Class Equipment.

NOTE: Third Harmonic Spec Follows the Formula: 30* PFC. (Power Factor at 230 VAC).

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

10.5 Power Factor Vs Line Voltage at Full Load

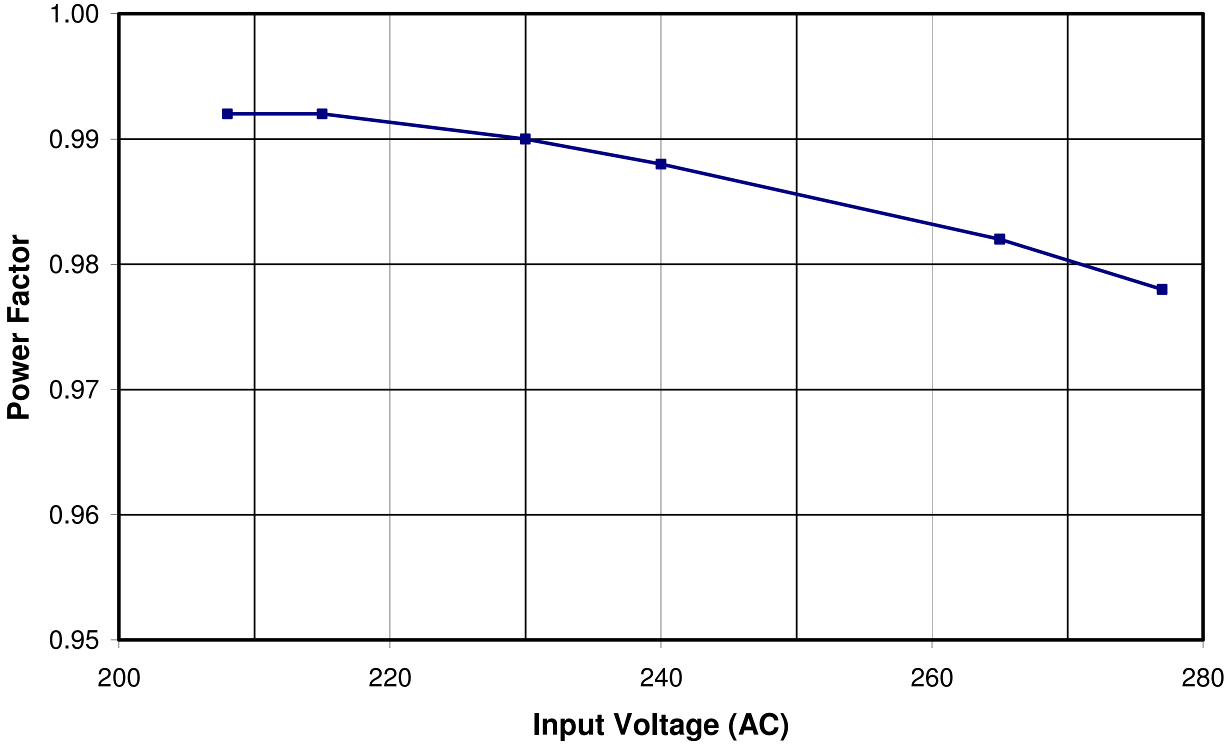


Figure 13 – Power Factor (PF) vs Input Line Voltage (VAC).

INPUT VOLTAGE (AC)	POWER FACTOR
208	0.992
215	0.992
230	0.990
240	0.988
265	0.982
277	0.978

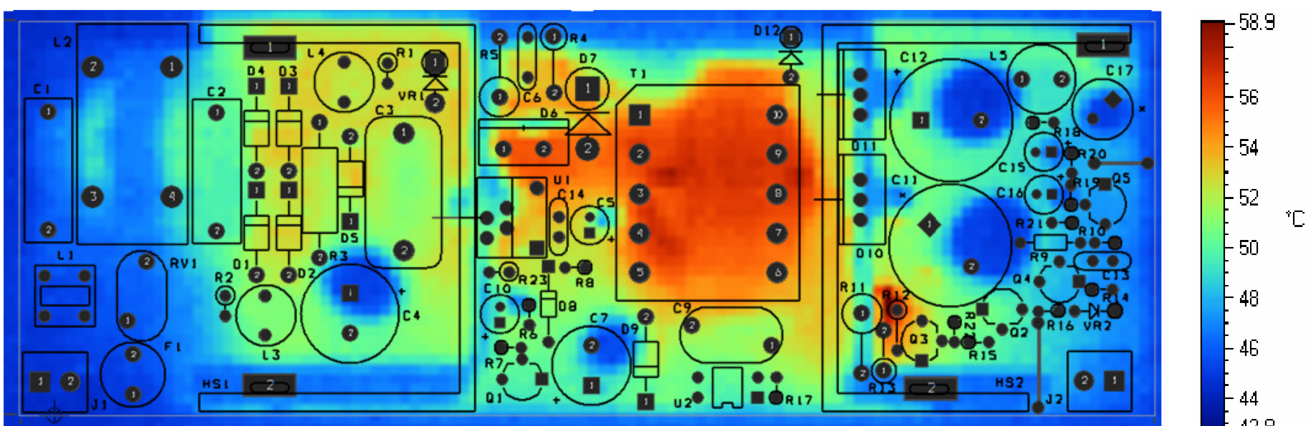
Table 3: Power Factor Measurements at Full Load.

11 Thermal Performance

Two sets of data were taken on the UUT. One set was taken with the unit inside a closed cardboard box at room temperature. The second set of data was taken with the UUT in a metal box encapsulated with thermal-conductive Epoxy. Results are shown below.

Item	**Temperature (°C)**			
	UUT Open Frame		**UUT Encapsulated with thermal epoxy in a metal case.**	
	208 VAC	277 VAC	208 VAC	277 VAC
Ambient	25	25	25	25
TOPSwitch (U1)	77	78	63	59
Transformer (T1)	77	79	66	63
Output Rectifiers (D10, D11)	70	69	62	57

Table 4: Temperatures of Critical Components in the Power Supply.



208 VAC, 75 W load, 25 ºC Ambient

Figure 14 – Infrared Thermograph of Open Frame Operation at Room Temperature.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

12 Waveforms

All waveforms are shown with LEDs used as load.

12.1 Drain Voltage and Current, Normal Operation

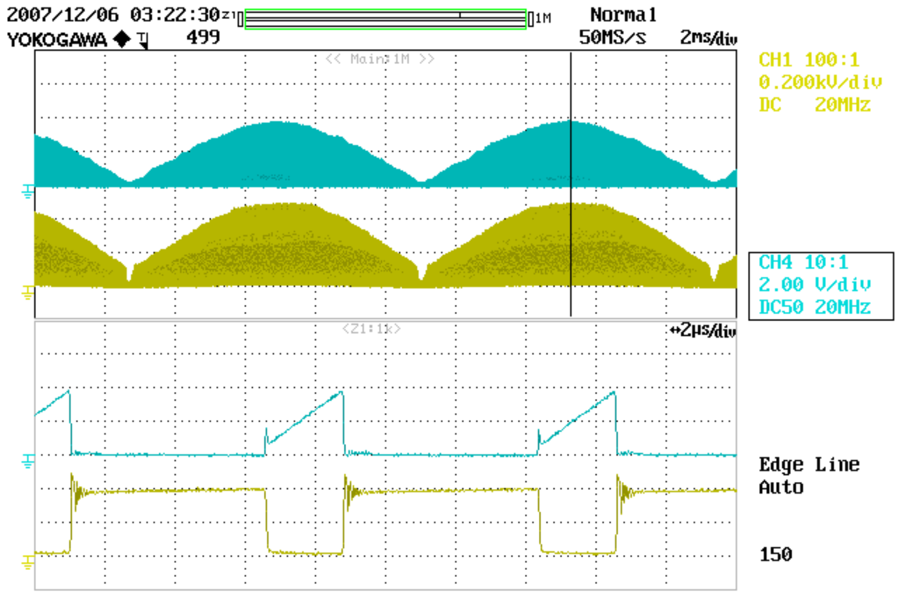


Figure 15 – 208 VAC, Full Load.
Upper: ID 2.0 A / Div.
Lower: VDRAIN 200 V / Div.

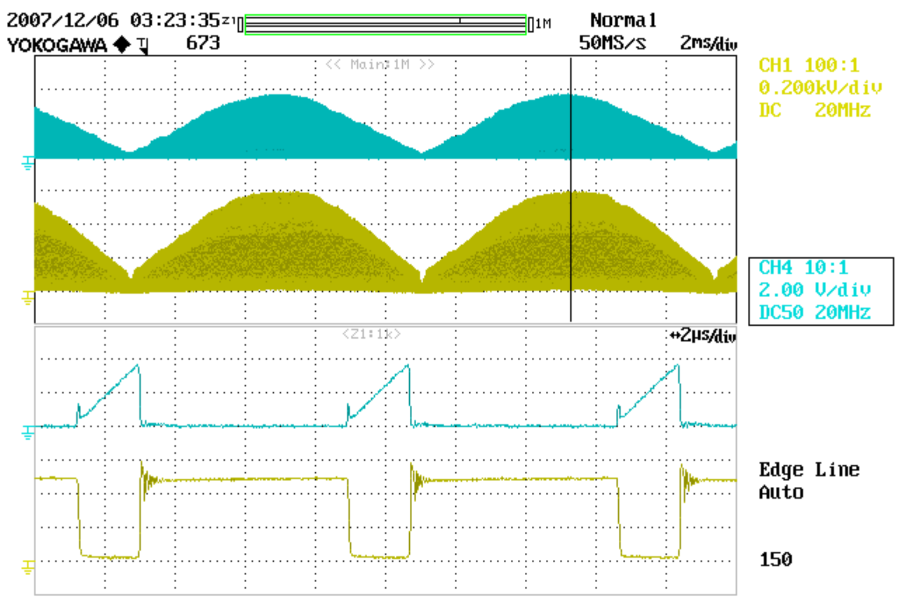


Figure 16 – 277 VAC, Full Load.
Upper: ID 2.0 A / Div.
Lower: VDRAIN 200 V / Div.

12.2 Output Voltage Start-up Profile

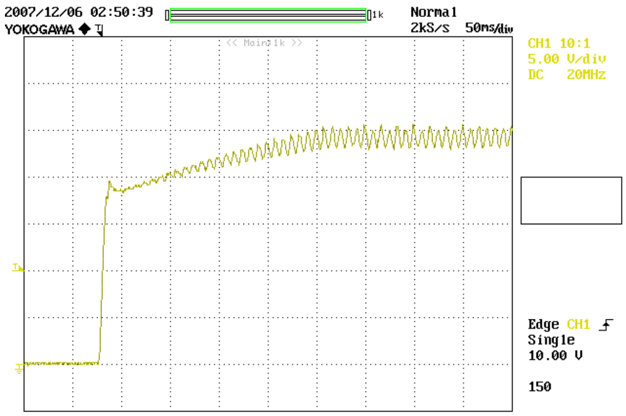


Figure 17 – Start-up Profile, 208 VAC.
5 V, 50 ms / div.

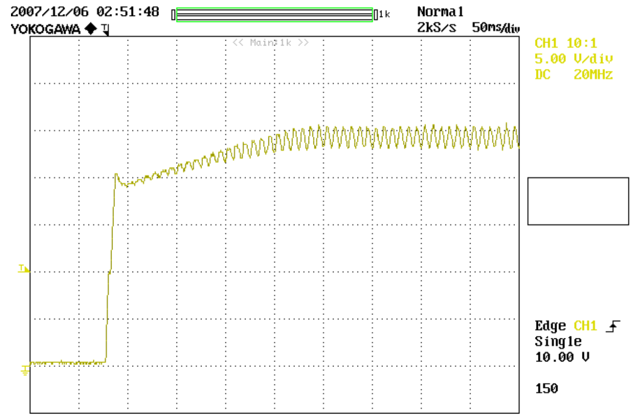


Figure 18 – Start-up Profile, 277 VAC.
5 V, 50 ms / div.

12.3 Drain Voltage and Current Start-up Profile

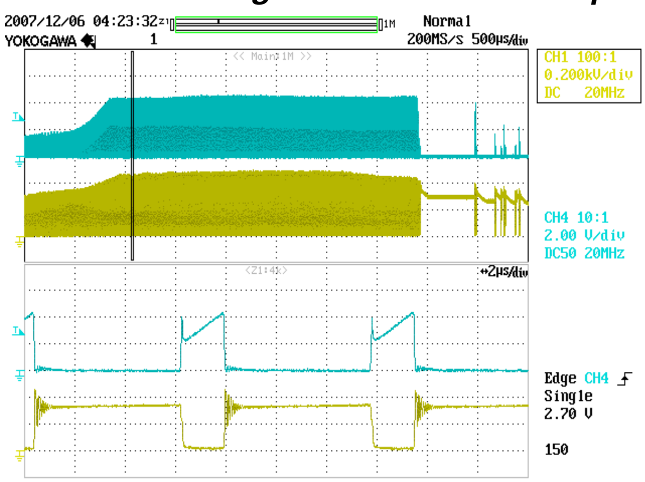


Figure 19 – 208 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 2.0 A / div.
Lower: V_{DRAIN}, 200 V / div.

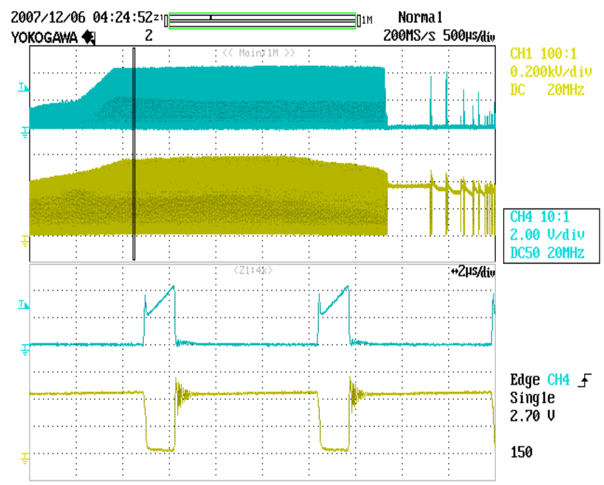


Figure 20 – 277 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 2.0 A / div.
Lower: V_{DRAIN}, 200 V / div.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

12.4 Output Ripple Measurements

12.4.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of a 4987BA probe adapter. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs (see Figure 21 and Figure 22).

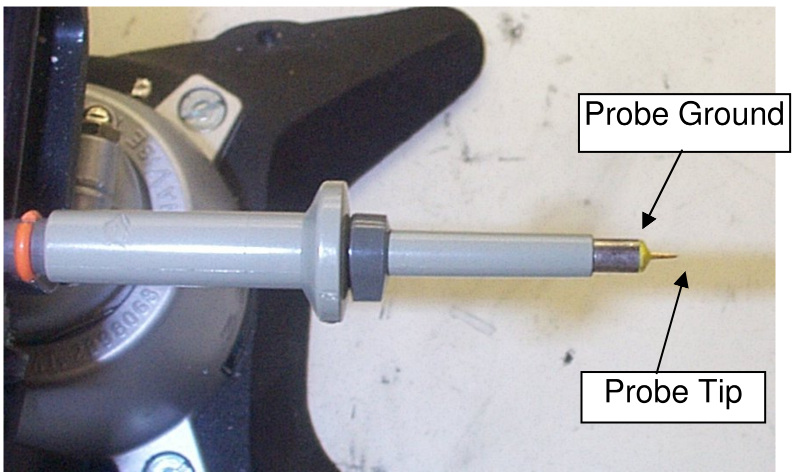


Figure 21 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed).

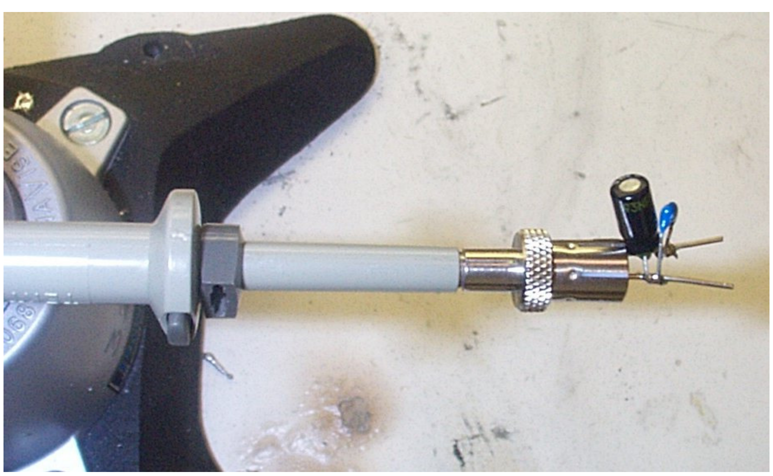


Figure 22 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added).

12.4.2 Measurement Results

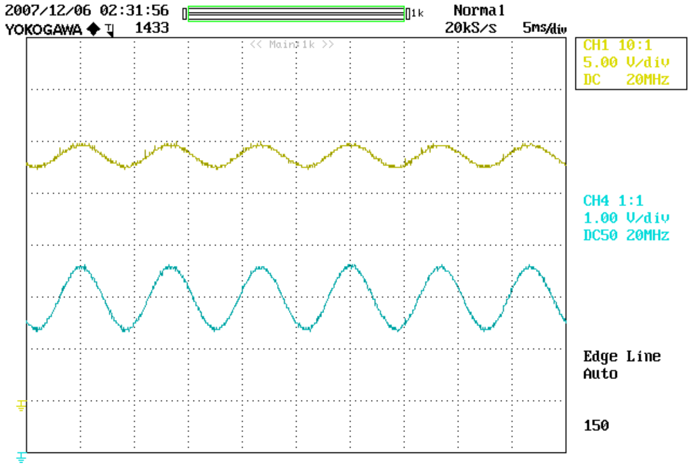


Figure 23 – Output Ripple 208 VAC, Full Load.
Upper: V_{OUT}, 5 V / div.
Lower: I_{OUT}, 1 A/ div V, 5 ms / div.

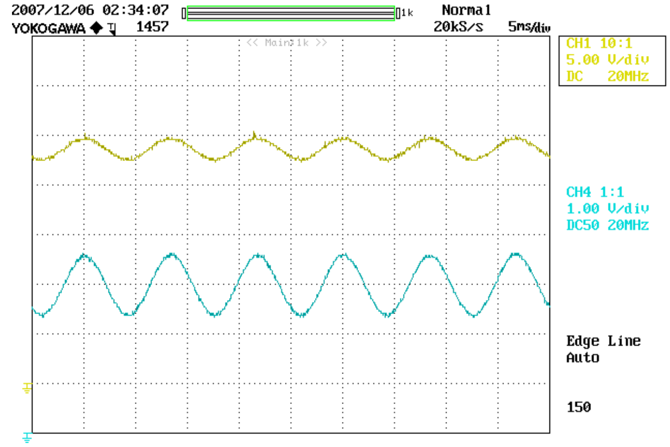


Figure 24 – Output Ripple 230 VAC, Full Load.
Upper: V_{OUT}, 5 V / div.
Lower: I_{OUT}, 1 A/ div V, 5 ms / div.

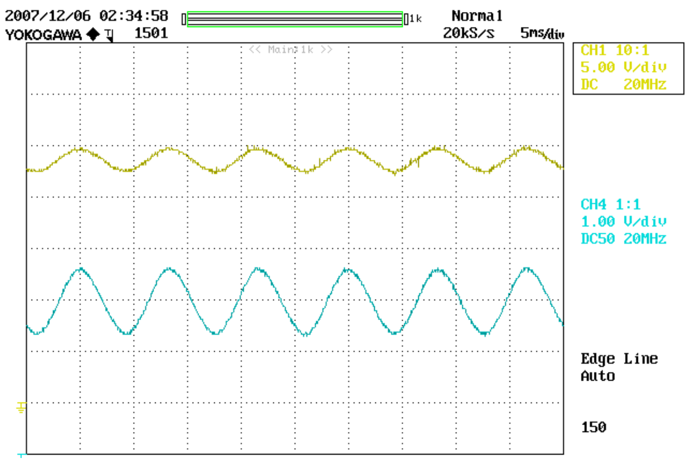


Figure 25 – Output Ripple 277 VAC, Full Load.
Upper: V_{OUT}, 5 V / div.
Lower: I_{OUT}, 1 A/ div V, 5 ms / div.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

13 Control Loop Analysis

Following are the loop plots measured at 208 VAC and 277 VAC. Since it is a single stage PFC power supply, the loop bandwidth is necessarily low and in this case crossover occurs at approximately 35 – 40 Hz.

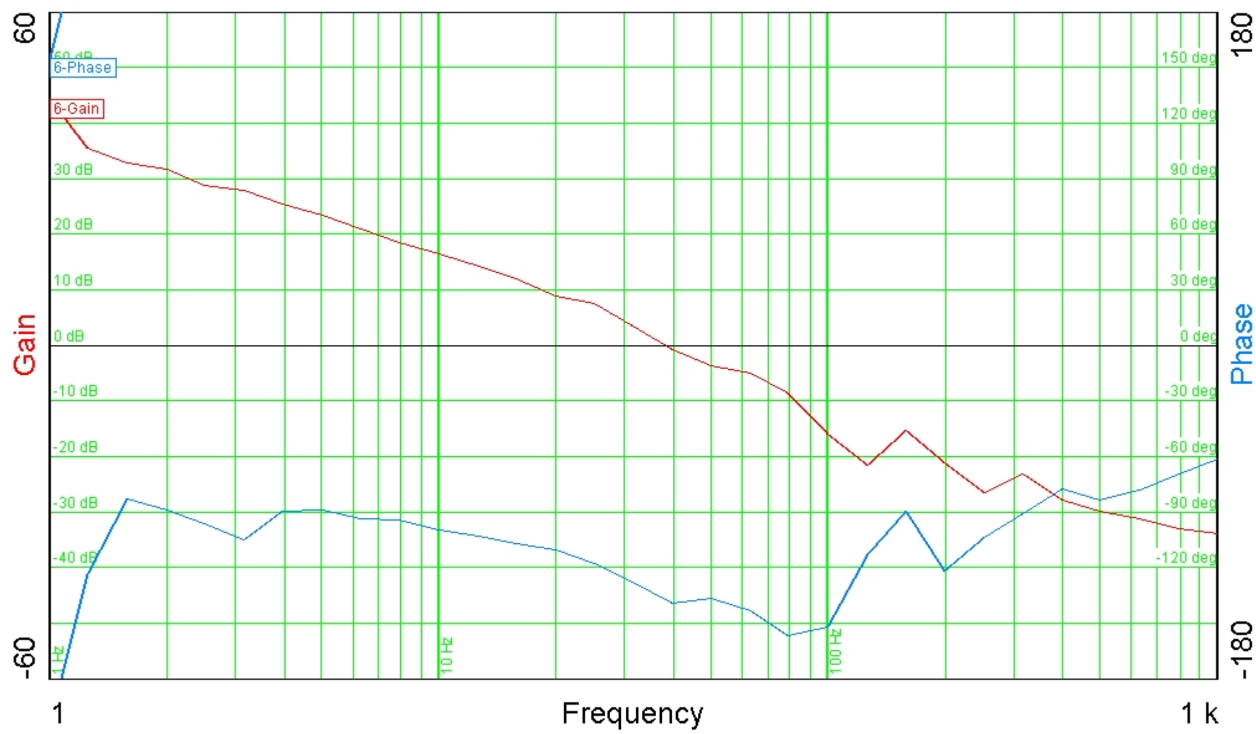


Figure 26 – Bode Plot Measured at 208 VAC and Full Load. Crossover Occurs at Approximately 38 Hz With a Phase Margin of Approximately 50 Degrees.

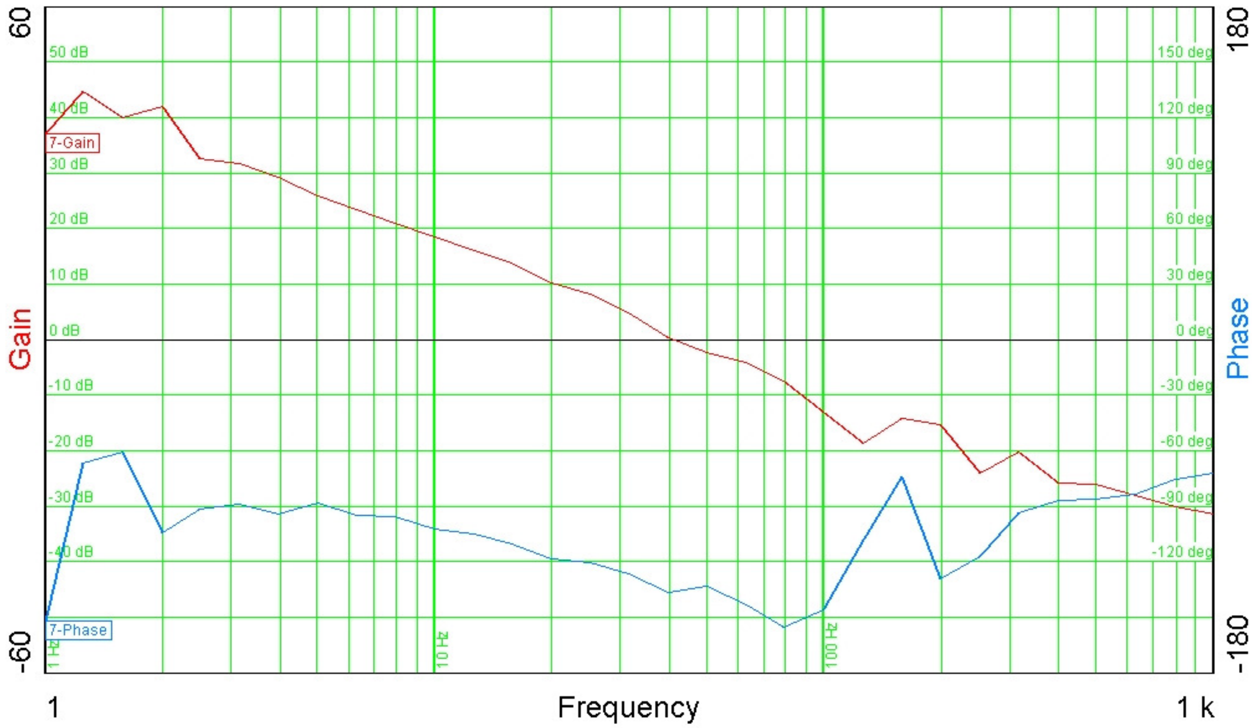


Figure 27 – Bode Plot Measured at 277 VAC and Full Load. Crossover Occurs at Approximately 40 Hz With a Phase Margin of Approximately 45 Degrees.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

14 Surge Test

14.1 Surge Test Results with 1.2/50 µs Waveform

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Number Of Surges	Test Result (Pass/Fail)
+500	230	L to N	90	10	Pass
-500	230	L to N	90	10	Pass
+1000	230	L and N to G	90	10	Pass
-1000	230	L and N to G	90	10	Pass

14.2 Surge Test Results with 0.5 µs-100 kHz Ring-Waveform

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Number Of Surges	Test Result (Pass/Fail)
+2500	230	L to N	90	10	Pass
-2500	230	L to N	90	10	Pass
+2500	230	L and N to G	90	10	Pass
-2500	230	L and N to G	90	10	Pass

15 Conducted EMI

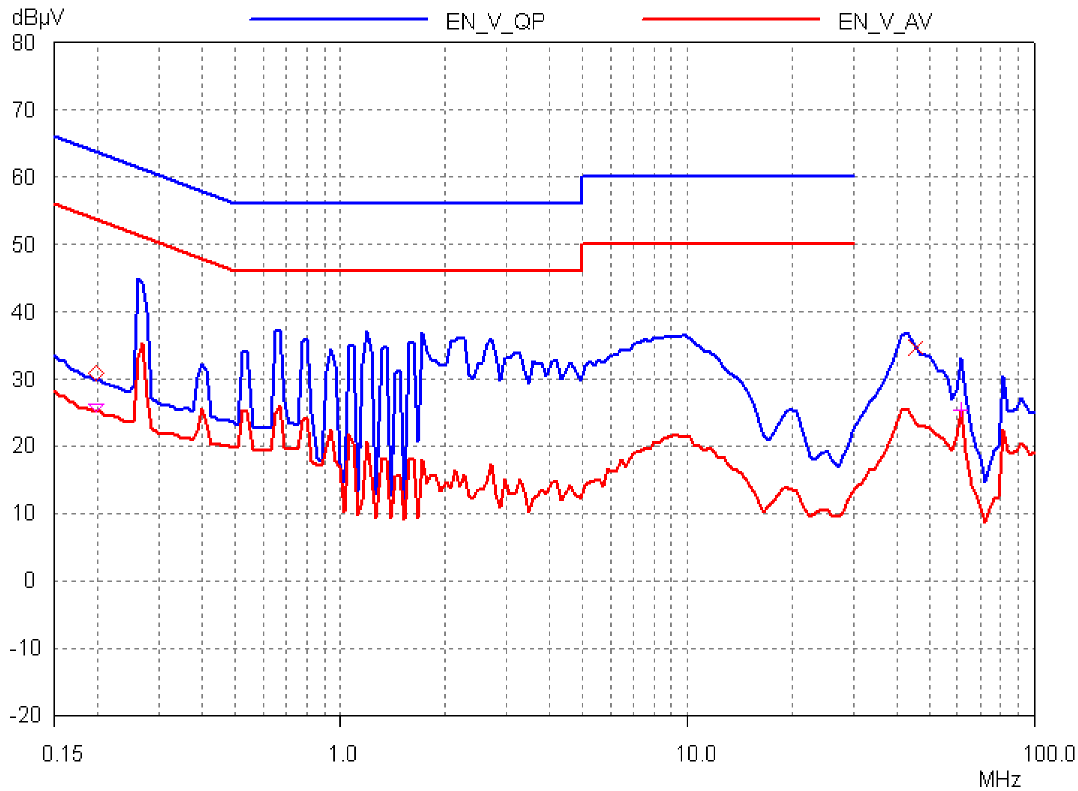


Figure 28 – Conducted EMI, 230 VAC Full Load, UUT Placed on a Grounded Metal Plate.

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

16 Revision History

Date	Author	Revision	Description & changes	Reviewed
01-Apr-08	KM	1.6	Added redrawn schematic	

Notes

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

For the latest updates, visit our website: *www.powerint.com*

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Rueckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3911
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

JAPAN
Kosei Dai-3 Bldg.,
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 807-808A,
Pacheer Commercial Centre,
555 Nanjing Rd. West
Shanghai, P.R.C. 200041
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail: chinasales@powerint.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-41138020
Fax: +91-80-41138023
e-mail: indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

UNITED KINGDOM
1st Floor, St. James's House
East Street, Farnham
Surrey, GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)
Room A, B & C 4th Floor, Block C
Elec. Sci. Tech. Bldg.
2070 Shennan Zhong Rd.
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

ITALY
Via De Amicis 2
20091 Bresso MI – Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#15-08/10 Goldhill Plaza,
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760