Voltage level shifting

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Abstract A brief description of voltage shifting circuits.

1   Introduction

In applications requiring a unipolar AC voltage signal, the signal may be delivered from a bi-polar voltage amplifier/generator and repositioned relative to a zero volt reference (an earth ground) using a voltage level shifting circuit. In addition, the voltage level shifting technique is frequently used to generate high voltage DC outputs from lower voltage AC sources. The maximum voltage (AC or DC) produced at the output of a single stage of the level shifting circuit is nominally equal to the peak-to-peak value of the AC signal delivered by the amplifier/generator.

2   AC voltage shifting

An example of an AC voltage shifting circuit diagram (Villard circuit) is shown in Figure 1. Figure 2 shows the input and the output voltage of the circuit. In order to move the voltage signal toward negative values, it is necessary to reverse the diode shown on the schematic in Figure 1. Additionally, if the capacitors C1 and C2 are polar, they also need to be reversed.
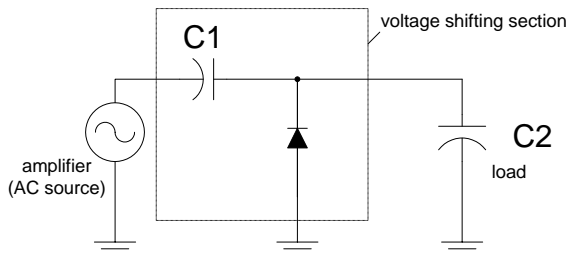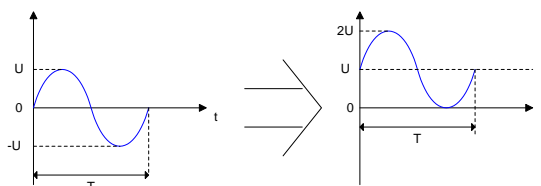

Figure 1: Villard voltage level shifting circuit.

Figure 2: Shifted signal.

The steady state current drawn from the AC source (amplifier, for example) follows the dependency:

$$I = \frac{C1 \cdot C2}{C1 + C2} \cdot \frac{dU}{dt} \qquad (1)$$

For a sinusoidal AC voltage input

$$U = U \cdot \sin(2\pi ft) \qquad (2)$$

the current is:

$$I = \frac{C1 \cdot C2}{C1 + C2} \cdot 2\pi fU \cos(2\pi ft) \qquad (3)$$

The output voltage U_{out} across the capacitor C2 is:

$$U_{out} = U \cdot \frac{C1}{C1 + C2} \qquad (4)$$

3   Example

Consider the following example:
U=1000 · sin (2πft) V;
f=100 Hz;
C1=C2=63 nF.
The maximum current is 20 mA (eq. 3) and the voltage across the C2 is 1000 V (eq. 4). These results are shown in Figure 3.

When the capacitor C1 becomes smaller (C1=31.5 nF), the output voltage value drops (Figure 4) according to equation 4. Current I also decreases, as the total capacitance of the circuit decreased.
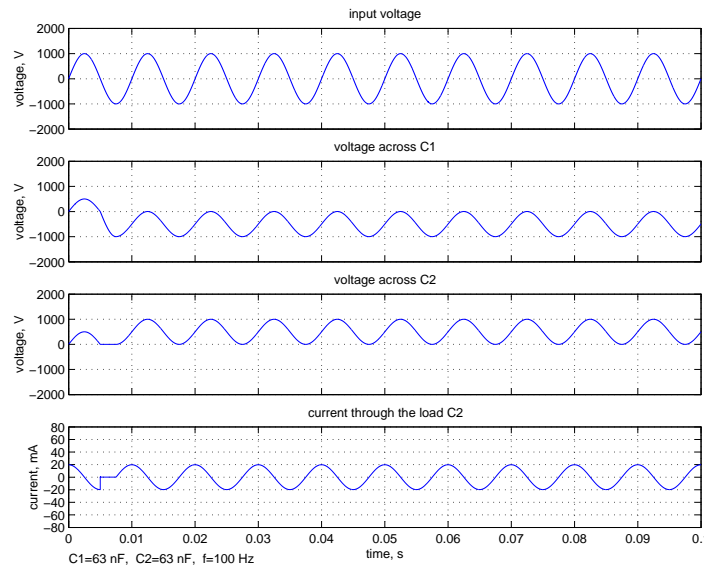
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Figure 3: Simulation results for the circuit shown in Figure 1, where f=100 Hz, C1=C2=63 nF.

When considering a choice of capacitors for the voltage shifting circuit, two factors have to be taken into account: total capacitance of C1 and C2 connected in series($\frac{C1 \cdot C2}{C1+C2}$), and the ratio of a capacitive divider formed by both capacitors ($\frac{C1}{C1+C2}$). It is important to pay attention on the voltage rating of the capacitors.

The frequency of the input voltage signal also influences choice of capacitors. For example, if the frequency is changed from 100 Hz to 1 kHz, the current drawn from the source multiplies by the factor of 10 (Figure 5). Capacitor values have to be lowered by the factor of 10 to get back to the 20 mA current level.

The output voltage U_{out} from the capacitive divider is maximized for C1>>C2. For example, let C1=12,000 nF and C2=1 nF. Results of a simulation with these C1 and C2 values are shown in Figure 6.

4   DC voltage generation

By combining several stages of the basic circuit from Figure 1, a DC high voltage signal can be obtained. Figure 7 presents a two stage DC voltage multiplier generating positive output DC voltage. A similar, two stages negative DC voltage circuit is shown in Figure 8.
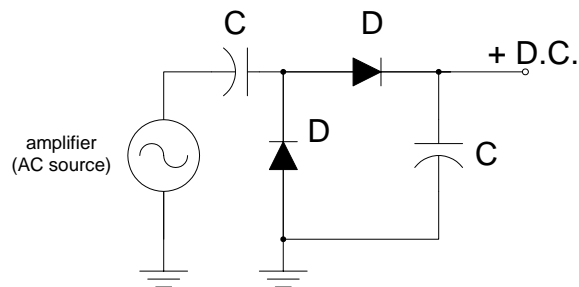

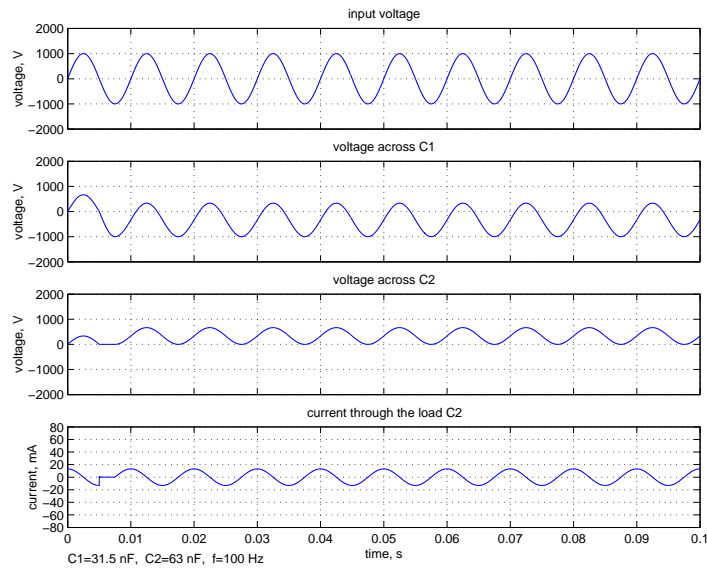Figure 7: Positive voltage multiplier.

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Figure 4: Simulation results for the circuit shown in Figure 1, where f=100 Hz, C1=31.5 nF, C2=63 nF.
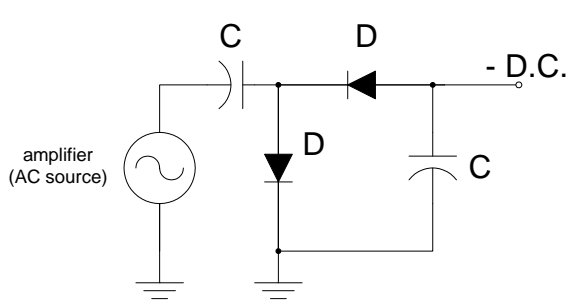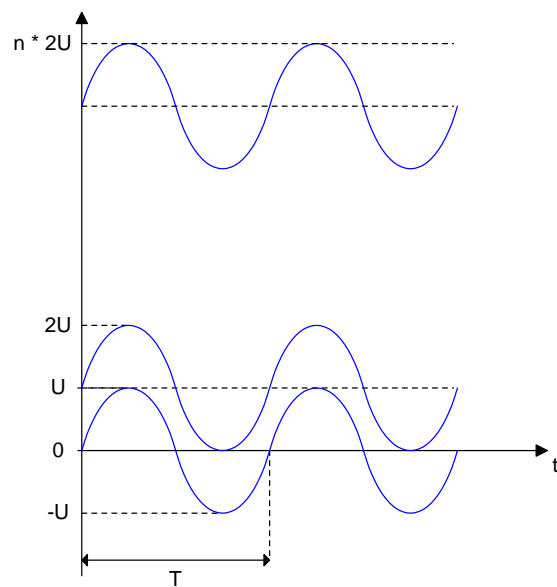

Figure 8: Negative voltage multiplier.

Figure 9: DC multiplier signal.

The number of stages that can be used in this kind of design is limited by current capabilities of
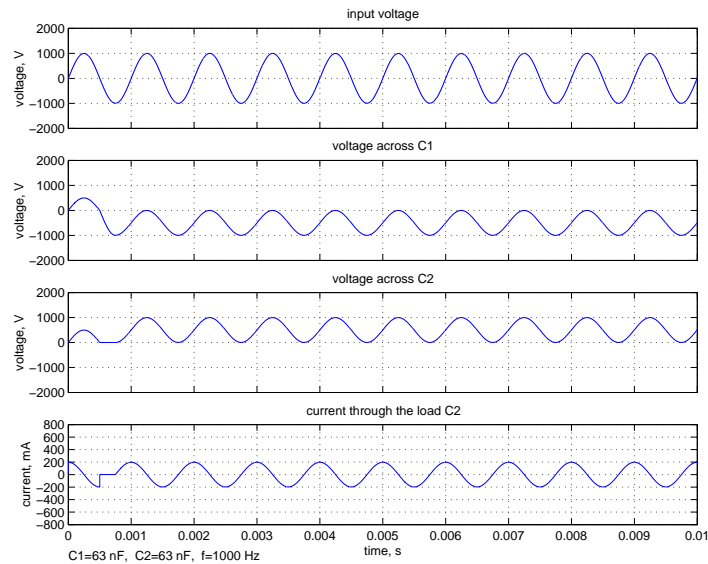

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Figure 5: Simulation results for the circuit shown in Figure 1, where f=1000 Hz, C1=C2=63 nF.

the circuit. The DC output voltage has an AC voltage ripple δU (Figure 10) given by equation [1]:

$$\delta U = \frac{I}{fC} \cdot \frac{n \cdot (n+1)}{4},\qquad(5)$$

where I is the load current and n is the number of stages. A voltage drop ΔU (Figure 10) due to the load can be calculated using formula [1]:

$$\Delta U = \frac{I}{fC} \left(\frac{2n^3}{3} - \frac{n}{6} \right)\qquad(6)$$
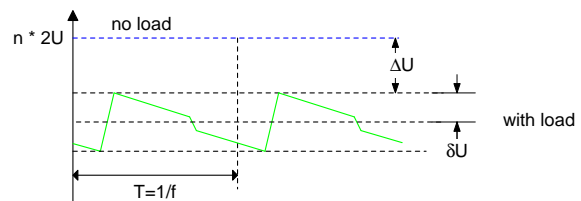

Figure 10: Voltage ripple and voltage drop.

References

[1] E. Kuffel, W. S. Zaengl, and J. Kuffel. *High Voltage Engineering: Fundamentals*. Newnes, 2 edition, 2000.
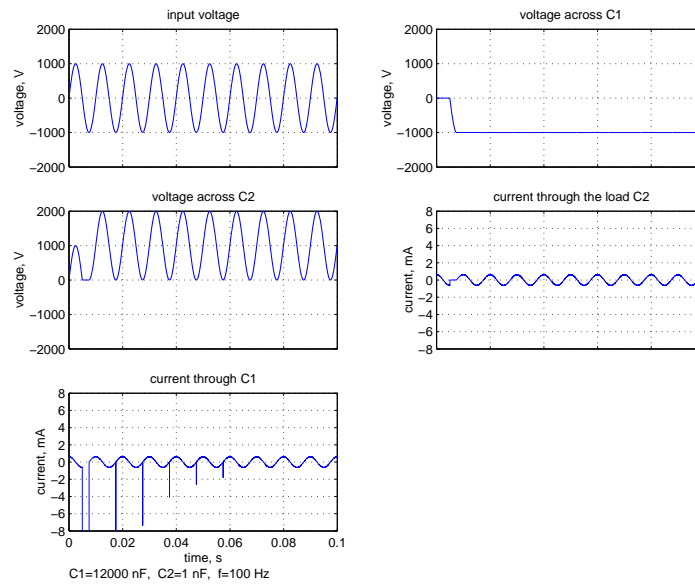
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Figure 6: Simulation results for f=1000 Hz, C1=12000 nF, C2=1 nF.