Application Note – iW3620 Design considerations to select PFC inductor

This application note provides the design considerations for selecting PFC inductor in the LED driver design with iW3620.

Figure 1 shows a universal AC input line LED driver design with power factor correction.

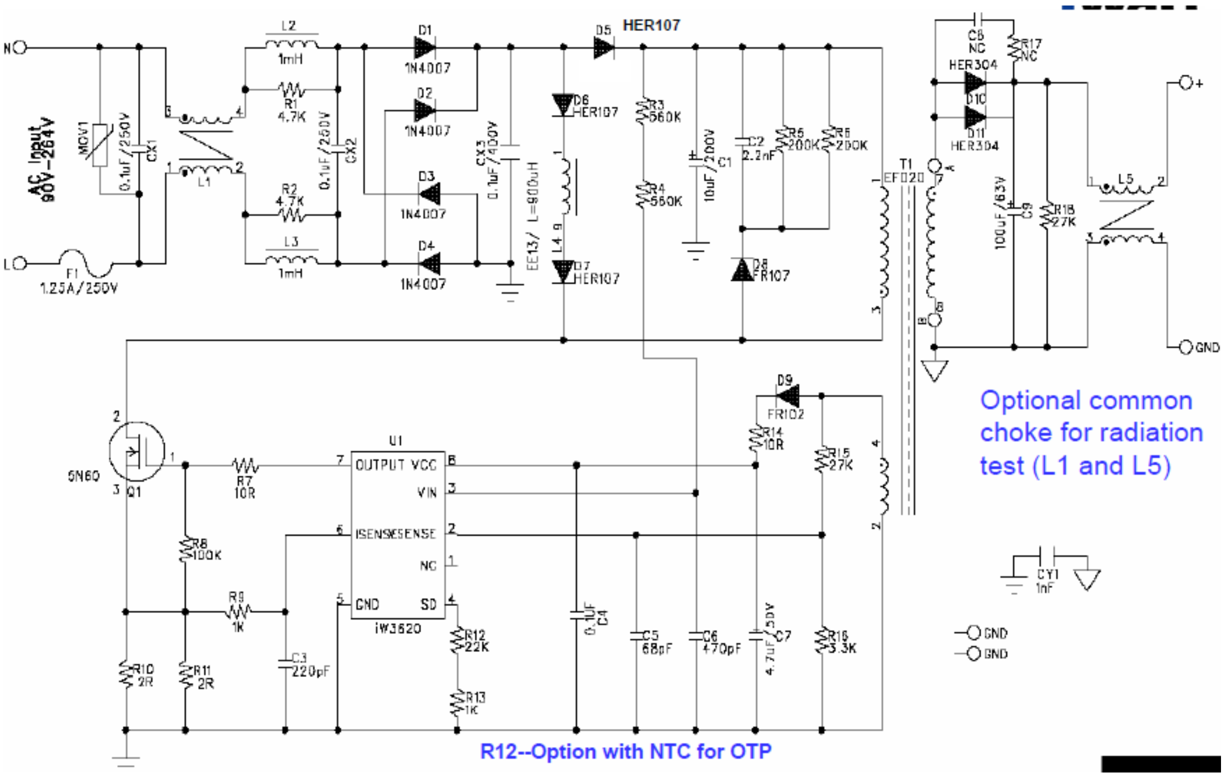

Figure 1 An iW3620 design – 28V/0.5A for universal AC input

1 Considerations for selecting PFC inductor

The PFC inductor is selected based on the following considerations.

1. Support the output loading. The PFC inductor stores energy when MOSFET turns on and releases partial energy to the output loading when MOSFET turns off.
2. Boost the bulk capacitor voltage level Vbulk. Vbulk has to be limited at the highest input voltage.
3. Meet the power factor requirement. The lower the inductance, the higher the power factor.

4. Meet the efficiency requirement. Higher PFC inductance often leads to higher efficiency because less power is processed through the boost circuit..

Figure 2 shows a simplified schematic.

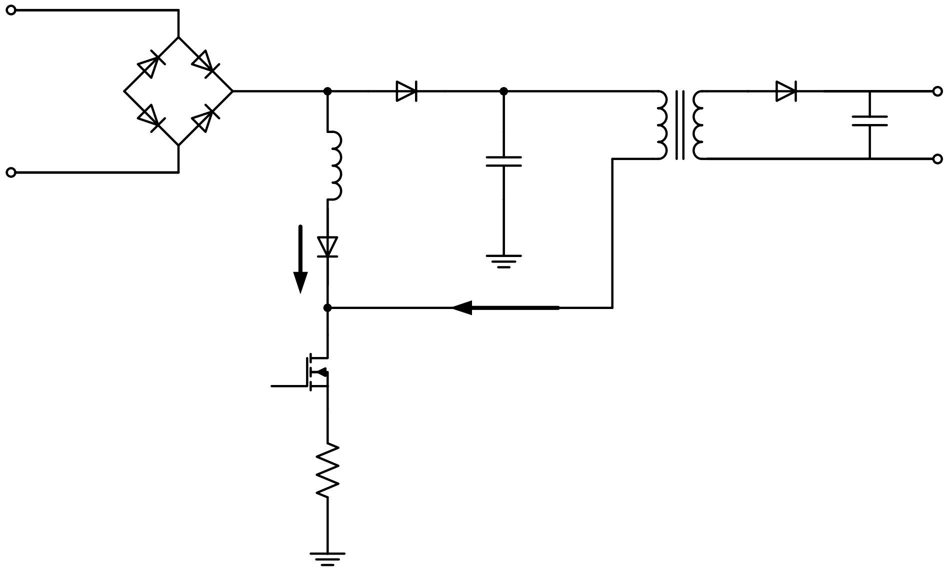

Figure 2 A simplified schematic

2 PFC inductor operating modes

Figure 3 shows the active operating modes for inductor Lpfc.

When MOSFET Q1 turns on, input voltage is applied on Lpfc. The inductor current rises with slope Vin/Lpfc. The transformer T1 primary winding current rises with slope Vbulk/Lm.

When MOSFET Q1 turns off, the inductor current continues flowing through the transformer primary winding Np. Partial energy is transferred to the secondary side loading. Partial energy is transferred into the bulk capacitor Cbulk. The energy in the transformer is transferred to the output loading.

It is noted that Figure 3 does not include the state when both Lpfc and Lm having zero current. Figure 3 also assume the Vbulk is always higher than Vin such that D1 does not conduct in steady state operation. This is usually true when Vin is at high line. When Vin is at low line, D1 also helps to charge the bulk capacitor.

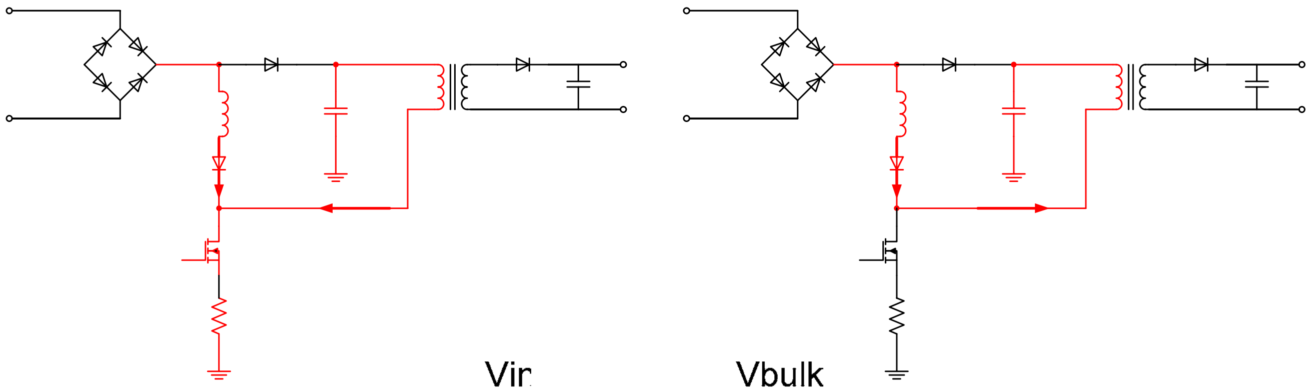

Figure 3 Operating Modes

3 Determine bulk capacitor voltage

Assumption:

- Vbulk is always higher than Vin voltage. Diode D1 does not conduct in steady state operation. If $V_{in} = V_{amp}\sin(\omega t)$, then Vbulk>Vamp.
- Vbulk ripple is negligible, i.e. Vbulk is a constant DC voltage.
- Both PFC inductor and transformer are in DCM operating mode.

When Q1 turns on, the bulk capacitor releases energy to the transformer T1. The energy is then transferred to the output load when Q1 turns off. When Q1 turns off, the bulk capacitor is charged by the PFC inductor.

The power release from Cbulk in one cycle can be expressed as $P_{o2} = \frac{(V_{bk}T_{on})^2}{2L_mT_p}$

The power input from PFC inductor to the bulk capacitor is $P_i = \frac{V_{in}T_{on}T_{rst}V_{bk}}{2L_{pfc}T_p}$

Since $V_{in} = V_{amp}\sin(\omega t)$, by power balance during half AC cycle

$$\frac{1}{\pi}\int_0^{\pi}\frac{V_{amp}\sin(\omega t)T_{on}T_{rst}V_{bk}}{2L_{pfc}T_p}\,d\omega t = \frac{(V_{bk}T_{on})^2}{2L_mT_p}$$

By VinTon balance on PFC inductor $T_{rst} = \frac{V_{in}T_{on}}{V_{bk} + N_{ps}(V_{out} + V_d) - V_{in}}$

The ratio between the PFC inductance and the magnetizing inductance vs. Vbulk is calculated to be

$$K_r = \frac{L_{pfc}}{L_m} = \frac{1}{\pi V_{bk}} \int_0^{\pi} \frac{\left[V_{amp} \sin(\omega t)\right]^2}{V_{bk} + N_{ps}\left(V_{out} + V_d\right) - V_{amp} \sin(\omega t)} d\omega t$$

Where

- Vamp = AC input voltage amplitude
- Vbulk = bulk capacitor voltage
- Lm = magnetizing inductance
- Nps = primary to secondary turn ratio
- Vout = output voltage
- Vd = output rectifier forward voltage drop

Assume the input voltage is 264Vac; the number of primary winding is 78; the number of secondary winding is 28, the output voltage is 28V, the output diode forward voltage drop is 0.5V.

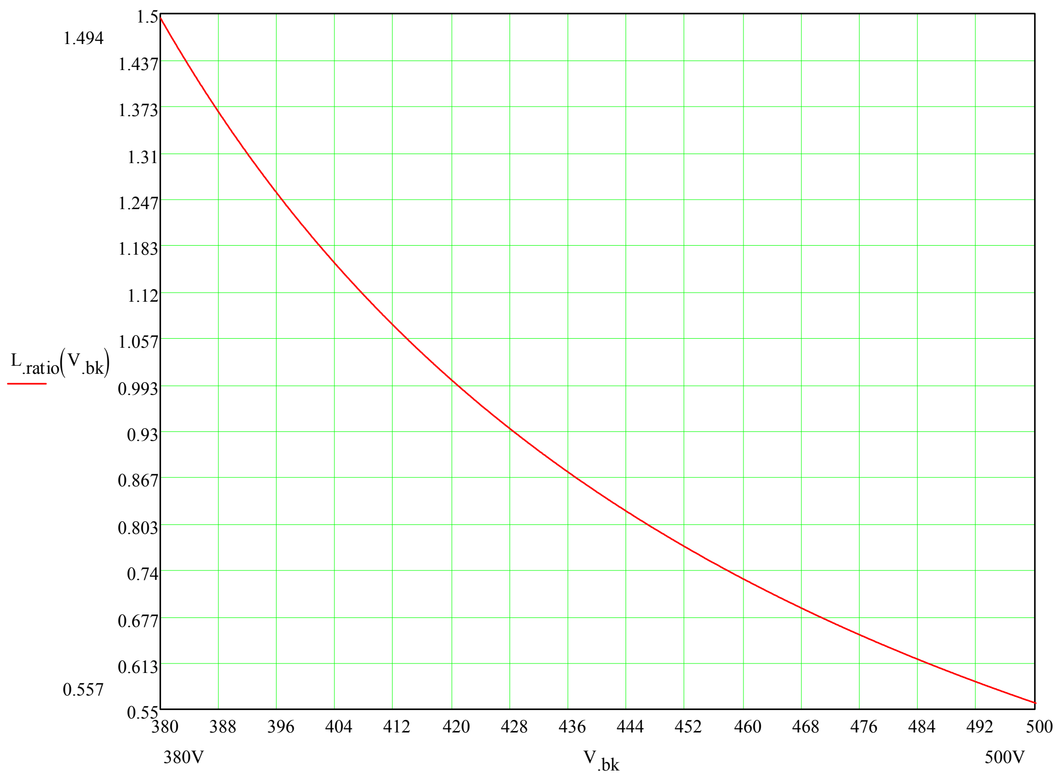

Figure 4 Kr ratio vs. Vbulk when AC input is 264V.

For example, if limit the average bulk voltage to 460V, from Figure 4, the ratio of PFC inductance vs. the magnetizing inductance is about Kr = 0.72.

4 PFC inductance and Flyback transformer magnetizing inductance

Assume Vbulk is always higher than Vin, then the power transferred from PFC inductor to the output loading can be expressed as $P_{o1} = \frac{V_{in} T_{on} T_{rst} N_{ps} (V_{out} + V_d)}{2 L_{pfc} T_p} \eta_x$. The power delivered to the output loading from the bulk capacitor is $P_{o2} = \frac{(V_{bk} T_{on})^2}{2 L_m T_p} \eta_x$.

The total output power can be derived that $$P_{out} = \frac{(V_{bk} T_{on})^2}{2 T_p} \eta_x \left(\frac{1}{K_L L_{pfc}} + \frac{1}{L_m} \right)$$

Where $$K_L = \frac{1}{\frac{1}{\pi} \int_0^{\pi} \left(\frac{V_{amp} \sin(\omega t)}{V_{bk}} \right)^2 \frac{N_{ps}(V_{out} + V_d)}{V_{bk} + N_{ps}(V_{out} + V_d) - V_{amp} \sin(\omega t)} d\omega t}$$

Pout can also be rewritten as $$P_{out} = \frac{(V_{bk} T_{on})^2}{2 L_{eq} T_p} \eta_x$$

Where $$\frac{1}{L_{eq}} = \frac{1}{K_L L_{pfc}} + \frac{1}{L_m}$$

Leq can represent the equivalent magnetizing inductance in a normal Flyback circuit design without considering the PFC inductor.

So the design process is, if Vbulk is known by estimation or measurement, Leq can be calculated by following iW3620 design spreadsheet. Once Leq is obtained, the PFC inductance and the Lm can be calculated by

$$L_{pfc} = K_r L_m, \qquad L_m = \left(\frac{1}{K_L K_r} + 1 \right) L_{eq}$$

Leq is usually designed at the lowest AC input where enough output power is needed to support the loading. So Lpfc and Lm are also calculated considering lowest Vbulk voltage.

For example, for a universal AC input line, 28V/0.5A output design, the desired L_{eq} is calculated to be 0.62mH. At AC input voltage 90Vac, average V_{bulk} is estimated to be 114V. Then calculate K_L = 1.666. We have L_m = 1.13mH; L_{pfc} = 0.82mH.

It is noted that if the AC input voltage drops, less power is transferred to the bulk capacitor from the PFC inductor. The diode D1 starts to forward bias when the PFC inductor is not enough to charge up the bulk capacitor.

The bulk capacitor voltage is also determined by the bulk capacitance. High bulk capacitance leads to lower voltage ripple on the bulk capacitor.