PWM Step-Up DC-DC Converter

Features

- **Low Start-Up Voltage 0.9V**
- **Fixed 300kHz Operating Frequency**
- **Built-In Internal Soft-Start Circuit**
- **Low Operating Current**
- **3.3V and 5V (±2.5%) Fixed (APW7077) or Adjustable Output Voltage (APW7077A)**
- **High Efficiency Up to 88% at 400mA Output Current**
- **High Output Current Up to 1A**
- **Compact Package: SOT-23-5**
- **Lead Free and Green Devices Available (RoHS Compliant)**

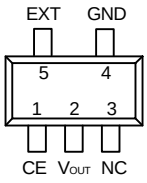
Applications

- **Cellular and Portable Phones**
- **Portable Audio**
- **Camcorders and Digital Still Camera**
- **Hand-held Instrument**
- **PDAs**

General Description

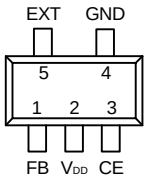
The APW7077/A series are multi- function PWM step-up DC-DC converter with an adaptive voltage mode controller and higher efficiency application from one to four cells battery packs. The APW7077/A series are set PWM operating mode, voltage-mode to follow portable application. And built-in driver pin, EXT pin, for connecting to an external transistor or MOSFET during light load, the device will automatically skip switching cycles to maintain high efficiency. The APW7077/A series consist of PWM controller, reference voltage, phase compensation, oscillator, soft-start, driver block. It will be provided to operate suitable voltage without external compensation circuit. The APW7077/A series have fixed voltage and adjustable voltage version from a wide input voltage ranges 0.7V to 5.5V for step-up DC-DC converter. The start-up is guaranteed at 1V and the device is operating down to 0.7V, and providing up to 300mA loading current. Besides, low quiescent current (switch-off) is guaranteed.

Pin Configuration



SOT-23-5 (Top View)

APW7077



SOT-23-5 (Top View)

APW7077A

Ordering and Marking Information

APW7077/A - □□□□-□□□ Assembly Material Handling Code Temperature Range Package Code Voltage Code	Package Code B : SOT-23-5 Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Voltage Code 33 : 3.3V 50 : 5.0V Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APW7077 - 33B : 77RX X - Date Code, R : 3.3V	APW7077A B : A77X X - Date Code
APW7077 - 50B : 77ZX X - Date Code, Z : 5.0V	

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7	V
V_{IO}	Input / Output Pins (CE, FB, EXT)	-0.3 to 7	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Junction Temperature Range	-40 to 150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$R_{\theta JA}$	Thermal Resistance – Junction to Ambient SOT-23-5	200	°C/W

Electrical Characteristics

(for all values T_A = 25°C, V_{OUT} = 3.3V, unless otherwise noted)

Symbol	Parameter	Test Conditions	APW7077A			Unit
			Min.	Typ.	Max.	
STEP-UP SECTION						
V_{IN}	Minimum Operating Input Voltage	$V_{OUT} = V_{DD}$	-	0.9	-	V
V_{DD}	Operating Voltage	$V_{IN} = V_{DD}$	1.9	-	5.5	V
	Start-Up Voltage	Io<10mA, $V_{OUT} = V_{DD}$ (<5.5V)	-	0.9	1	V
		V_{OUT} = 12V, Io<10mA, $V_{DD} = V_{IN}$	1.9	2.0	-	V
f_{SW}	Operating Frequency	V_{DD} = 3.3V, VFB = 0.5V	270	300	330	kHz
	Oscillator Frequency Line Regulation	2.0V<V_{DD}<5.5V	-	±1.2	-	%
D_{MAX}	Maximum Duty Cycle	V_{FB} = 0.5V	81	88	95	%
	Maximum Duty Line Regulation	2.0V<V_{DD}<5.5V	-	±0.5	-	%
POWER MOSFET						
I_{SOURCE}	EXT Output Source Current	Duty≤5%, EXT = V_{DD}-0.4V	-70	-110	-150	mA
I_{SINK}	EXT Output Sink Current	Duty≤5%, EXT = 0.4V	80	120	160	mA
CONTROL SECTION						
	Output Voltage Range	External Divider	2.0	-	-	V
V_{FB}	Feedback Voltage	I_{LOAD} = 0mA	0.98	1	1.02	V
	Feedback Voltage Line Regulation	2.0V<V_{DD}<5.5V	-	±0.1	-	%
I_{FB}	Feedback Input Current	V_{FB} = 1.4V	-	0.03	50	nA
T_{SS}	Soft-Start Time		10	25	40	ms
	Soft-Start Threshold Voltage	Duty = 50%	-	1.65	-	V
	Soft-Start Hysteresis Voltage		-	150	-	mV
Iq	Operating Current	$V_{DD} = V_{CE}$ = 3.3V, V_{FB} = 0.5V	-	150	230	µA
		$V_{DD} = V_{CE}$ = 3.3V, V_{FB} = 1.1V	-	100	150	µA
I_{OFF}	Stand-by Current	$V_{DD} = V_{CE}$ = 3.3V, V_{FB} = 1.3V	-	17	25	µA
	Switch-Off Current	V_{DD} = 3.3V, V_{CE} = 0V	-	1	2	µA
V_{CE}	Logic LOW (V_{IL})		-	-	0.7	V
	Logic HIGH(V_{IH})		1.2	-	-	V
I_{CE}	CE Pin Input Current	V_{CE} = 0V	-	1	2	µA
		V_{CE} = 3.3V	-	0.07	50	nA

Electrical Characteristics (Cont.)

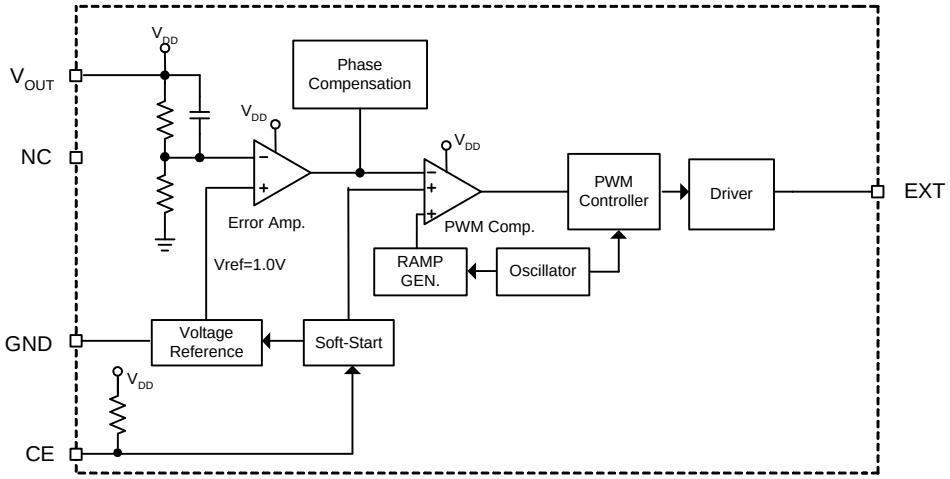
(for all values T_A = 25°C, V_{OUT} = 3.3V, unless otherwise noted)

Symbol	Parameter	Test Conditions	APW7077			Unit
			Min	Typ	Max	
STEP-UP SECTION						
V_{IN}	Minimum Operating Input Voltage		0.7	-	-	V
	Operating Voltage		1	-	5.5	V
	Start-Up Voltage	APW7077_33, Io<10mA	-	0.9	-	V
		APW7077_33, 10mA<Io<100mA	-	1.1	-	V
		APW7077_50, Io<10mA	-	0.9	-	V
		APW7077_50, 10mA<Io<100mA	-	1.1	-	V
V_{HOLD}	Hold Voltage	I_{LOAD} = 10mA	-	0.7	0.8	V
f_{SW}	Operating Frequency	V_{OUT} = 3.3VX96%	270	300	330	kHz
D_{MAX}	Maximum Duty Cycle	V_{OUT} = 3.3VX96%	81	88	95	%
POWER MOSFET						
I_{SOURCE}	EXT Output Source Current	Duty≤5%, EXT = 2.9V	-70	-110	-150	mA
I_{SINK}	EXT Output Sink Current	Duty≤5%, EXT = 0.4V	80	120	160	mA
CONTROL SECTION						
V_{OUT}	APW7077-33	I_{IN} = 0mA	3.218	3.3	3.383	V
	APW7077-50	I_{IN} = 0mA	4.875	5	5.125	V
T_{SS}	Soft-Start Time		10	25	40	ms
	Soft-Start Threshold Voltage	Duty = 50%	-	1.65	-	V
	Soft-Start Hysteresis Voltage		-	150	-	mV
Iq	Operating Current	V_{CE} = V_{OUT}, V_{OUT} = 0.96V_{OUT}	-	200	300	µA
		V_{CE} = V_{OUT}, V_{OUT} = 1.04V_{OUT}	-	160	240	µA
I_{OFF}	Stand-by Current	V_{CE} = V_{OUT}, V_{OUT} = 1.3V_{OUT}	-	35	55	µA
	Switch-Off Current	V_{CE} = 0V	-	1	2	µA
V_{CE}	Logic LOW (V_{IL})		-	-	0.7	V
	Logic HIGH (V_{IH})		1.2	-	-	V
I_{CE}	CE Pin Input Current	V_{CE} = 0V	-	1	2	µA
		V_{CE} = 2.0V	-	0.07	50	nA

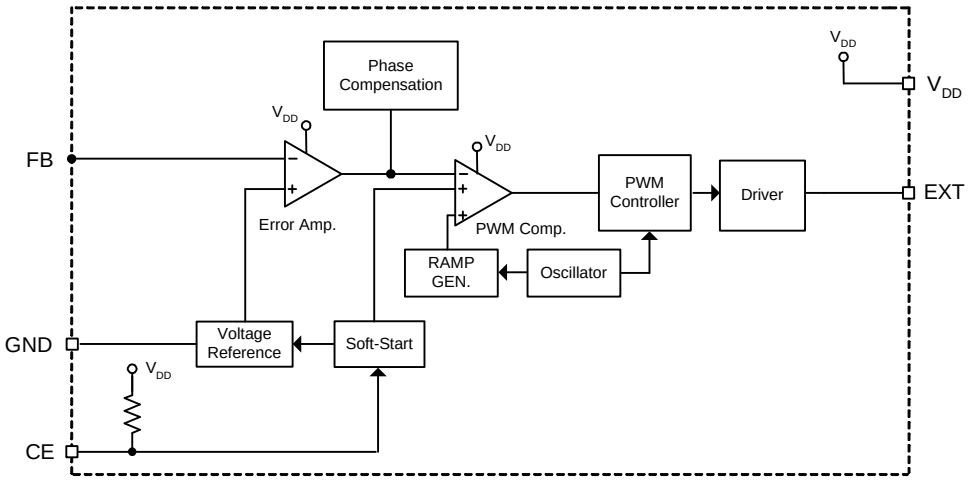
Pin Description

PIN		PIN NAME	FUNCTION
APW7077	APW7077A		
1	3	CE	Chip enable input. High = operating mode; Low = shutdown mode
5	5	EXT	External MOSFET or transistor drive pin.
4	4	GND	Ground pins of the circuit.
X	2	VDD	Supply voltage.
X	1	FB	FB: Internal 1.0V reference voltage. Use a resistor divider to set the output voltage from and VOUT = $\left(1+\frac{R2}{R1}\right)$VFB.
3	X	NC	No internal connection to the pin.
2	X	V_{OUT}	V_{OUT} Provides bootstrap power to the IC.

Block Diagram



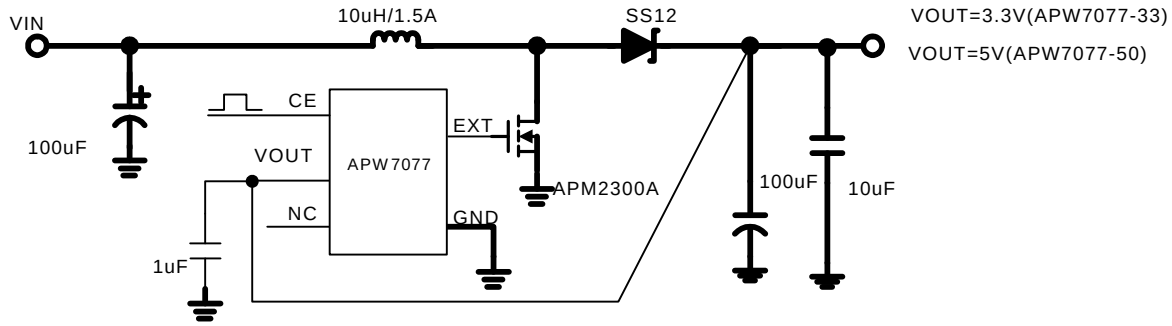
APW7077



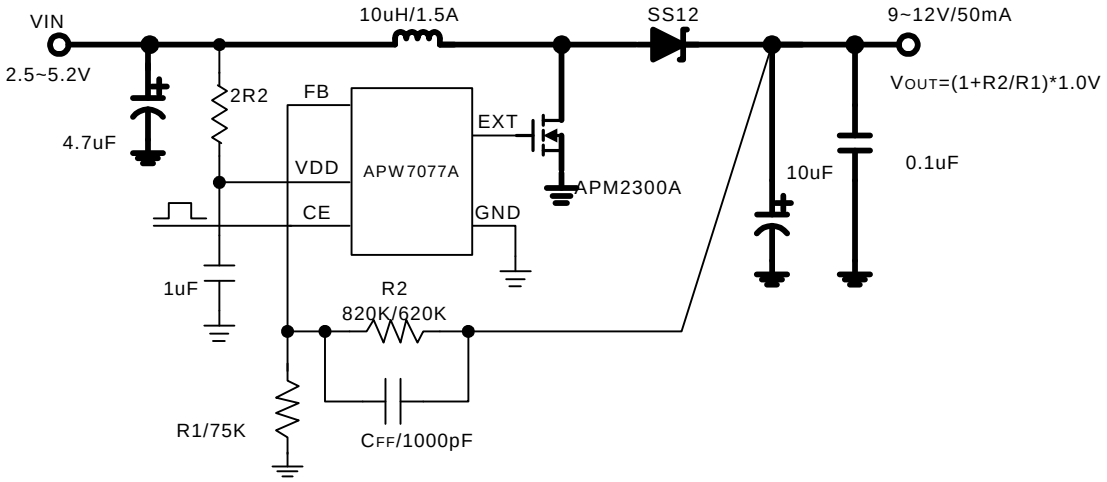
APW7077A

Typical Application Circuit

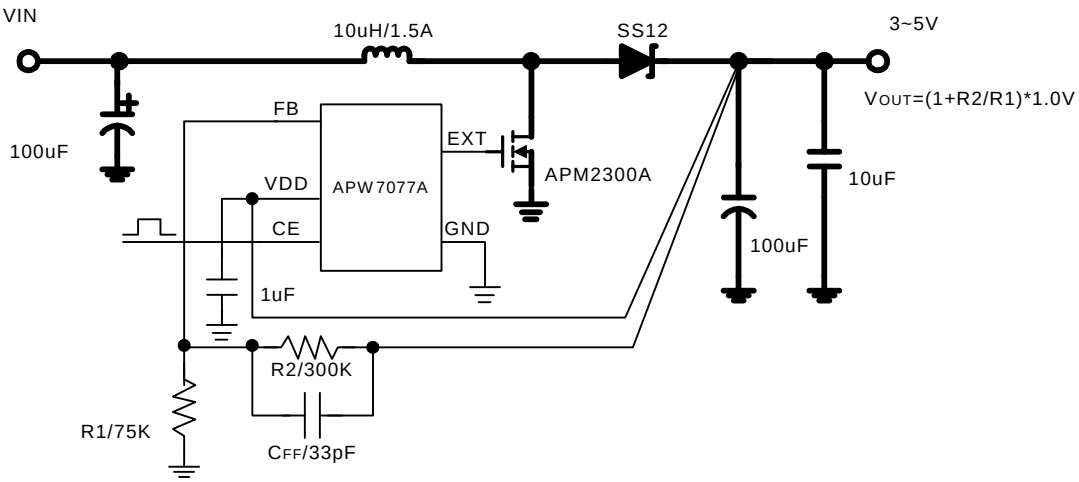
Application Circuit for APW7077



Application Circuit for APW7077A



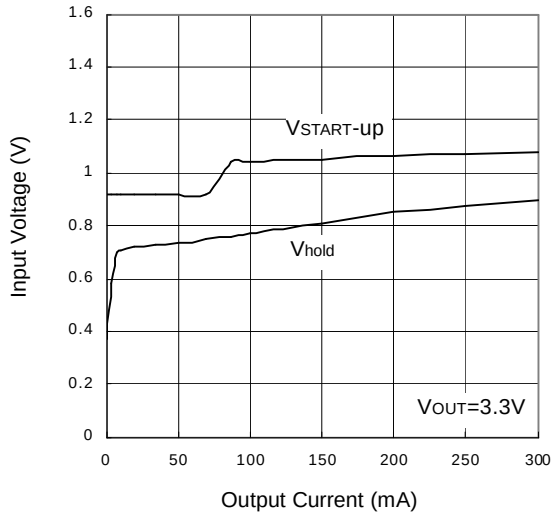
Application Circuit for APW7077A



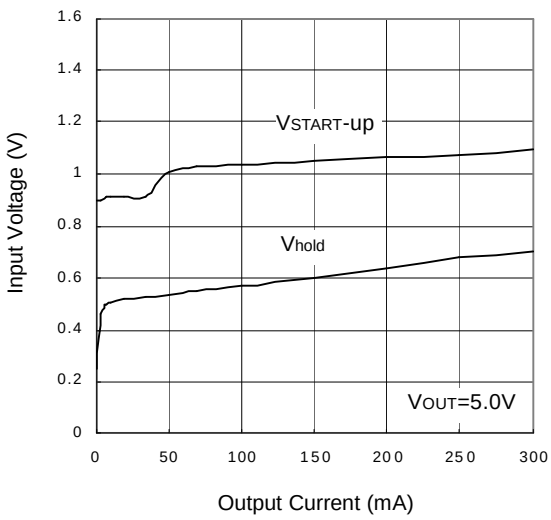
*R1≦100KΩ is recommended

Typical Operating Characteristics

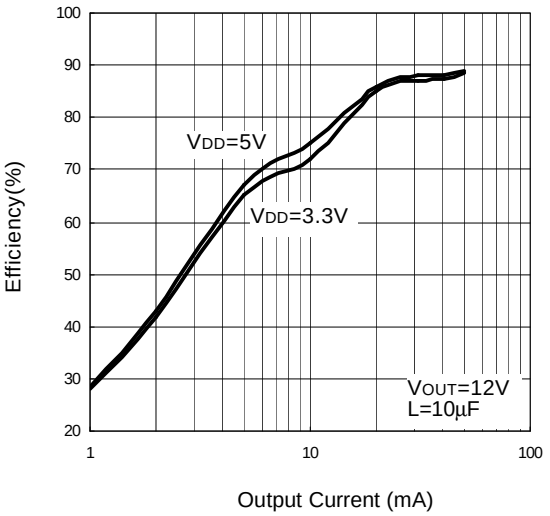
Start-up/Hold Voltage vs. Output Current



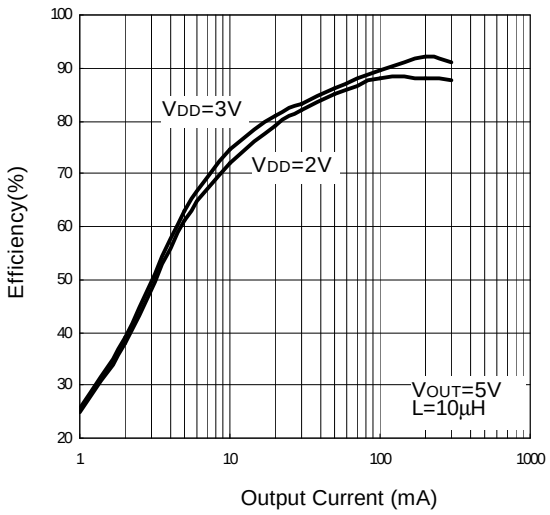
Start-up/Hold Voltage vs. Output Current



Efficiency vs. Output Current

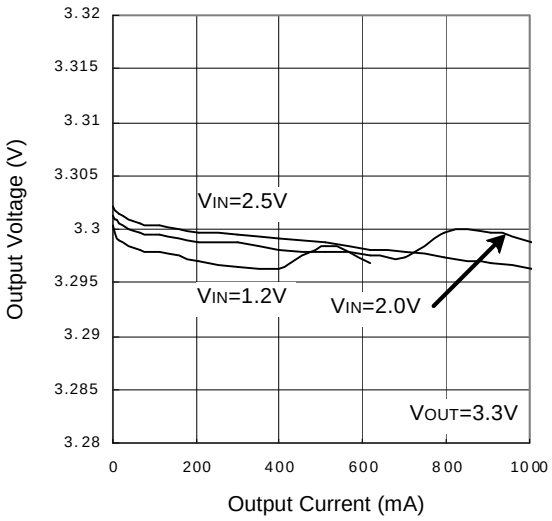


Efficiency vs. Output Current

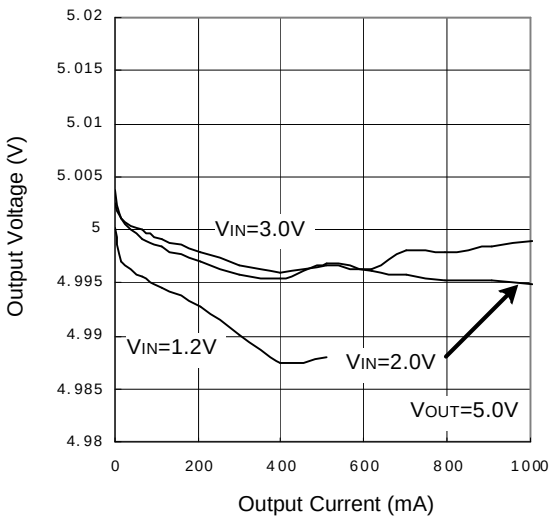


Typical Operating Characteristics (Cont.)

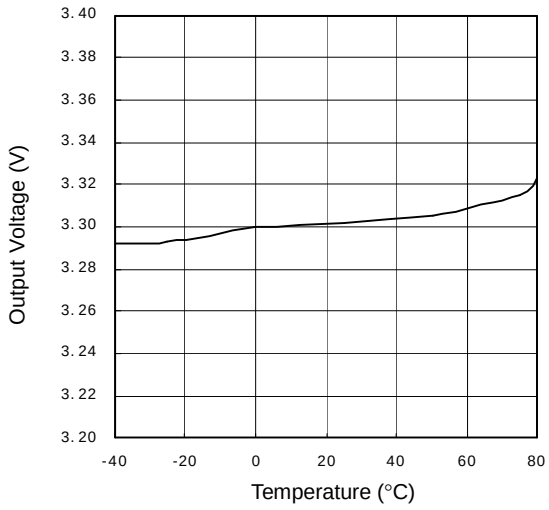
Output Voltage vs. Output Current



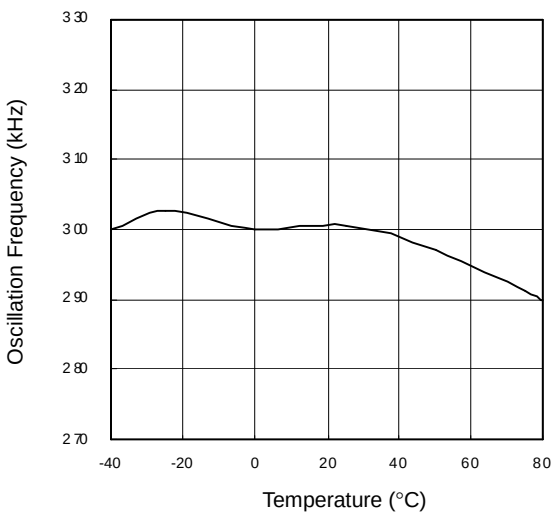
Output Voltage vs. Output Current



Output Voltage vs. Temperature

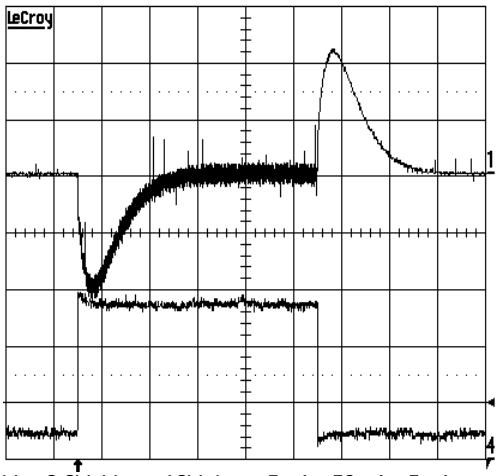


Oscillation Frequency vs. Temperature



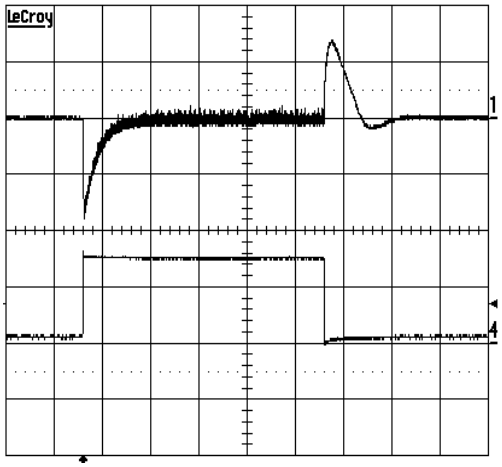
Typical Operating Characteristics (Cont.)

Load Transient Waveform



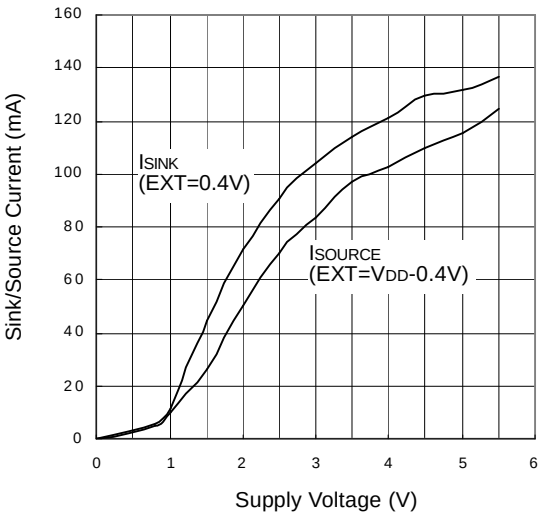
V_{IN}=3.3V, V_{OUT}=12V, I_{OUT}=5mA->50mA->5mA
L=10µH, C_{OUT}=4.7µF+0.1µF, Cff=560pF
CH1:V_{OUT}, 100mV/DIV, Time=1ms/DIV
CH4:I_{OUT}, 20mA/DIV

Load Transient Waveform

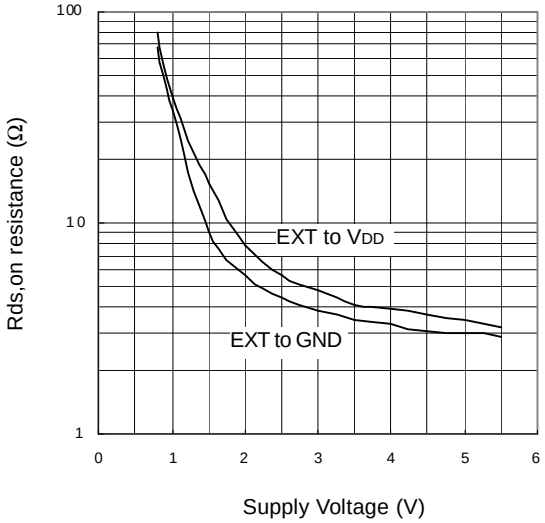


V_{IN}=3.3V, V_{OUT}=5V, I_{OUT}=10mA->300mA->10mA
L=10µH, C_{OUT}=22µF+22µF+0.1µF, Cff=33pF
CH1:V_{OUT}, 100mV/DIV, Time=1ms/DIV
CH4:I_{OUT}, 200mA/DIV

EXT Driving Current vs. Supply Voltage

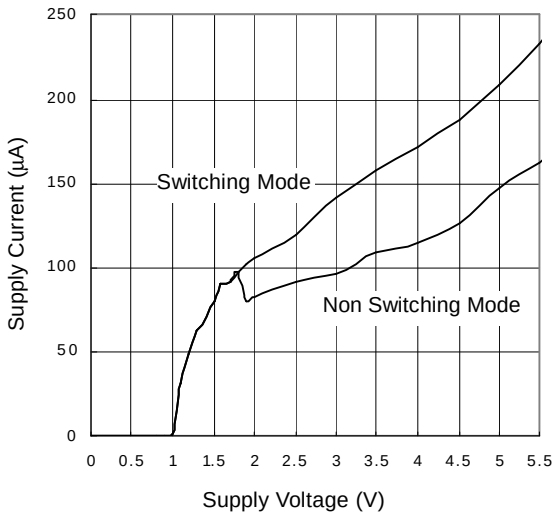


EXT Rds,on vs. Supply Voltage

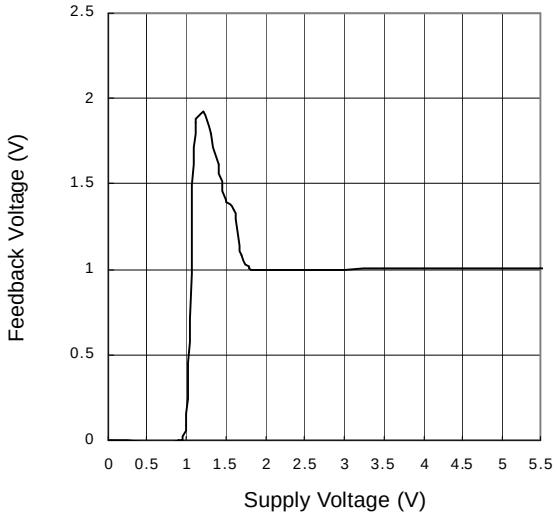


Typical Operating Characteristics (Cont.)

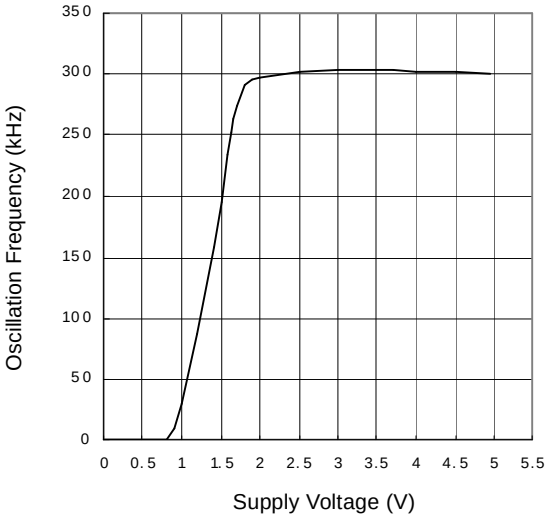
Supply Current vs. Supply Voltage



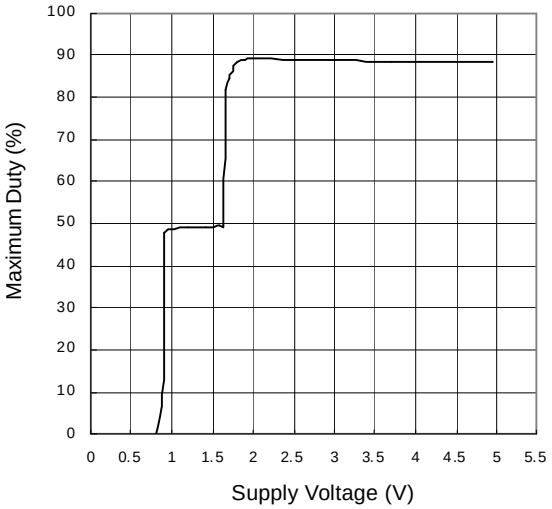
Feedback Voltage vs. Supply Voltage



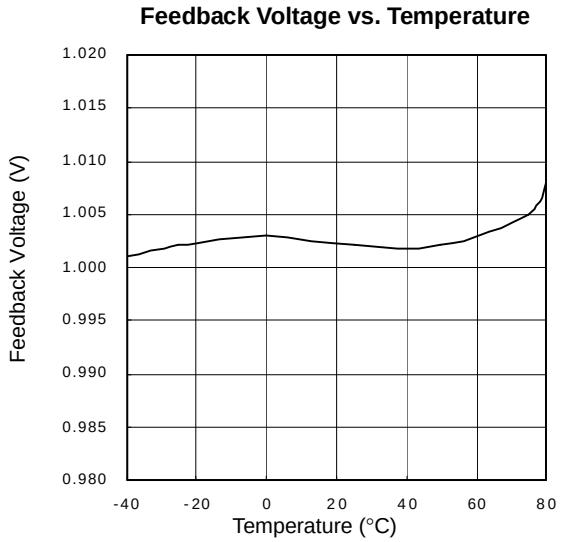
Oscillation Frequency vs. Supply Voltage



Maximum Duty vs. Supply Voltage



Typical Operating Characteristics (Cont.)



Function Description

Operation

The APW7077/A series are low noise fixed frequency voltage–mode PWM DC–DC controllers, and consist of start–up circuit, reference voltage, oscillator, loop compensation network, PWM control circuit, and low ON resistance driver.

APW7077 provides on–chip feedback resistor and loop compensation network, the system designer can get the regulated fixed output voltage 3.3V and 5.0V with a small number of external components, it is optimized for battery powered portable products where large output current is required. APW7077A provides internal reference voltage 1.0V and output voltage setting by external resistance for higher voltage requirement. The quiescent current is typically 120μA (V_{OUT} = 3.3V, fsw = 300kHz), and can be further reduced to about 1.0μA when the chip is disabled (V_{CE} < 0.7V).

The APW7077/A operation can be best understood by referring to the block diagram. The error amplifier monitors the output voltage via the feedback resistor divider by comparing the feedback voltage with the reference voltage. When the feedback voltage is lower than the reference voltage, the error amplifier output will decrease. The error amplifier output is then compared with the oscillator ramp voltage at the PWM controller.

When the feedback voltage is higher than the reference voltage, the error amplifier output increases and the duty cycle decreases. When the external power switch is on, the current ramps up in the inductor, storing energy in the magnetic field. When the external power switch is off, the energy stored in the magnetic field is transferred to the output filter capacitor and the load. The output filter capacitor stores the charge while the

Function Description (Cont.)

Operation (Cont.)

inductor current is higher than the output current, and then sustains the output voltage until the next switching cycle.

As the load current decreases, the switch transistor turns on for a shorter duty cycle. Under the light load condition, the controller will skip switching cycles to reduce power consumption, therefore, high efficiency is maintained at light loads.

Fixed Output Voltage (for APW7077 only)

The APW7077 V_{OUT} is set by an integrate feedback resistor network. This is trimmed to a selected voltage 3.3V or 5.0V with an accuracy of +/-2.5%.

Setting Output Voltage (for APW7077A only)

For APW7077A, the output voltage is adjustable. The output voltage is set using the FB pin and a resistor divider connected to the output as shown in the typical operating circuit. The internal reference voltage is 1.0V with 2% variation, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$V_{OUT} = (1 + \frac{R2}{R1}) \times 1.0V$$

To avoid the thermal noise from feedback resistor, (R_1+R_2) resistance smaller than 1MΩ and 1% variation is recommended.

Soft-Start

There is a soft-start function integrated in APW7077/A series to avoid the over shooting when power on. When power is applied to the device, the soft-start circuit first pumps up the output voltage to let V_{DD}(or V_{OUT}) approximately 1.65V at a fixed duty cycle 50%. This is the voltage level at which the controller can operate normally. When supply voltage more than 1.65V, the internal reference voltage will be ramp up to let output voltage reach to setting voltage without over shooting issue whenever heavy load or light load condition. The soft-start time 25ms is setting by internal circuit.

Oscillator

The oscillator frequency is internally set to 300kHz at an accuracy of +/-10% and with low temperature coefficient of 3.3%/°C.

Enable/Disable Operation

The APW7077/A series offer IC shutdown mode by chip enable pin (CE pin) to reduce current consumption. When voltage at pin CE is greater than 1.2V, the chip will be enabled, which means the controller is in normal operation. When voltage at pin CE is less than 0.7V, the chip is disabled, which means IC is shutdown and quiescent current become 1μA.

The CE pin is pulled high to V_{DD}(or V_{OUT}) by internal resistor, and this resistance is greater than 1MΩ . Therefore, this chip will enable normally when CE pin is floating.

Important: DO NOT apply a voltage between 0.7V to 1.2V to pin CE as this is the CE pin's hysteresis voltage range. Clearly defined output states can only be obtained by applying voltage out of this range.

Compensation

The device is designed to operate in continuous conduction mode. An internal compensation circuit was designed to guarantee stability over the full input/output voltage and full output load range.

Step–Up Converter Operating Mode

The step–up DC–DC controller is designed to operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

Function Description (Cont.)

Step–Up Converter Operating Mode (Cont.)

For a step up converter in a CCM, the duty cycle D is given by

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

In higher output voltage or small output current application, the step–up DC–DC controller operated in discontinuous conduction mode almost. For a step-up converter in a DCM, the duty cycle D is given by

$$D = \sqrt{\frac{2 \cdot L}{T_S \cdot R_{LOAD}} \cdot \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{OUT}}{V_{IN}} - 1 \right)}$$

External components values can be calculated from these equations, however, the optimized value should obtained through experimental results.

Critical Inductance Value

The minimum value of inductor to maintain continuous conduction mode can be determined by the following equation.

$$L \geq \frac{V_{OUT} \times D(1 - D)^2}{fsw \times I_O \times Ratio}$$

A system can be designed to operate in continuous mode for load currents above a certain level usually 20 to 50% (Ratio define as 0.2~0.5) of full load at minimum input voltage. When I_O smaller than (I_O*Ratio), the controller system will into DCM.

ΔI_L is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses. Based on 20%(Ratio=0.2) current ripple, V_{OUT}=5V, I_O=1A and V_{IN} =1.8V system, the inductance value is calculated as 6.9µH and a 6.8µH inductor is used.

The inductor current ripple has an expression

$$\Delta I_L = \frac{V_{IN} \times D}{fsw \times L}$$

The maximum DC input current can be calculated as

$$I_L(max) = \frac{V_{OUT} \times I_O(max)}{V_{IN}(min)}$$

The inductor peak current can be calculated as

$$I_{PK} = \frac{V_{OUT} \times I_O}{V_{IN}} + \frac{\Delta I_L}{2}$$

NOTES:

D – On–time duty cycle
I_L – Average inductor current
I_{PK} – Peak inductor current
I_O – Desired dc output current
V_{IN} – Nominal operating dc input voltage
V_{OUT} – Desired dc output voltage
ESR – Equivalent series resistance of the output capacitor

Inductor Selection

APW7077/A series are designed to work well with a 6.8 to 12µH inductors in most applications 10µH is a sufficiently low value to allow the use of a small surface mount coil, but large enough to maintain low ripple. Lower inductance values supply higher output current, but also increase the ripple and reduce efficiency. Higher inductor values not only reduce ripple and improve efficiency, but also limit output current. The inductor should have small DCR, usually less than 0.2Ω, to minimize loss. It is necessary to choose an inductor with a saturation current greater than the peak current which the inductor will encounter in the application.

The inductor ripple current is important for a few reasons. One reason is the peak switch current will be the average inductor current (I_L) plus ΔI_L.

As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or ΔI_L is greater than the average inductor current. Therefore, continuous conduction mode occurs when ΔI_L is less than the average inductor current.

Function Description (Cont.)

Inductor Selection (Cont.)

Care must be taken to make sure that the switch will not reach its current limit during normal operation.

The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

Output Capacitor

The output capacitor is used for sustaining the output voltage when the external MOSFET or bipolar transistor is switched on and smoothing the ripple voltage.

The output capacitance needed is calculated in equation.

$$C_{OUT}(min) = \frac{I_O(max) \times D}{fsw \times \Delta V_{OUT}}$$

The ESR is also important because it determines the peak to peak output voltage ripple according to the approximated equation:

$$ESR = \frac{\Delta V_{OUT}}{\Delta I_O}$$

With 1% output voltage ripple, low ESR capacitor should be used to reduce output ripple voltage. In general, a 100µF to 220µF low ESR (0.10Ω to 0.30Ω) Tantalum capacitor should be appropriate. The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. A minimum value of 10µF is recommended and may be increased to a larger value.

Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The size used is dependant on the application and board layout.

If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful conditions while a 22µF to 47µF capacitor may be required for higher power and dynamic loads. Small ESR Tantalum or ceramic capacitor should be suitable and the total input ripple voltage can be calculated

$$\Delta V_{IN} = \Delta I_L \times ESR$$

Design Example

It is supposed that a step–up DC–DC controller with 3.3V output delivering a maximum 1000 mA output current with 100 mV output ripple voltage powering from a 2.4V input is to be designed.

Design parameters:

V_{IN} = 2.4V

V_{OUT} = 3.3V

I_O = 1.0A

ΔV_{OUT} = 100mV

fsw= 300kHz

Ratio = 0.2 (typical for small output ripple voltage)

Assume the diode forward voltage and the transistor saturation voltage are both 0.3V. Determine the maximum steady state duty cycle at V_{IN} = 2.4V:

D=0.273

Calculate the maximum inductance value which can generate the desired current output and the preferred delta inductor current to average inductor current ratio:

L=10µH

Function Description (Cont.)

Design Example(Cont.)

Determine the average inductor current and peak inductor current:

I_L=1.38A
ΔI_L=0.218A
Ipk=1.45A

Therefore, a 10µH inductor with saturation current larger than 1.73 A can be selected as the initial trial.

Determine the output capacitance value for the desired output ripple voltage:

C_{OUT}=33µF

The ESR of the output capacitor is 0.05Ω. Therefore, a Tantalum capacitor with value of 33 µF to 47µF and ESR of 0.05Ω can be used as the output capacitor. However, according to experimental result, 220µF output capacitor gives better overall operational stability and smaller ripple voltage.

Component Selection

Diode Selection

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. The diode is the largest source of loss in DC–DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, VF, and the reverse recovery time, trr. The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the P–N junction. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

External Switch Transistor

The APW7077/A can drive up to 110mA of gate drive current. An N-channel MOSFET with a relatively low threshold voltage, low gate charge and low RDS(ON) is required to optimize overall circuit performance. The APW7077/A Evaluation Board uses a APM2300A. This NMOS device was chosen because it demonstrates an RDS_ON of 45mΩ and a total gate charge Qg of 12nC (typ.).

Layout Consideration

Ground Plane

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance). Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency.

Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.

The output capacitor, C_{OUT}, should also be placed close to the diode. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple and efficiency.

Switching Noise Decoupling Capacitor

On APW7077 fixed voltage application, a 0.1µF ceramic capacitor should be placed close to the V_{OUT} pin and GND pin of the chip to filter the switching spikes in the output voltage monitored by the V_{OUT} pin.

Feedback Network

On APW7077A application, the feedback networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the GND pin.

If no analog ground plane is available, then this ground must tie directly to the GND pin. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Prevent connect feedback network on output decoupling MLCC.

Input Capacitor

In APW7077A high output voltage application circuit, the input voltage (V_{IN}) is tied to chip supply pin (V_{DD}). The input capacitor C_{IN} in V_{IN} must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 1µF capacitor can be placed in parallel with C_{IN}, close to the V_{DD} pin, to shunt any high frequency noise to ground.

Inductor

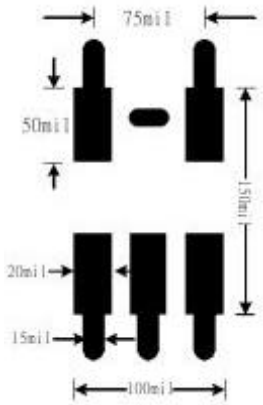
To minimize copper trace connections that can inject noise into the system, the inductor, switch, and Schottky diode should be placed as close as possible to minimize the noise coupling into other circuits.

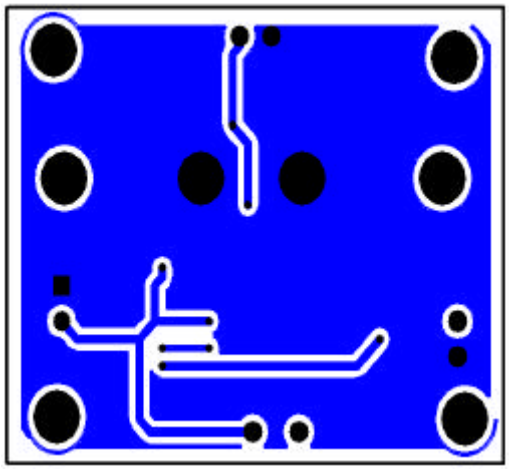
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

Layout Consideration (Cont.)

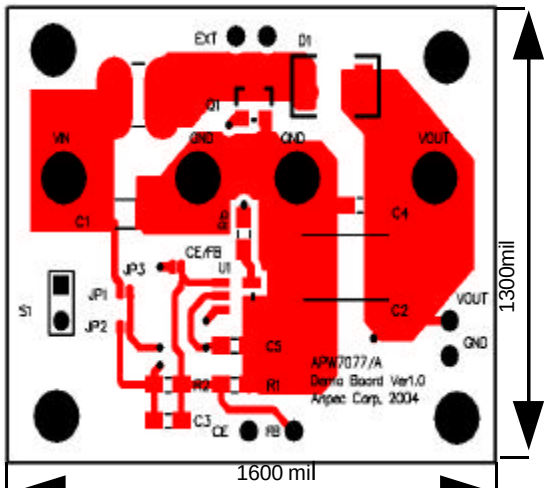
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS (Cont.)





Bottom Layer

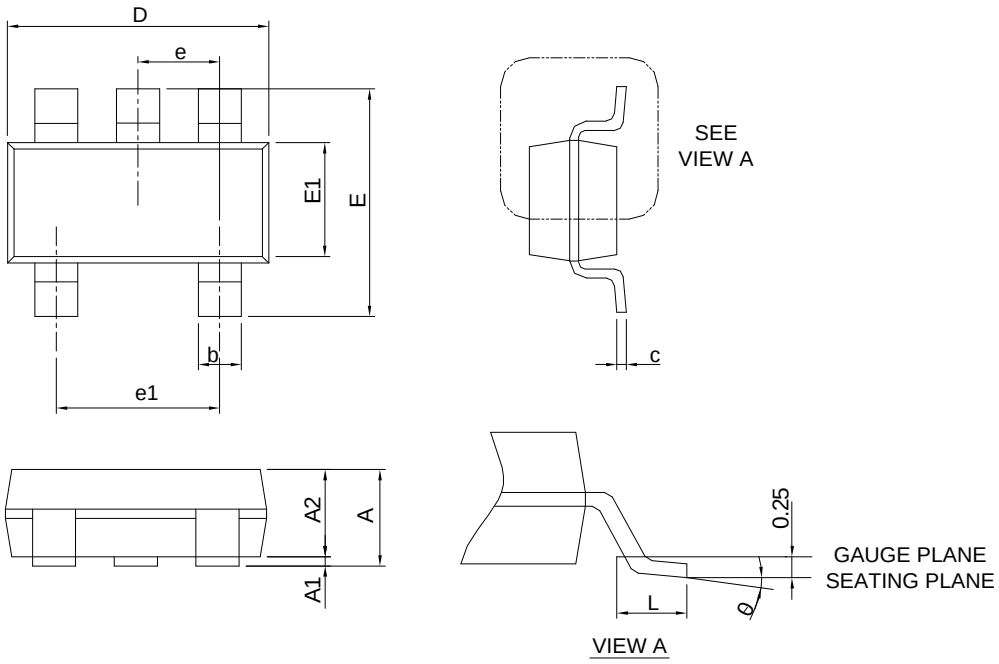
Demo Board Circuit Layout



Top Layer

Package Information

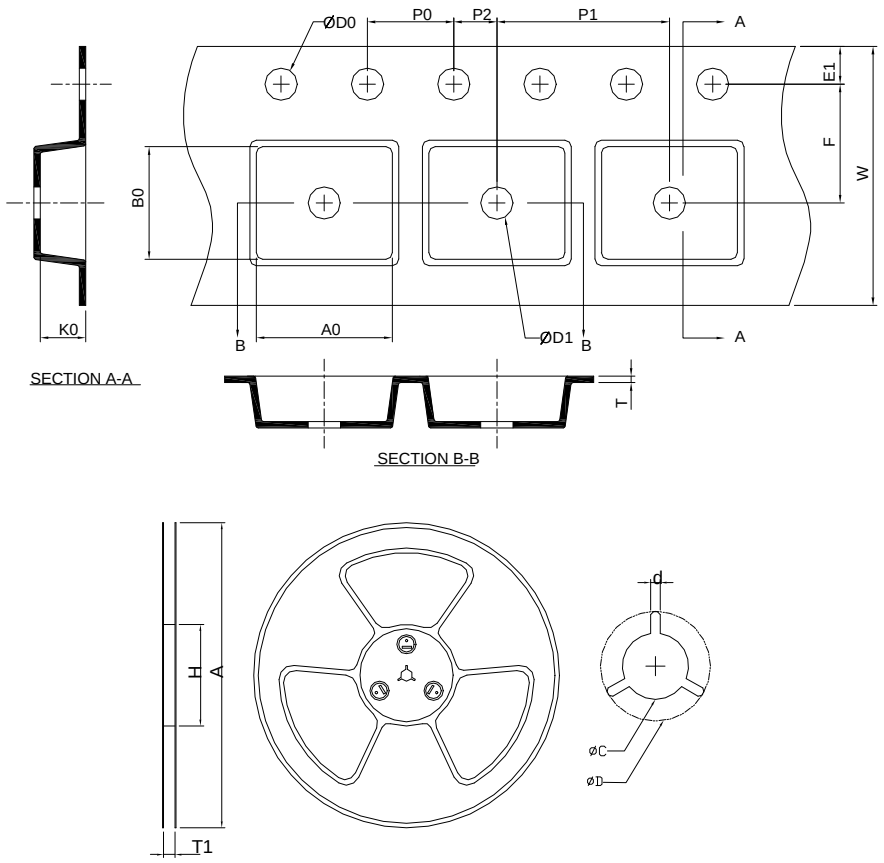
SOT-23-5



SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.016	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



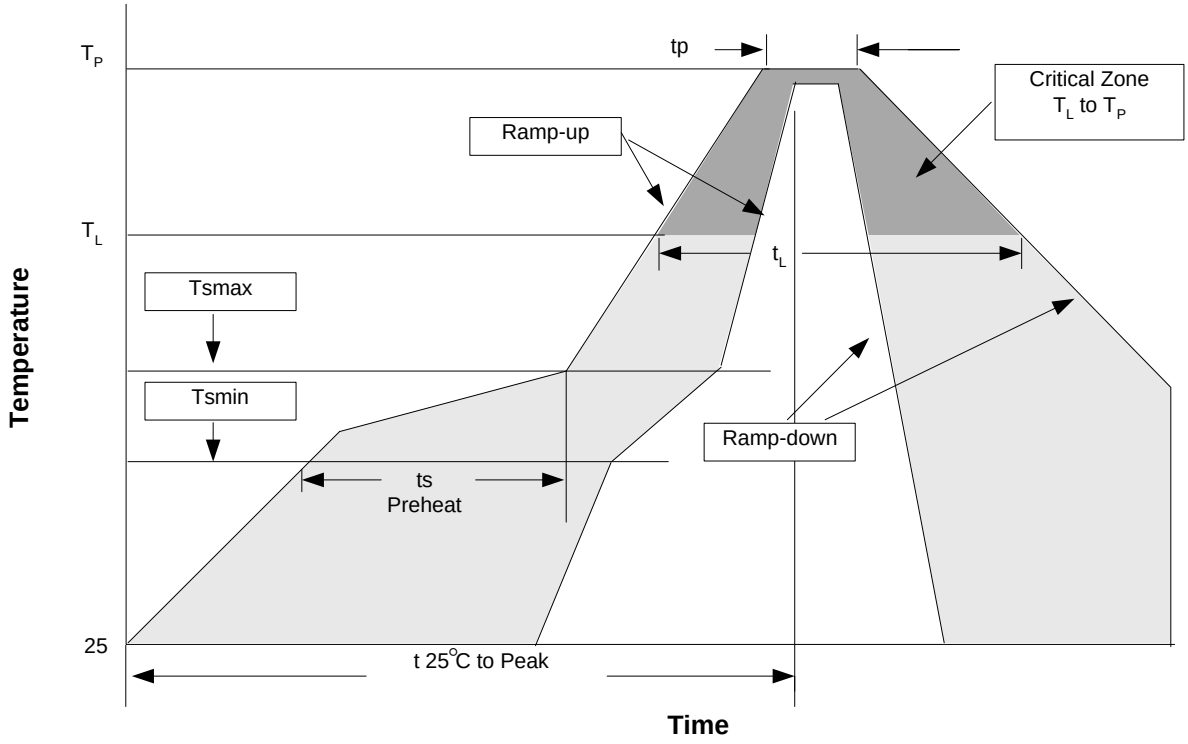
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

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