MOTOROLA

High Performance Current Mode Controllers

UC3842B, 43B
UC2842B, 43B

**HIGH PERFORMANCE
CURRENT MODE
CONTROLLERS**

The UC3842B, UC3843B series are high performance fixed frequency current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in an 8–pin dual–in–line and surface mount (SO–8) plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX843B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
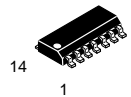- Low Startup and Operating Current

N SUFFIX
PLASTIC PACKAGE
CASE 626
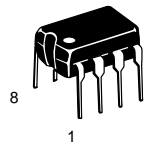
D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS

Compensation	1		8	V_{ref}
Voltage Feedback	2		7	V_{CC}
Current Sense	3		6	Output
R_T/C_T	4		5	Gnd

(Top View)

Compensation	1		14	V_{ref}
NC	2		13	NC
Voltage Feedback	3		12	V_{CC}
NC	4		11	V_C
Current Sense	5		10	Output
NC	6		9	Gnd
R_T/C_T	7		8	Power Ground

(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC384XBD		SO–14
UC384XBD1	$T_A = 0°$ to $+70°C$	SO–8
UC384XBN		Plastic
UC284XBD		SO–14
UC284XBD1	$T_A = -25°$ to $+85°C$	SO–8
UC284XBN		Plastic
UC384XBVD		SO–14
UC384XBVD1	$T_A = -40°$ to $+105°C$	SO–8
UC384XBVN		Plastic

X indicates either a 2 or 3 to define specific device part numbers.

Simplified Block Diagram

Pin numbers in parenthesis are for the D suffix SO–14 package.

Rev 1

UC3842B, 43B UC2842B, 43B

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	− 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA

Power Dissipation and Thermal Characteristics
  D Suffix, Plastic Package, SO–14 Case 751A
    Maximum Power Dissipation @ T_A = 25°C
    Thermal Resistance, Junction–to–Air
  D1 Suffix, Plastic Package, SO–8 Case 751
    Maximum Power Dissipation @ T_A = 25°C
    Thermal Resistance, Junction–to–Air
  N Suffix, Plastic Package, Case 626
    Maximum Power Dissipation @ T_A = 25°C
    Thermal Resistance, Junction–to–Air
	
	P_D
	$R_{\theta JA}$
	
	P_D
	$R_{\theta JA}$
	
	P_D
	$R_{\theta JA}$
		
		862
		145
		
		702
		178
		
		1.25
		100
			
			mW
			°C/W
			
			mW
			°C/W
			
			W
			°C/W

Operating Junction Temperature	T_J	+150	°C

Operating Ambient Temperature
  UC3842B, UC3843B
  UC2842B, UC2843B
  UC3842BV, UC3843BV
	T_A	
		0 to + 70
		− 25 to + 85
		−40 to +105
			°C

Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	− 30	− 85	−180	− 30	− 85	−180	mA
OSCILLATOR SECTION								

Frequency
  T_J = 25°C
  T_A = T_{low} to T_{high}
  T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)
	f_{OSC}	
		49
		48
		225
			
			52
			–
			250
				
				55
				56
				275
					
					49
					48
					225
						
						52
						–
						250
							
							55
							56
							275
								kHz

Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V

Discharge Current (V_{OSC} = 2.0 V)
  T_J = 25°C
  T_A = T_{low} to T_{high} (UC284XB, UC384XB)
  (UC384XBV)
	I_{dischg}	
		7.8
		7.5
		–
			
			8.3
			–
			–
				
				8.8
				8.8
				–
					
					7.8
					7.6
					7.2
						
						8.3
						–
						–
							
							8.8
							8.8
							8.8
								mA

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for UC3842B, UC3843B T_{high} = +70°C for UC3842B, UC3843B
       −25°C for UC2842B, UC2843B   +85°C for UC2842B, UC2843B
       −40°C for UC3842BV, UC3843BV   +105°C for UC3842BV, UC3843BV

UC3842B, 43B UC2842B, 43B

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB

Output Current
  Sink (V_O = 1.1 V, V_{FB} = 2.7 V)
  Source (V_O = 5.0 V, V_{FB} = 2.3 V)
	I_{Sink}
	I_{Source}
		2.0
		– 0.5
			12
			–1.0
				–
				–
					2.0
					– 0.5
						12
						–1.0
							–
							–
								mA

Output Voltage Swing
  High State (R_L = 15 k to ground, V_{FB} = 2.3 V)
  Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)
    (UC284XB, UC384XB)
    (UC384XBV)
	V_{OH}
	V_{OL}
		5.0
		
		–
		–
			6.2
			
			0.8
			–
				–
				
				1.1
				–
					5.0
					
					–
					–
						6.2
						
						0.8
						0.8
							–
							
							1.1
							1.2
								V

CURRENT SENSE SECTION								

Current Sense Input Voltage Gain (Notes 4 & 5)
  (UC284XB, UC384XB)
  (UC384XBV)
	A_V	
		2.85
		–
			
			3.0
			–
				
				3.15
				–
					
					2.85
					2.85
						
						3.0
						3.0
							
							3.15
							3.25
								V/V

Maximum Current Sense Input Threshold (Note 4)
  (UC284XB, UC384XB)
  (UC384XBV)
	V_{th}	
		0.9
		–
			
			1.0
			–
				
				1.1
				–
					
					0.9
					0.85
						
						1.0
						1.0
							
							1.1
							1.1
								V

Power Supply Rejection Ratio V_{CC} = 12 V to 25 V, Note 4	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								

Output Voltage
  Low State (I_{Sink} = 20 mA)
    (I_{Sink} = 200 mA)   (UC284XB, UC384XB)
    (UC384XBV)
  High State (I_{Source} = 20 mA) (UC284XB, UC384XB)
    (UC384XBV)
    (I_{Source} = 200 mA)
	V_{OL}
	
	V_{OH}
		–
		–
		–
		13
		–
		12
			0.1
			1.6
			–
			13.5
			–
			13.4
				0.4
				2.2
				–
				–
				–
				–
					–
					–
					–
					13
					12.9
					12
						0.1
						1.6
						1.6
						13.5
						13.5
						13.4
							0.4
							2.2
							2.3
							–
							–
							–
								V

Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								

Startup Threshold (V_{CC})
  UCX842B, BV
  UCX843B, BV
	V_{th}	
		15
		7.8
			
			16
			8.4
				
				17
				9.0
					
					14.5
					7.8
						
						16
						8.4
							
							17.5
							9.0
								V

Minimum Operating Voltage After Turn–On (V_{CC})
  UCX842B, BV
  UCX843B, BV
	$V_{CC(min)}$	
		9.0
		7.0
			
			10
			7.6
				
				11
				8.2
					
					8.5
					7.0
						
						10
						7.6
							
							11.5
							8.2
								V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
       3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
         T_{low} = 0°C for UC3842B, UC3843B T_{high} = +70°C for UC3842B, UC3843B
              –25°C for UC2842B, UC2843B   +85°C for UC2842B, UC2843B
              –40°C for UC3842BV, UC3843BV   +105°C for UC3842BV, UC3843BV
      4. This parameter is measured at the latch trip point with V_{FB} = 0 V.
      5. Comparator gain is defined as: $A_V \dfrac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$
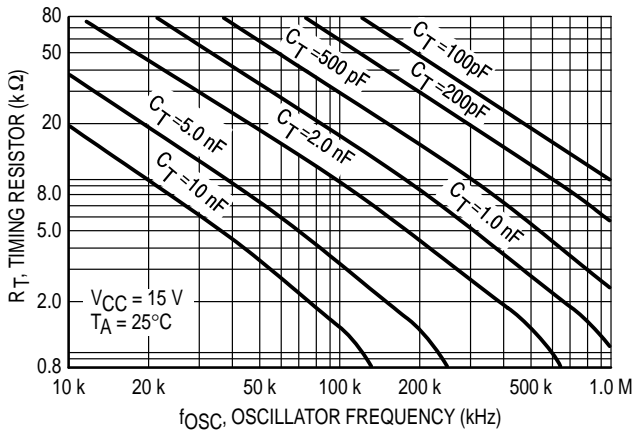
UC3842B, 43B UC2842B, 43B

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, BV			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	94	96	–	94	96	–	
(UC384XBV)		–	–	–	93	96	–	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	$I_{CC} + I_C$							mA
Startup (V_{CC} = 6.5 V for UCX843B,		–	0.3	0.5	–	0.3	0.5	
(V_{CC} 14 V for UCX842B, BV)								
Operating (Note 2)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
       3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

     T_{low} = 0°C for UC3842B, UC3843B T_{high} = +70°C for UC3842B, UC3843B
           –25°C for UC2842B, UC2843B   +85°C for UC2842B, UC2843B
           –40°C for UC3842BV, UC3843BV   +105°C for UC3842BV, UC3843BV

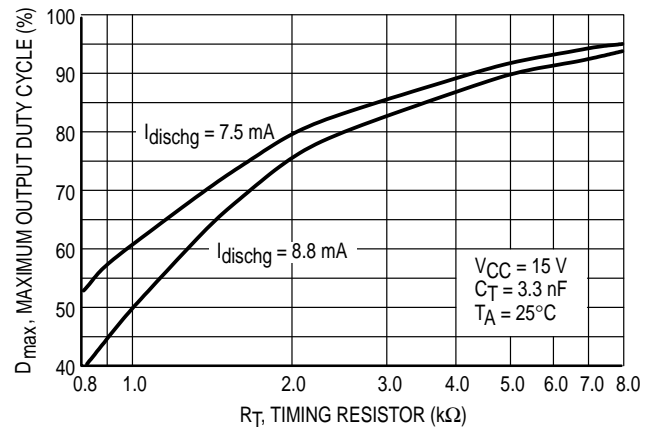**Figure 1. Timing Resistor versus Oscillator Frequency**

Figure 2. Output Deadtime versus Oscillator Frequency
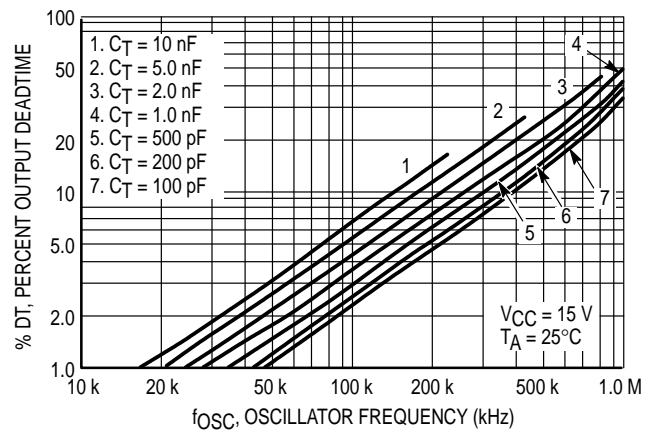
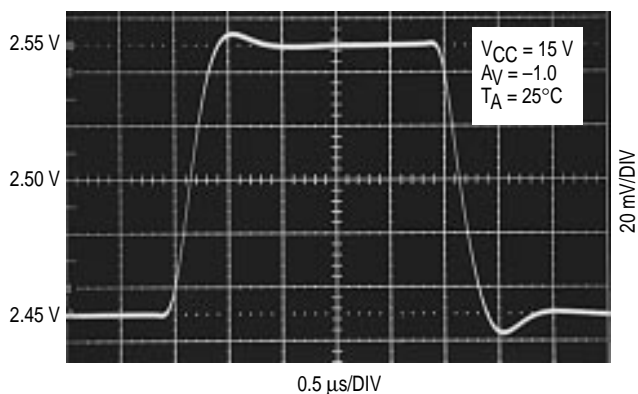**Figure 3. Oscillator Discharge Current versus Temperature**
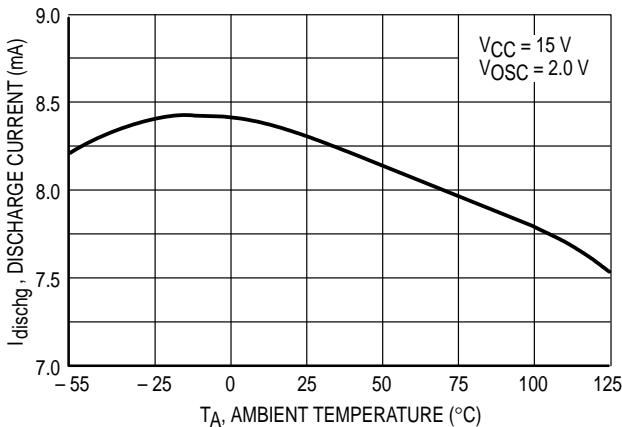
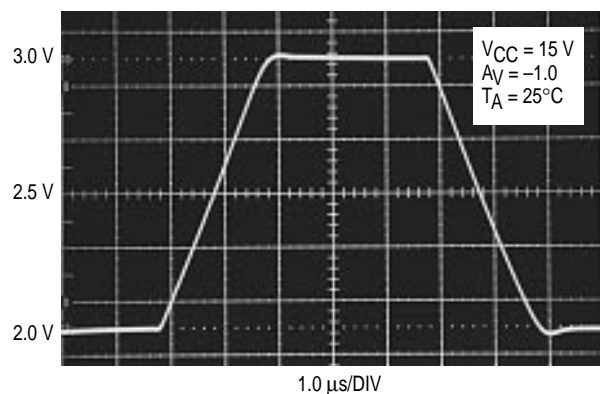**Figure 4. Maximum Output Duty Cycle versus Timing Resistor**
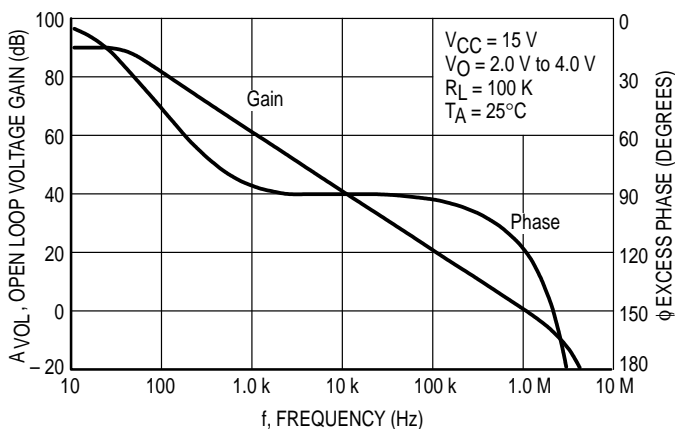
UC3842B, 43B UC2842B, 43B

Figure 5. Error Amp Small Signal Transient Response

V_{CC} = 15 V
A_V = −1.0
T_A = 25°C

20 mV/DIV

0.5 μs/DIV

Figure 6. Error Amp Large Signal Transient Response

V_{CC} = 15 V
A_V = −1.0
T_A = 25°C

1.0 μs/DIV

Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

V_{CC} = 15 V
V_O = 2.0 V to 4.0 V
R_L = 100 K
T_A = 25°C

A_{VOL}, OPEN LOOP VOLTAGE GAIN (dB)

φ EXCESS PHASE (DEGREES)

f, FREQUENCY (Hz)

Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

V_{CC} = 15 V

T_A = 25°C
T_A = 125°C
T_A = −55°C

V_{th}, CURRENT SENSE INPUT THRESHOLD (V)

V_O, ERROR AMP OUTPUT VOLTAGE (V)
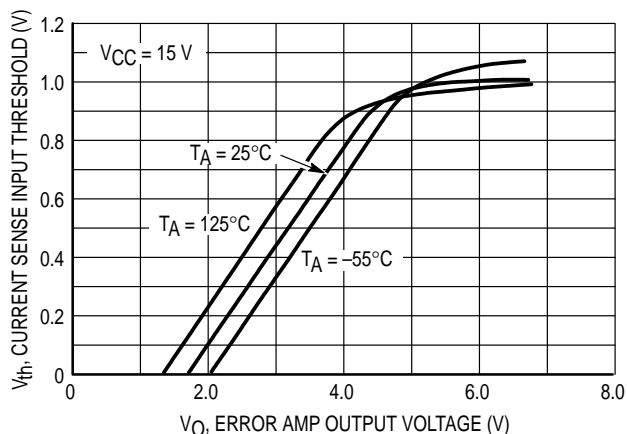
Figure 9. Reference Voltage Change versus Source Current

V_{CC} = 15 V

T_A = 125°C
T_A = −55°C
T_A = 25°C

ΔV_{ref}, REFERENCE VOLTAGE CHANGE (mV)

I_{ref}, REFERENCE SOURCE CURRENT (mA)
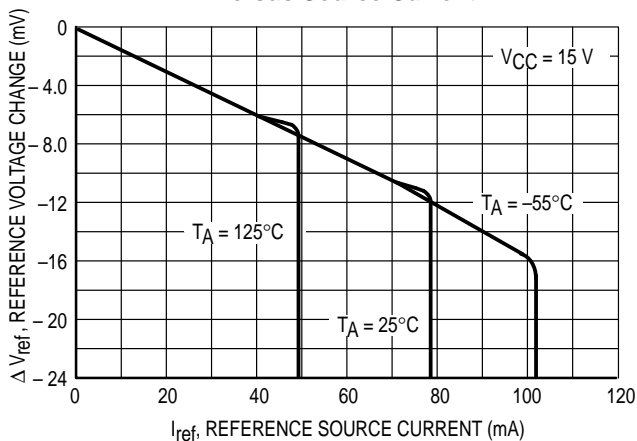
Figure 10. Reference Short Circuit Current versus Temperature

V_{CC} = 15 V
$R_L \leq 0.1 \, \Omega$

I_{SC}, REFERENCE SHORT CIRCUIT CURRENT (mA)

T_A, AMBIENT TEMPERATURE (°C)
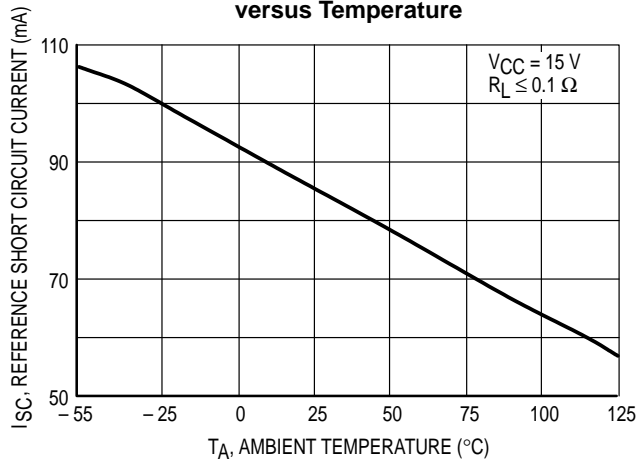
UC3842B, 43B UC2842B, 43B

Figure 11. Reference Load Regulation

Δ V$_O$, OUTPUT VOLTAGE CHANGE (2.0 mV/DIV)

V$_{CC}$ = 15 V
I$_O$ = 1.0 mA to 20 mA
T$_A$ = 25°C

2.0 ms/DIV
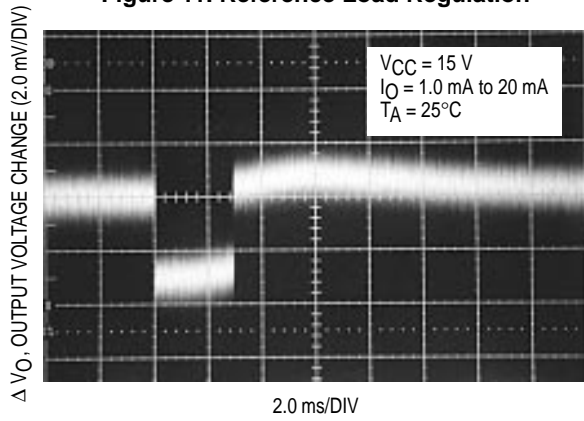
Figure 12. Reference Line Regulation

Δ V$_O$, OUTPUT VOLTAGE CHANGE (2.0 mV/DIV)

V$_{CC}$ = 12 V to 25
T$_A$ = 25°C

2.0 ms/DIV
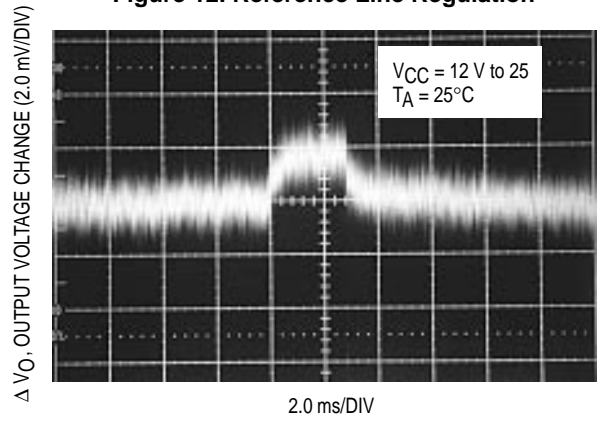
Figure 13. Output Saturation Voltage versus Load Current

V$_{sat}$, OUTPUT SATURATION VOLTAGE (V)

V$_{CC}$

Source Saturation
(Load to Ground)

V$_{CC}$ = 15 V
80 μs Pulsed Load
120 Hz Rate

T$_A$ = 25°C

T$_A$ = −55°C

T$_A$ = −55°C

T$_A$ = 25°C

Sink Saturation
(Load to V$_{CC}$)

Gnd

I$_O$, OUTPUT LOAD CURRENT (mA)
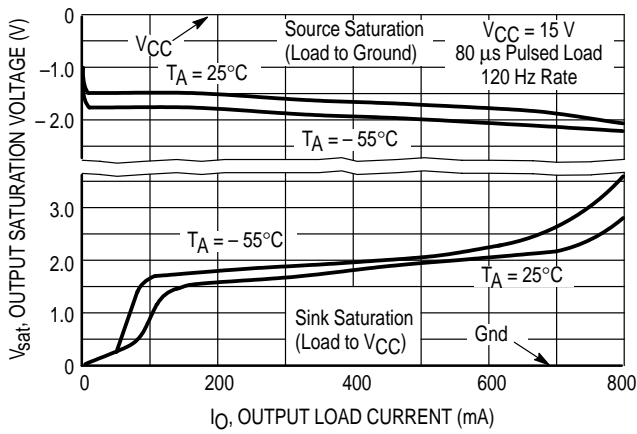
Figure 14. Output Waveform

90%

10%

V$_{CC}$ = 15 V
C$_L$ = 1.0 nF
T$_A$ = 25°C

50 ns/DIV
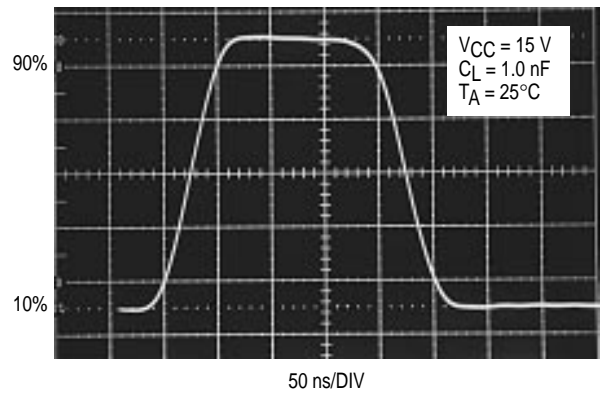
Figure 15. Output Cross Conduction

V$_O$, OUTPUT VOLTAGE

I$_{CC}$, SUPPLY CURRENT

V$_{CC}$ = 30 V
C$_L$ = 15 pF
T$_A$ = 25°C

20 V/DIV

100 mA/DIV

100 ns/DIV
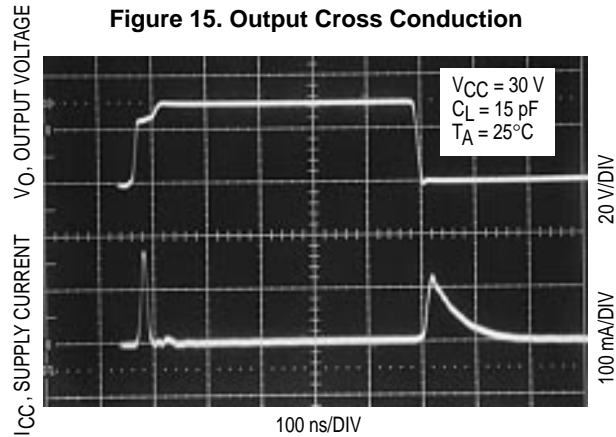
Figure 16. Supply Current versus Supply Voltage

I$_{CC}$, SUPPLY CURRENT (mA)

UCX843B

UCX842B

R$_T$ = 10 k
C$_T$ = 3.3 nF
V$_{FB}$ = 0 V
I$_{Sense}$ = 0 V
T$_A$ = 25°C

V$_{CC}$, SUPPLY VOLTAGE (V)
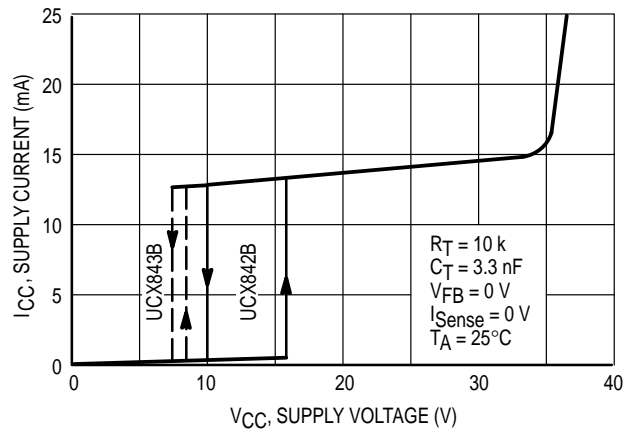
UC3842B, 43B UC2842B, 43B

PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

UC3842B, 43B UC2842B, 43B
OPERATING DESCRIPTION

The UC3842B, UC3843B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise–sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi–unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The non–inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the non–inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842B, UC3843B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V(Pin\ 1) - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 26).

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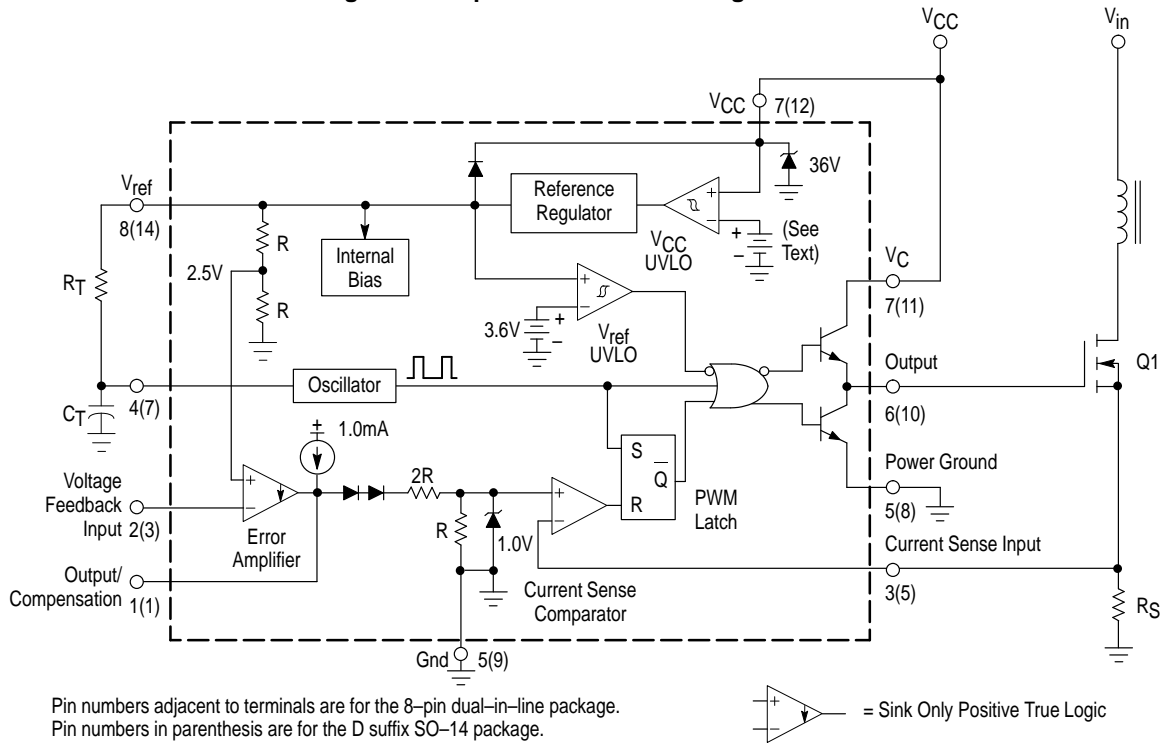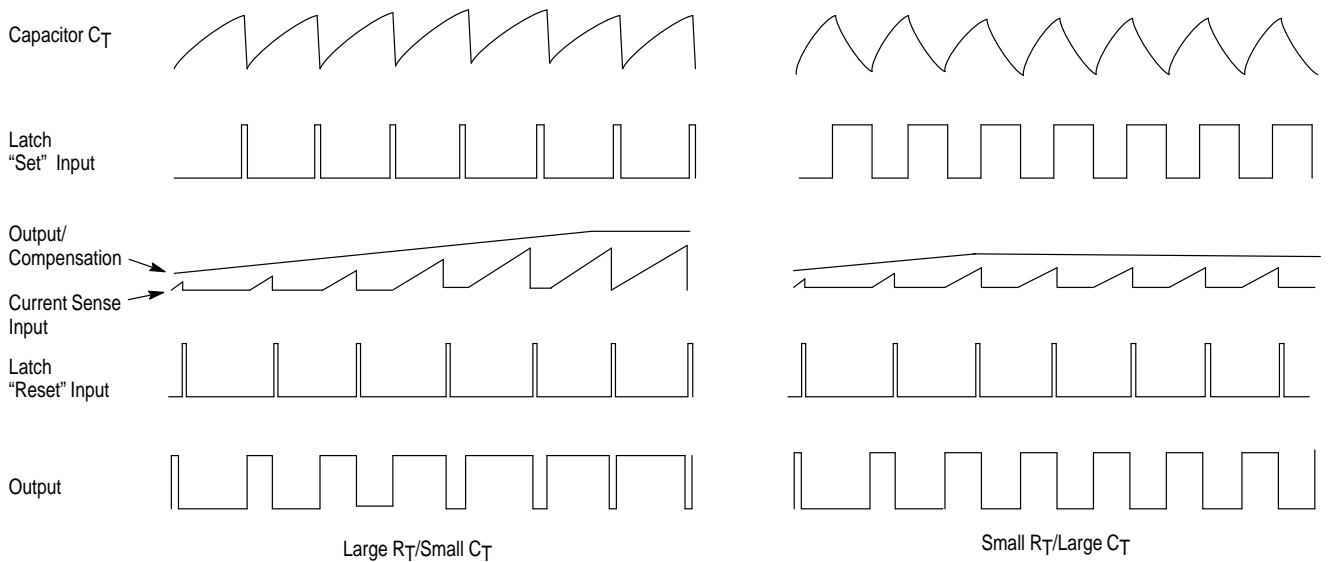**Figure 17. Representative Block Diagram**

Pin numbers adjacent to terminals are for the 8–pin dual–in–line package.
Pin numbers in parenthesis are for the D suffix SO–14 package.

= Sink Only Positive True Logic

Figure 18. Timing Diagram

Capacitor C_T

Latch "Set" Input

Output/Compensation

Current Sense Input

Latch "Reset" Input

Output

Large R_T/Small C_T

Small R_T/Large C_T

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Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842B, and 8.4 V/7.6 V for the UCX843B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX842B makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 33). The UCX843B is intended for lower voltage dc–to–dc converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage (V_{CC}) for the UCX842B is 11 V and 8.2 V for the UCX843B.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 25 shows proper power and control ground connections in a current–sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short–circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise–generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn–on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I\, m_2/m_1)\,(m_2/m_1)$. This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn–on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).
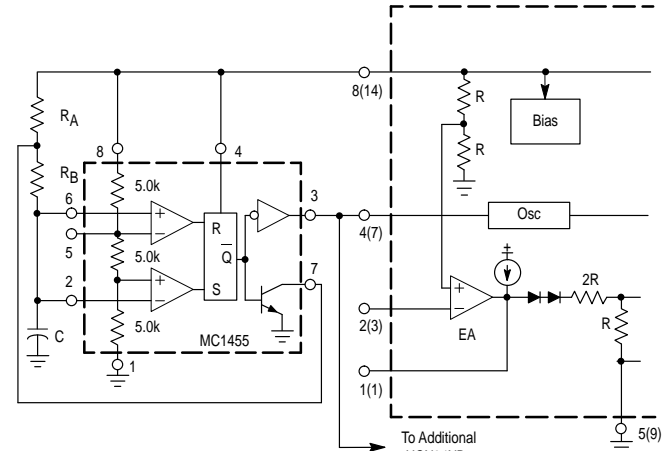
Figure 19. Continuous Current Waveforms
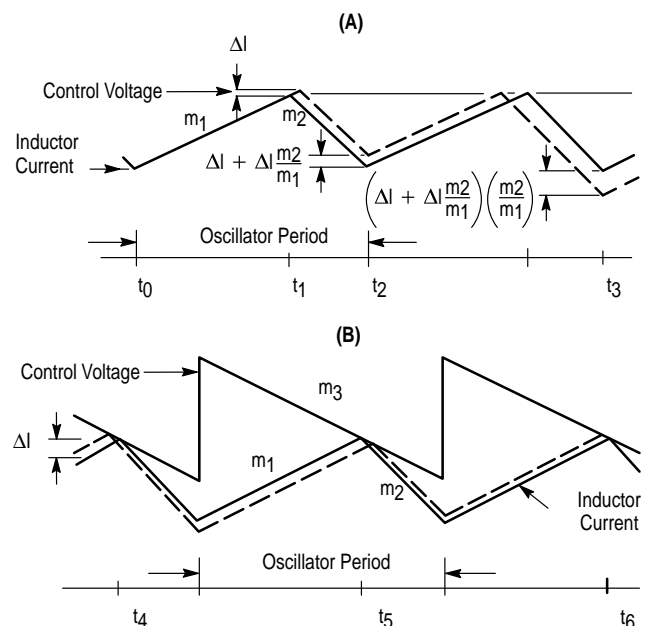
Figure 20. External Clock Synchronization
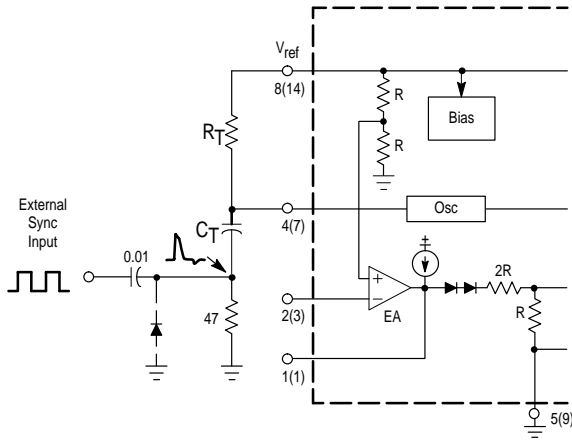
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.
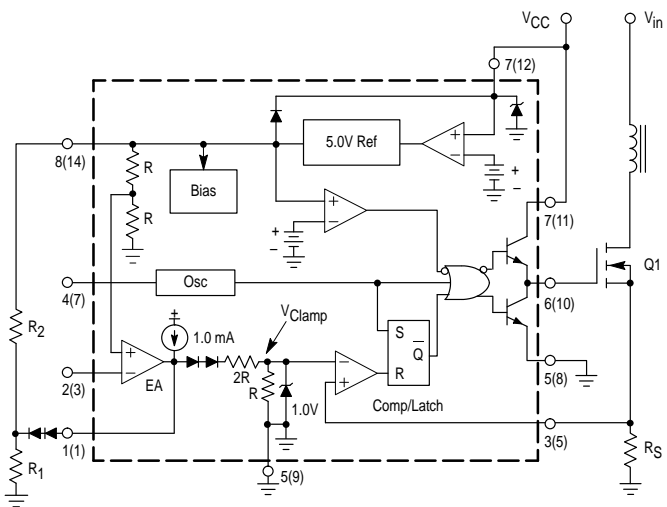
Figure 21. External Duty Cycle Clamp and Multi–Unit Synchronization

$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{(max)} = \frac{R_B}{R_A + 2R_B}$$
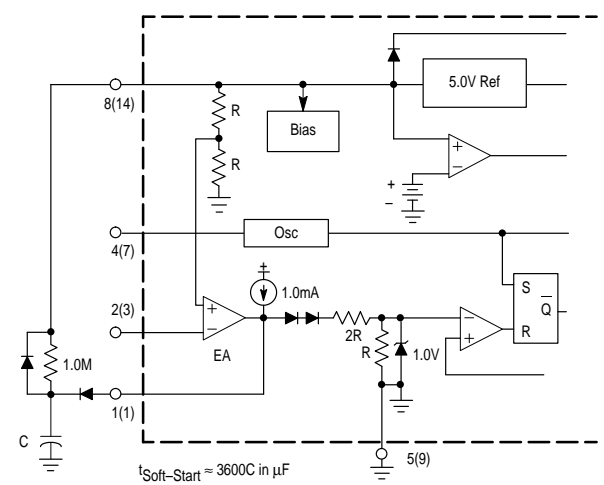
Figure 22. Adjustable Reduction of Clamp Level

$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad \text{Where: } 0 \leq V_{Clamp} \leq 1.0 \text{ V}$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 23. Soft–Start Circuit

$$t_{Soft-Start} \approx 3600C \text{ in } \mu F$$

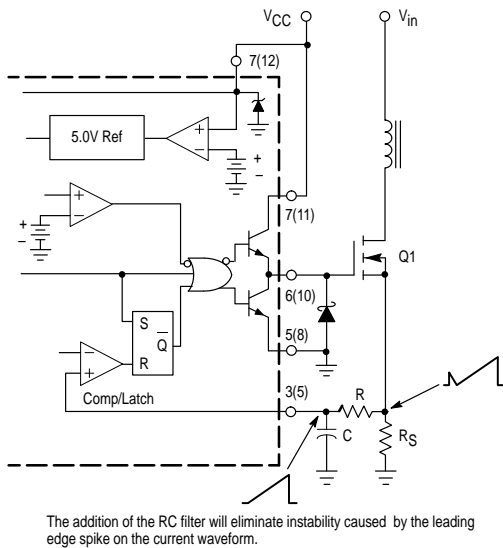**Figure 24. Adjustable Buffered Reduction of Clamp Level with Soft–Start**

$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)} \qquad \text{Where: } 0 \le V_{Clamp} \le 1.0 \text{ V}$$

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{VC}{3\,V_{Clamp}}\right] C \frac{R1\,R2}{R1 + R2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$
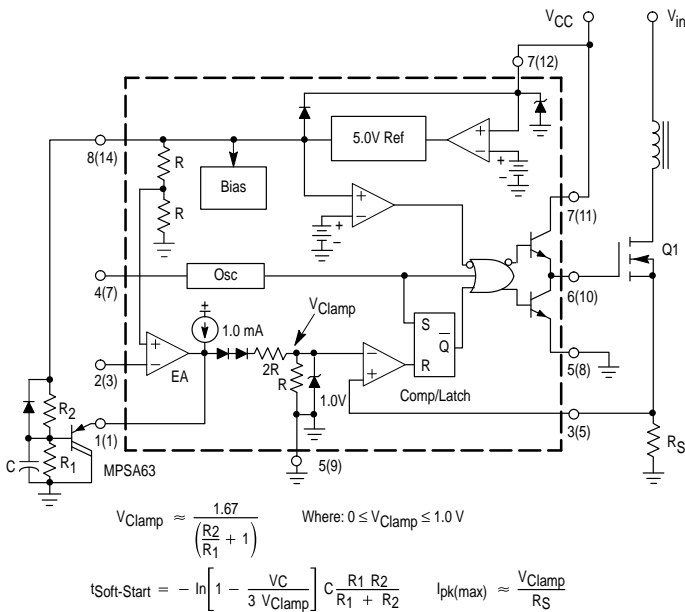
Figure 25. Current Sensing Power MOSFET

$$V_{Pin\,5} \approx \frac{R_S\,I_{pk}\,r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
$R_S = 200$

Then : $V_{Pin\,5} \approx 0.075\,I_{pk}$
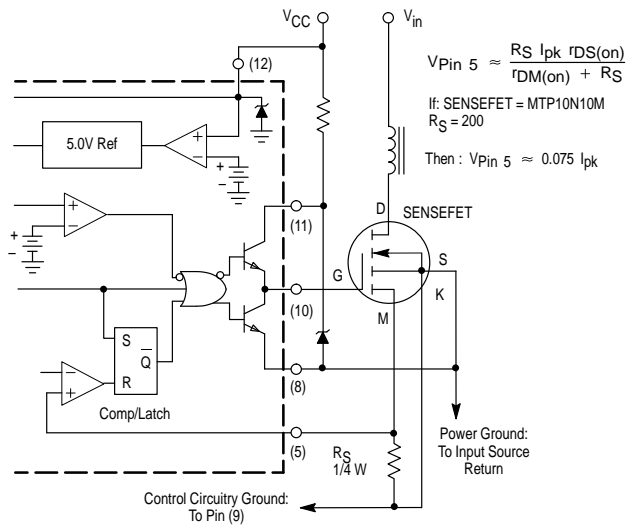
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over–current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

Figure 26. Current Waveform Spike Suppression

The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. MOSFET Parasitic Oscillations

Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.
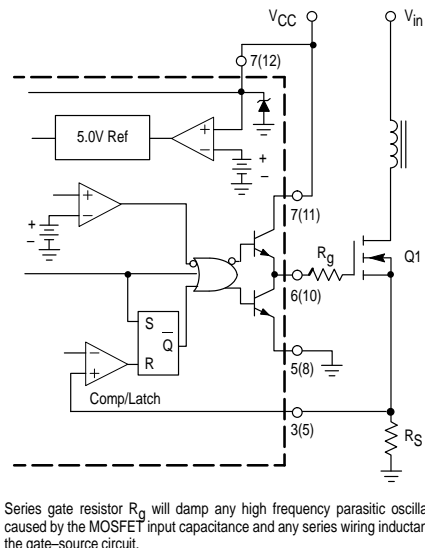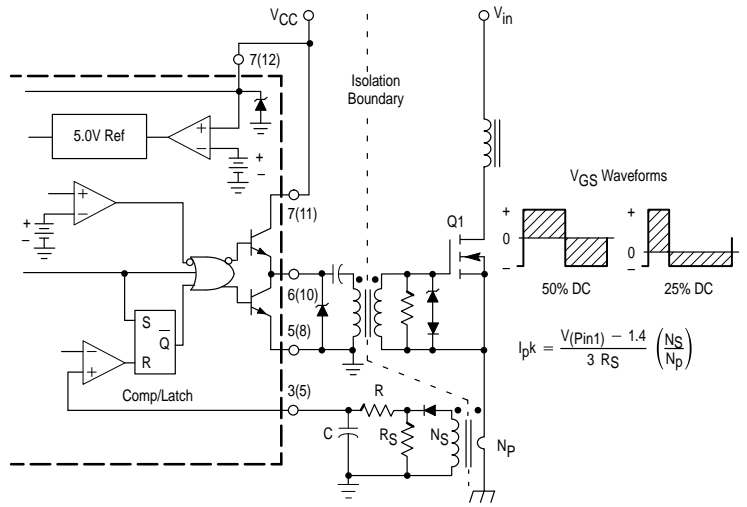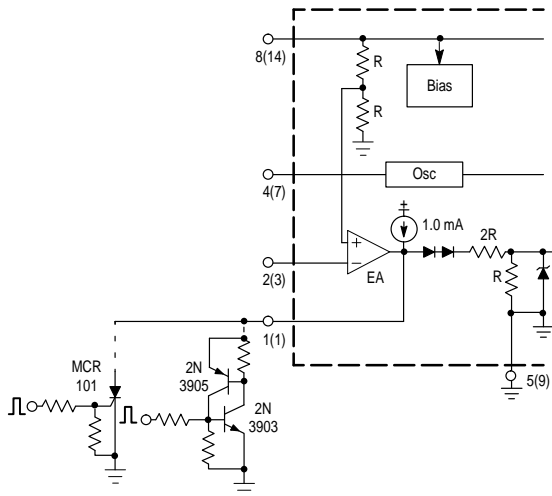
Figure 28. Bipolar Transistor Drive
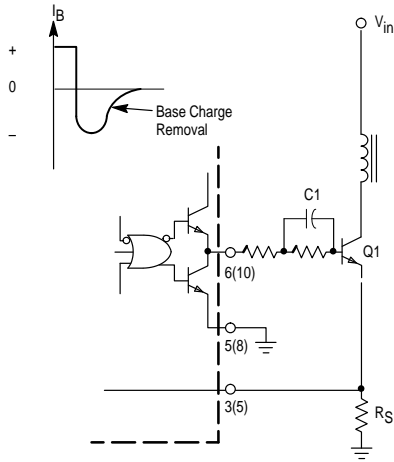
The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

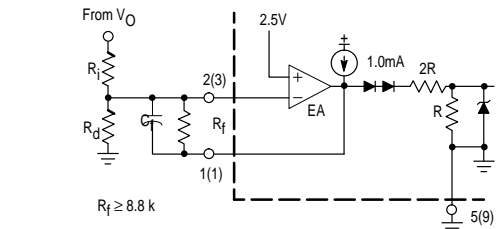**Figure 29. Isolated MOSFET Drive**

$$I_{pk} = \frac{V(Pin1) - 1.4}{3\ R_S}\left(\frac{N_S}{N_p}\right)$$

Figure 30. Latched Shutdown

The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

**Figure 31. Error Amplifier Compensation**

$R_f \geq 8.8$ k

Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.
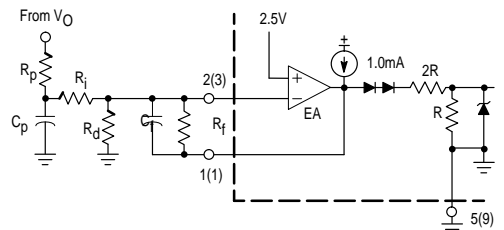
Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.
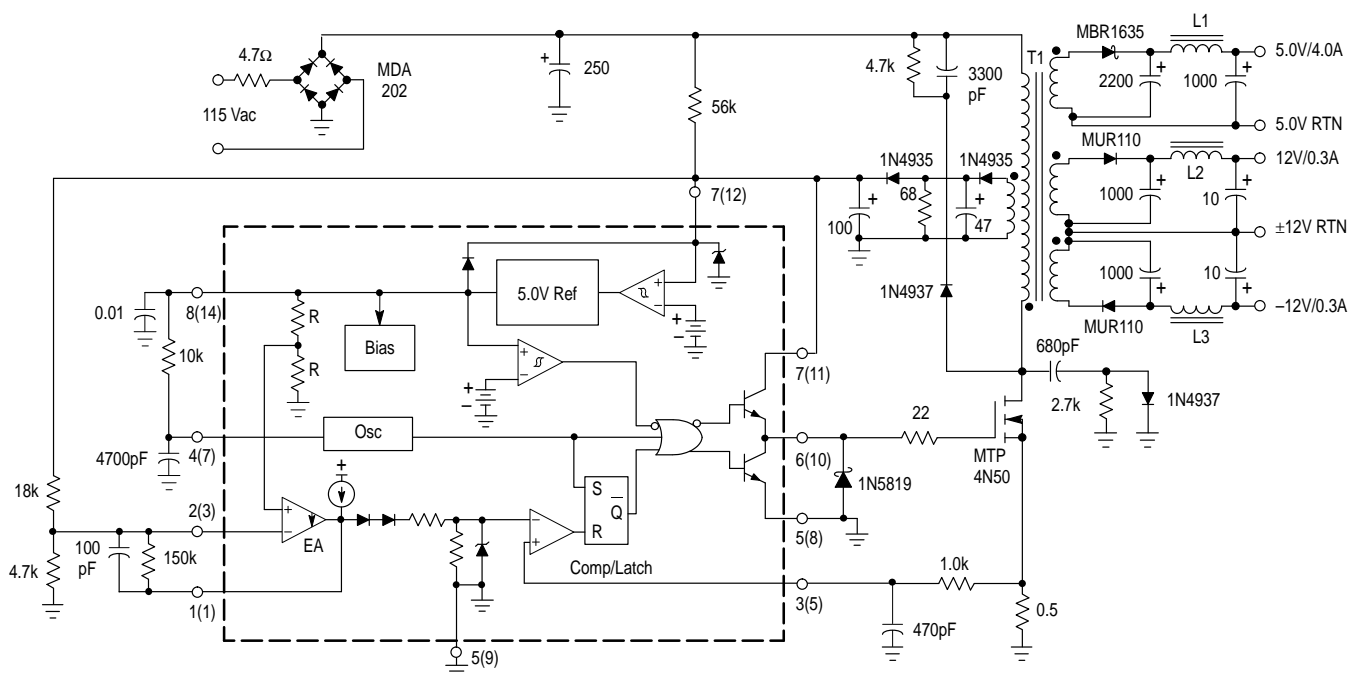
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Figure 32. Slope Compensation
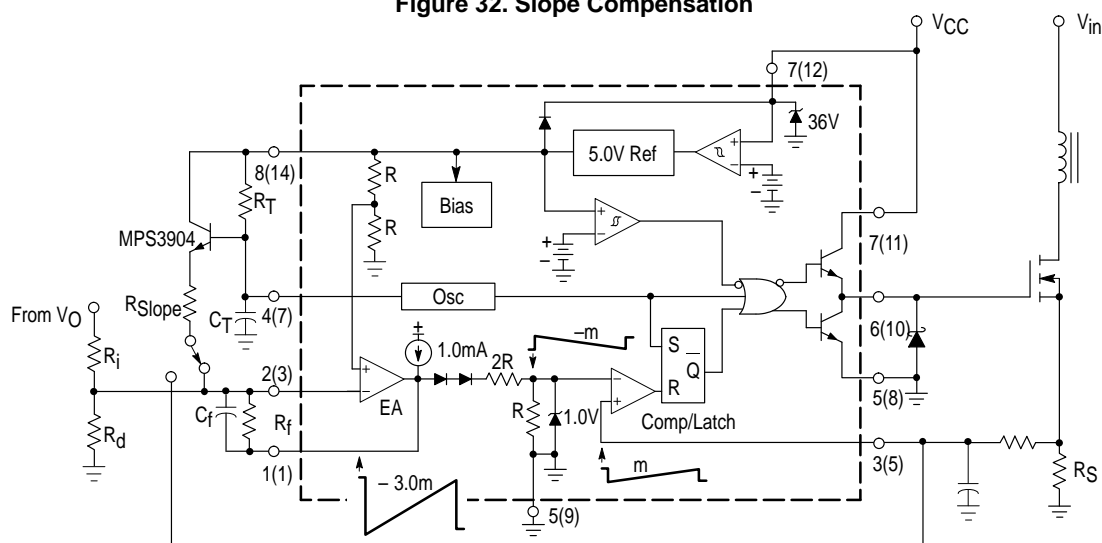
The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.
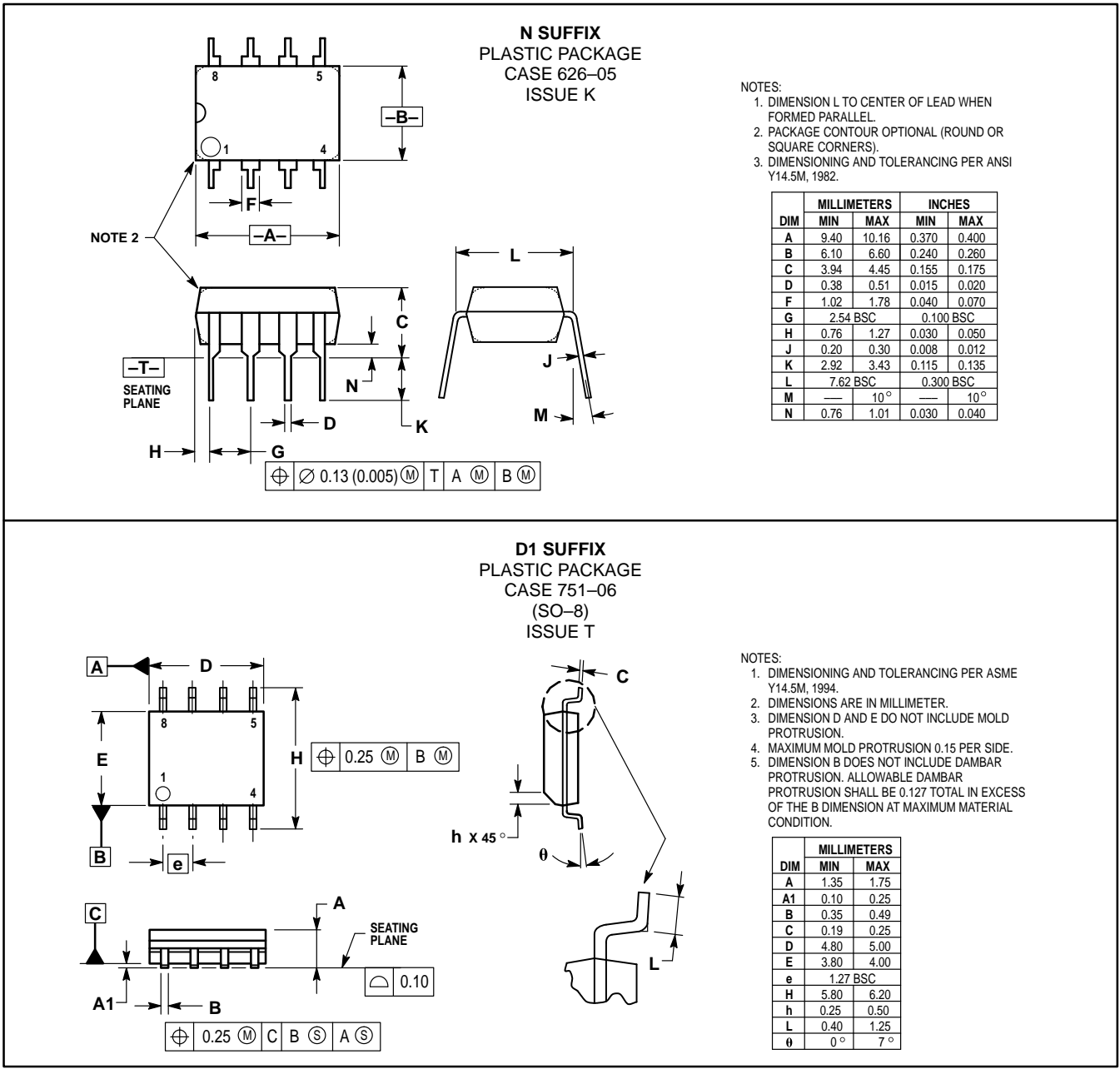
Figure 33. 27 W Off–Line Flyback Regulator

L1 – 15 μH at 5.0 A, Coilcraft Z7156
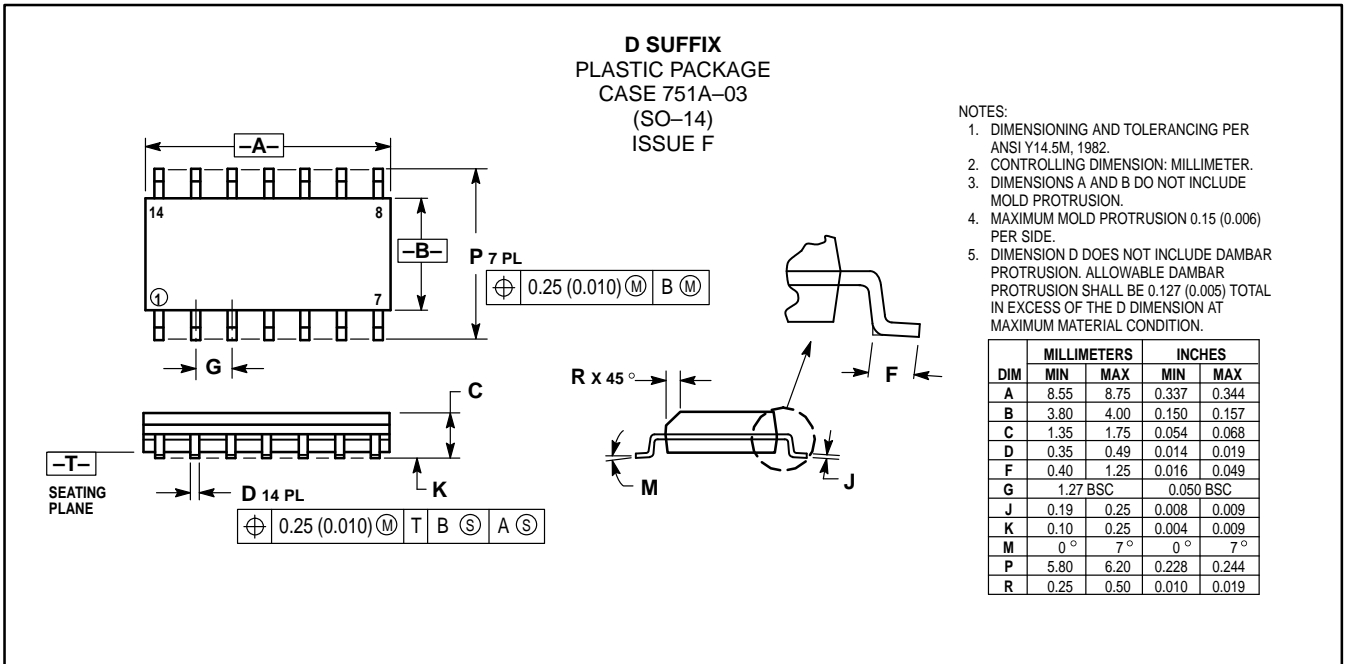L2, L3 – 25 μH at 5.0 A, Coilcraft Z7157

T1 – Primary: 45 Turns #26 AWG
   Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
   Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
   Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
   Core: Ferroxcube EC35–3C8
   Bobbin: Ferroxcube EC35PCB1
   Gap: ≈ 0.10" for a primary inductance of 1.0 mH

Test		Conditions	Results
Line Regulation:	5.0 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ± 0.5%
	±12 V		Δ = 24 mV or ± 0.1%
Load Regulation:	5.0 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A	Δ = 300 mV or ± 3.0%
	±12 V	V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 60 mV or ± 0.25%
Output Ripple:	5.0 V	V_{in} = 115 Vac	40 mV$_{pp}$
	±12 V		80 mV$_{pp}$
Efficiency		V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted

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UC3842B, 43B UC2842B, 43B

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K

NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D1 SUFFIX
PLASTIC PACKAGE
CASE 751–06
(SO–8)
ISSUE T

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

UC3842B, 43B UC2842B, 43B
OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

MOTOROLA

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