High Power Factor Flyback PWM Controller

FEATURES

- **Built-in Soft Start**
- **Very Low Startup Current**
- **Under Voltage Lockout with 7.7V Hysteresis**
- **VCC Over Voltage Protection (OVP)**
- **Clear External EA Feedback Network before Power On**
- **Transition Mode (TM) Operation**
- **Highly Linear Analog Multiplier**
- **Proprietary "Frequency Adjusting" for Higher PF and Low THD**
- **3.3us Min. OFF Time**
- **270KHz Max Frequency Clamp**
- **Trimmed 1.5% Internal Voltage Reference**
- **Restart Timer for Stand-alone Applications**
- **Cycle-by-Cycle Current Limiting**
- **Built-in Leading Edge Blanking (LEB)**
- **Audio Noise Free Operation**
- **10V to 32V Wide Range of VCC Voltage**
- **800mA Drive Capability**

APPLICATIONS

- **LED Lighting Application**
- **Single Stage High PF Flyback AC/DC SMPS**

GENERAL DESCRIPTION

SFL320 is a high power factor flyback PWM controller special for LED lighting applications. The IC adopts transition mode (TM) operation for high efficiency and low EMI.

SFL320 will ***Clear External EA Feedback Network*** before IC power on. The IC also has ***Soft Start*** control to soften the stress on the MOSFET during power on period.

In SFL320, a highly linear analog multiplier is integrated to achieve low THD and high power factor. The zero current detector (ZCD) ensures TM operation. A restart timer is for stand alone applications. The IC also has the function of ***Min. OFF time*** and ***Max. Frequency Clamp*** to limits power MOS Vds spike when LED output is short.

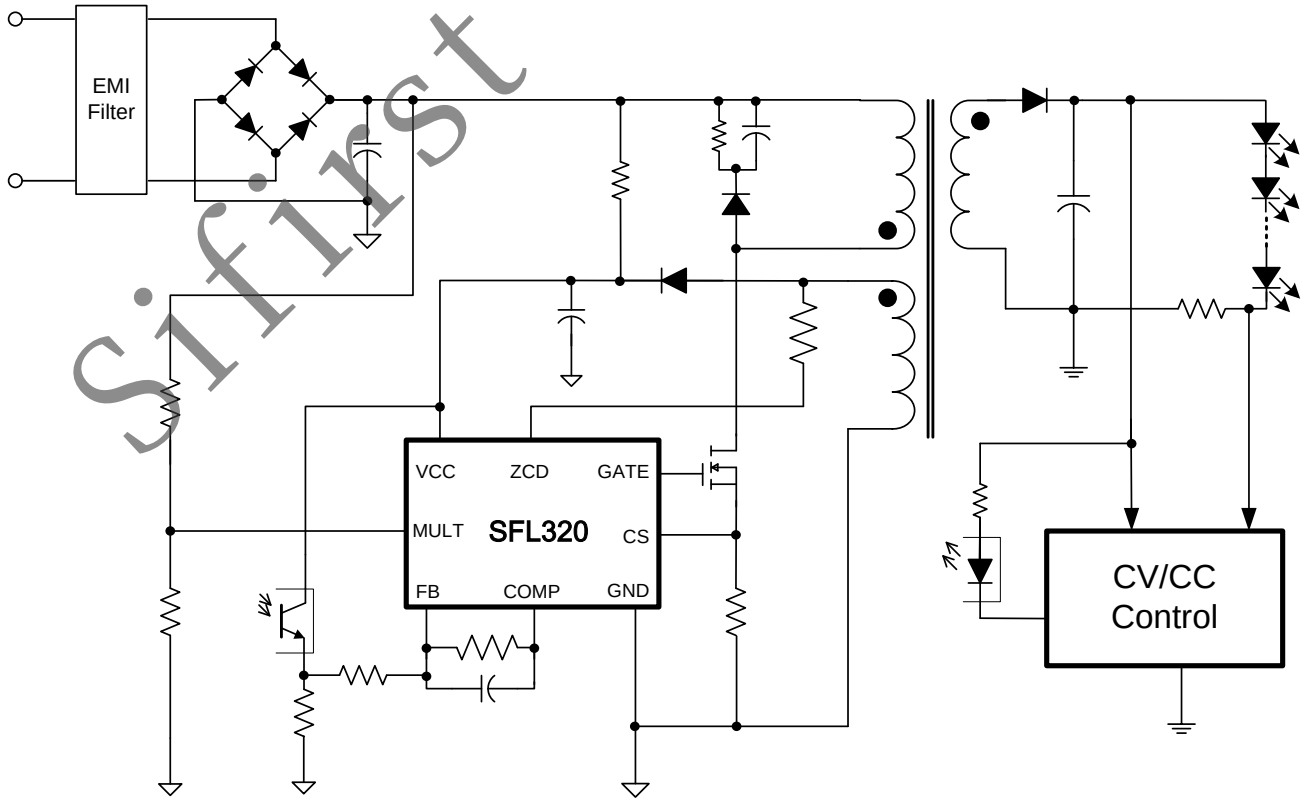
In SFL320, the proprietary "***Frequency Adjusting***" can help to improve THD performance, while ensures audio noise free operation. A ***VCC Over Voltage Protection*** (VCC OVP) is integrated to improve system reliability.

SFL320 integrates functions and protections of Under Voltage Lockout (UVLO), VCC Over Voltage Protection (OVP), Soft Start Control, Cycle-by-cycle Current Limiting (OCP), GD Clamping, VCC Clamping, Leading Edge Blanking (LEB), etc.

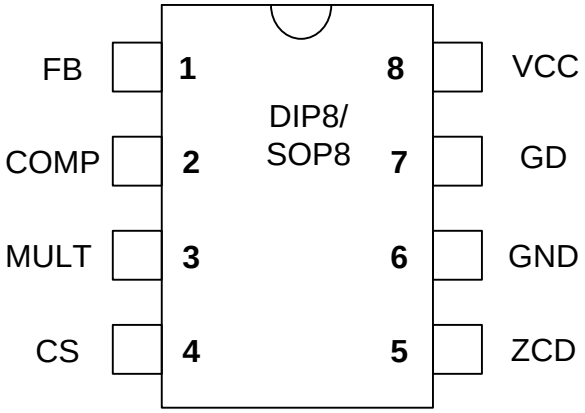
In SFL320, VCC OVP is auto-recovery mode protection.

SFL320 is available in SOP-8 and DIP-8 packages.

TYPICAL APPLICATION



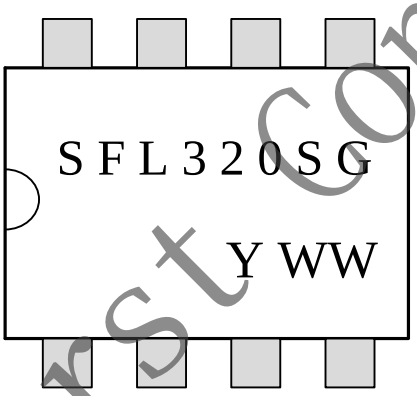
Pin Configuration



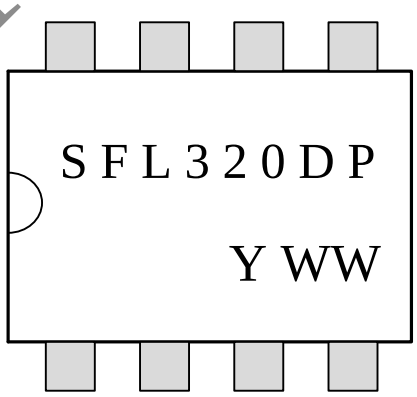
Ordering Information

Part Number	Top Mark	Package		Tape & Reel
SFL320SG	SFL320SG	SOP8	Green	
SFL320SGT	SFL320SG	SOP8	Green	Yes
SFL320DP	SFL320DP	DIP8	RoHS	

Marking Information

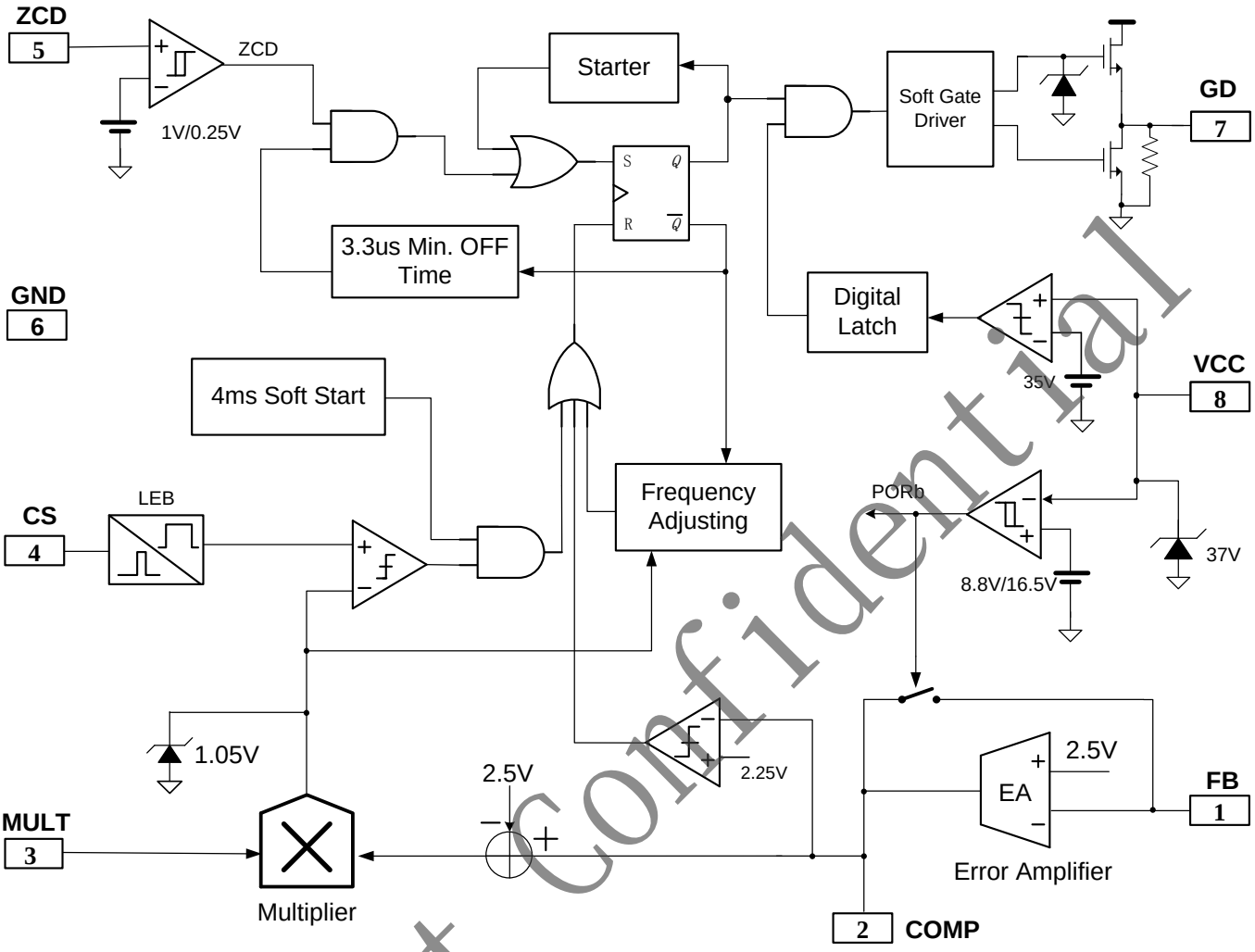


YWW: Year&Week code



YWW: Year&Week code

Block Diagram



Pin Description

Pin Num	Pin Name	I/O	Description
1	FB	I	Inverting input of the error amplifier. Before power on, this pin is internally shorted to COMP pin to clear external feedback network.
2	COMP	O	Output of the error amplifier. A feedback network is placed between this pin and pin 1. The voltage of COMP and pin CS generates PWM duty cycle.
3	MULT	I	Input to the multiplier stage. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	I	Current sense input pin.
5	ZCD	I	Zero current detection input. A negative going edge triggers a new switching cycle. If it is connected to GND, the operation will be disabled.
6	GND	P	IC ground pin.
7	GD	O	Totem-pole gate driver output to drive the external MOSFET.
8	VCC	P	IC power supply pin.

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VCC DC Supply Voltage	37	V
VCC DC Clamp Current	10	mA
GD pin	20	V
FB, COMP, MULT, CS, voltage range	-0.3 to 7	V
ZCD Pin Max. Sink/Source Current	50(source) /10(sink)	mA
Package Thermal Resistance (DIP-8)	90	^{o}C/W
Package Thermal Resistance (SOP-8)	150	^{o}C/W
Maximum Junction Temperature	150	^{o}C
Operating Temperature Range	-40 to 85	^{o}C
Storage Temperature Range	-65 to 150	^{o}C
Lead Temperature (Soldering, 10sec.)	260	^{o}C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VCC	10 to 32	V
Operating Ambient Temperature	-40 to 85	^{o}C

ELECTRICAL CHARACTERISTICS

(T_A = 25^{O}C, VCC=14.5V if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VCC Pin)						
Ivcc_Startup	VCC Start up Current	VCC=11V, Measure current into VCC		5	15	uA
UVLO(ON)	VCC Under Voltage Lockout Exit (Startup)		15.5	16.5	17.5	V
UVLO(OFF)	VCC Under Voltage Lockout Enter		8.0	8.8	9.6	V
UVLO(Hys)	UVLO Hysteresis	UVLO(ON)-UVLO(OFF)		7.7		V
VCC_OVP	VCC Over Voltage Protection trigger		33	35	37	V
VCC_Clamp	VCC Zener Clamp Voltage	I(VCC) = 5mA	35	37	39	V
I_VCC_Op	Operation Current	@70KHz, GD=1nF		4	5.5	mA
I_VCC_quiet	Quiescent Current	No Switching		3	4	mA
T_Softstart	Soft Start Time			4		mSec
Error Amplifier Section (FB and COMP Pin)						
V_{FBREF}	Voltage Feedback Input Threshold		2.45	2.500	2.55	V
ΔV_{FB_line}	Line Regulation	10V<VCC<32V		4	10	mV
ΔV_{FB_Temp}	Temperature Stability	-40^{O}C <T_A <125^{O}C		13		mV
G_V	Voltage Gain	Note 3	60	80		dB
GBW	Unit Gain Bandwidth	Note 3		1.2		MHz
I_{COMP}_source	Source Current	V_{COMP}=3.6V, V_{INV}=2.4V	-2	-4.8	-10	mA
I_{COMP}_sink	Sink Current	V_{COMP}=3.6V, V_{INV}=2.6V	-2	-4.8		mA
V_{COMP}_Clamp_U	Upper Clamp Voltage	I_{COMP} (source)=0.5mA		5.4		V
V_{COMP}_min_duty	COMP under voltage gate clock is off			2.3		V
Multiplier Section (MULT Pin)						
Vmult	Linear Operating Range		0~3.5			V
K	Multiplier Gain	V_{MULT}=1V, V_{COMP}=4V	0.32	0.38	0.44	1/V
ΔVcs/ ΔVmult	Output Max. Slope	V_{MULT}=from 0 to 0.5V, V_{COMP}=Upper Clamp	0.95	1.1		V/V

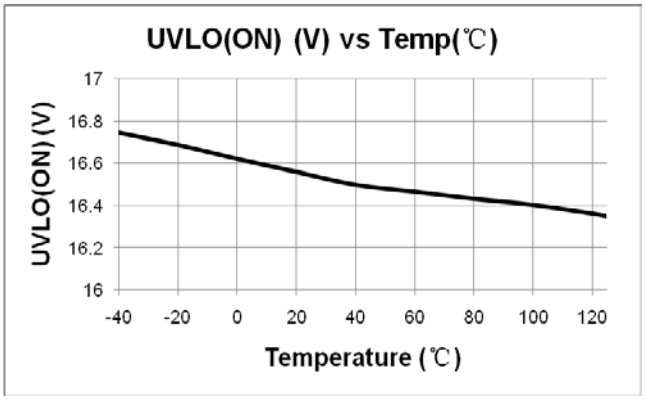
		Voltage				
Current Sense Section (CS Pin)						
V_{CS}_clamp	Current Sense Reference Clamp		0.95	1.05	1.1	V
T_blanking	CS Input Leading Edge Blanking Time			250		nSec
T_D_OC	Over Current Detection and Control Delay	CL=1nF at GD,		100		nSec
Zero Current Detection (ZCD Pin)						
Vzcd_H	Upper Clamp Voltage	Izcd=2.5mA	5.4	6	6.6	V
Vzcd_L	Lower Clamp Voltage	Izcd=-2.5mA		0		V
V_{ZCDA}	Arming Voltage (Positive going edge)			0.7		V
V_{ZCDT}	Triggering Voltage (Negative going edge)			0.25		V
T_{min}_OFF	Minimum OFF time	Note 3		3.3		uSec
I_{ZCD}_source	Source Current Capability		-2.5		-5	mA
I_{ZCD}_sink	Sink Current Capability	Note 3	3			mA
Starter and Max Switching Frequency Limitation Section						
T_{start}	Start Timer Period		45	55	65	us
f_{sw}_max	Max switching frequency			270		KHz
Gate Drive Section (GD Pin)						
VOL	Output Low Level	Io = 100 mA (sink)			1.5	V
VOH	Output High Level	Io = 100 mA (source)	8			V
GD_Clamp	Output Clamp Voltage Level	VCC=24V		16		V
T_r	Output Rising Time	GD = 1nF		50		nSec
T_f	Output Falling Time	GD = 1nF		30		nSec

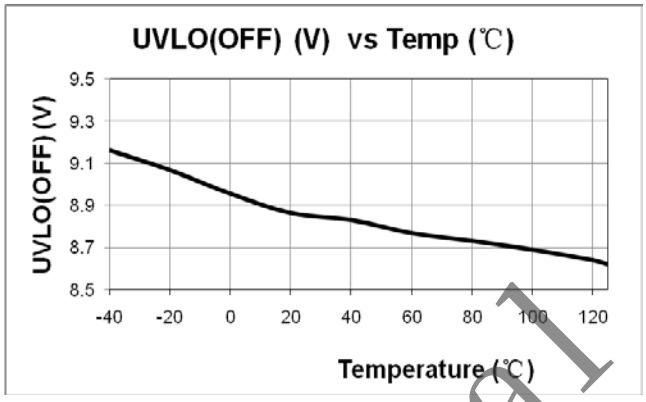
Note 1. Stresses beyond those listed under **"**Absolute Maximum Ratings**"** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

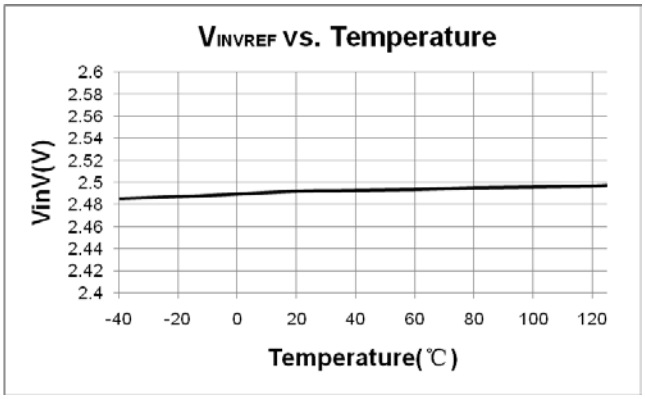
Note 2. The device is not guaranteed to function outside its operating conditions.

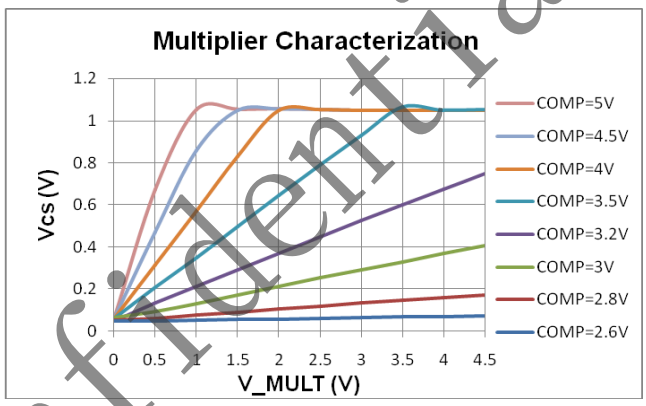
Note 3. Guaranteed by design.

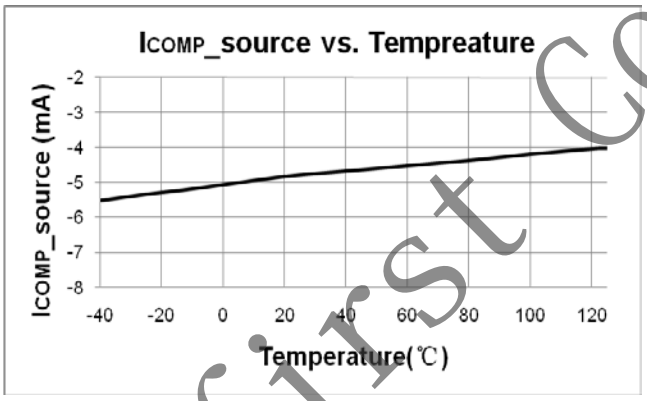
CHARACTERIZATION PLOTS

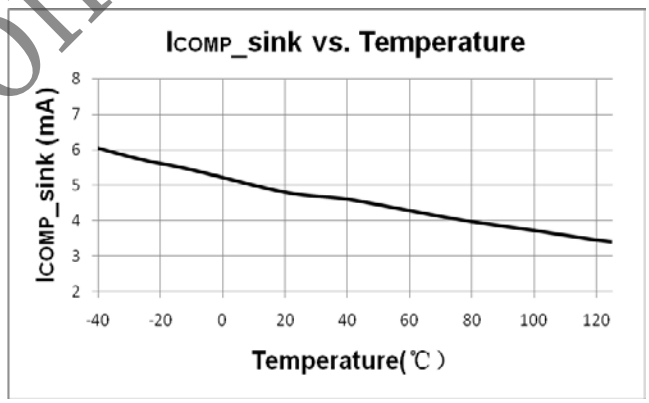


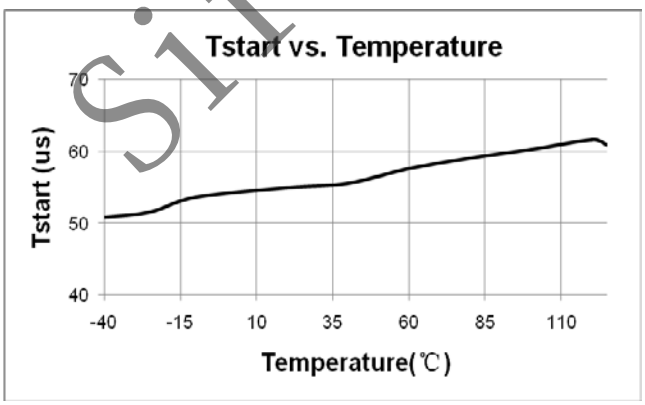


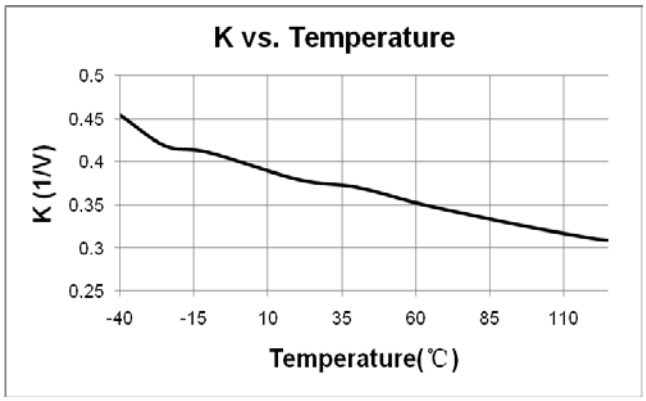












OPERATION DESCRIPTION

SFL320 is a high performance, high power factor flyback PWM controller special for LED lighting applications. The built-in high level protection features improves the system reliability and performance without increasing the system cost.

◆ UVLO (with 7.7V Hysteresis) and 5uA Startup Current

Fig.1 shows a typical startup circuit. Before the IC begins switching operation, it consumes only startup current (typically 5uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 16.5V(typical), SFL320 begins switching and the IC current consumed increased to 3mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 8.8V). The selection of Rst and Cdd should be a trade off between the power loss and startup time.

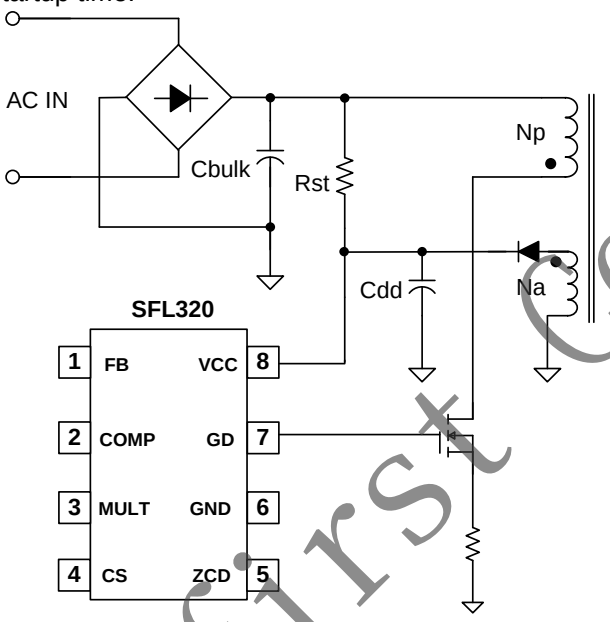


Fig.1

◆ Low Operating Current

The operating current in SFL320 is as small as 3mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ 4ms Soft Start

SFL320 features an internal 4ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

◆ Error Amplifier

The inverting input of the EA is compared to an internal reference voltage (2.5V) to determine COMP voltage. An external loop compensation network is placed between COMP and FB. .
When COMP voltage is below 2.25V, PWM cycle will stop.

◆ Clear External EA Feedback Network

SFL320 features a control that clear the external EA feedback network before IC power on, as shown in Fig.2. This control can ensure the system start up softly by clearing the residue voltage on C1 and reduce the output LED current spike when system does the ON/OFF testing.

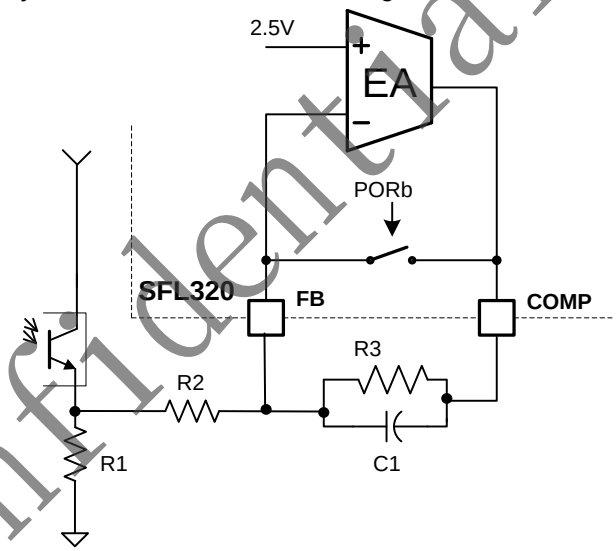


Fig.2

◆ Analog Multiplier for Power Factor Correction

The analog multiplier output limits the MOSFET peak current with respect to the AC half wave rectified input voltage. By controlling the CS comparator threshold as the AC line voltage traverses sinusoidally from zero to peak line voltage, the load appears to be resistive to the AC line. The multiplier in SFL320 has two inputs. One is the error amplifier (EA) output voltage (V_{COMP}), while the other is V_{MULT} which is obtained by a resistor divider from the rectified line. The multiplier output can be expressed as the following equation:

$$V_{Multiplier} = 0.38 \times V_{MULT} \times (V_{COMP} - 2.5V)$$

The analog multiplier in SFL320 is specially designed to achieve high linearity over a wide dynamic range. Special efforts have been made to assure universal line applications with respect to a 90 to 264 VAC range.
The multiplier output is clamped to 1.05V internally.

◆ Frequency Adjusting

In SFL320, a proprietary function of “Frequency adjusting” is integrated. By setting a low frequency clamp which tracks the variation of the AC half wave rectified input voltage, the PFC THD performance can be improved, as shown in Fig.3.

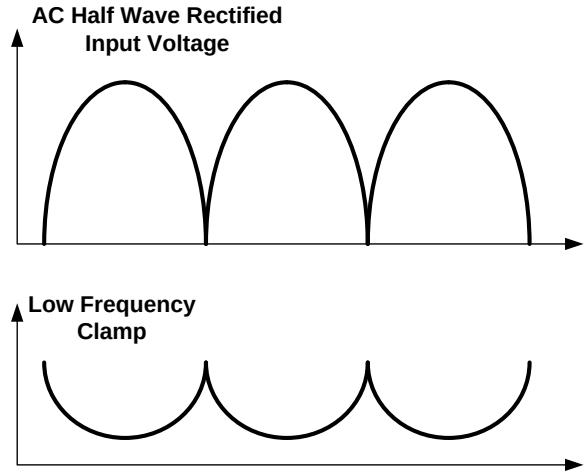


Fig.3

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the current limiting comparator is disabled and cannot switch off the gate driver. Thus, conventional RC filtering is not necessary and the propagation delay of current limit protection can be minimized.

◆ 3.3us Minimum OFF Time and 270KHz Maximum Switching Frequency Clamp

In SFL320, a minimum OFF time (typically 3.3us) is implemented to suppress ringing when GATE is off. The maximum frequency of SFL320 is clamped to 270KHz (typical). The minimum OFF time and maximum switching frequency camp are necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup.

◆ Zero Current Detector (ZCD)

SFL320 can perform zero current detection by using an auxiliary winding of the inductor. When the stored energy is fully released to the output, the voltage on ZCD goes down. If ZCD pin voltage drops below 0.25V, an internal ZCD comparator is triggered and a new switching cycle is initiated following the ZCD triggering. The power MOSFET is always turned on with zero inductor current such that the turn-on loss and noise can be minimized.
An internal restart timer (55us, typical) is built in to ensure proper start up operation.
The maximum and minimum voltage of ZCD pin is internally clamped to 5.8V and 0V respectively.

◆ VCC OVP (Over Voltage Protection)

When VCC voltage is higher than 35V (typical), VCC OVP (Over Voltage Protection) will be triggered in SFL320 and it is a protection of auto recovery mode (as mentioned below).

◆ Auto Recovery Mode Protection

As shown in Fig.4, once a fault condition (VCC OVP) is detected, switching will stop. This will cause VCC to fall because no power is delivered form the auxiliary winding. When VCC falls to UVLO(OFF) (typical 8.8V), the protection is reset and the operating current reduces to the startup current, which causes VCC to rise, as shown in Fig.4. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

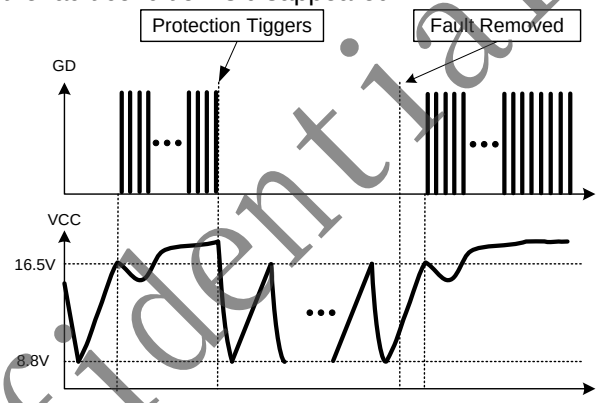


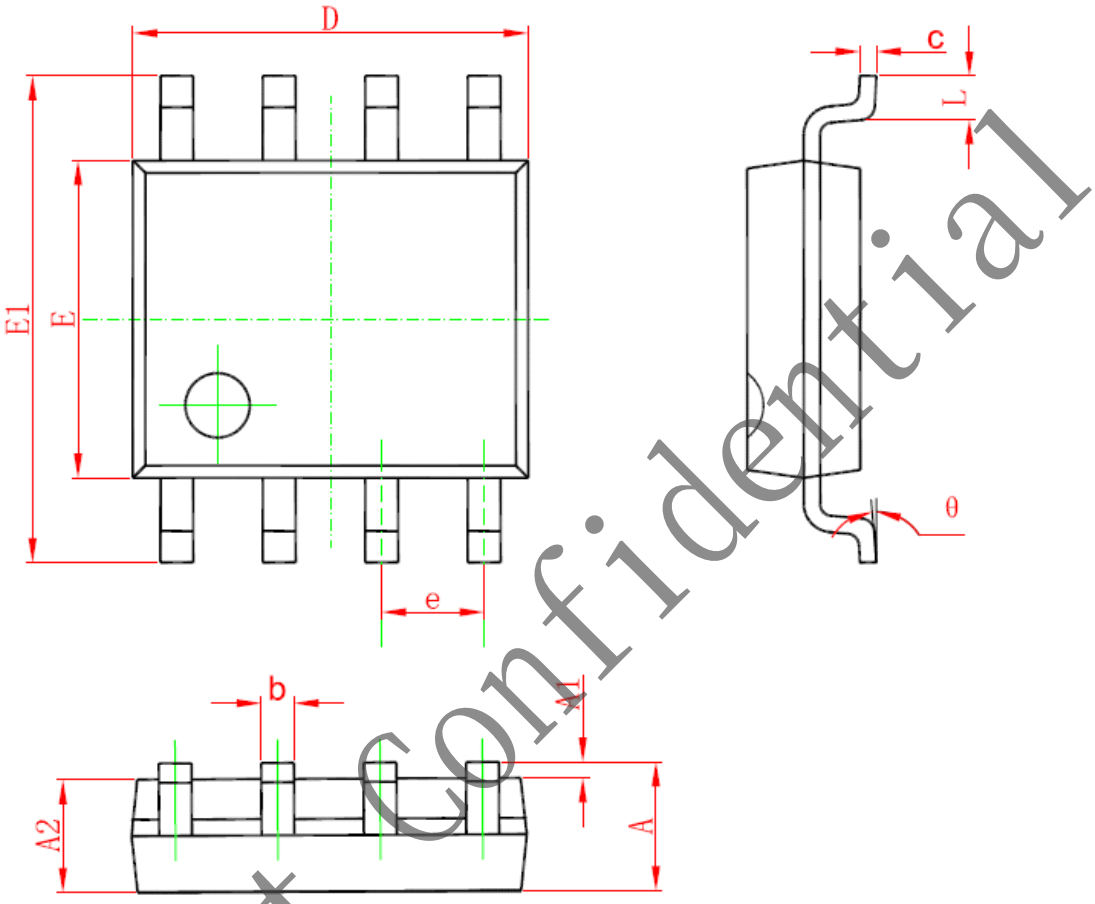
Fig.4

◆ Soft Gate Drive

SFL320 has a fast totem-pole gate driver with 800mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 16V clamp is added for MOSFET gate protection at higher than expected VCC input. A soft driving waveform is implemented to minimize EMI.

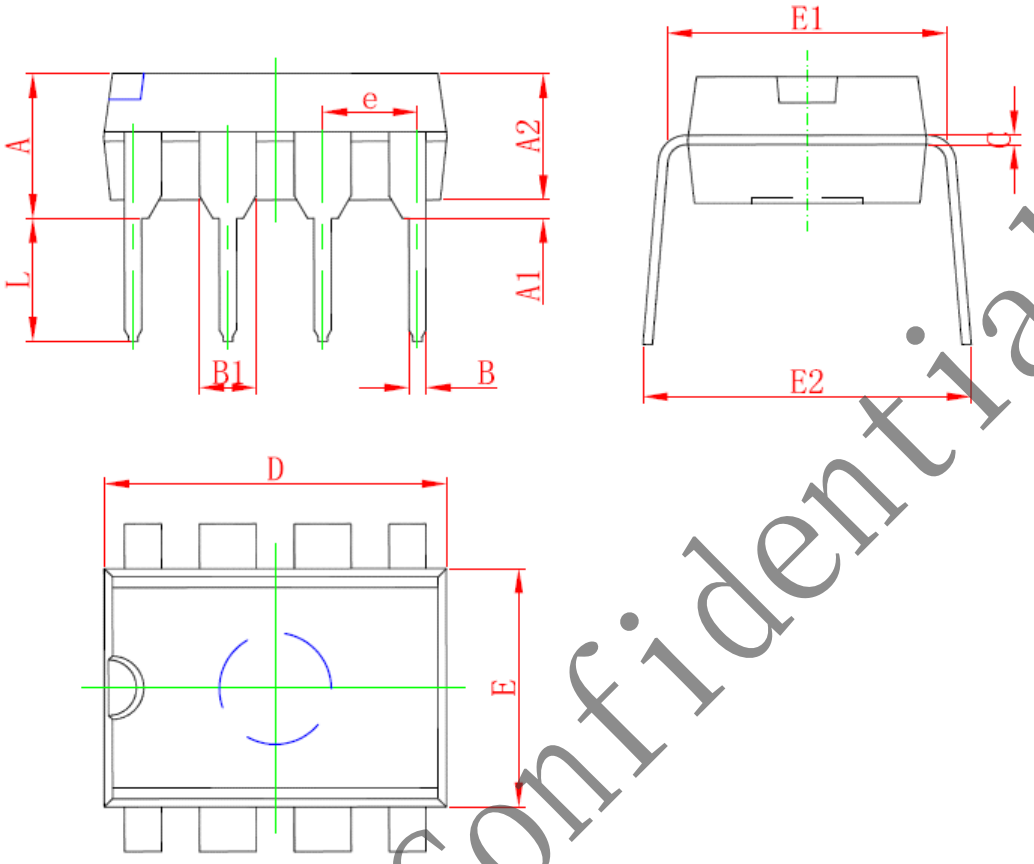
PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.06 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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