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## High Efficiency, Step-up DC/DC Converter

### Features

- Output Voltage up to 24V
- Internal MOSFET with high switch current up to 3A
- 20 $\mu$ A Quiescent (Switch-off) Supply Current
- 90% Efficiency
- Up to 450KHz Switching Frequency
- Using Internal Power Switches
- SOP-8L Package

### Applications

- PDA
- DSC
- LCD Panel
- RF-Tags
- MP3
- Wireless Equipment
- Portable Instrument

### Description

The CH1003 is a compact, high efficiency, and low voltage step-up DC/DC converter including an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.

The low start-up input voltage below 1.6V. The high switching rate minimized the size of external components. Besides, the 20 $\mu$ A low quiescent (Switch-off) current together with high efficiency maintains long battery lifetime.

The output voltage is set with two external resistors.

## Typical Application Circuits

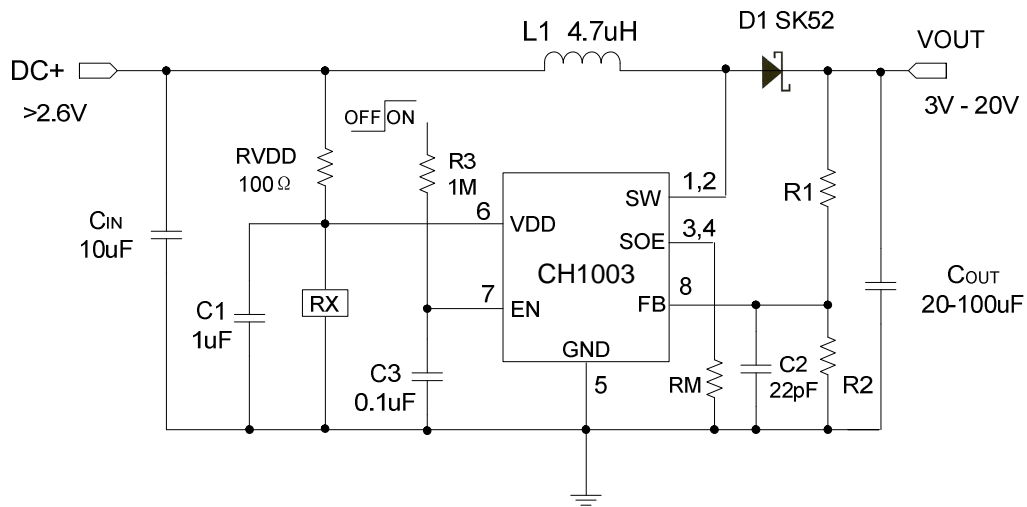


Figure 1 (2.6V Stat-up input Voltage)

\* RX can be a Zener Diodes or Resistor: The Ratio of RX/RVDD must to keep VDD voltage less than 5.5V. The resistor RM can be set to 50mΩ usually.

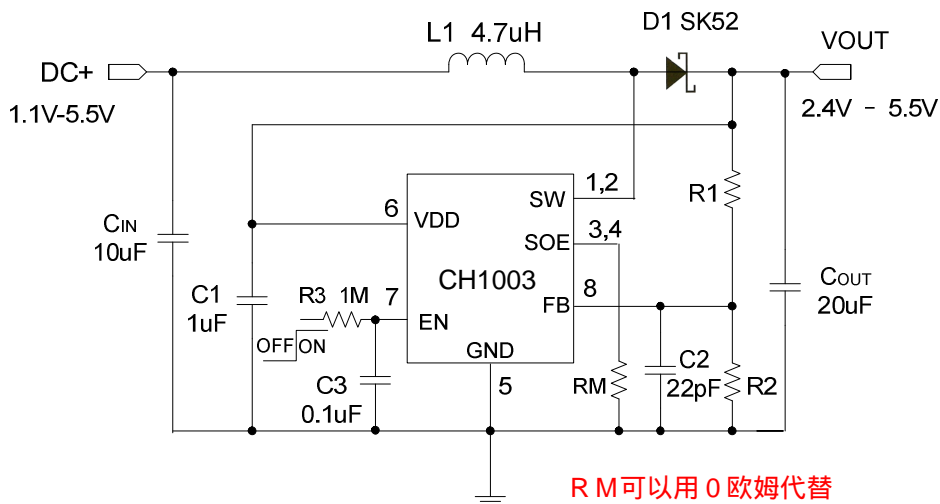


Figure 2 (1.1V Stat-up input Voltage)

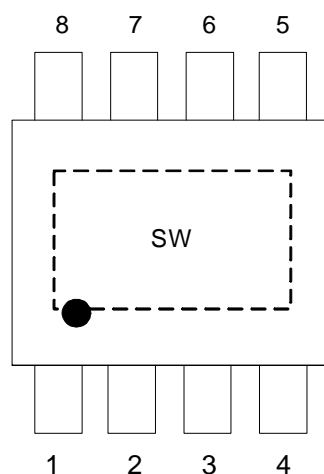
\* The resistor RM can be set to 50mΩ usually.

## Absolute Maximum Ratings (Note 1)

- Supply Voltage.....-0.3V to 6V
- SW Pin Switch Voltage.....-0.3V to 28V
- Other I/O Pin Voltages.....-0.3V to 6V
- SW Pin Switch Current .....3A
- Operating Junction Temperature.....125°C
- Storage Temperature Range .....-65°C ~ +150°C

**Note 1:** Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

## Pin Assignment



SOP- 8L

PIN NUMBER	PIN NAME	FUNCTION
1	SW	Switch Output
2	SW	Switch Output
3	SOE	Source of the MOSFET
4	SOE	Source of the MOSFET
5	GND	Ground
6	VDD	Input
7	EN	ON/OFF Control(High Enable)
8	FB	Feedback

## Electrical Characteristics

( $V_{IN} = 1.5V$ , VDD set to 3.3V, Load Current = 0A,  $T_A = 25^\circ C$ , unless otherwise specified)

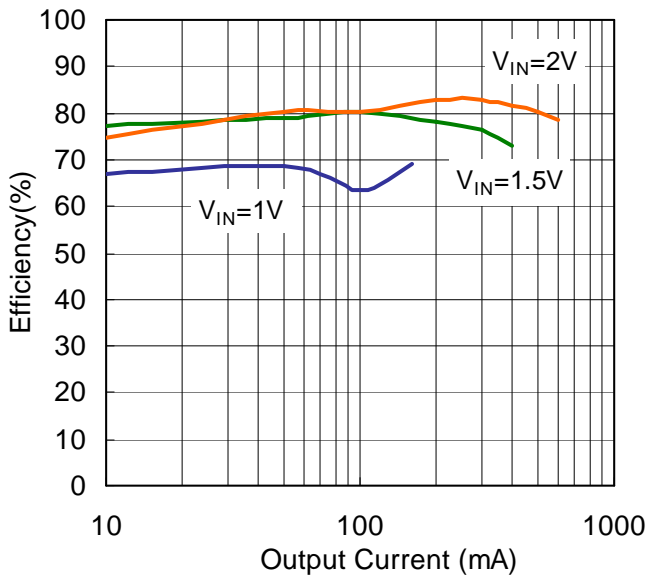
Parameter	Test Conditions	Min	Typ	Max	Units
Start-UP Voltage	$I_L = 1mA$	1.00			V
Operating VDD Range	VDD pin voltage	2		5.5	V
Switch-off Current I ( $V_{IN}$ )	$V_{IN} = 5V$		20		$\mu A$
No Load Current I ( $V_{IN}$ )	$V_{IN} = 1.5V, V_{OUT} = 3.3V$		40		$\mu A$
Feedback Reference Voltage	Close Loop, VDD = 3.3V	1.182	1.212	1.242	V
Switching Frequency	VDD = 3.3V			450	KHz
SW ON Resistance	VDD = 3.3V		0.07		$\Omega$
Current Limit Setting	VDD = 3.3V		3		A
Line Regulation	$V_{IN} = 1.5 \sim 2.5V, I_L = 100mA$		55		mV/V
Load Regulation	$V_{IN} = 2.5V, I_L = 1 \sim 300mA$		0.1		mV/mA
En Input High		1			V
En Input Low				0.6	V
Maximum $V_{RM}$			145		mV

## Typical Performance Characteristics

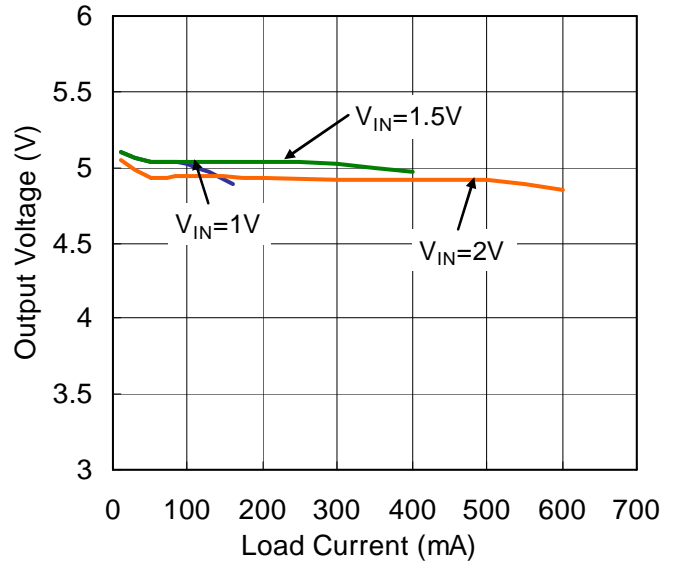
TA=25°C, C<sub>IN</sub> =10 μF, C<sub>OUT</sub> =20 μF, L=4.7 μH, unless otherwise noted.

Refer to Test Circuit Figure 1

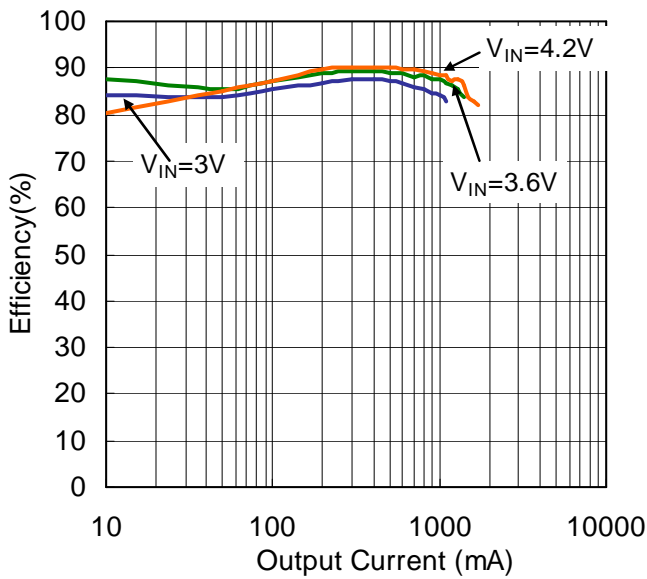
**Efficiency vs. Output Current  
(V<sub>out</sub>=5V)**



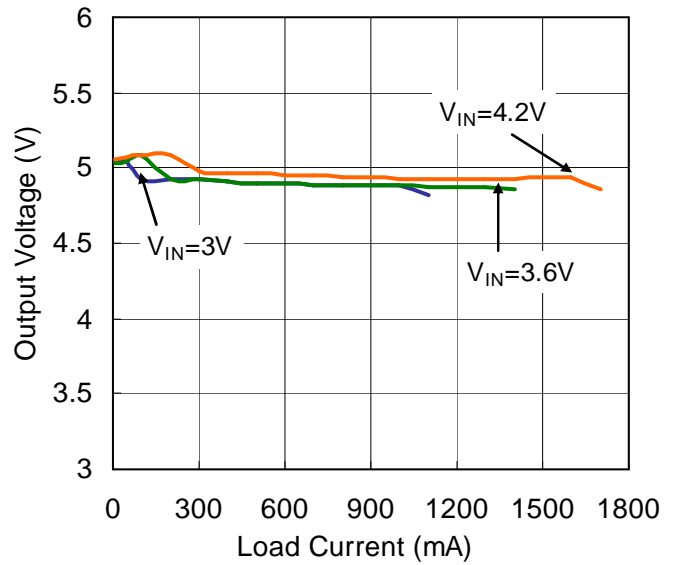
**Output Voltage vs. Load Current  
(V<sub>out</sub>=5V)**



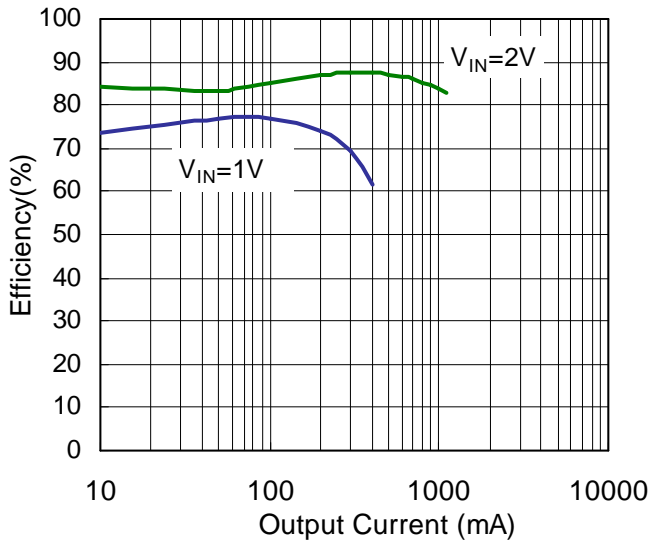
**Efficiency vs. Output Current  
(V<sub>out</sub>=5V)**



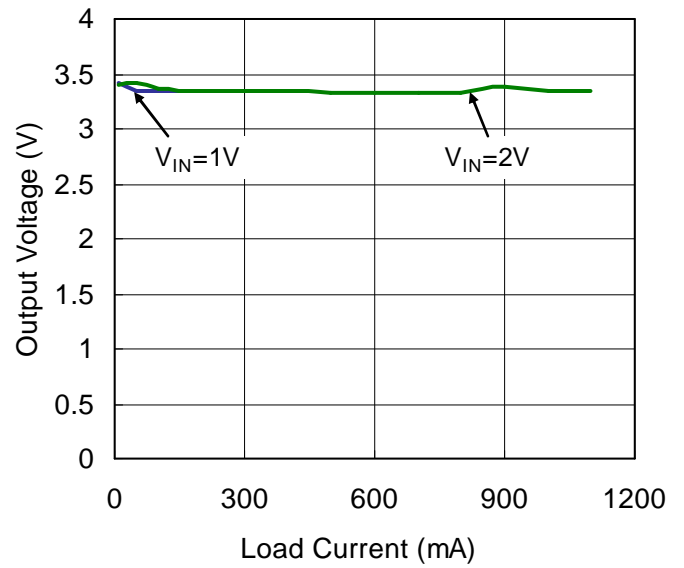
**Output Voltage vs. Load Current  
(V<sub>out</sub>=5V)**



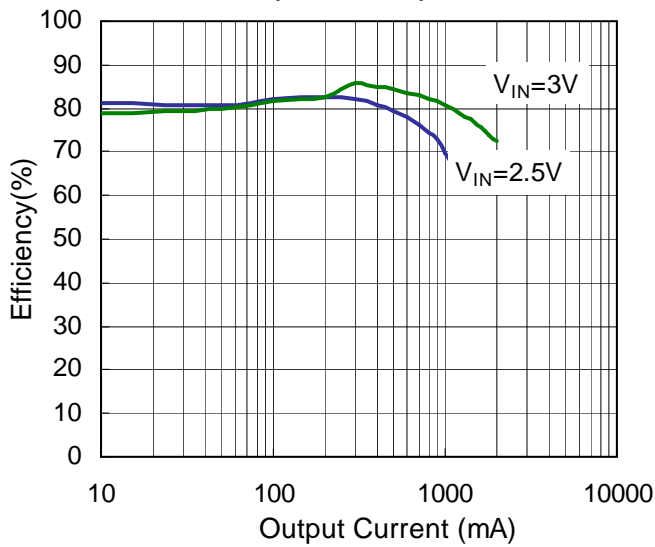
**Efficiency vs. Output Current  
(Vout=3.3V)**



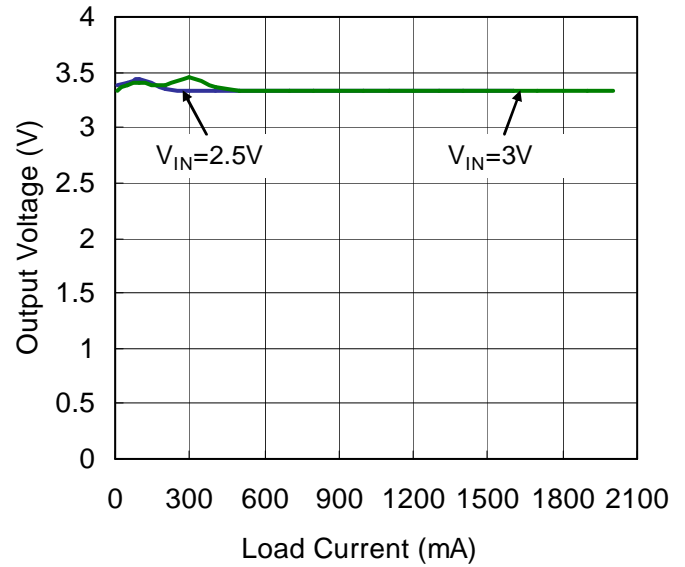
**Output Voltage vs. Load Current  
(Vout=3.3V)**



**Efficiency vs. Output Current  
(Vout=3.3V)**

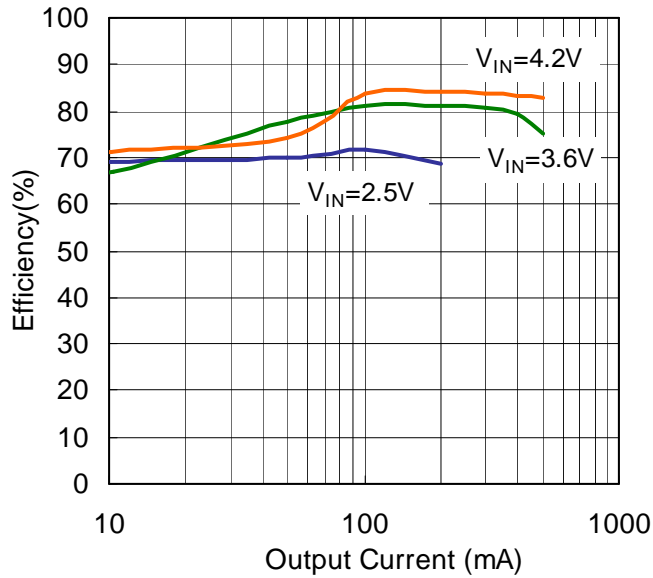


**Output Voltage vs. Load Current  
(Vout=3.3V)**

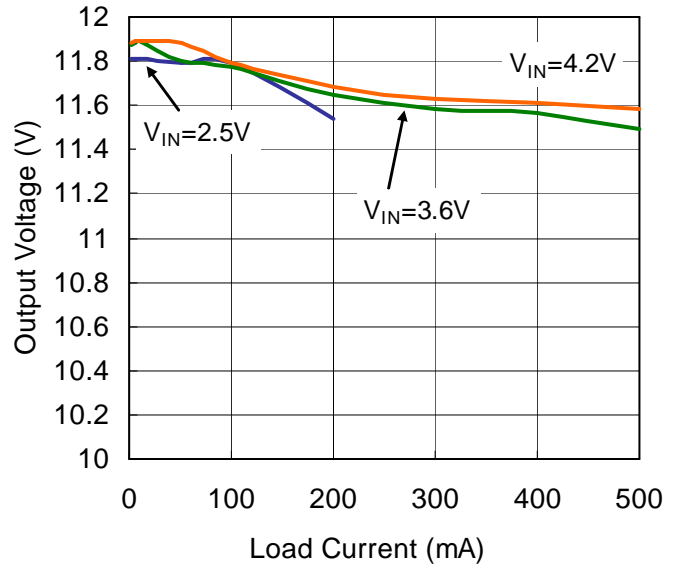


$T_A=25^{\circ}\text{C}$ ,  $C_{IN}=10\ \mu\text{F}$ ,  $C_{OUT}=20\ \mu\text{F}$ ,  $L=10\ \mu\text{H}$  (high saturated inductor current), unless otherwise noted.

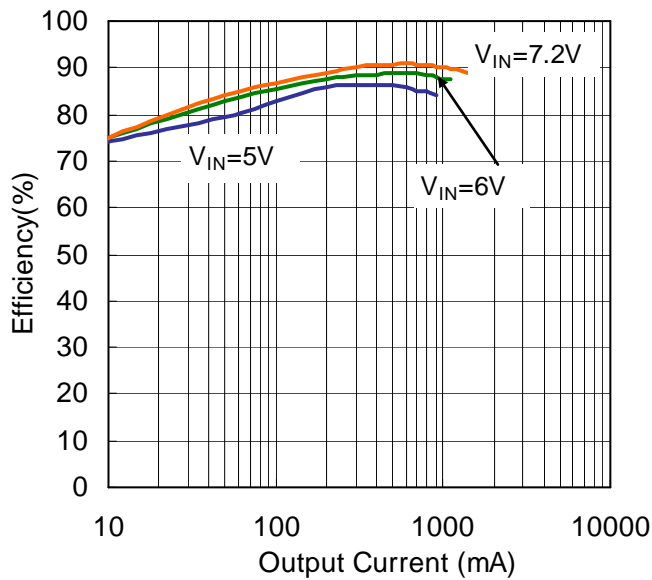
**Efficiency vs. Output Current  
( $V_{out}=12\text{V}$ )**



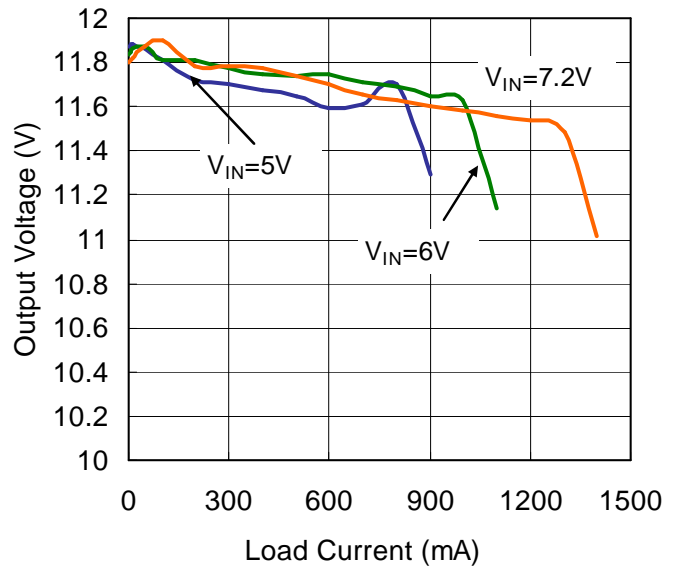
**Output Voltage vs. Load Current  
( $V_{out}=12\text{V}$ )**



**Efficiency vs. Output Current  
( $V_{out}=12\text{V}$ )**



**Output Voltage vs. Load Current  
( $V_{out}=12\text{V}$ )**



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## Pin Information

**SW (Pin 1/ Pin 2):** Switch Pin. Connect inductor between SW and VIN. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

**SOE (Pin 3/ Pin 4):** Source of the MOSFET. Connect resistor to GND.

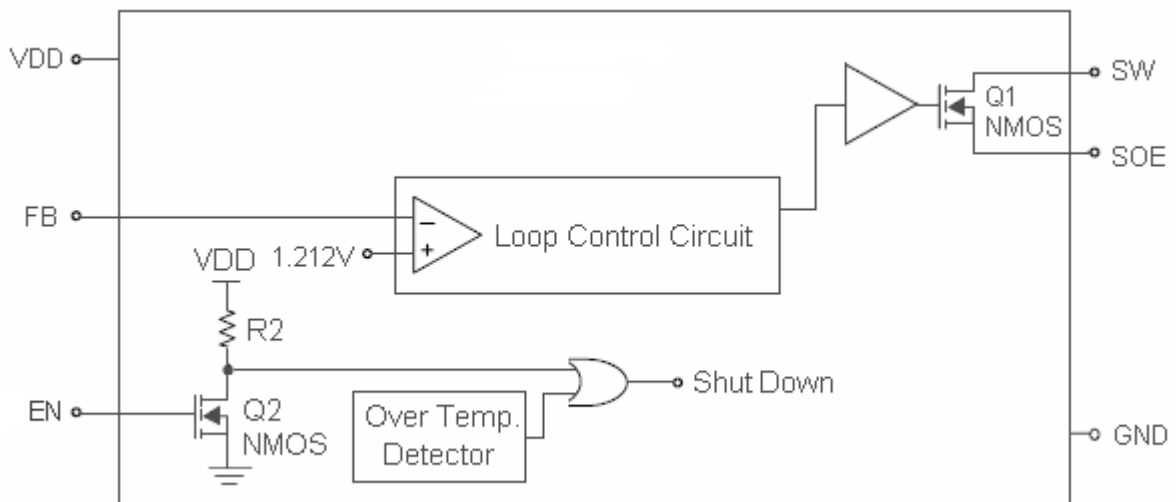
**GND (Pin 5):** Signal and Power Ground. Provide a short direct PCB path between GND and the (–) side of the output capacitor(s).

**VDD (Pin 6):** Input positive power pin.

**EN (Pin 7):** En Control Input. Forcing this pin above 1V enables the part. Forcing this pin below 0.6V shuts down the device. In shutdown, all functions are disabled, drawing <math><1\mu\text{A}</math> supply current. Do not leave EN floating.

**FB (Pin 8):** Feedback Input to the  $g_m$  Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 3.3V to 20V by:  $V_{\text{OUT}} = 1.212\text{V} \cdot [1 + (R1/R2)]$ .

## Block Diagram





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## Application Information

### Output Voltage Setting

Referring to Typical Application Circuits, the output voltage of the switching regulator ( $V_{OUT}$ ) can be set with Equation (1).

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 1.212V \quad (1)$$

### Current-limiting Resistance Setting

$$R_M = \frac{0.145}{I_{MAX,switch}}$$

### Feedback Loop Design

Referring to the Typical Application Circuits. The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

- Follow Equation (1)
- Higher R reduces the quiescent current (Path current =  $1.212V/R2$ ), however resistors beyond 5MW are not Recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pin.

For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such high impedance feedback loop is sensitive to any interference, which requires careful PCB layout and avoid any interference, especially to FB pin. To improve the system stability, a proper value capacitor between FB pin and GND pin is suggested. An empirical suggestion is around 22pF.

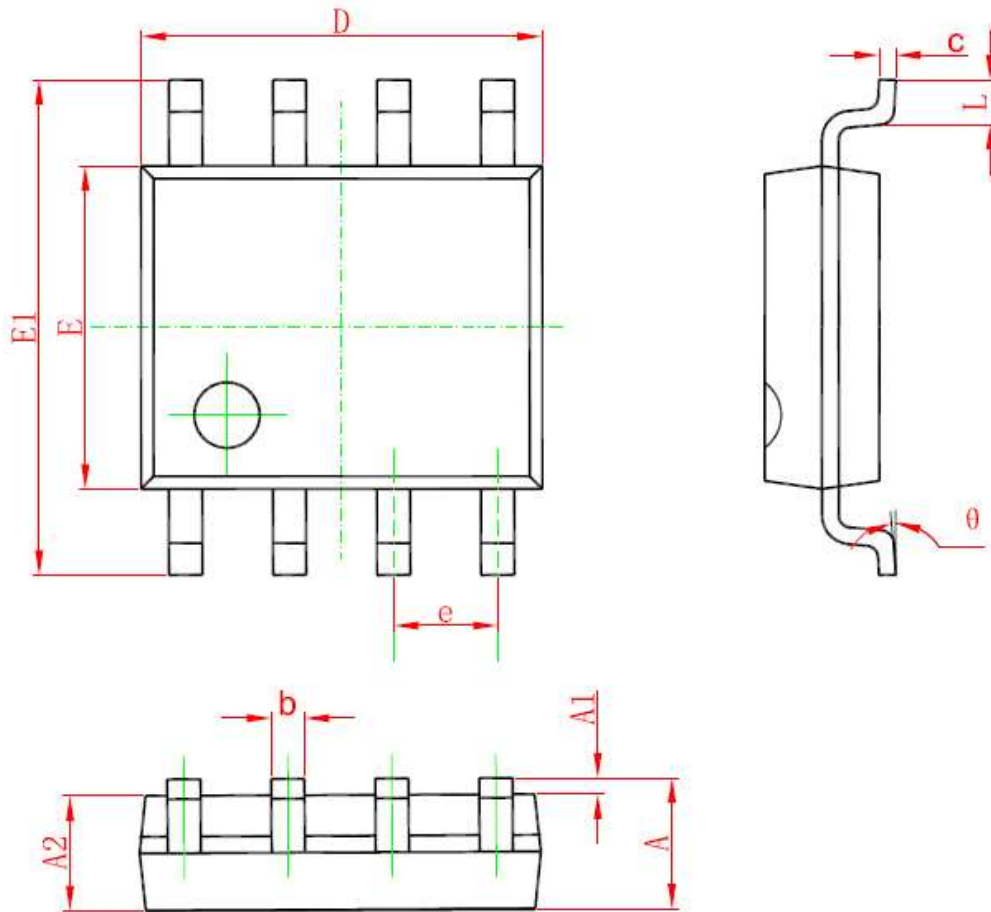
### PCB Layout Guide

PCB Layout shall follow these guidelines for better system stability:

- A full GND plane without gap break.
- VDD to GND noise bypass - Short and wide connection for the 20uF MLCC capacitor between Pin 6 and Pin 5.
- VIN to GND noise bypass - Add a 10uF capacitor close to L1 inductor, when  $V_{IN}$  is not an idea voltage source.
- Minimized FB node copper area and keep far away from noise sources.

## Packaging Information

### SOP-8L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°