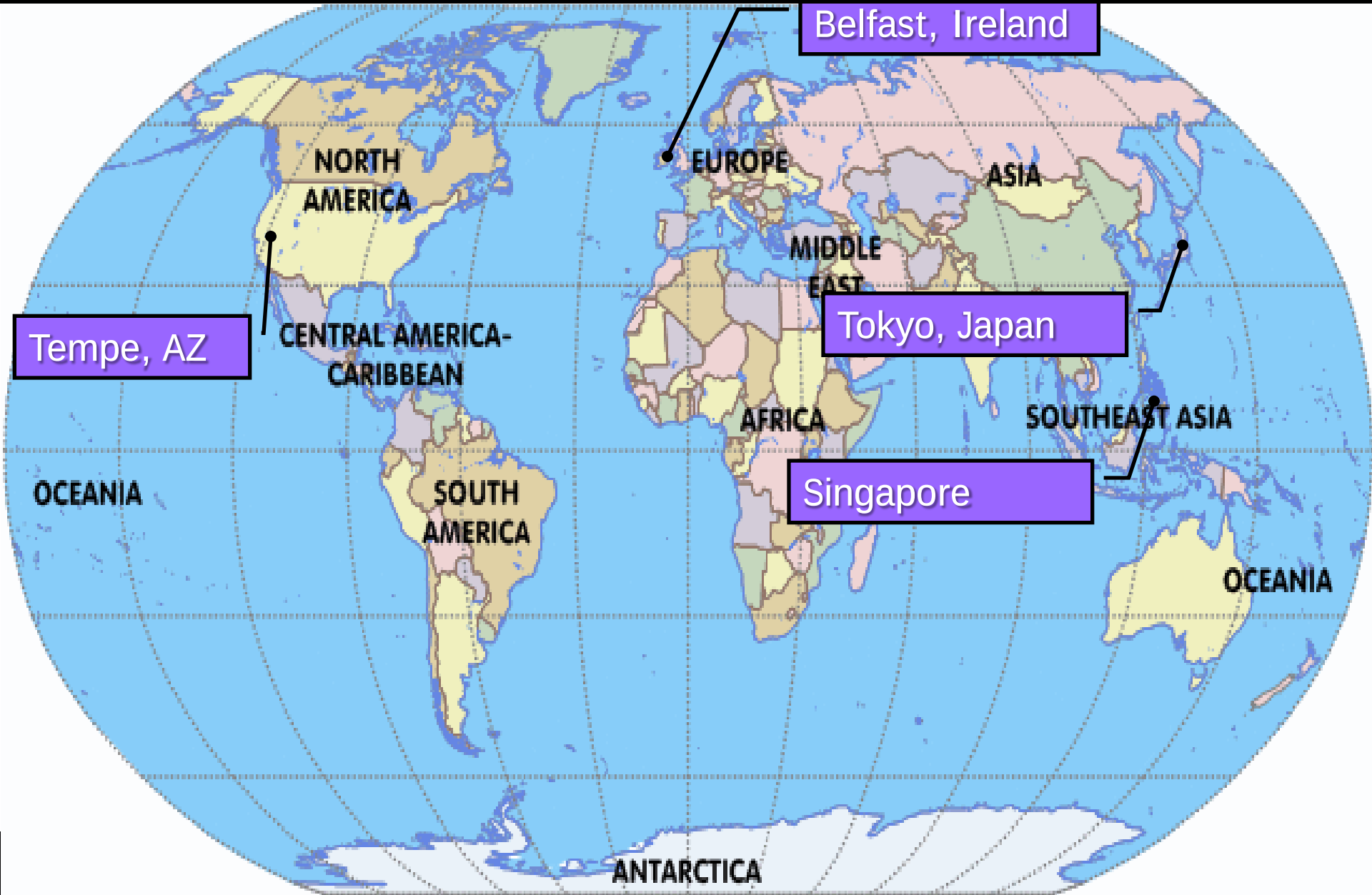
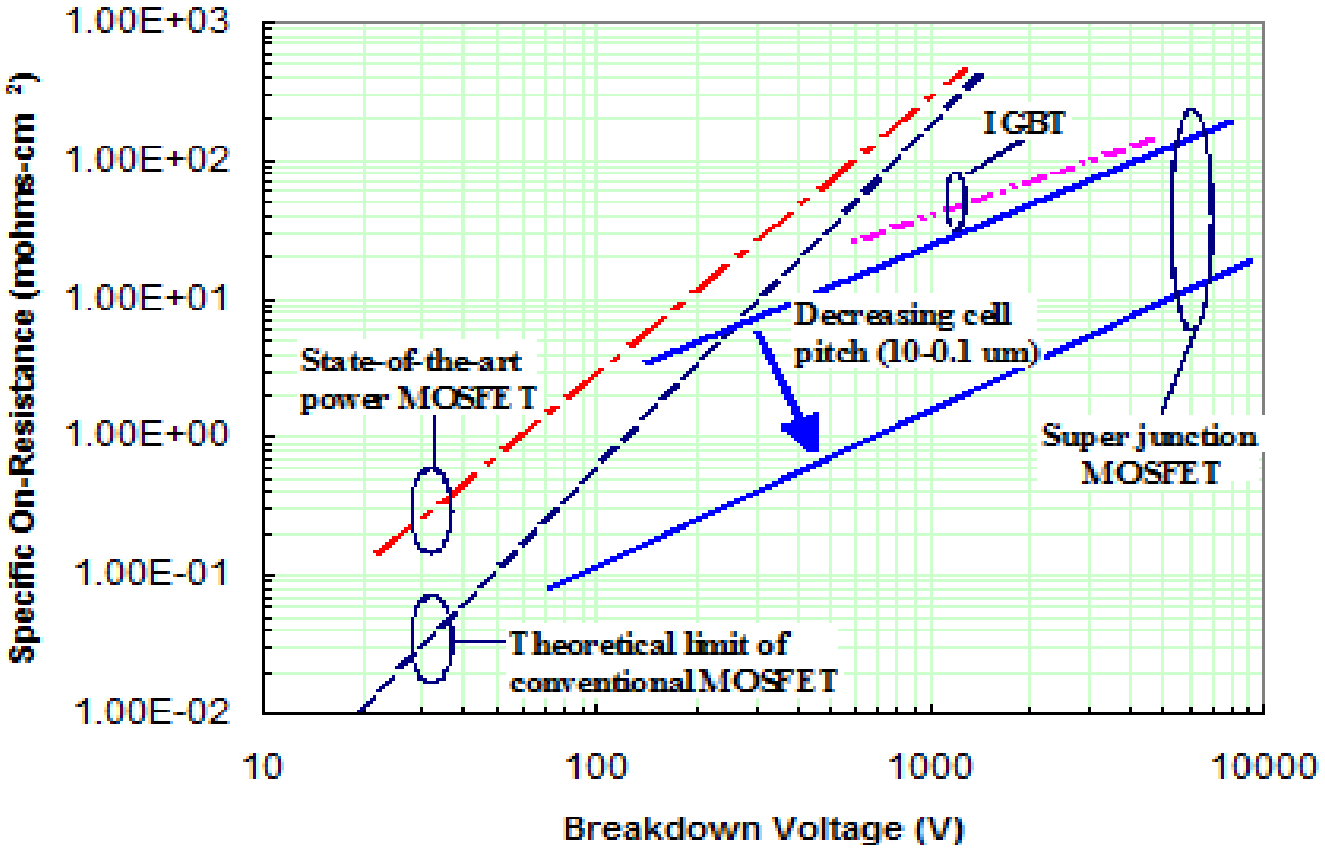

ICEMOS TECH
Mems Superjunction
High Voltage MOSFETs
Product Launch
Tokyo
Aug 4th 2011

OPERATING LOCATIONS

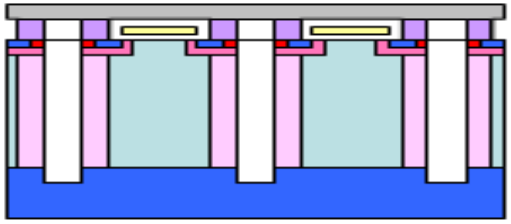


ICEMOS Superjunction Advantage

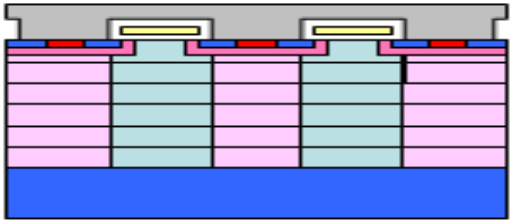


Superjunction Technology comparison

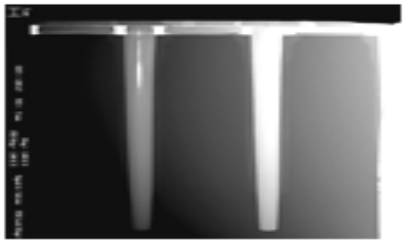
ICEMOS MEMS TrenchFET



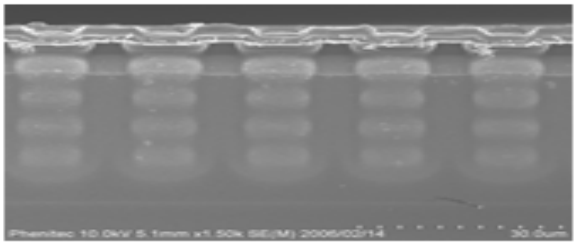
Competitor Multiple Epi



TRENCH



Multiple Epi



The ICEMOS ™ Superjunction MOSFETs employs a single epi layer to achieve 700V blocking voltage whereas ICEMOS competitors use multiple epi layers in some cases up to seven epi layers to achieve 700v blocking voltages.

Device Title	BVDSS (V)	ID (A)	RDSON (ohm)	Vth (Volts)	Cross Reference
ICE20N65	650	20	0.170	2.1-3.9	SPP20N65C3
ICE20N60	600	20	0.160	2.1-3.9	STM20N60
ICE15N60	600	15	0.250	2.1-3.9	IPA60R380C6
ICE10N60	600	10	0.370	2.1-3.9	SPP07N65C3

IceMOS Value Proposition

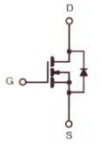
ICEMOS TECHNOLOGY LTD

Preliminary Data Sheet
ICE20N60

ICE20N60 N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	20A	Max
$V_{(BR)DSS}$	I_D=250uA	600V	Max
$r_{DS(on)}$	V_{GS}=10V	0.23 Ω	Typ

Features
- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dV/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



T0220
Full-PAK

Isolated
(T0-220)

Maximum Ratings and Thermal Characteristics [b] (T_A=25°C unless otherwise noted)

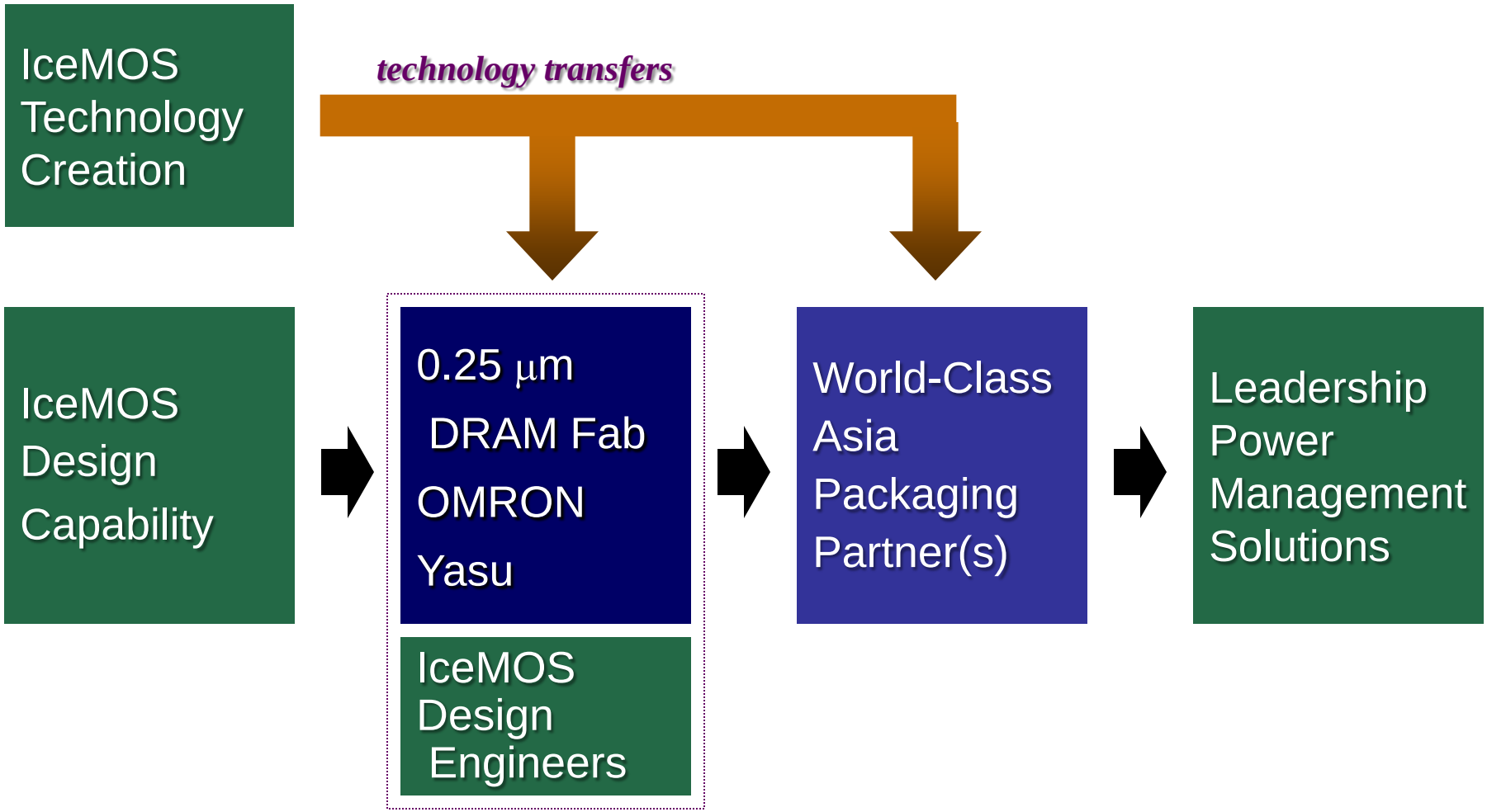
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	
Drain Current	- Continuous (Tc = 25° C)	I_D	20	A
	- Pulsed (limited by Tjmax)	I_{DM}	62	
Repetitive Avalanche Current (limited by Tjmax)		I_{AR}	7	A
Energy in Avalanche (single pulse, ID = 3.5A)		EAS	690	mJ
Maximum Power Dissipation (Tc = 25° C)		P_D	35	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
dV/dt voltage slope (Vds=480V, ID=20A, Tj = 125 °C		dV/dt	50.0	V/ns
Thermal Resistance[a]	- Junction-to-Ambient	R_{thJA}	62	°C/W
	- Junction-to-Case	R_{thJC}	3.60	

a When mounted on 1inch square 2oz copper clad FR-4

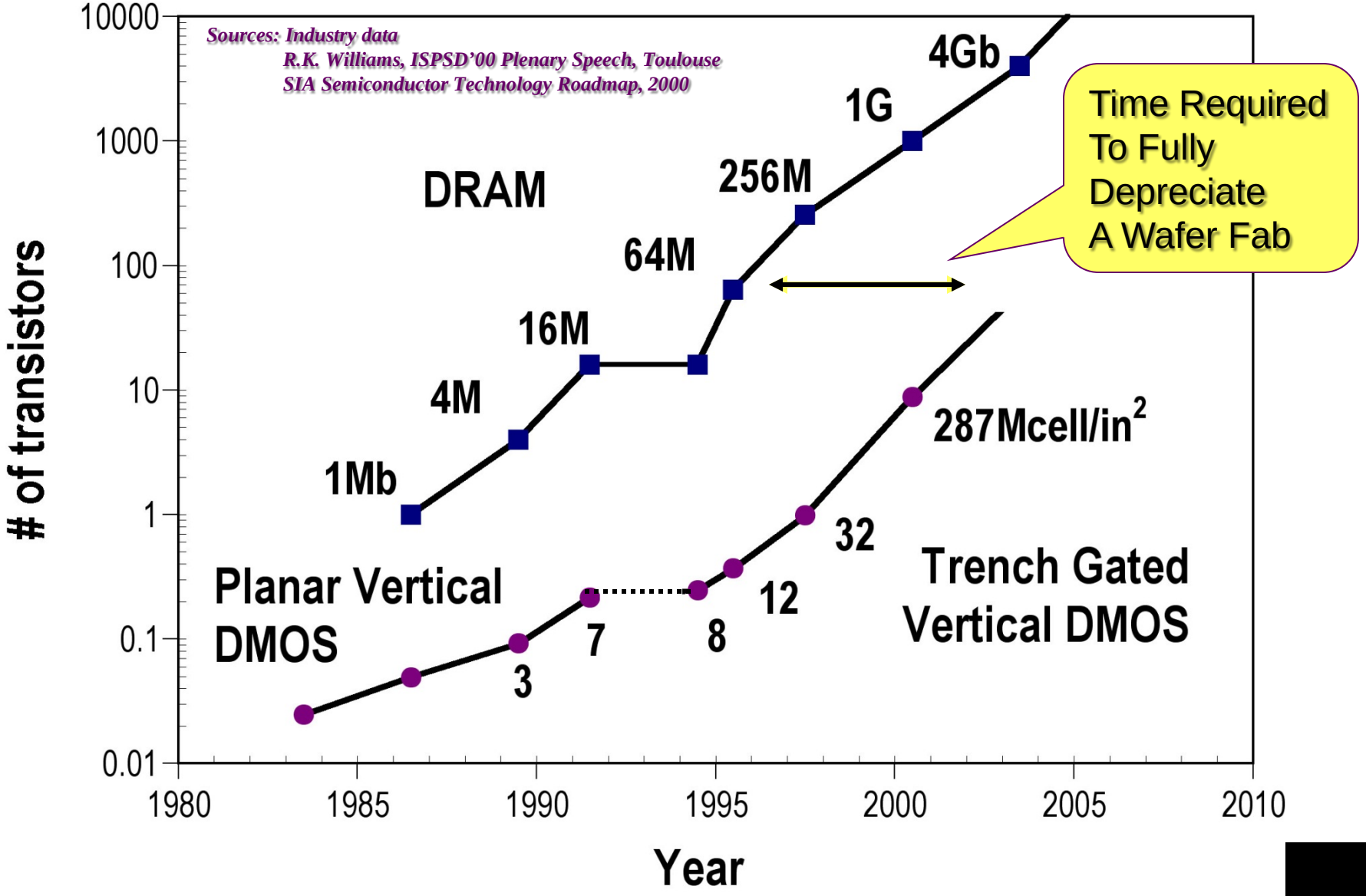
b Preliminary Data Sheet - Specifications subject to change.

- The Superjunction (SJ) DMOSFET is the Most Cost Effective *Gate-Controlled* Power Device Above 400V
- IceMOS has IP and Know-how to Manufacture SJ DMOSFETs & Rectifiers
- IceMOS can be an alternative Technology Partner.

Omron & IceMOS Strategic Partnership



Omron fabrication facility excellent equipment and engineering resources for the development and production of MEMS SJ MOSFET.



Applications that stand to Benefit from IceMOS Eco Friendly Superjunction

- LED TV Drivers & Power Supplies
- Lighting HID & LED Ballast
- Electric and Hybrid Cars
- Batteries for Electric Cars
- Photovoltaic SOLAR Inverters
- Servers, Laptops and Tablets

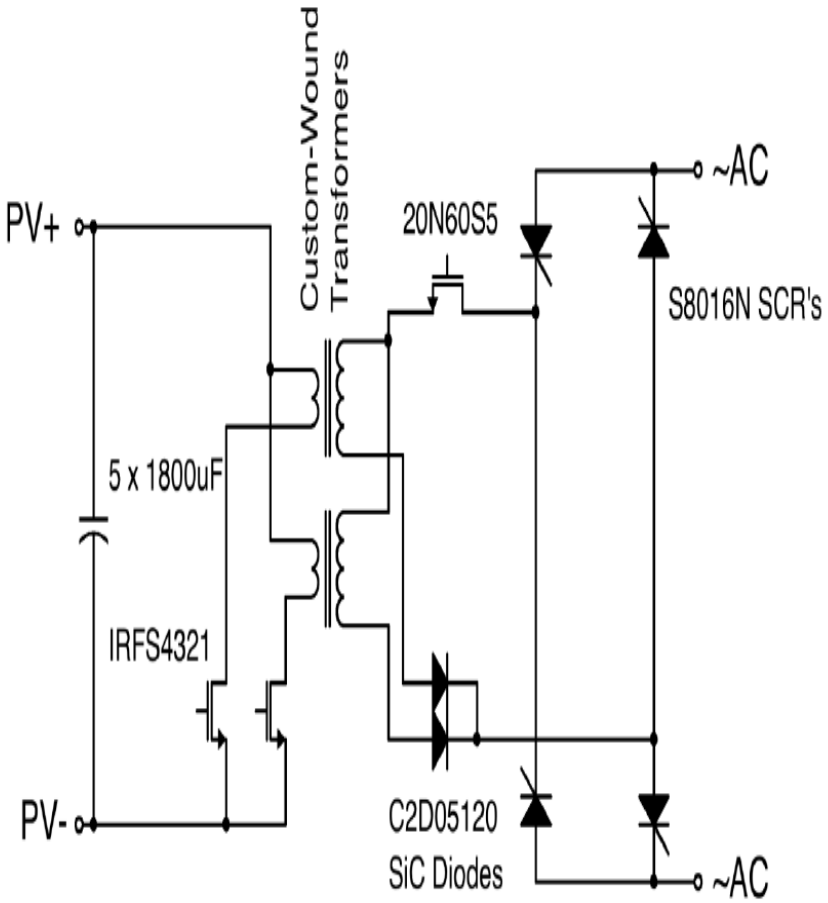
Speciality Lighting Applications for Superjunction

- SJ MOS is used in:
  - –PFC's to avoid input surge currents
  - –lamp ballasts:
  - •High-intensity discharge lamp ballast
  - •LED drivers

- Xenon head light ballast

- High Intensity Discharge Light Ballast

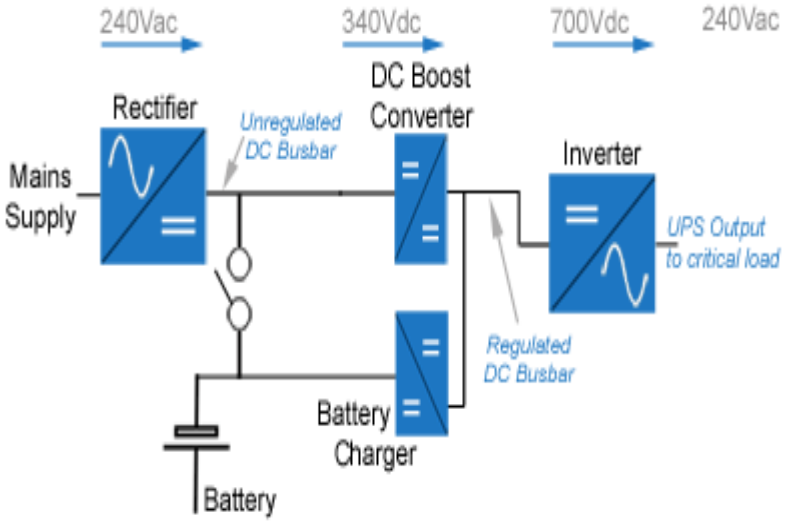
PhotoVoltaic for Solar Energy Conversion



- MICRO PV Inverter

Uninterruptible Power Supply UPS

- ***Trend is to use more and more SJ MOS in UPS, with NPC structure, Schneider electric (world leader) is planning to go on SJ MOS for 2014 in part of their product line.***



- **High power**
- **–100 – 1000 kVA: Industrial, IDC, telecom**
- **–From $50k to $400+k**

“Quality is in the Detail”

IceMOS Culture: Attention to detail at every step.

Design Optimization for performance.

Design Centering for Manufacturability.

Applying Scientific Principles in disciplined fashion.

Design of Experiments“DOE”.

Six Sigma Design Cp, Cpk, SPC.

Application of Scientific Principles in a Disciplined Engineering Fashion aided by CAD Modelling

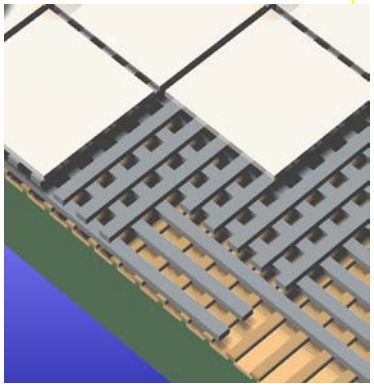
Scientific Principles

$$BV = E_c t_{epi}$$

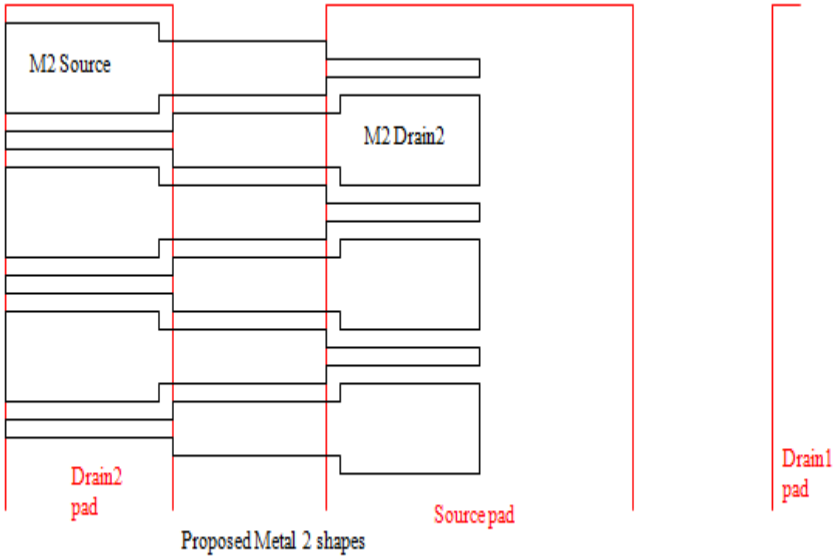
$$Q = \frac{N_d \cdot W}{2} = \frac{\varepsilon_{si} E_c}{2}$$

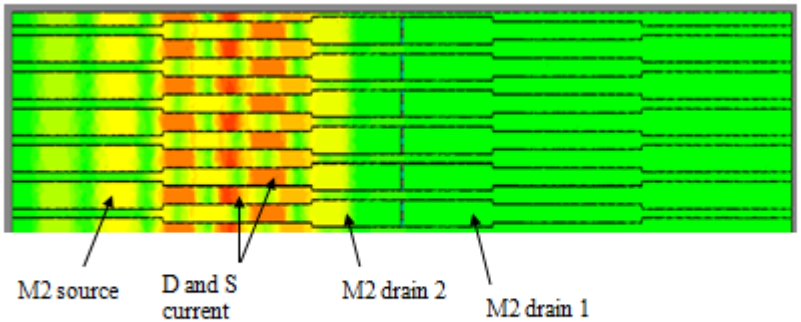
$$R_{on} = \frac{t_{epi}}{q\mu_n N_d} = \frac{W \cdot BV}{2q\mu_n E_C Q} = \frac{W \cdot BV}{2\mu_n E_C{}^2}$$

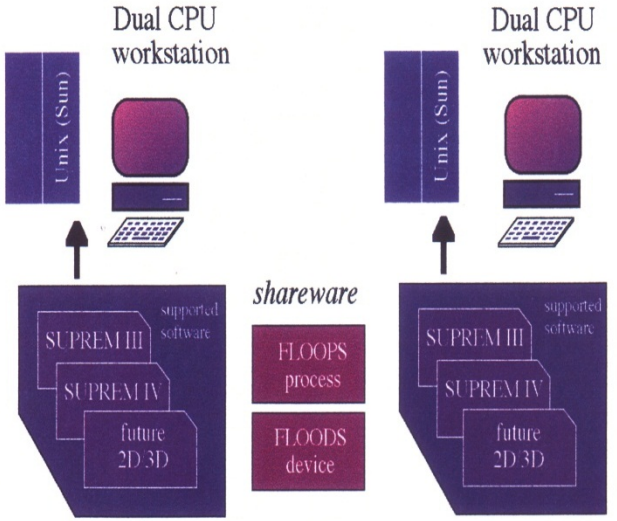
Disciplined Engineering

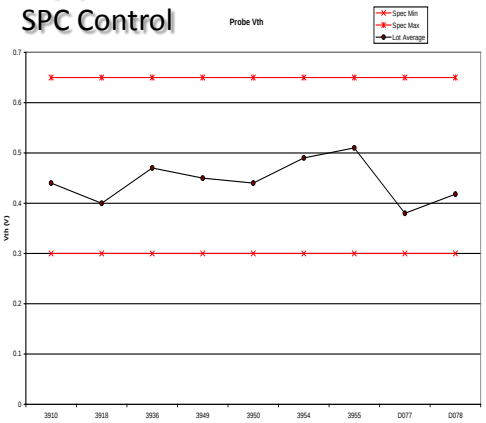


Innovation



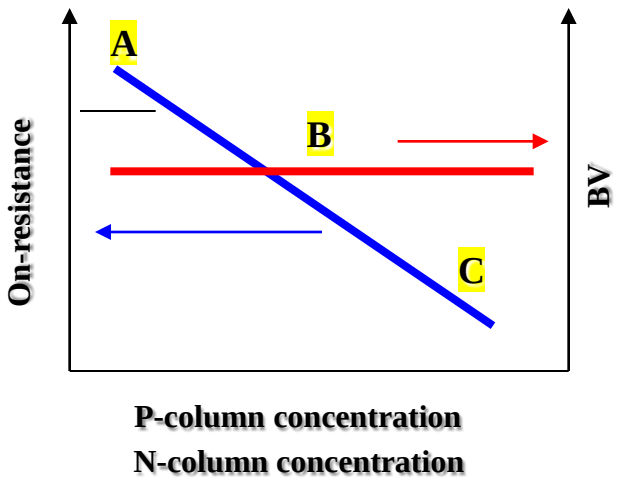


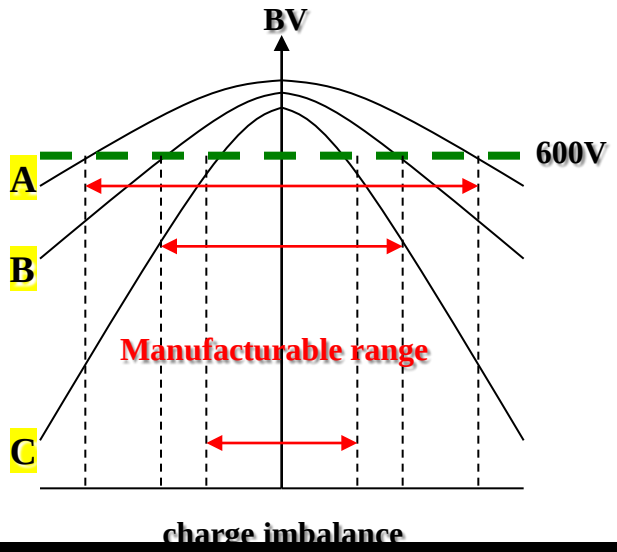




$$R_{DSON} = R_{CH} + R_S + R_D + R_{M1} + R_{M2}$$

Centering for Manufacturability BV and Rdson





- As long as the equation is satisfied, on-resistance is reversely-proportional to N-column concentration, keeping the same BV.

- One important fact is ; When P and N charges are imbalanced, BV drops. Higher concentration results in more drop.

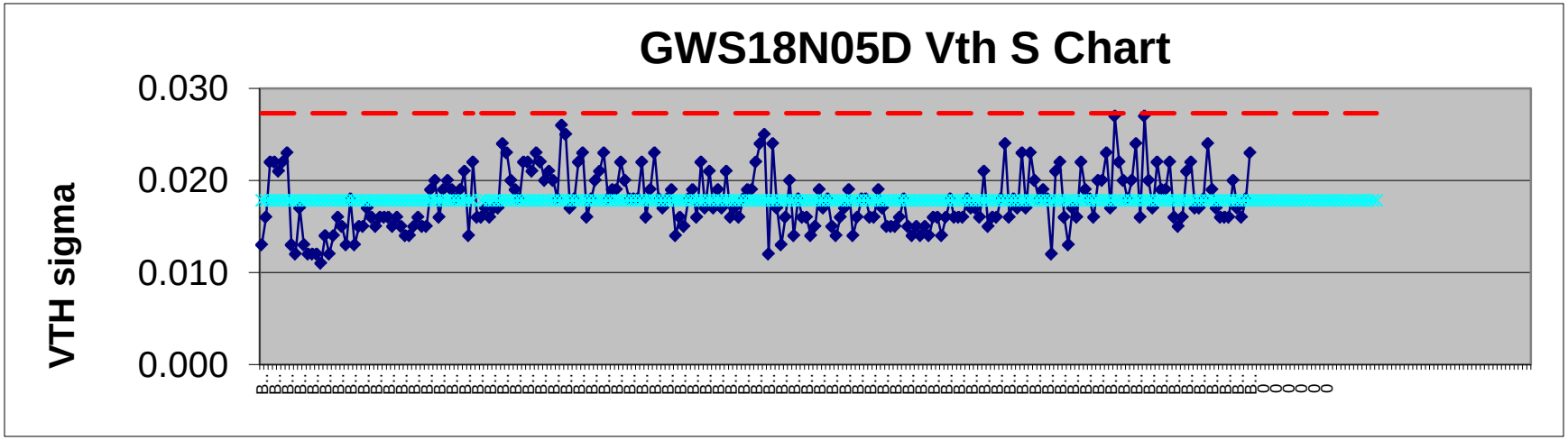
- Charge imbalance (%) is defined by ;

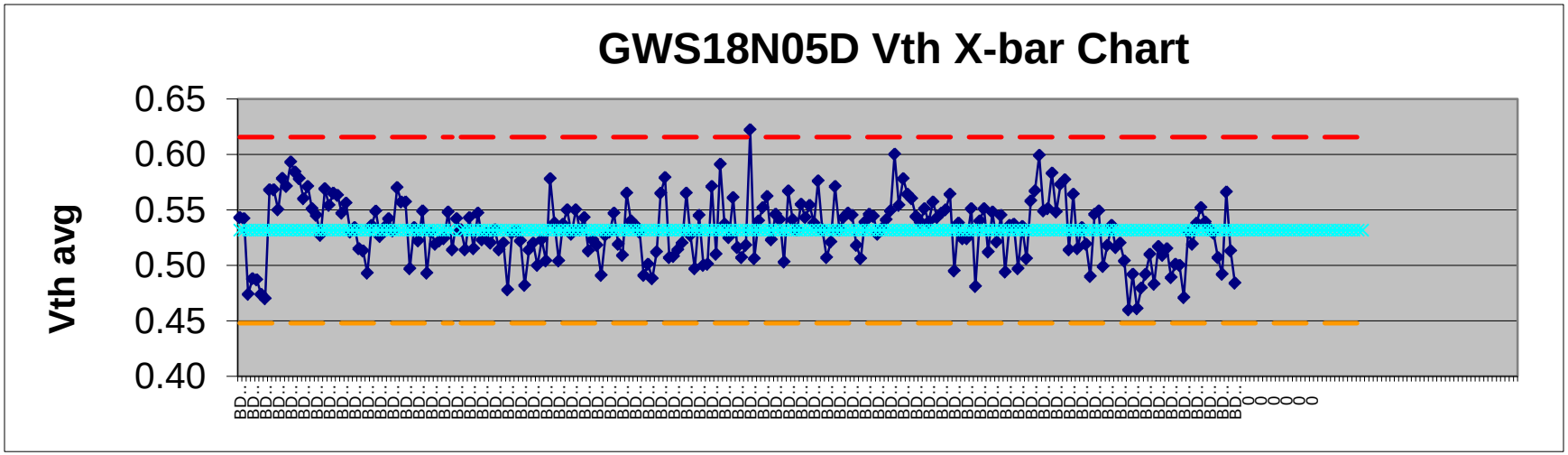
(P-charge - N-charge) / P-charge x 100

- Therefore to obtain lower on-resistance, both of N-column and P-column concentration must be increased, but within appropriate range of charge balance.

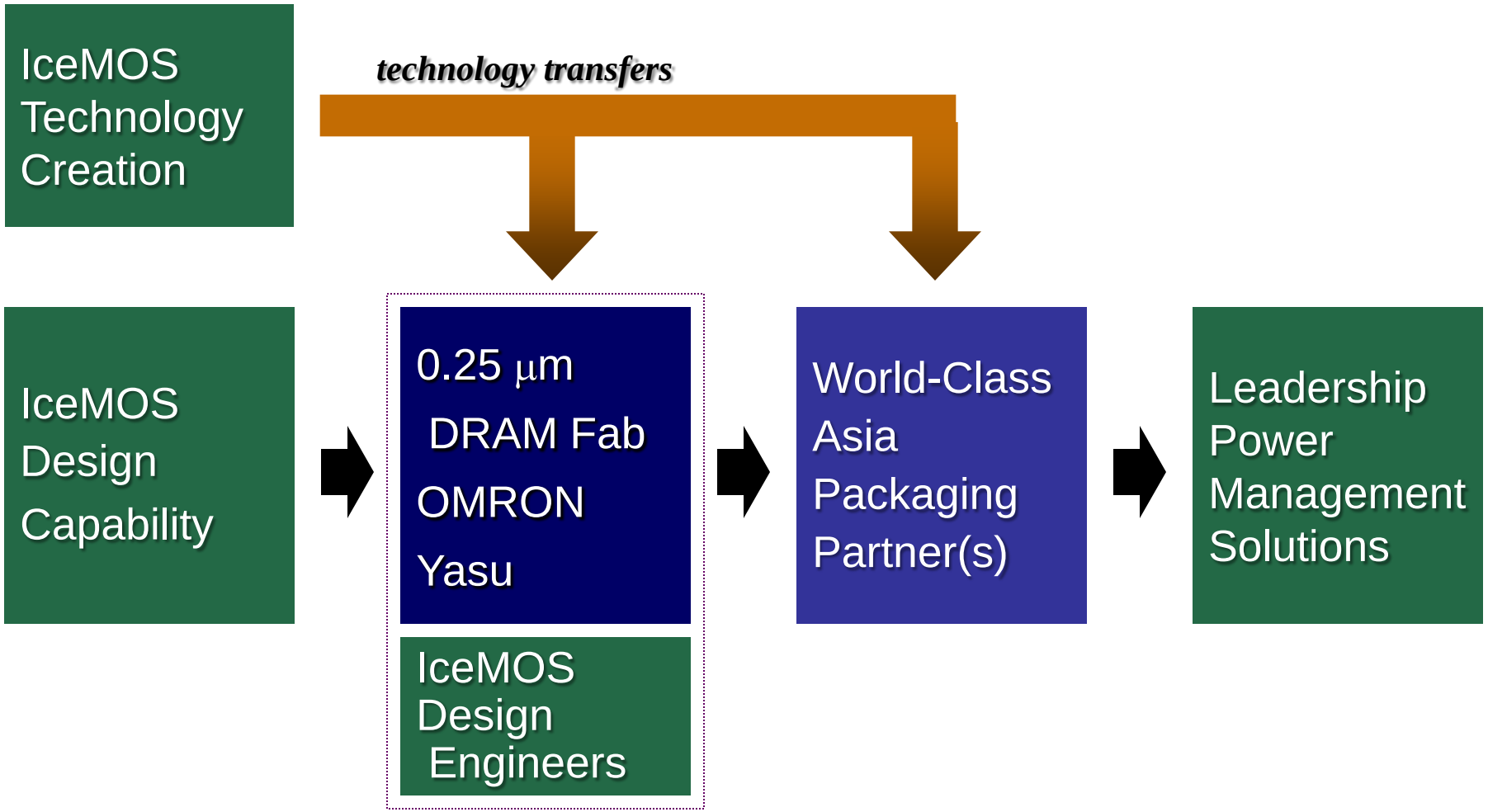
- In general charge balance is directly related to wafer process control and determined compromisingly.

Statistical Process Control



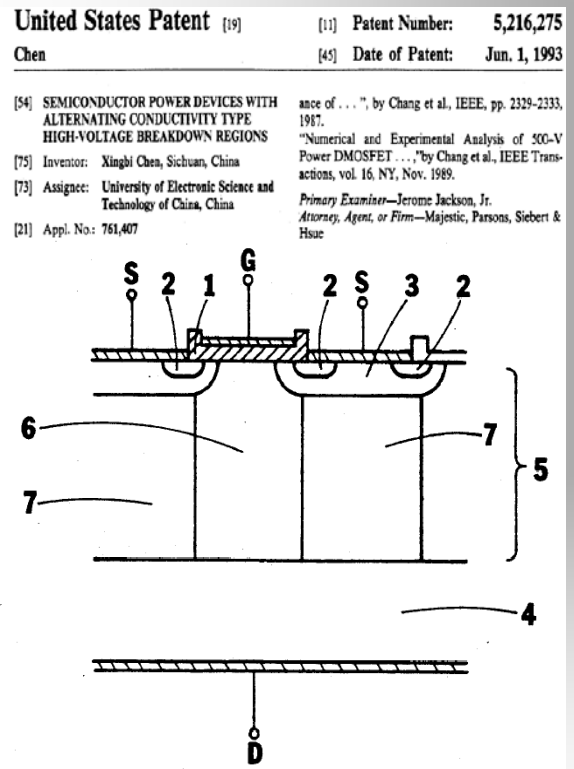


Omron & IceMOS Strategic Partnership



Many IceMOS Superjunction Patents Issued: over 100 issued and pending.

Court Tested Patents



United States Patent [19]
Chen

[11] Patent Number: 5,216,275
[45] Date of Patent: Jun. 1, 1993

[54] SEMICONDUCTOR POWER DEVICES WITH ALTERNATING CONDUCTIVITY TYPE HIGH-VOLTAGE BREAKDOWN REGIONS

[75] Inventor: Xingbi Chen, Sichuan, China

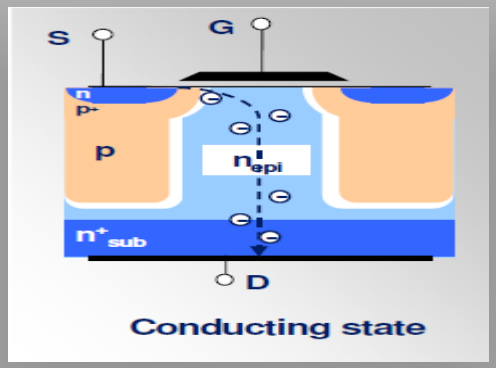
[73] Assignee: University of Electronic Science and Technology of China, China

[21] Appl. No.: 761,407

ance of . . . ", by Chang et al., IEEE, pp. 2329-2333, 1987.
"Numerical and Experimental Analysis of 500-V Power DMOSFET . . . ,"by Chang et al., IEEE Transactions, vol. 16. NY, Nov. 1989.

Primary Examiner—Jerome Jackson, Jr.
Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

Fundmental Device Patents



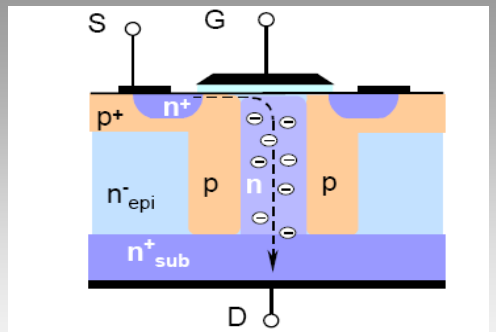
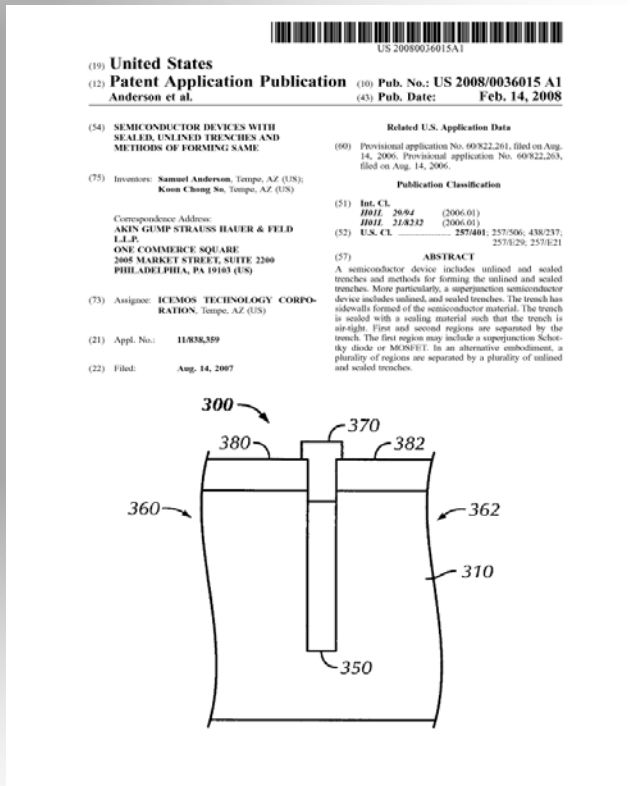


Fig. 3: Cross section of the new CoolMOS™ high voltage Power MOSFET.

Fundmental Technology Patents



US 20080036015A1

(19) United States
(12) Patent Application Publication
Anderson et al.

(10) Pub. No.: US 2008/0036015 A1
(43) Pub. Date: Feb. 14, 2008

(54) SEMICONDUCTOR DEVICES WITH SEALED, UNLINED TRENCHES AND METHODS OF FORMING SAME

(75) Inventors: Samuel Anderson, Tempe, AZ (US); Koon Chong So, Tempe, AZ (US)

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(73) Assignee: ICEMOS TECHNOLOGY CORPORATION, Tempe, AZ (US)

(21) Appl. No.: 11/838,359

(22) Filed: Aug. 14, 2007

Related U.S. Application Data

(60) Provisional application No. 60/822,261, filed on Aug. 14, 2006. Provisional application No. 60/822,263, filed on Aug. 14, 2006.

Publication Classification

(51) Int. Cl.
H01L 29/04 (2006.01)
H01L 21/8232 (2006.01)

(52) U.S. Cl. 257/401; 257/506; 438/237; 257/E29; 257/E21

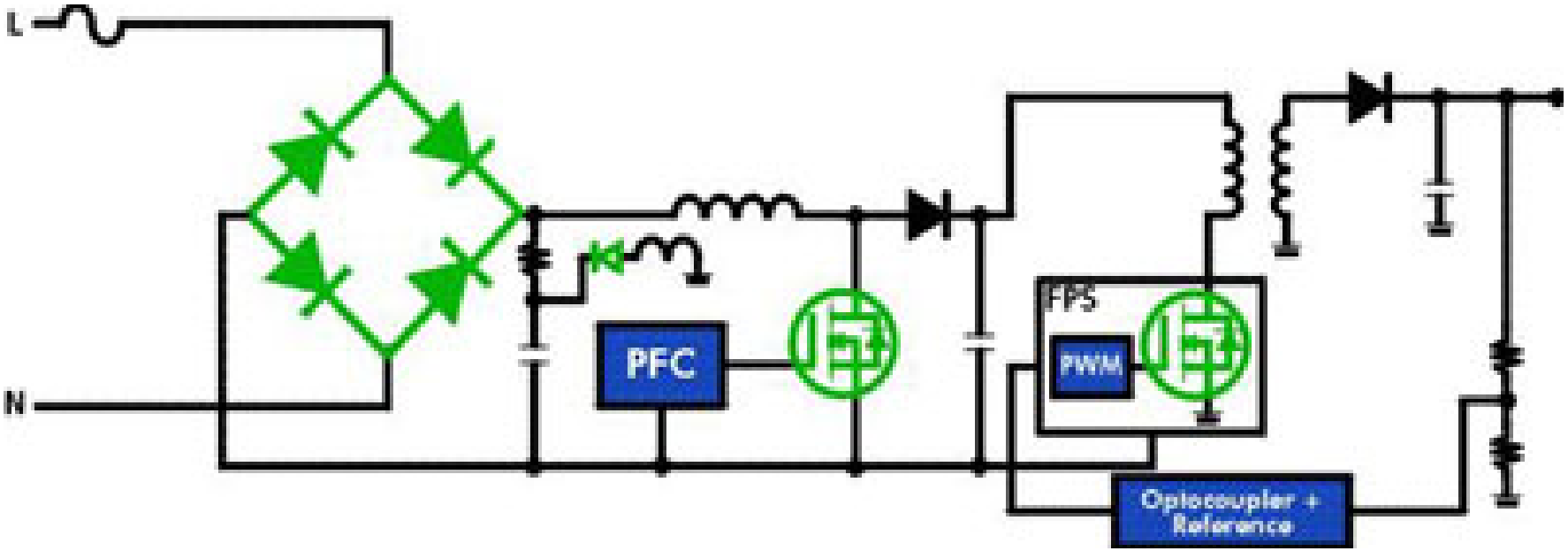
(57) ABSTRACT

A semiconductor device includes unlined and sealed trenches and methods for forming the unlined and sealed trenches. More particularly, a superjunction semiconductor device includes unlined, and sealed trenches. The trench has sidewalls formed of the semiconductor material. The trench is sealed with a sealing material such that the trench is air-tight. First and second regions are separated by the trench. The first region may include a superjunction Schottky diode or MOSFET. In an alternative embodiment, a plurality of regions are separated by a plurality of unlined and sealed trenches.

more to come …

Product Schedules

Part Number	Max. V_{DS} (V)	Max. $R_{DS(ON)}$ mΩ 10V	4.5V	2.5V	Max. I_D(A)	Qg (nC) 10V	Qgs (nC) Typ.	Qgd (nC)	Package Type	Status
ICE5N50	500	600			±20	79	21	47	DPAK	available
ICE4N65	650	800			±20	79	21	47	DPAK	available
ICE20N60	600	250			±80	105	26	42	TO220	available
ICE20N65	650	170			±20	87	11	33	TO220	available



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