Current Mode PWM Controller

Description

AT3263 is highly integrated current mode PWM control IC optimized for high performance low standby power offline fly back converter applications. To meet the international power conservation requirements, optimized green mode is integrated to improve the efficiency at light or no load conditions with no audible noise. Slope compensation is integrated to ensure the stability at high load. Lead edge blanking is integrated to prevent the false trigger at the transition of the switch. Soft switching control at the gate drive can improve the EMI performance of the power supply. The Gate-drive output is clamped at 18V to protect the power MOS. AT3263 offers many protection functions with auto self-recovery feature, including Cycle-by-Cycle current limiting, over load protection (OLP) and under voltage lockout (UVLO).

Excellent EMI performance is achieved with frequency jitter technique together with soft switching control at the totem pole gate driver.

AT3263 is offered in SOT23-6, SOP-8 and DIP-8 packages.

Features

●Frequency jitter function to improve EMI performance of power supply

●No-audible-noise green mode Control

● External Programmable PWM Switching Frequency

● Internal Slope Compensation

● Low VDD Startup Current and Low Operating Current

● Leading Edge Blanking

● UVLO

● Gate Max Output Voltage Clamp at 18V

● Overload Protection (OLP).

● Line Compensation Over Current Protection (OCP)

Applications

Offline AC/DC fly back converter for

● Battery Charger

● Power Adaptor

● Set-Top Box Power Supplies

● Open-frame SMPS

● PC 5V Standby Power

Pin Assignments

S6 Package (SOT23-6)

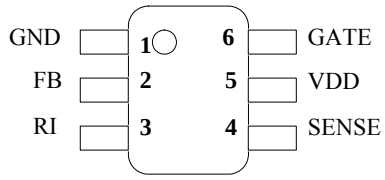


Figure 1. Pin Assignment of AT3263 for SOT23-6

PD8&SOP8 Package (P-DIP8&SOP8)

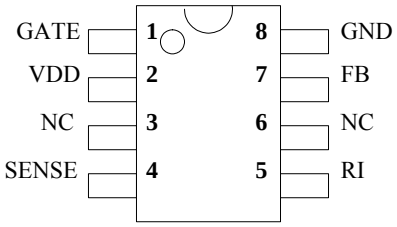
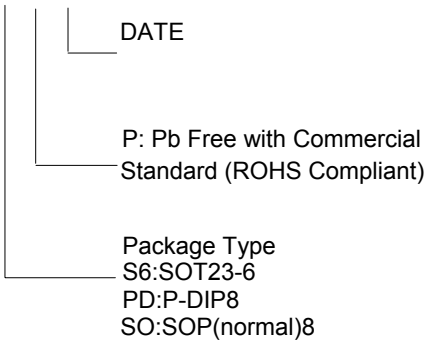


Figure 2. Pin Assignment of AT3263 for P-DIP8&SOP8

Ordering Information

AT3263□□□



Typical Application Circuit

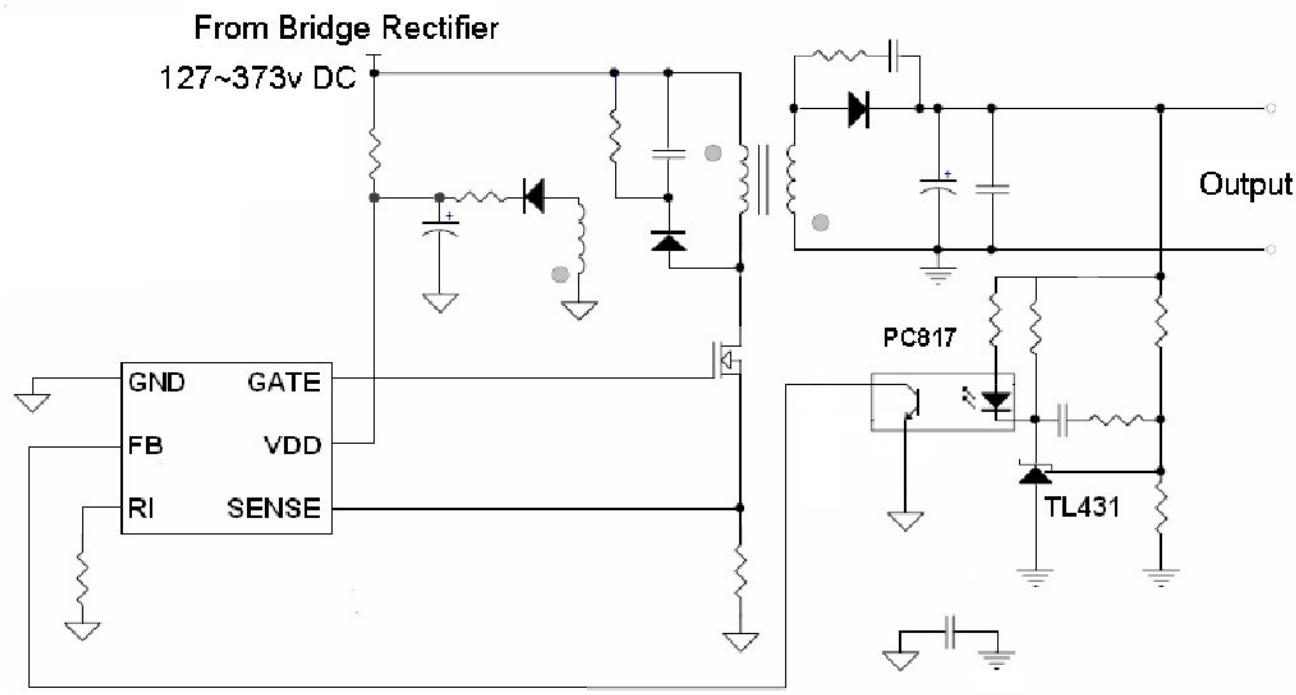


Figure3. Typical Application Circuit of AT3263

Functional Pin Description

Pin Name	Pin Function
GND	Ground
FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 6.
RI	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
SENSE	Current sense input pin. Connected to MOSFET current sensing resistor node.
VDD	Chip DC power supply pin.
GATE	Totem-pole gate drive output for the power MOSFET.

Block Diagram

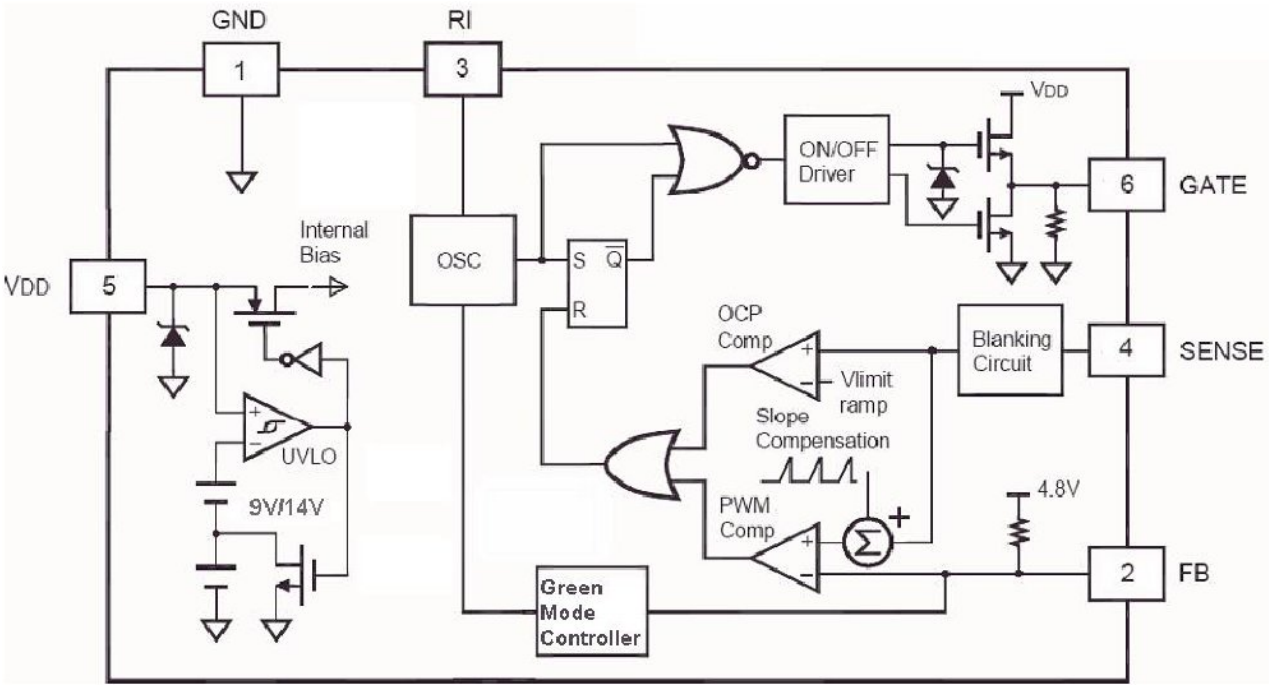


Figure 4. Block Diagram of AT3263

Absolute Maximum Ratings

- VDD to GND---------- - 0.3V to + 30V
- VDD clamped current---------- 10mA
- VFB, VSENSE and VRI to GND---------- - 0.3V to + 7V
- Junction Temperature---------- - 20°C to + 150°C
- Storage Temperature Range---------- - 55°C to + 160°C

Note：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage, V_{DD}---------- 25V
- RI resistor value---------- 100kOhm
- Operation Temperature Range---------- - 20°C to + 85°C

Electrical Characteristics

(TA = 25°C, RI=100kOhm, VDD=16V if not otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SUPPLY SECTION						
Chip start up current via VDD pin	I_set	Vdd=12V, measure current into VDD pin		5	25	uA
Operation current	I_op	VDD=16V,VFB=3V		1.4		mA
VDD UVLO enter	UVLO_L		8	9	10	V
VDD UVLO exit	UVLO_H		13	14	15	V
VDD clamp voltage	VDD_CLP	I(VDD)=10mA		34		V
FEEDBACK SECTION						
PWM input gain	A_PWM	ΔVFB/ΔVCS		2		
VFB open loop voltage	VFB_O			5.3		V
FB pin short circuit current	VFB_S	Short FB pin to gnd and measure current		0.8		mA
Zero duty cycle FB threshold	VFB_th_L			0.75		V
Power limiting FB threshold	VFB_th_P			3.7		V
Power limiting delay time	T_PL_D			35		mS
Input impedance	R_FB			6		KΩ
Maxim duty cycle	D_MAX	VDD=18V, FB=3V,CS=0		80		%
OSCILLATOR						
Normal oscillation frequency	Fosc		60	65	70	KHz
Frequency temperature stability	Δf_Temp	TA -20°C to +100°C		5		%
Frequency supply stability	Δf_Sup	VDD 12-25V		5		%
Operating RI range	RI_range		50	100	150	KΩ
RI open load voltage	RI_open			2		V
Burst mode base frequency	Fosc-BM			22		KΩ
Frequency modulate range (jitter)	Δf_OSC		-3		3	%
Jitter frequency	f_jitter			32		Hz
CURRENT SENSE SECTION						
Leading edge blanking time	T_blank			300		nS
Sense pin input impedance	R_sense			40		kΩ
Over current threshold voltage at Sense pin	VTH_OC	FB=3.3V	0.70	0.75	0.80	V
Over current protect delay	T_OC_D	CS>VTH_OC, FB=3.3V		75		nS
GATE OUTPUT						
Output low level	VOL	Io=-20mA			0.8	V
Output high level	VOH	Io=20mA	10V			V
Output voltage clamped level	VG_CLP			18		V
Output rising time	T_r	Cl=1nf		220		nS
Output falling time	T_f	Cl=1nf		70		nS

OPERATION DESCRIBTION

Over-view description

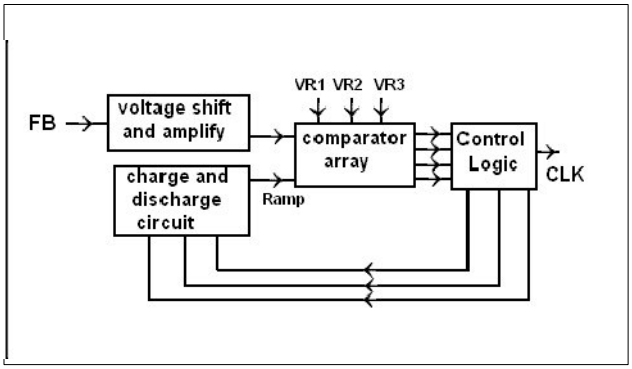
The AT3263 includes all necessary function to build an easy and cost effective solution for low power supplies to meet the international power conservation requirements.

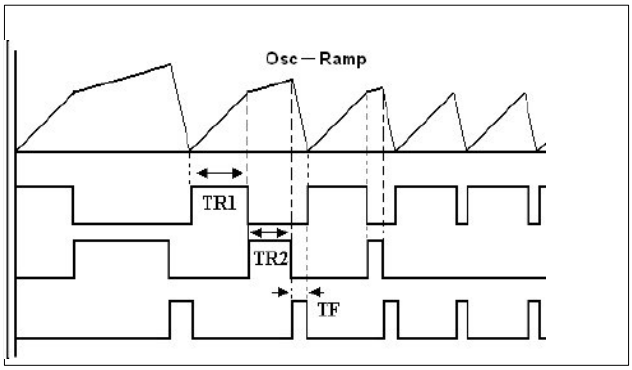
Start-up current

Startup current of AT3263 is designed to be very low so that VDD could be charged up above UVLO (exit) threshold level and device starts up quickly. Also a large value startup resistor can be used to minimize the power loss.

Green Mode Operation （Patent）

At light load or no load condition, the switch loss become the major loss of the power supply, to reduce the power wasted in light and no load condition, based on a special designed voltage controlled oscillator, green mode operation of the power supply can be achieved by using AT3263. The controller will judge the load condition base on the voltage of FB pin. In light load the FB voltage will decrease, when VFB is lower than a set threshold voltage, a FB depending time (TR2) will be generated by the oscillator and decrease the operating frequency of the power supply, the minimum frequency is set about 23kHZ. The function block and the working waveform can be depicted as below:





When VFB decrease further, the power supply will enter into burst mode operation to decrease the power consumed at no load condition. Besides there is no audible noise in any load condition.

Oscillator Operation

A resistor from RI pin to ground will generate a constant current source for AT3263. This current is used to charge/discharge an internal capacitor and hence the internal clock and switching frequency are determined. Increase the resistance will decrease the current source and reduce the switching frequency. The relation between Ri and switching frequency is:

$$f_{PWM} = \frac{6500}{R_I}(khz)$$

Built-in Slope Compensation

The sensed voltage across the sense resistor is used for pwm control, and pulse by pulse current limit, Built-in slope compensation circuit adds a voltage ramp onto the current sense input voltage. This greatly improves the close loop stability and prevents the sub-harmonic oscillation of peak current mode pwm control scheme.

Leading Edge Blanking

Each time when the power MOSFET is switched on, a turn-on spike will inevitably occur on the sense-resistor. To avoid premature termination of the switching pulse, a 270 nsec leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Gate Driver

The output stage of AT3263 is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increases efficiency and enhances reliability. The output driver is clamped by an internal 18V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

Frequency Jitter

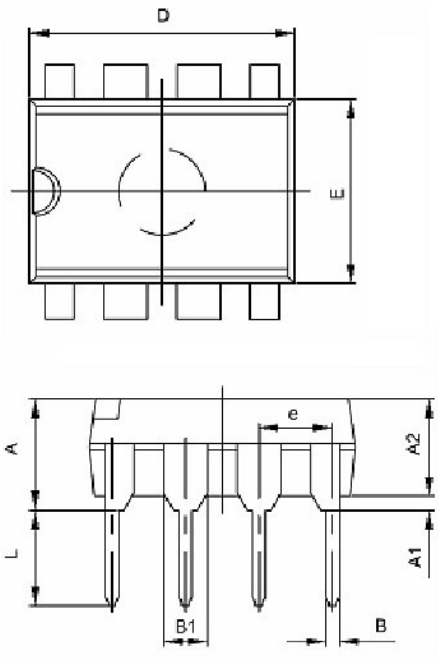
The frequency jitter function is integrated in the controller, the jitter is modulated by a periodic signal, the modulate signal frequency is much smaller than the oscillator frequency, By this way，the EMI noise has a wider spectrum with lower amplitudes.

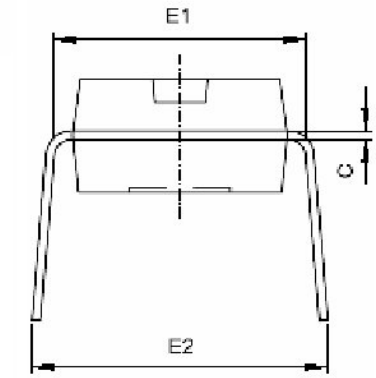
Protect Functions

To increase the reliability of power supply system many protection functions is integrated in this controller, including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO). At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL (power limit debounce time), the controller reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

Outline Information

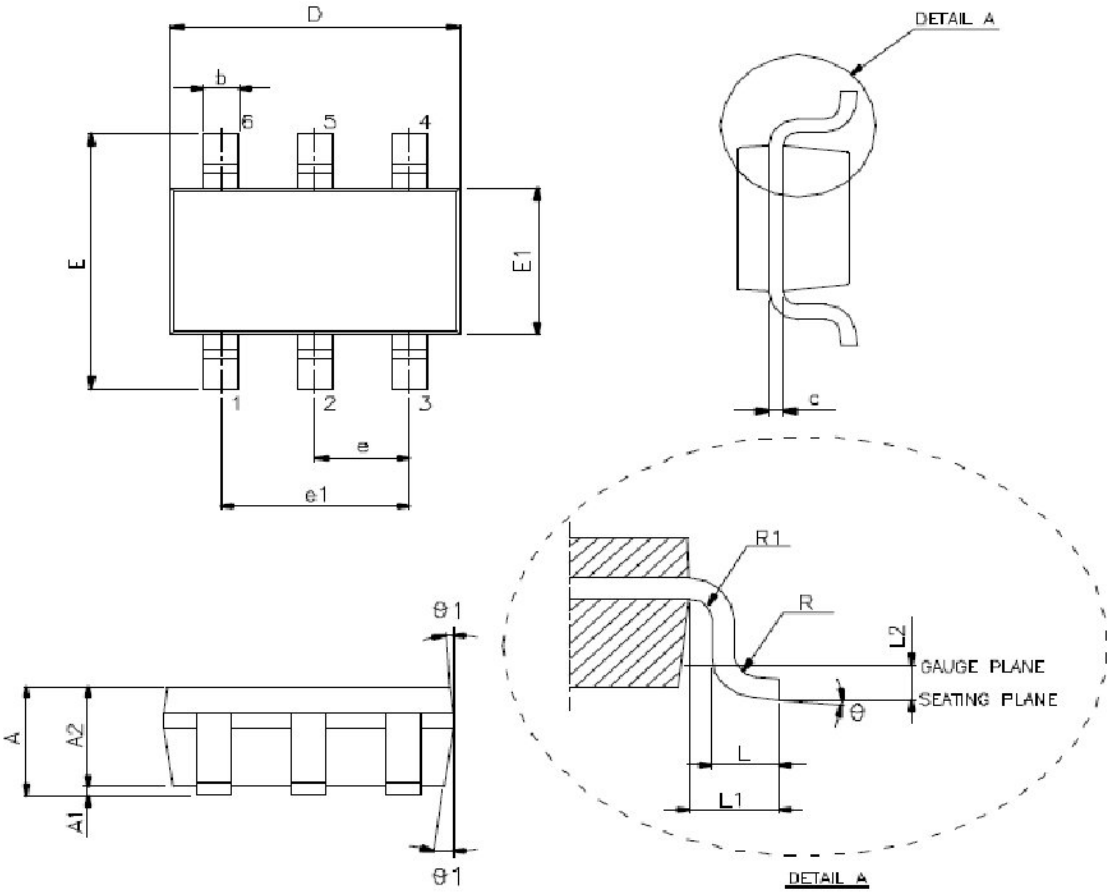
P-DIP-8 Package





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

SOT-26 Package (Unit: mm)



SYMBOL	MIN.	NOM.	MAX.	SYMBOL	MIN.	NOM.	MAX.
A	–	–	1.45	e1		1.90 BSC.	
A1	–	–	0.15	L	0.30	0.45	0.60
A2	0.90	1.15	1.30	L1		0.60 REF.	
b	0.30	–	0.50	L2		0.25 BSC.	
c	0.08	–	0.22	R	0.10	–	–
D	2.90 BSC.			R1	0.10	–	0.25
E	2.80 BSC.			θ	0°	4°	8°
E1	1.60 BSC.			θ1	5°	10°	15°
e	0.95 BSC						

-End of Specifications-

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