Features

- Cell Balance Controller for Li-ion, $LiFePO_4$ Battery Pack
- Active Charge Balance
- Automatic Synchronous Work
- Programmable Separated Balancing and Detecting Time
- Constant Off-time Modulation
- Balancing Current Operate in CCM
- External On/Off Control
- Programmable Working Voltage
- Over Temperature Protection
- Manage 1% Voltage Difference Between Two Cells
- Off Current under 1uA
- SOP-16 Package

Applications

- Portable Consumer Electronics
- Electric traffic tools(E-Bike,E-Car)
- Hand-Held Tools

General Description

The GS7708 is a cell balance controller design for Li-ion/$LiFePO_4$ battery Pack, especially for high capacity battery and high balancing current applications.

The GS7708 uses inductor to reserve energy and drives an external PMOS and an external NMOS for energy diversion between two cells. The balancing current can be set by external components L, Rcs and Coff as shown in figure 1.

To get the accurate voltage of battery, The GS7708 will stop balancing when detecting. The length of balancing time and detecting time can be set by external capacitors Cbal and Cdet as shown in figure 1.

For N cells balancing, there must be N-1 GS7708 working in a series. All the chips can synchronous working automatically, which eliminate interference of voltage detection in detecting time.

Programmable working voltage function helps users to define the minimal voltage of two cells to start balance.

External On/Off Control makes GS7708 compatible with MCU controlled BMS.

Typical Application

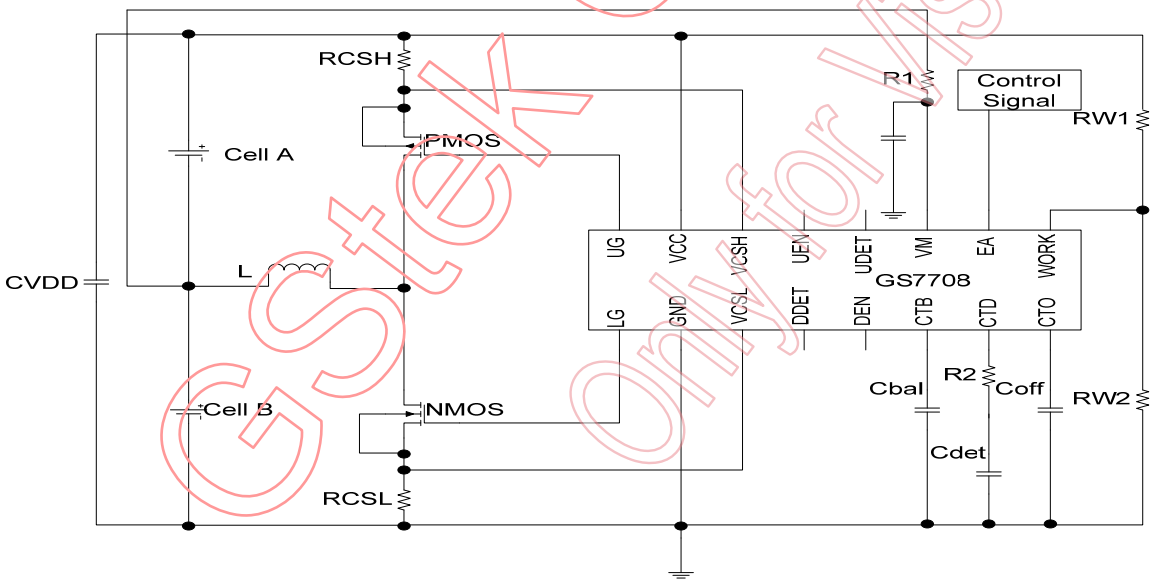


Figure 1 Typical Application Circuit of GS7708

Function Block Diagram

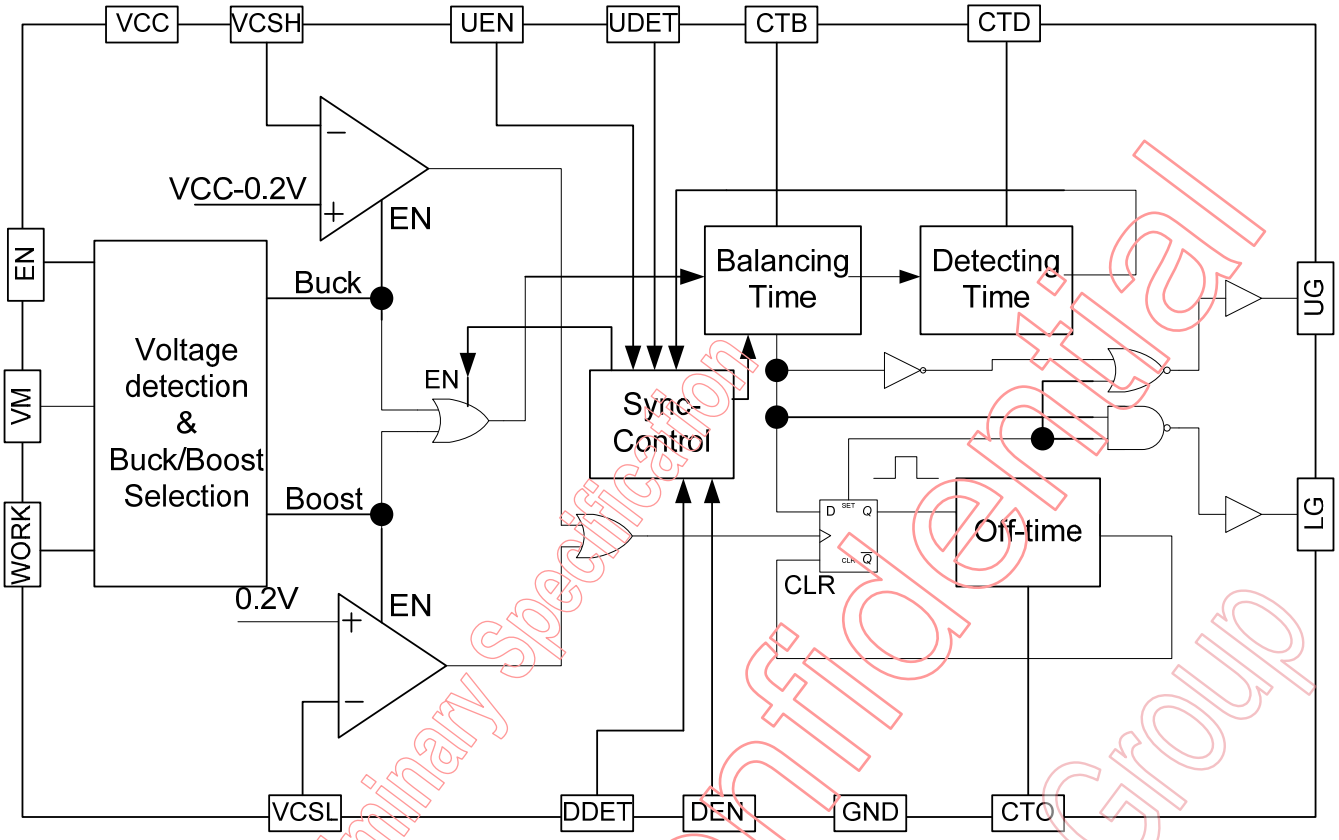


Figure 2 Function Block Diagram

Ordering Information

GS7708PP- R

1. Package
2. Shipping

No	Item	Contents
1	Package	SO: SOP-16
2	Shipping	R: Tape & Reel, T: Tube

Example: GS7708 SOP-16 Tape & Reel ordering information is “GS7708SO-R”

Pin Configuration

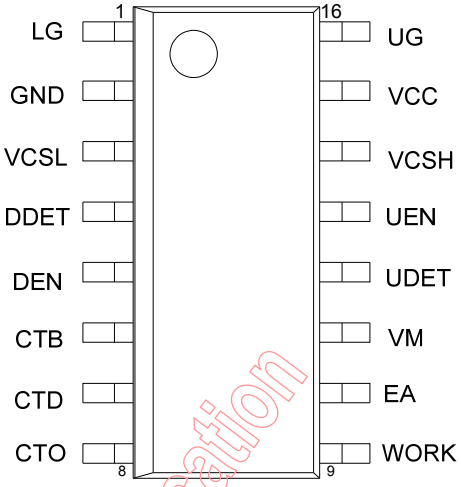


Figure 3, SOP-16 Package

Pin Descriptions

No. SOP-16	Name	I/O type	Pin Function
1	LG	O	Gate driver of external NMOSFET
2	GND	I/O	Ground pin.
3	VCSL	I	Sense the low-side peak current
4	DDET	I	Synchronous pin for receiving lower-side chip signal.
5	DEN	O	Synchronous pin for enabling lower-side chip.
6	CTB	O	Setting balancing time by a capacitor connect to gnd.
7	CTD	O	Setting detecting time by a capacitor connect to gnd.
8	CTO	O	Setting off-time by a capacitor connect to gnd.
9	WORK	I	Setting the starting voltage for cell balancing
10	EA	I	Chip enable pin
11	VM	I	Battery voltage sensing pin
12	UDET	I	Synchronous pin for receiving upper-side chip signal.
13	UEN	O	Synchronous pin for enabling upper-side chip.
14	VCSH	I	Sense the high-side peak current
15	VCC	I/O	Chip power supply
16	UG	O	Gate driver of external PMOSFET

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
VCC to GND	V_{VCC}	-0.3 ~14	V
Analogy Output Voltage	V_{CTB}, V_{CTD}, V_{CTO}	-0.3 ~6	V
Analogy Output Voltage	V_{UG}, V_{LG}	-0.3~ V_{VCC}	V
Analogy Output Voltage	V_{UEN}, V_{DEN}	-0.3~ V_{VCC}	V
Analogy Input Voltage	V_{VCSL}, V_{WORK}	-0.3 ~6	V
Analogy Input Voltage	V_{DDET}, V_{EA}, V_{VM}, V_{UDET}, V_{VCSH}	-0.3~ V_{VCC}	V
Package Power Dissipation at $T_A \leqq 25°C$	P_{D_SOP-16}	1000	mW
Junction Temperature Range	T_J	-45 ~ 150	°C
Storage Temperature Range	T_{STG}	-65 ~ 150	°C
Lead Temperature (Soldering, 10sec)	T_{LEAD}	260	°C
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}	2K	V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	θ_{JA_SOP-16}	100	°C/W

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
VCC to GND	V_{VCC}	5 ~ 8.4	V
Junction Temperature	T_J	- 40 ~ 125	°C
Ambient Temperature	T_A	-40 to 85	°C

Electrical Characteristics

(VCC =6.5V, VGND=0V, T_A = 25°C, unless noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Section						
VDD operation voltage	V_{DD}		5		8.4	V
IC off current	I_{OFF}				1	uA
IC operation current	I_{OP}	Balancing, f=200KHz		10		mA
		Static			600	uA
Enable On/Off Control						
Turn on threshold	V_{ON}	T=-40°C~125°C	2			V
Turn off threshold	V_{OFF}				0.8	V
Programmable Working Voltage						
Working threshold voltage	V_{WK}			1		V
Hysteresis	V_{WKHYS}			100		mV
Timing Section						
CT_BAL threshold voltage	V_{CT_BAL}			2		V
CT_BAL source current	I_{CT_BAL}			10		uA
CT_DET threshold voltage	V_{CT_DET}			2		V
CT_DET source current	I_{CT_DET}			10		uA
CT_OFF threshold voltage	V_{CT_OFF}			2		V
CT_OFF source current	I_{CT_OFF}			10		uA
Current Sense Section						
VCSH turn point voltage	V_{CSH}	'VCC-VCSH'		200		mv
VCSL turn point voltage	V_{CSL}			200		mv
Leading edge blanking time	T_{LEB}	Guarantee by design		300		ns

Propagation delay to turn off the Gate	T_{PDH}	VCSH PIN		130		ns
	T_{PDL}	VCSL PIN		70		ns
Gate Section						
Rising Time	T_{RH}	High-side Gate,C_L=3nF		25		ns
	T_{RL}	Low-side Gate,C_L=3nF		25		ns
Falling Time	T_{FH}	High-side Gate,C_L=3nF		25		ns
	T_{FL}	Low-side Gate,C_L=3nF		25		ns
Dead Time	T_{DH}	High to Low,C_L=3nF		10		ns
	T_{DL}	Low to High,C_L=3nF		10		ns
SYN Control (Note 5)						
UEN sink current	I_{UEN}			-120		uA
DEN source current	I_{DEN}			120		uA
UDET sink current	I_{UDET}			-90		uA
DDET source current	I_{DDET}			90		uA
Balancing Function						
Balancing function start when the difference voltage of two cells greater than V_{UBAL}	V_{UBAL}				0.01*VCC	mV
The difference voltage of two cells is less than V_{BAL} when balancing function finished	V_{BAL}				0.007*VCC	mV
Over Temperature Protection						
Threshold Temperature	T_{OTP}			150		°C
Hysteresis	T_{HYS}			30		°C

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

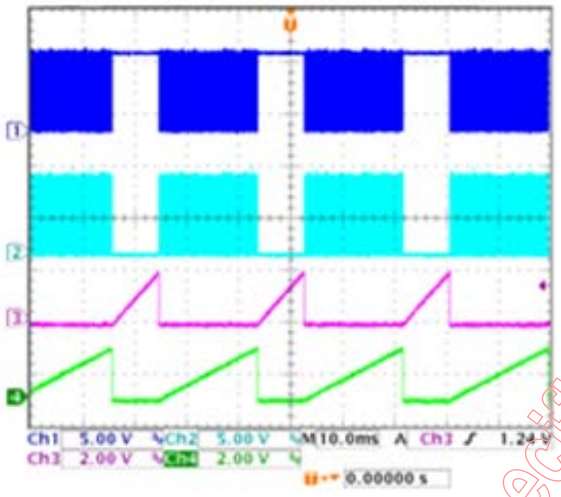
Note 3. θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

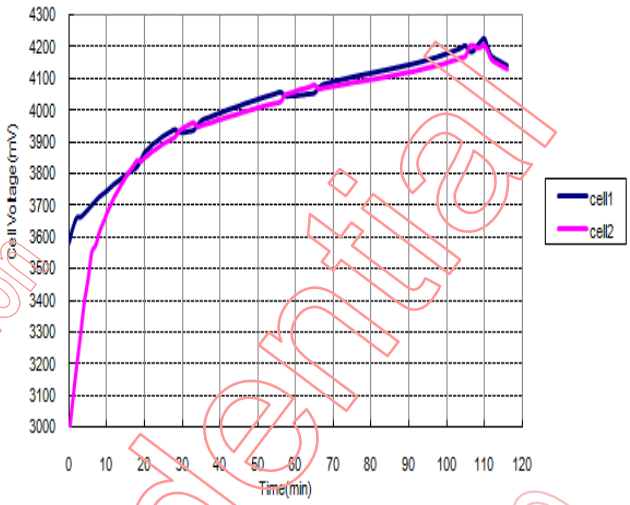
Note 5. Negative value means current flow into this pin.

Typical Performance

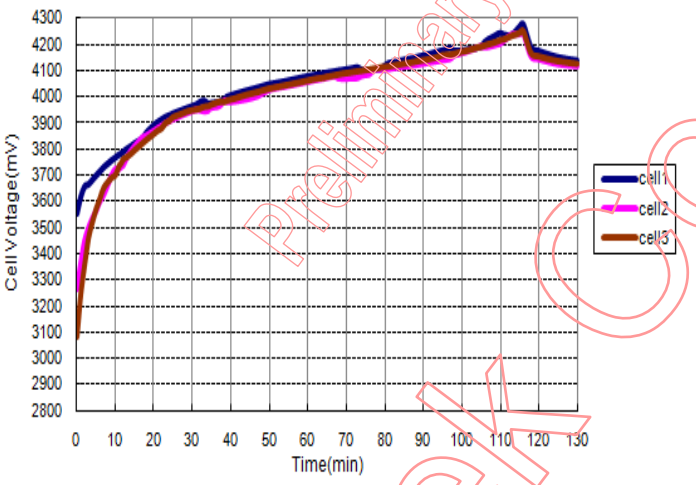
Balancing Working Sequency
(CH1:UG CH2:LG CH3:CTD CH4:CTB)



Two Cell Balancing



Three Cells Balancing
(Two Chips Synchronous Working)



Functional Descriptions

EA On/Off Control

The GS7708 is turned off when V_{EA}<0.8V and consume under 1uA current; GS7708 is turned on when V_{EA}>2V.

Programmable Working Voltage

The starting voltage of balancing function can be programmed in GS7708. User may define it by adjusting RW1 and RW2. The defined starting voltage is

$V_{defined}=V_{WK}*(1+RW1/RW2)$

For example, if RW1=40kΩ, RW2=10kΩ, then the defined working voltage is 5V.

Cell Balance Movements

The GS7708 drives a PMOS switch which is in parallel with the upper cell and a NMOS switch which is in parallel with the lower one.

The GS7708 turns on the PMOS switch first when the upper cell voltage is higher than the lower one, otherwise, it turns on the NMOS switch first if the lower cell voltage is higher.

Separated Detection and Balance

The GS7708 will stop balancing when detecting the middle voltage of two cells, thus, the interference caused by balancing current can be avoided, a much more reliable battery voltage we could get for the next period of balancing.

Programmable Balancing Time

The balancing time of GS7708 can be programmed by capacitor C_{Bal} seen in fig. 1. The timing current of CTB pin is I_{CT_BAL}, the threshold voltage is V_{CT_BAL}, thus

$T_{Bal}=(C_{Bal}* V_{CT\_BAL})/ I_{CT\_BAL}$

Programmable Detecting Time

The same as balancing time, the detecting time of GS7708 can be programmed by capacitor C_{Det}

$T_{Det}=(C_{Det}*V_{CT\_DET})/ I_{CT\_DET}$

Programmable Off-time

The GS7708 is off-time modulation, the off-time can be programmed by capacitor C_{Off} seen in Figure 1.

$T_{Off}=(C_{Off}*V_{CT\_OFF})/ I_{CT\_OFF}$

Balancing Current Design

To design the balancing current, the balancing current waveform (peak and ripple) should be determined first,

$I_{Balance}=I_{peak}-I_{ripple}/2$ (1)

For example, a 4.5A balancing current with peak current 6A, ripple 3A and frequency is 200KHz, assume the voltage of each cell is 3.2V, thus, the off-time T_{OFF} is $1/2f_s$=2.5us,

$C_{Off}=T_{Off}*I_{CT\_OFF}/V_{CT\_OFF}=2.5u*10u/2=12.5pF$ (2)

$R_{CS}=V_{CS}/I_{peak}=0.2/6=33m\Omega$ (3)

$L=V_{cell}*T_{OFF}/I_{ripple}=3.2*2.5u/3=2.67uH$ (4)

Make sure that the balancing current is operating in CCM.

Synchronous Control

To eliminate interference of voltage detection in detecting time, the GS7708 can automatic synchronous balancing and detecting while two or more chips working together. This function is realized by connecting UDET, UEN pin to DEN, DDET pin of the upper chip and connecting DEN, DDET pin to UDET, UEN pin of the lower one.

The max number N_{MAX} of GS7708 that can work in a series is determined by the SYN control time and the propagation delay time of SYN signals.

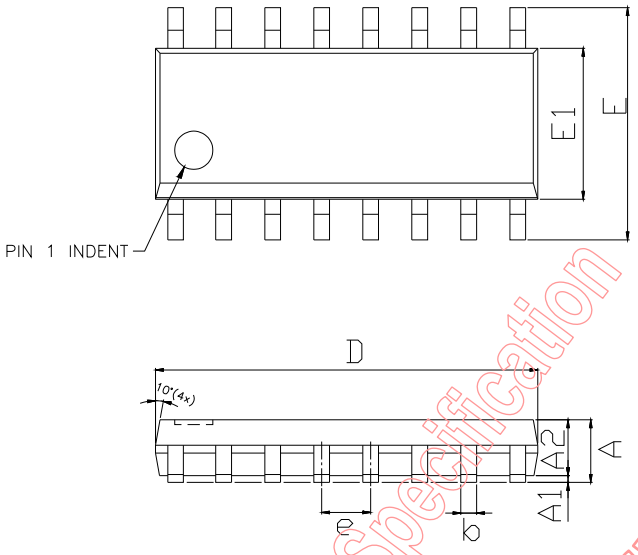
Assume UEN rising delay time (or DEN fall delay time) is T_{OD} and UEN falling delay time (or DEN rise delay time) is T_{CD}, usually $T_{OD}<T_{CD}$, thus

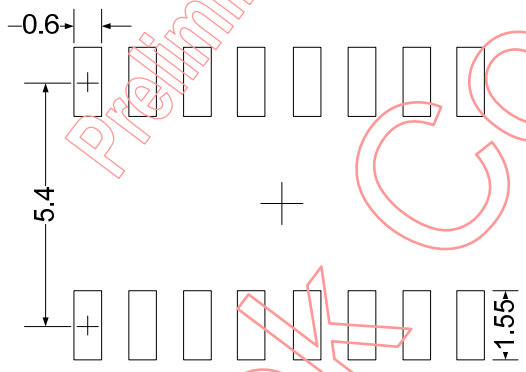
$N_{MAX}=T_{CLOSE\_SYN}/T_{CD}+1$ (1)

If $T_{OD}>T_{CD}$ for special reasons, then

$N_{MAX}=T_{OPEN\_SYN}/T_{OD}+1$ (2)

Package Dimensions, SOP-16





Unit: mm

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.45 REF.	
b	0.33	0.51
C	0.17	0.25
D	9.80	10.20
E	5.79	6.20
E1	3.80	4.00
e	1.27 REF.	

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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