ICE2QRxx65/80x

Quasi Resonance CoolSET Design Guide

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Power Management & Supply

Never stop thinking.

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1 Introduction

This design guide describes how to design quasi-resonant flyback converters using ICE2QRxx65/80x, which is a new Quasi-resonant PWM CoolSET developed by Infineon Technologies
Firstly, the basic description of CoolSET will be given including the main features and Pin's layout. Then an overview of quasi-resonant flyback converter will be given, followed by the introduction of ICE2QRxx65/80x's functions and operations. A typical application example, input power curves, PCB layout recommendation, product profolio and design equations will be given in the last part of this document.

2 CoolSET description

ICE2QRxxxx is a second generation quasi-resonant PWM CoolSET with power MOSFET and startup cell in a single package optimized for off-line power supply applications such as LCD TV, and notebook adapter. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system average efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption at standby mode operation and low output voltage ripple. The numerous protection functions give a full protection of the power supply system in failure situation. All of these make the ICE2QRxx65/80x an outstanding power CoolSET for quasi-resonant flyback converter in the market.
In addition, numerous protection functions have been implemented in the CoolSET to protect the system and customize the CoolSET for the chosen applications. All of these make the ICE2QRxx65/80x an outstanding product for real quasi-resonant flyback converter in the market.

2.1 Main features

- High voltage (650V/800V) avalanche rugged CoolMOS® with startup cell
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in high voltage startup cell
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- Foldback Point Correction with digitalized sensing and control circuits
- VCC undervoltage and overvoltage protection with Autorestart mode
- Over Load /open loop Protection with Autorestart mode
- Built-in Over temperature protection with Autorestart mode
- Adjustable output overvoltage protection with Latch mode
- Short-winding protection with Latch mode
- Maximum on time limitation
- Maximum switching period limitation

2.2 Pin layout

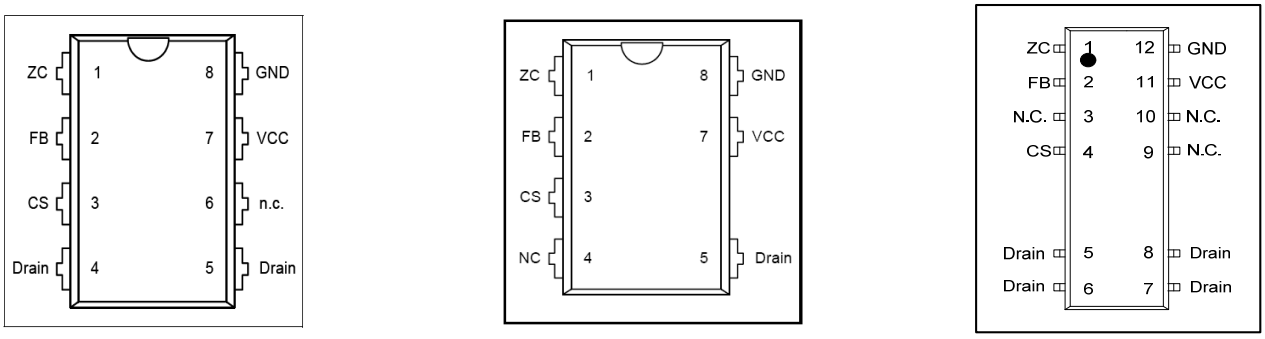


Figure 1 Pin configurations (top view), DIP-8 version; DIP-7 (Z) version; and DSO-12 (G) version;

2.3 Pin functions

2.3.1 ZC (Zero Crossing)

Three functions are incorporated at the ZC pin. First, during MOSFET off time, the de-magnetization of the transformer is detected when the ZC voltage falls below V_{ZCCT} (100mv). Second, after the MOSFET is turned off, an output overvoltage fault will be assumed if V_{ZC} is higher than V_{ZCOVP} (3.7V). Finally, during the MOSFET on time, a current depending on the bus voltage flows out of this pin. Information on this current is then used to adjust the maximum current limit. More details on this function are provided in Section 4.

2.3.2 FB (Feedback)

Usually, an external capacitor is connected to this pin to smooth the feedback voltage. Internally, this pin is connected to the PWM signal generator for switch-off determination (together with the current sensing signal), and to the digital signal processing for the frequency reduction with decreasing load during normal operation. Additionally, the openloop/overload protection is implemented by monitoring the voltage at this pin.

2.3.3 CS (Current Sensing)

This pin is connected to the shunt resistor for the primary current sensing externally and it is also used to determine the PWM signal generator for switch-off (together with the feedback voltage) internally. Moreover, short-winding protection is realised by monitoring the V_{cs} voltage during on-time of the main power switch.

2.3.4 Drain

This pin is connected to the drain of the 650V/800V CoolMOS®.

2.3.5 VCC (Power supply)

The VCC pin is the positive supply of the CoolSET and should be connected to auxiliary winding of the main transformer.

2.3.6 GND (Ground)

This is the common ground of the CoolSET. Note that the current sense resistor ground should be connected to bulk capacitor ground in order to avoid strong noise interruption.

3 Overview of quasi-resonant flyback converter

Figure 2 shows a typical application of ICE2QRxx65/80x in quasi-resonant flyback converter. In this converter, the mains input voltage is rectified by the diode bridge and then smoothed by the capacitor C_{bus} where the bus voltage V_{bus} is available. The transformer has one primary winding W_p, one or more secondary windings (here one secondary winding W_s), and one auxiliary winding W_a. When quasi-resonant control is used for the flyback converter, the typical waveforms are shown in Figure 3. The voltage from the auxiliary winding provides information about demagnetization of the power transformer, the information of input voltage and output voltage.

As shown in Figure 3, after switch-on of the power switch the voltage across the shunt resistor V_{CS} shows a spike caused by the discharging of the drain-source capacitor. After the spike, the voltage V_{CS} shows information about the real current through the main inductance of the transformer L_p. Once the measured current signal V_{CS} exceeds the maximum value determined by the feedback voltage V_{FB}, the power switch is turned off. During this on-time, a negative voltage proportional to the input bus voltage is generated across the auxiliary winding.

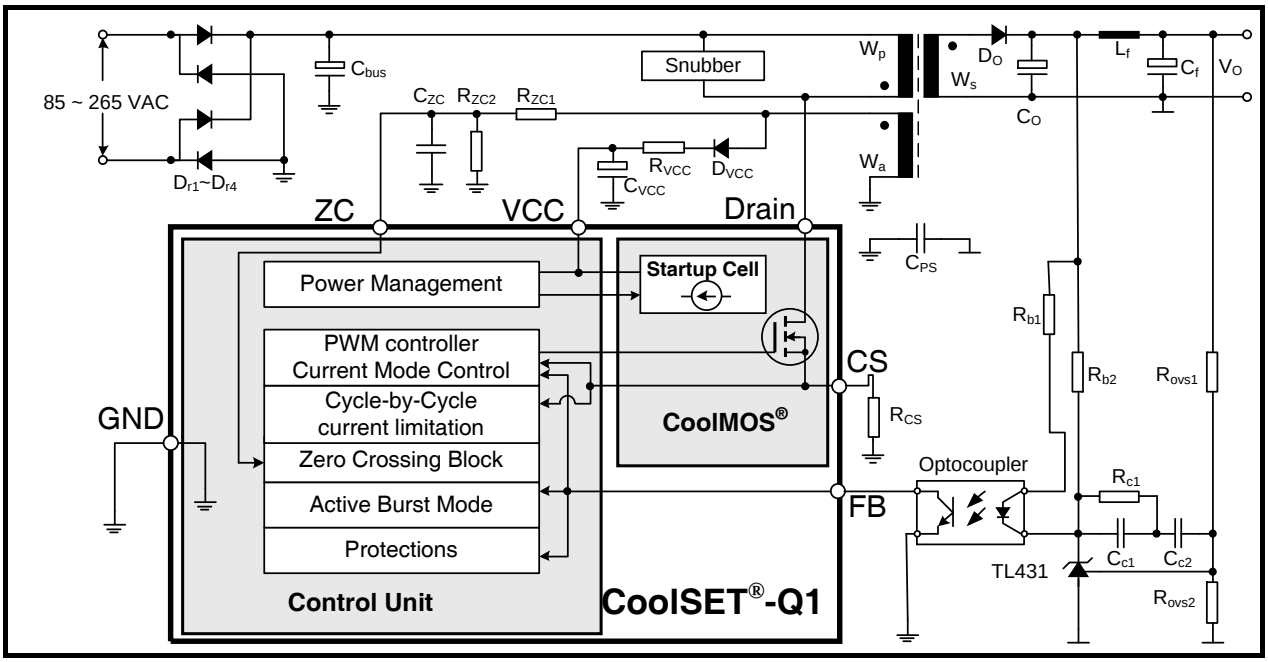


Figure 2 Typical Application of ICE2QRxx65/80x

The drain-source voltage of the power switch V_{ds} will rise very fast after MOSFET is turned off. This is caused by the energy stored in the leakage inductance of the transformer. A snubber circuit, RCD in most cases, can be used to limit the maximum drain source voltage caused. After the oscillation 1, the drain-source voltage goes to its steady value. Here, the voltage v_{Refl} is the reflected value of the secondary voltage at the primary side of the transformer and is calculated as:

$$V_{Refl} = \frac{V_{out} + V_{do}}{n} \quad (1)$$

where n the turns ratio of the transformer, which is defined in this document as:

$$n = N_S/N_P \quad (2)$$

with N_p and N_s are the turns count of the primary and secondary winding, respectively.

After the oscillation 1 is damped, the drain-source voltage of the power switch shows a constant value of $V_{bus}+V_{Refl}$ until the transformer is fully demagnetized. This duration builds up the first portion of the off-time t_{off1}.

After the secondary side current falls to zero, the drains-source voltage of the power switch shows another oscillation (oscillation 2 in Figure 3, this is also mentioned as the main oscillation in this document). This oscillation happens in the circuit consisting of the equivalent main inductance of the transformer L_p and the capacitor across the drain-source (or drain-ground) terminal C_{DS} which includes $C_{o(er)}$ of the MOSFET. The frequency of this oscillation is calculated as:

$$f_{OSC2} = \frac{1}{2\pi\sqrt{L_P \cdot C_{DS}}} \quad (3)$$

The amplitude of this oscillation begins with a value of v_{Refl} and decreases exponentially with the elapsing time, which is determined by the losses factor of the resonant circuit. The first minimum of the drain voltage appears at the half of the oscillation period after the time t_4 and can be apporximated as:

$$V_{dsMin} = V_{bus} - V_{Refl} \quad (4)$$

In the quasi-resonant control, the power switch is switched on at the minimum of the drain-source voltage. From this kind of operation, the switching-on losses are minimized, and switching noise due to dV_{ds}/dt is reduced compared to a normal hard-switching flyback converter.

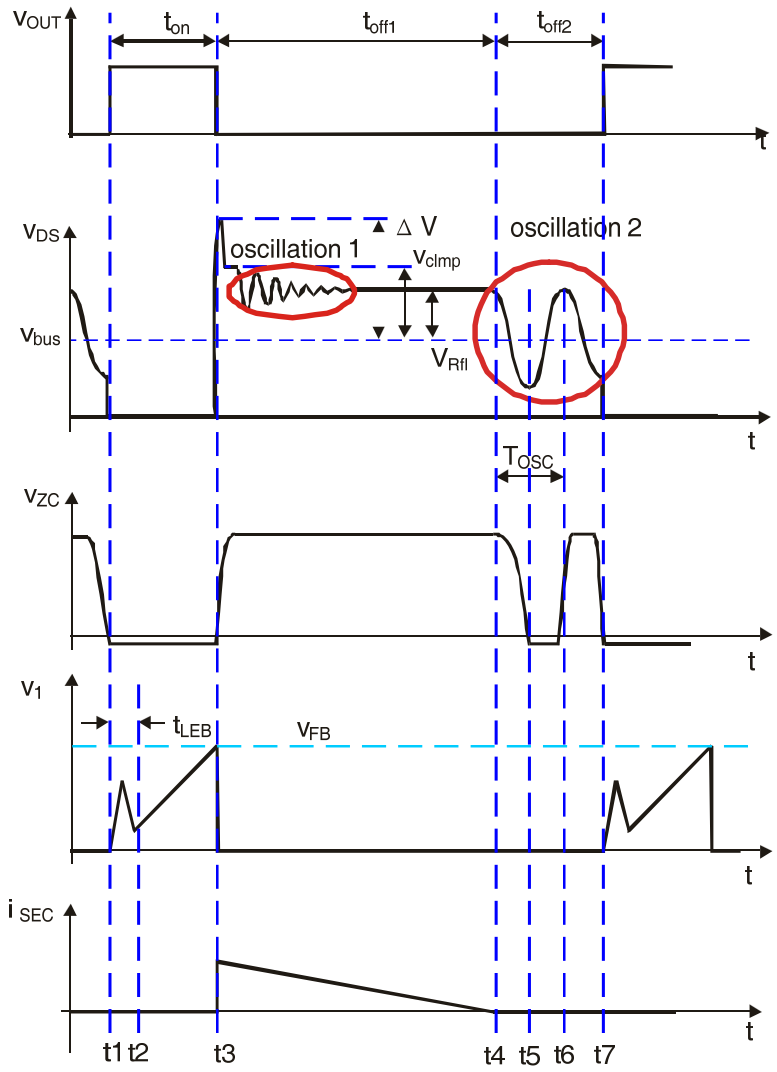


Figure 3 Key waveforms of a quasi-resonant flyback converter

4 Functional description and component design

4.1 VCC Pre-Charging and Typical VCC Voltage During Start-up

In the CoolSET ICE2QRxx65/80xx, a startup cell is integrated to the CoolMOS. The startup cell provides a pre-charging of the VCC capacitor till VCC voltage reaches the VCC turned-on threshold V_{VCCon} and the CoolSET begins to operate.

Once the mains input voltage is applied, a rectified voltage shows across the capacitor C_{bus}. The high voltage device provides a current to charge the VCC capacitor C_{vcc}. Before the VCC voltage reaches a certain value, the amplitude of the current through the high voltage device is only determined by its channel resistance and can be as high as several mA. After the VCC voltage rises to certain level, the CoolSET controls the startup cell so that a constant current around 1mA is provided to charge the VCC capacitor. It stops until the VCC voltage exceeds the turned-on threshold V_{VCCon}. As shown in the time phase I of Figure 4, the VCC voltage increase almost linearly.

The time taken for the charging VCC to turn-on threshold can then be approximately calculated as:

$$t_1 = \frac{V_{VCCon} \cdot C_{VCC}}{I_{VCCcharge2}} \quad [5]$$

where $I_{VCCcharge2}$ is the charging current from the startup cell which is 1.1mA, typically.

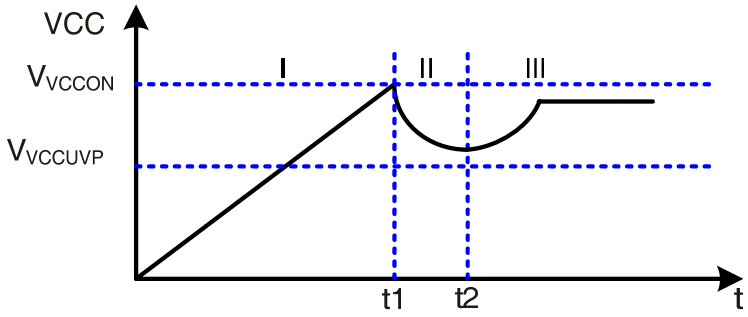


Figure 4 VCC voltage at start up

When the VCC voltage exceeds the turned-on threshold V_{VCCon} at time t_1, the startup cell is switched off, and the CoolSET begins to operate with a soft-start. Because the energy from the auxiliary winding is not enough to supply the CoolSET operation when output voltage is low, the VCC voltage drops (Phase II). Once the output voltage is high enough, the VCC capacitor receives energy from the auxiliary winding from the time point t_2 on. The VCC voltage will then reach a constant value depending on output load.

Precaution : For a typical application, start up should be VCC ramps up first, other pin (such as FB pin) voltage will follow VCC voltage to ramp up. It is recommended not to have any voltage on other pins (such as FBB; BBA and CS) before VCC ramps up.

4.1.1 VCC Capacitor

Since there is a VCC undervoltage protection, the capacitance of the VCC capacitor should be selected to be high enough to ensure that enough energy is stored in the VCC capacitor so that the VCC voltage will never touch the VCC under voltage protection threshold V_{VCCUVP} before the output voltage is built up. Therefore, the capacitance should fulfill the following requirement:

$$C_{VCC} \geq \frac{I_{VCCop} \cdot (t_2 - t_1)}{V_{VCCon} - V_{VCCUVP}} \quad [6]$$

with I_{VCCop} the operating current of the CoolSET.

4.2 Soft-Start

After CoolSET supply voltage is higher than 18V, which corresponding to t1 of Fig.4, CoolSET will start switch with a soft start. The soft start function is built inside the CoolSET in a digital manner. During softstart, the peak current of the MOSFET is controlled by an internal voltage reference instead of the voltage on FB pin. The maximum voltage on CS pin for peak current control is increased step by step as shown in Figure 5. The maximum duration of softstart is 12ms with 4ms for each step.
During softstart, the over load protection function is disabled.

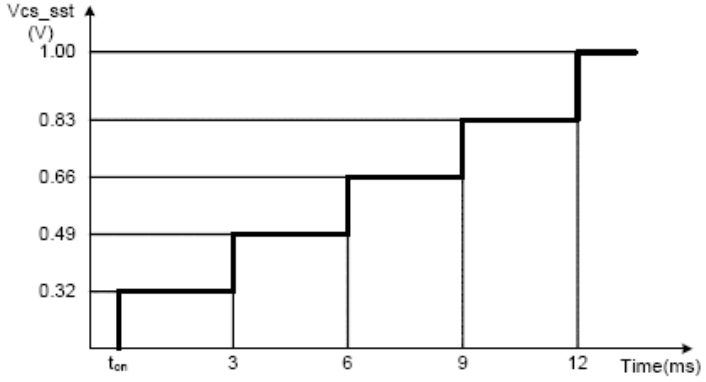


Figure 5 Maximum current sense voltage during softstart

4.3 Normal Operation

The PWM section of the CoolSET can be divided into two main portions: PWM controller for normal operation and PWM controller for burst mode operation. The PWM controller for normal operation will be described in the following paragraphs, while the PWM controller for burst mode operation will be discussed in the next section.
The PWM controller for normal operation consists of digital signal processing circuit including an up/down counter, a zero-crossing counter (ZC-counter) and a comparator, and analog circuit including a current measurement unit and a comparator. The switch-on and -off time point is determined by the digital circuit and the analog circuit, respectively. As input information for the switch-on determination, the zero-crossing input signal and the value of the up/down counter are needed, while the feedback signal V_{FB} and the current sensing signal V_{CS} are necessary for the switch-off determination. Details about the operation of the PWM controller in normal operation are illustrated in the following paragraphs.

4.3.1 Switch-on Determination

As mentioned above, the digital signal processing circuit consists of an up/down counter, a zero-crossing counter and a comparator. A ringing suppression time controller is implemented to avoid mistriggering by the ring after MOSFET is turned off. Functionality of these parts is described as in the following.

4.3.1.1 Up/down Counter

The up/down counter stores the number of zero crossing to be detected to switch on the main power switch after demagnetisation of the transformer. This value is a function of the feedback voltage, V_{FB} which contains information about the output power. Generally, a high output power results in a high feedback voltage, V_{FB} According to this information, the value in the up/down counter is changed to a low value in case of high feedback voltage, and to a high value in case of low feedback voltage. In ICE2QRxx65/80x, the lowest value of the counter is 1 and the highest 7. Following text explains how the up/down counter value changes in response to the feedback voltage V_{FB}. The feedback voltage V_{FB} is internally compared with three thresholds V_{FBZL}, V_{FBZH} and V_{FBR1}. According to the results, the value in the up/down counter is changed, which is summarised in Table 1 and Figure 6 respectively.
According to the comparison results the up/down counter counts upwards, keeps unchanged or counts downwards. However, the value in up/down counter is limited between 1 and 7. If the counter tends to count beyond this range, the attempt is ignored.
In normal case, the up/down counter can only be changed by one each time at the clock period of 48ms. However, to ensure a fast response to load increase, the counter is set to 1 in the following switching period after the regulation feedback V_{FB} exceeds the threshold V_{FBR1}.

V_{FB}	Up/down counter action
Always lower than V_{FBZL}	Count upwards until 7
Once higher than V_{FBZL}, but always lower than V_{FBZH}	No changes
Once higher than V_{FBZH}, but always lower than V_{FBR1}	Count downwards until 1
Once higher than V_{FBR1}	Counter set to 1

Table 1 Operation of the up/down counter

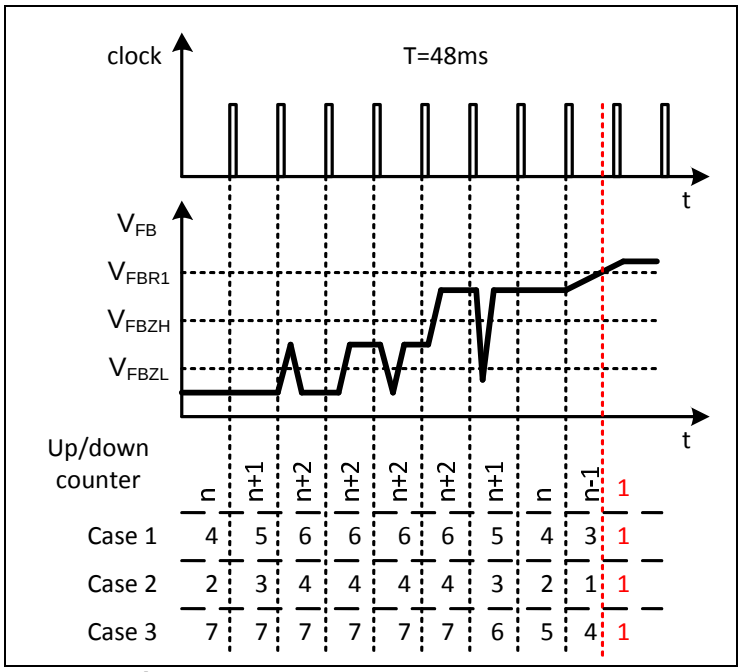


Figure 6 Up/down counter operation

4.3.1.2 Switch-on Determination

In the system, turn-on of the power switch depends on the value of the up/down counter, the value of the zero-crossing counter and the voltage at the ZC pin V_{ZC}. Turn-on happens only when the value in the both counters is the same and the voltage at the ZC is lower than the threshold V_{ZCCT}. For comparison of the values from both counters, a digital comparator is used. Once these counters have the same value, the comparator generates a signal which sets the on/off flip-flop, only when the voltage V_{ZC} is lower than the threshold V_{ZCCT}.
Another signal which may trigger the digital comparator is the output of a T_{sMax} clock signal, which limits the maximum off time to avoid the low-frequency operation.
During active burst mode operation, the digital comparator is disabled and no pulse will be generated.

4.3.2 Switch-off Determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between Current Sense pin and the common ground. The sensed voltage across the shunt resistor V_{CS} is applied to an internal current measurement unit, and its output voltage V_1 is compared with the feedback voltage V_{FB}. Once the voltage V_1 exceeds the voltage V_{FB}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V_1 and the V_{CS} is described by:

$$V_1 = G_{PWM} \cdot V_{CS} + V_{PWM} \quad [7]$$

where G_{PWM}=3.3, V_{PWM}=0.7
To avoid mistriggering caused by the voltage spike across the shunt resistor after switch-on of the main power switch, a 330ns leading edge blanking time (t_{LEB}) is applied to the output of the comparator.

4.4 Active Burst Mode Operation

At very low load condition, the CoolSET enters active burst mode operation to minimize the input power. Details about active burst mode operation are explained in the following paragraphs.

4.4.1 Entering Active Burst Mode Operation

For determination of entering active burst mode operation, three conditions apply:

- The feedback voltage is lower than the threshold of V_{EB}(1.25V). Accordingly, the peak voltage across the shunt resistor is 0.17V;
- The up/down counter has its maximal value of 7;
- The two above conditions have to been fulfilled for a certain blanking time duration t_{BEB} (30ms)

Once all of these conditions are fulfilled, the active burst mode flip-flop is set and the CoolSET enters burst mode operation and the gate will be turned off until V_{FB} increase to on threshold V_{BH}. The total blanking time to enter the active burst mode depends on the up counting time and the 30ms extra blanking time.

$$T_{totalblanking} = (7 - counter\_value) \times 48ms + 30ms$$

For example. If before the load change, current up/down counter value is 3, then the total blanking time will be:
(7-3) x 48ms + 30ms = 222ms.
This multi-conditional determination for entering active burst mode operation prevents mistriggering of entering active burst mode operation, so that the CoolSET enters active burst mode operation only when the output power is really low during the preset blanking time.

4.4.2 During Burst Mode Operation

After entering the Active Burst Mode the feedback voltage rises as V_O starts to decrease due to the inactive PWM section. One comparator observes the feedback signal if the voltage level V_{BH} (3.6V) is exceeded. In that case the internal circuit is again activated by the internal bias to start with switching.
Turn-on of the power MOSFET is triggered by the timer. The PWM generator for burst mode operation composes of a timer with a fixed frequency of 52 kHz, typically, and an analog comparator. Turn-off is resulted by comparison of the voltage signal V_1 with an internal threshold, by which the voltage across the shunt resistor V_{csB} is 0.34V, accordingly. A turn-off can also be triggered by the maximal duty ratio CoolSET which sets the maximal duty ratio to 50%. In operation, the output flip-flop will be reset by one of these signals which come first.

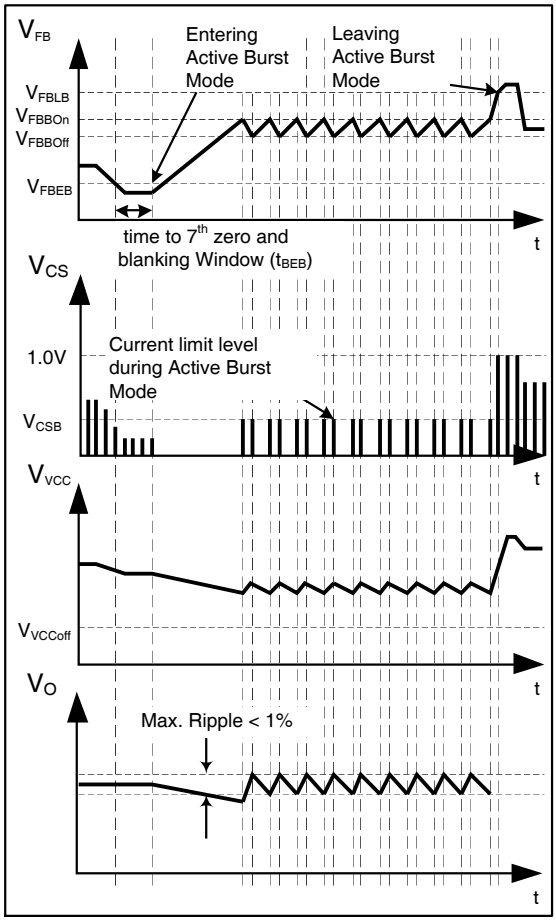


Figure 7 Signals in active burst mode

If the output load is still low, the feedback signal decreases as the PWM section is operating. When feedback signal reaches the low threshold V_{BL}(3.0V), the internal bias is reset again and the PWM section is disabled until next time regultaion signal increases beyond the V_{BH} threshold. During the active burst mode the feedback signal is changing like a saw tooth between 3.0V and 3.6V shown in Figure 7.

4.4.3 Leaving Active Burst Mode

The feedback voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 34% during active burst mode a certain load is needed so that feedback voltage can exceed VLB (4.5V). After leaving active burst mode, maximum current can now be provided to stabilize V_O. In addition, the up/down counter will be set to 1 immediately after leaving active burst mode. This is helpful to decrease the output voltage undershoot.

4.5 Current sense

The PWM comparator inside the CoolSET has two inputs: one from current sense pin and the other from feedback voltage. Before being sent to the PWM comparator, there is an offset and operational gain on current sense voltage. In normal operation, the relationship between feedback voltage and maximum current sense voltage is determined by equation (8).

$$V_{FB} = G_{PWM} V_{CS\_pk} + V_{PWM} \quad (8)$$

where G_{PWM}=3.3 and V_{PWM}=0.7

The absolute maximum current sense voltage, V_{CS_PK} is 1V. Therefore, the current sense resistor can be chosen according to the maximum required peak current in the transformer as shown in (9).

$$R_{CS} = 1 / I_{pk\_p} \quad (9)$$

The design procedure of quasi-resonant flyback transformer is shown in [2]. In addition, a leading edge blanking (LEB) is already built inside the current sense pin. The typical value of leading edge blanking time is 330ns, which can be thought as a minimum on time.

4.6 Feedback

Inside the CoolSET, the feedback (FB) pin is connected to the 5V voltage source through a pull-up resistor R_{FB}. Outside the CoolSET, this pin is connected to the collector of opto-coupler. Normally, a ceramic capacitor C_{FB}, 1nF for example, can be put between this pin and ground for smooting the signal.

Feedback voltage will be used for a few functions as following:

- It determines the maximum current sense voltage, equivalent to the transformer peak current.
- It determines the ZC counter value according to load condition

4.7 Zero crossing

The circuit components connected to zero crossing (ZC) pin include resistors R_{ZC1} and R_{ZC2} and capacitor C_{ZC}. The values of three components shall be chosen so that the three functions combined to this pin will perform as designed.

At first, the ratio between R_{ZC1} and R_{ZC2} is chosen first to set the trigger level of output overvoltage protection. Assuming the protection level of output voltage is V_{O_OVP}, the turns of auxiliary winding is Na and the turns of secondary output winding is Ns, the ratio is calculated as

$$\frac{R_{ZC2}}{R_{ZC1} + R_{ZC2}} < V_{ZCOVP} \frac{N_S}{V_O N_a} \quad (10)$$

In (10), V_{ZCOVP} is the trigger level of output overvoltage protection which can be found in product datasheet.

Secondly, as shown in Figure 3, there are two delay times for detection of the zero crossing and turn on of the MOSFET. The delay time t_{Delay1} is the delay from the drain-source voltage cross the bus voltage to the ZC voltage follows below 100mV. This delay time can be adjusted through changing C_{ZC}. The second one, t_{Delay2}, is the delay time from ZC voltage follows below 100mV to the MOSFET is turned on. This second delay time is determined by CoolSET internal circuit and cannot be changed. Therefore, the capacitance C_{ZC} is chosen to adjust the delay time t_{Delay1} MOSFET is justed turned on at the valley point of drain-source voltage. This is normally done through experiment.

Next, there is a foldback point correction integrated in this pin. This function is to decrease the peak current limit on current sense pin so that the maximum output power of the converter will not increase when the input voltage increases. This is done through sensing the current flowing out from ZC pin when MOSFET is turned on.

When the main power switch is turned on, the negative voltage on auxiliary winding can be calculated as

$$V_{aux} = -V_{BUS}\frac{N_a}{N_P} \tag{11}$$

Inside ZC pin, there is a clamping circuit so that the ZC pin voltage is kept at nearly zero. Therefore, the current flowing out from ZC pin at this moment is

$$I_{ZC\_ON} = \frac{V_{BUS}N_a}{R_{ZC1}N_P} \tag{12}$$

The threshold in ZC pin to start the foldback point correction is I_{ZC} = 0.5 mA. Therefore, R_{ZC1} can be chosen so that

$$R_{ZC1} = \frac{V_{BUS\_S}N_a}{0.5mA * N_P} \tag{13}$$

In (13), V_{BUS_S} is the voltage from which the maximum output power is desired to be maintained at constant level. The corresponding maximum current sense voltage in relation to the ZC current is shown in Figure 8.

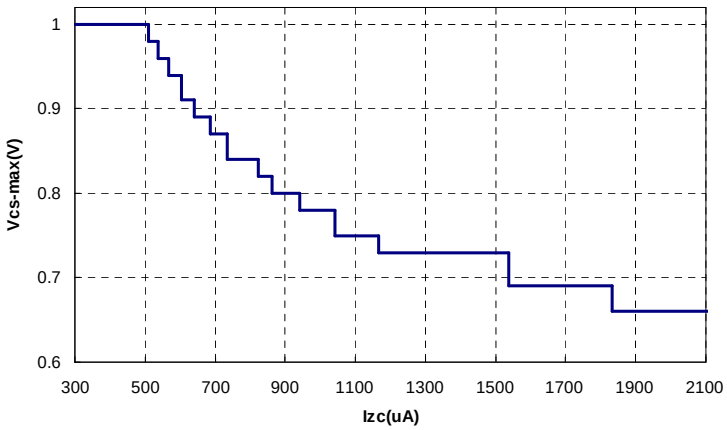


Figure 8 Maximum current sense limit versus ZC current during MOSFET on-state

In addition, as shown in Figure 3, an overshoot is possible on ZC voltages when MOSFET is turned off. This is because of the oscillation 1 on drain voltage, shown in Figure 3 may be coupled to the auxiliary winding. Therefore, the capacitance C_{ZC} and ratio can be adjusted to obtain the trade off between the output overvoltage protection accuracy and the valley switching performace.
If, however, the amplitude of the ring at the ZC pin is too small and the zero crossing cannot be detected, it is advised to increase the Drian_Source capacitor, C_{DS} of the MOSFET. But this capacitor would incur switching loss, the value is suggested to be as small as possible; best to be <100pF.
Furthermore, to avoid mis-triggerring of ZC detection just after MOSFET is turned off, a ring suppression time is provided. The ring suppression time is 2.5 µs typically if V_{ZC} is higher than 0.7V and it is 25 µs typically if

V_{ZC} is lower than 0.7V. During the ring suppression time, CoolSET can not be turned on again. Therefore, the ring suppression time can also be thought as a minimum off time.

4.8 Protections

The ICE2QRxx65/80x CoolSET provides full protection functions. The following table summarizes these protection functions.

VCC Overvoltage	Auto Restart Mode
VCC Undervoltage	Auto Restart Mode
Overload/Open Loop	Auto Restart Mode
Over Temperature	Auto Restart Mode
Output Overvoltage	Latched Off Mode
Short Winding	Latched Off Mode

During Operation, the VCC over voltage is continuously monitored. In case of an under- or an over-voltage, the CoolSET is reset and the main power switch is then kept off. After the VCC voltage falls below the threshold V_{VCCoff}, the startup cell is activated. The VCC capacitor is then charged up. Once the voltage exceeds the threshold V_{VCCon}, the CoolSET begins to operate with a new soft-start.

In case of open control loop or output over load, the feedback voltage will be pulled up. After a blanking time of 24ms, the CoolSET enters auto-restart mode. The blanking time here enables the converter to provide a high power in case the increase in V_{FB} is due to a sudden load increase.

During off-time of the power switch, the voltage at the zero-crossing pin is monitored for output over-voltage detection. If the voltage is higher than the preset threshold V_{ZCOVP}, the CoolSET is latched off after the preset blanking time.

If the junction temperature of CoolSET exceeds 140^{o}C, the CoolSET enters into auto-restart mode.

If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} during on-time of the power switch, the CoolSET is latched off. This is short-winding protection.

During latch-off protection mode, when the VCC voltage drops to 10.5V, the startup cell is activated and the VCC voltage is charged to 18V then the startup cell is hut down again and repeats the previous procedure. The latch-off mode can only be reset if the VCC voltage < 6.23V.

4.9 Others

For quasi-resonant flyback converters, it is possible that the operation frequency goes too low, which normally resulted in audible noise. To prevent it, in ICE2QRxx65/80x, a maximum on time and maximum switching period is provided.

The maximum on time in ICE2QRxx65/80x is 30 µs typically. If the gate is maintained ON for 30 µs, CoolSET will turn off the gate regardless of the current sense voltage.
When the MOSFET is off and CoolSET can not detect enough number of ZC to turn on the MOSFET, CoolSET will turn on the MOSFET when the maximum switching period, 50 µs typically, is reached. Please note that even a non-zero ZC pin voltage can not prevent CoolSET from turning on the MOSFET. Therefore, during soft start, a CCM operation of the converter is expected.

5 Typical application circuit

A 12W evaluation board with ICE2QR4780z is shown below as an example. The detailed information can be found in [5]. The application circuit is shown in Figure 9.

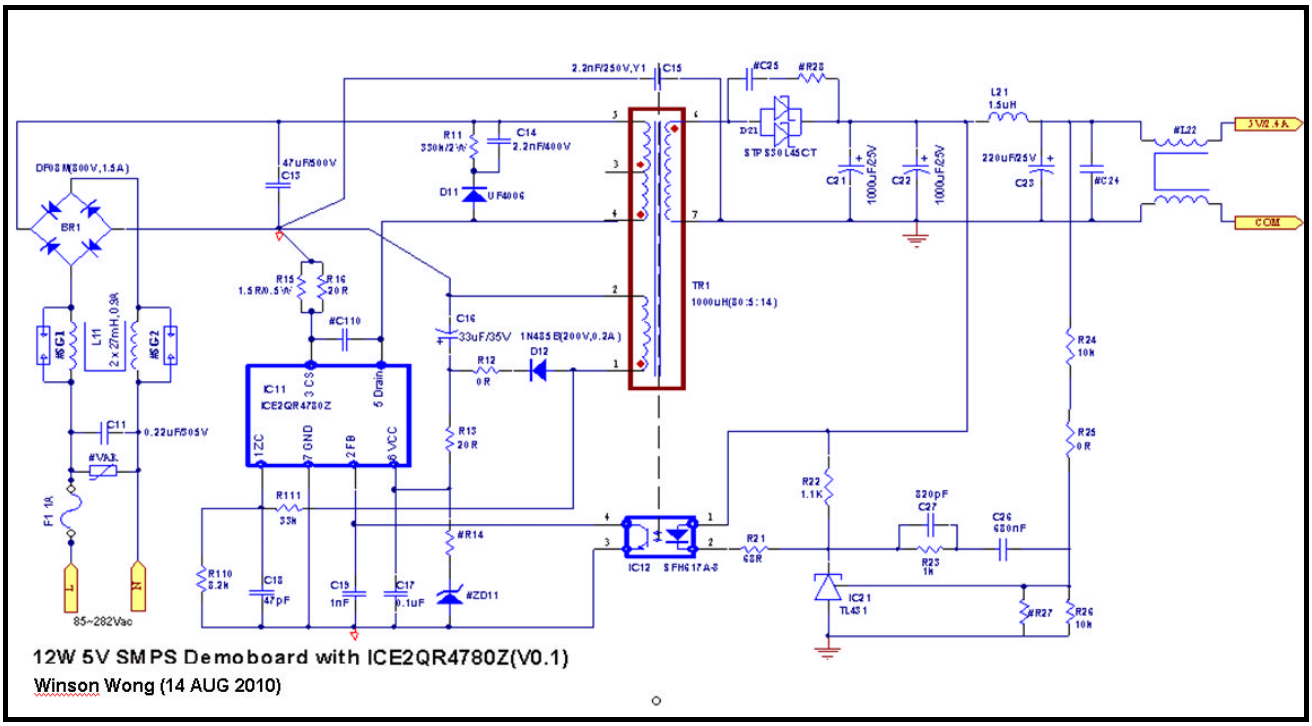


Figure 9 Schematic of the 12W 5V evalulation board with ICE2QR4780Z

6 Input Power Curves for Quasi Coolset 650V/800V

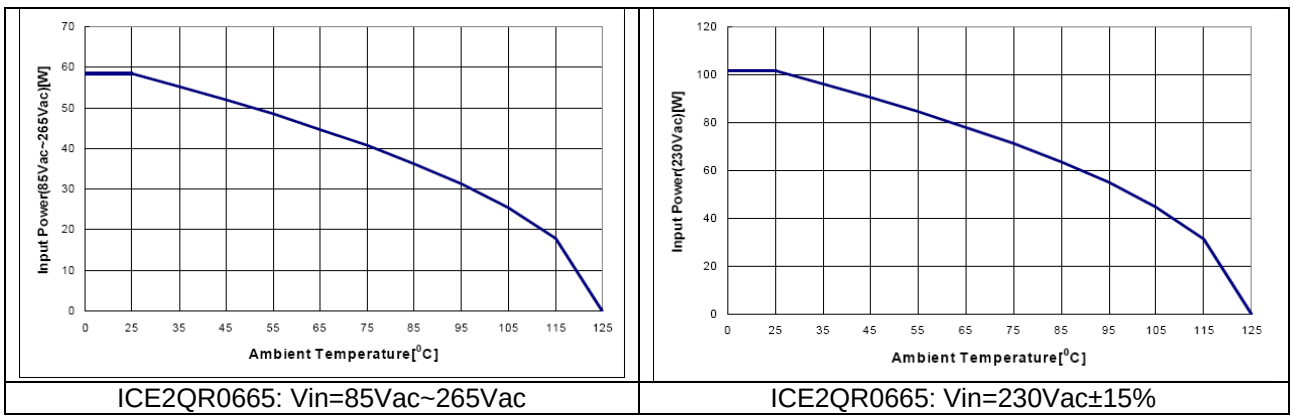
The purpose of the input power curve is to simplify the selection of the CoolSET® device. The curve is a function of ambient temperature to the input power of the system in which the input filter loss, bridge rectifier loss and the MOSFET power loss are considered. The only information needed is the required output power, the input voltage range, the operating ambient temperature and the efficiency of the system. The required input power can then be calculated as equation (14).

$$P_{in} = \frac{P_o}{\eta} \tag{14}$$

where P_{in} : input power, P_o : output power, η : efficiency

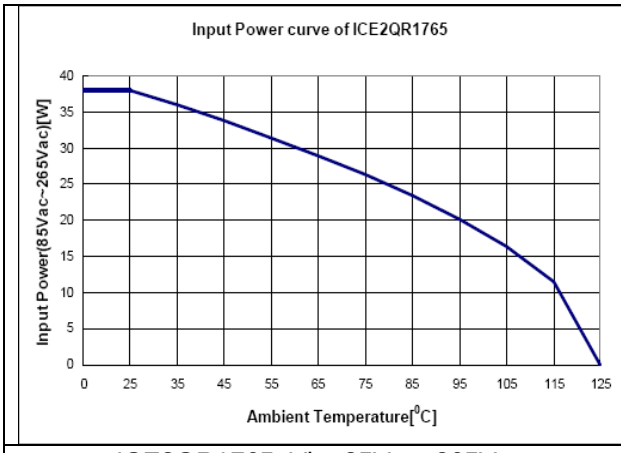
It then simply looks up the closed input power at the required ambient temperature from the input power curve.

The input power curves for the Quasi Resonant CoolSET family are listed below.

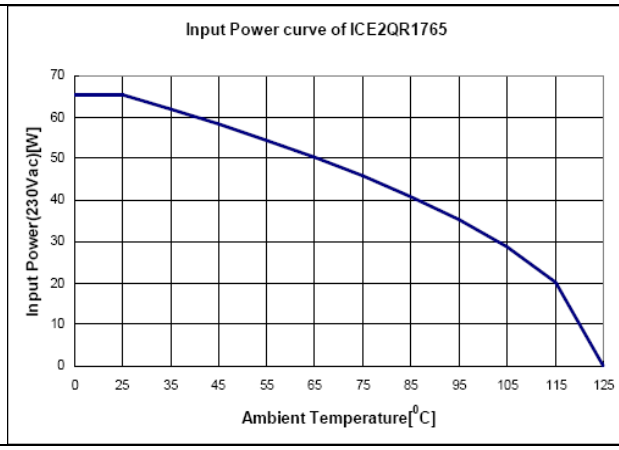


ICE2QR0665: Vin=85Vac~265Vac	ICE2QR0665: Vin=230Vac±15%

Figure 10 Input power curve for ICE2QR0665

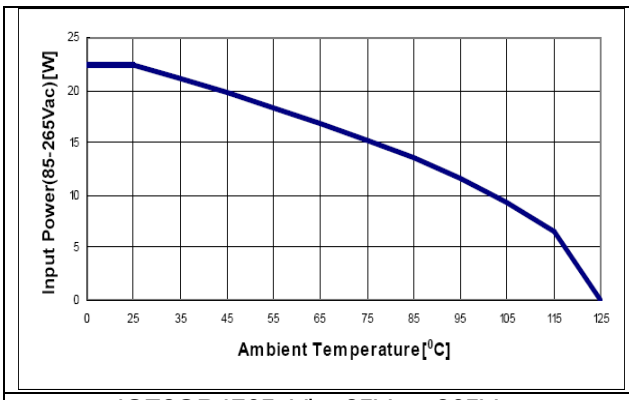


ICE2QR1765: Vin=85Vac~265Vac

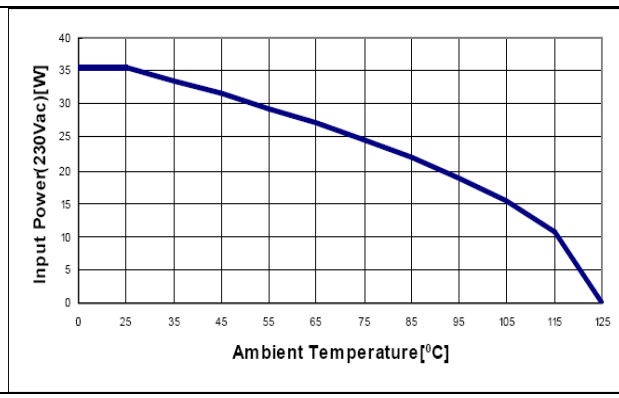


ICE2QR1765: Vin=230Vac±15%

Figure 11 Input power curve for ICE2QR1765

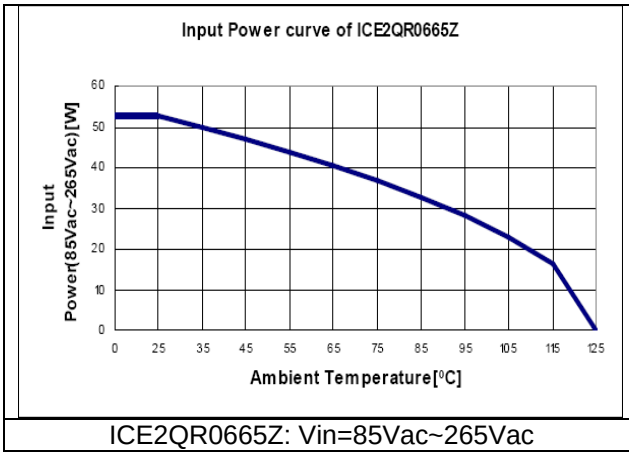


ICE2QR4765: Vin=85Vac~265Vac

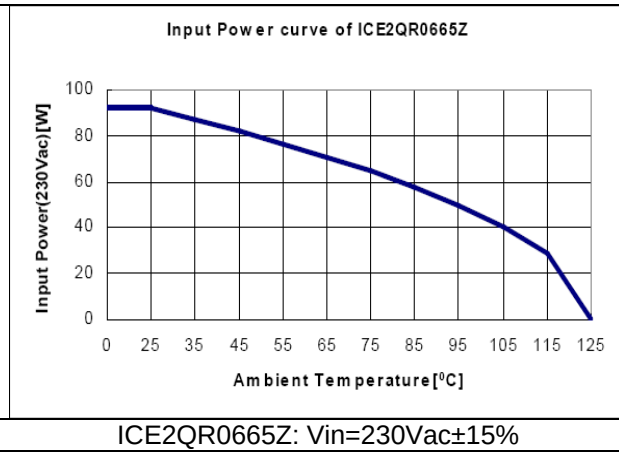


ICE2QR4765: Vin=230Vac±15%

Figure 12 Input power curve for ICE2QR4765

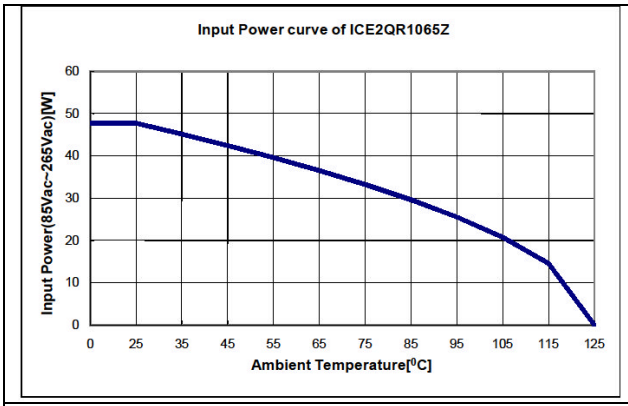


ICE2QR0665Z: Vin=85Vac~265Vac

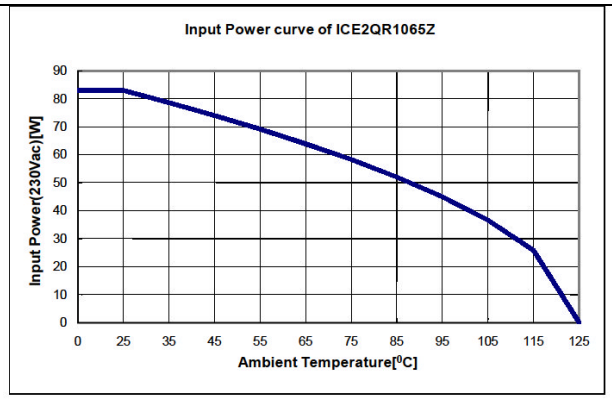


ICE2QR0665Z: Vin=230Vac±15%

Figure 13 Input power curve for ICE2QR0665Z

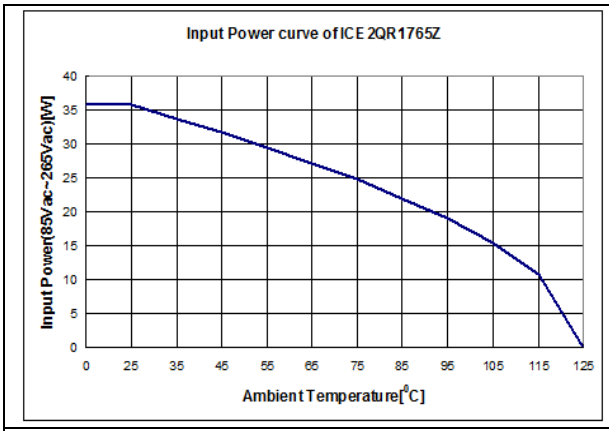


ICE2QR1065Z: Vin=85Vac~265Vac

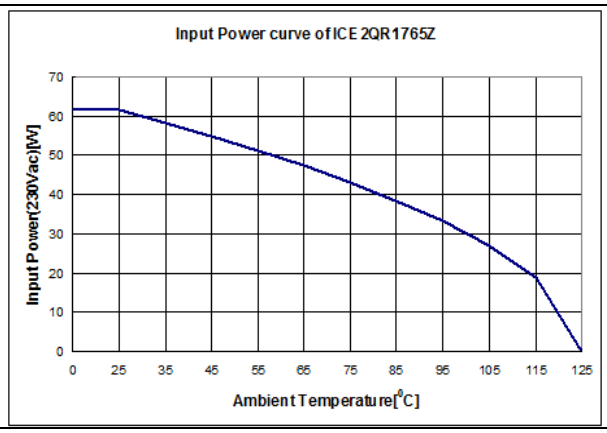


ICE2QR1065Z: Vin=230Vac±15%

Figure 14 Input power curve for ICE2QR1065Z

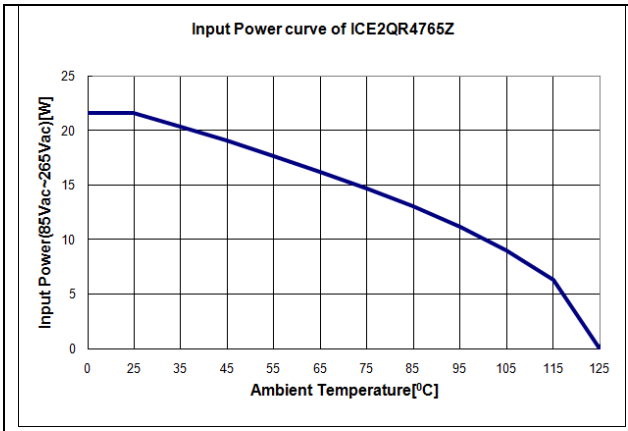


ICE2QR1765Z: Vin=85Vac~265Vac

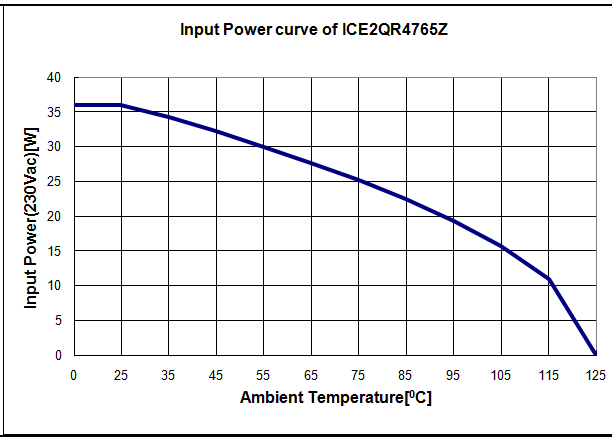


ICE2QR175Z: Vin=230Vac±15%

Figure 15 Input power curve for ICE2QR1765Z

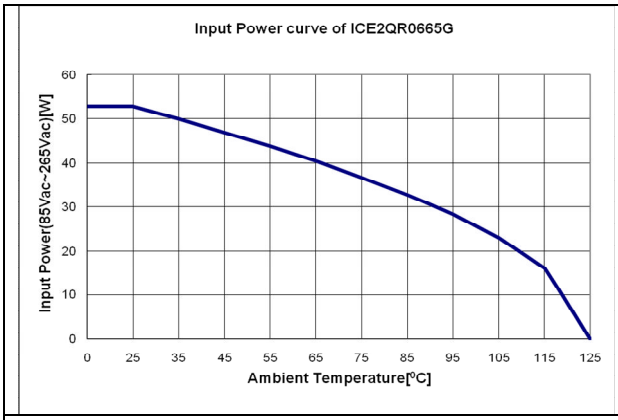


ICE2QR4765Z: Vin=85Vac~265Vac

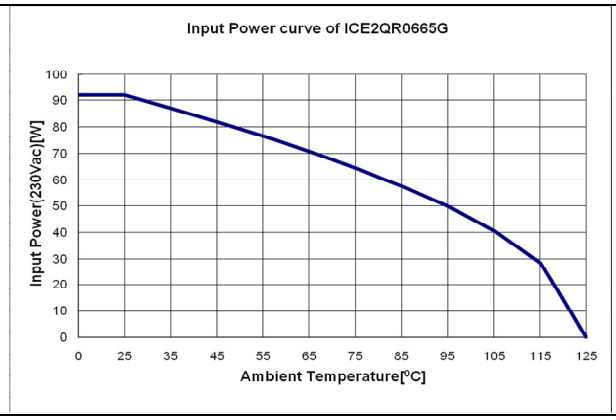


ICE2QR4765Z: Vin=230Vac±15%

Figure 16 Input power curve for ICE2QR4765Z

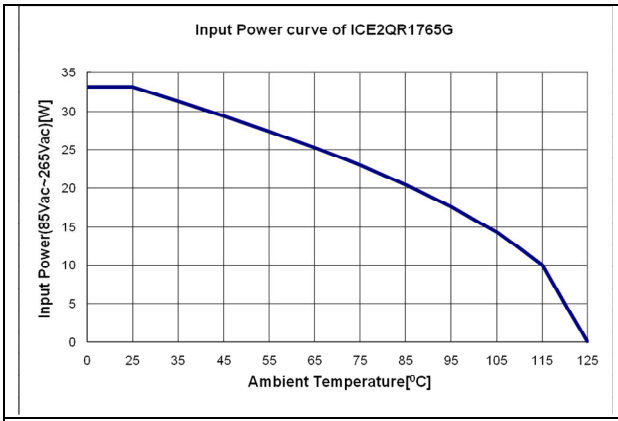


ICE2QR0665G: Vin=85Vac~265Vac

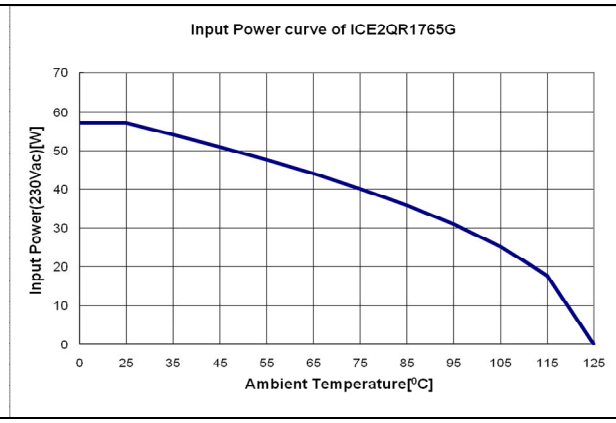


ICE2QR0665G: Vin=230Vac±15%

Figure 17 Input power curve for ICE2QR0665G

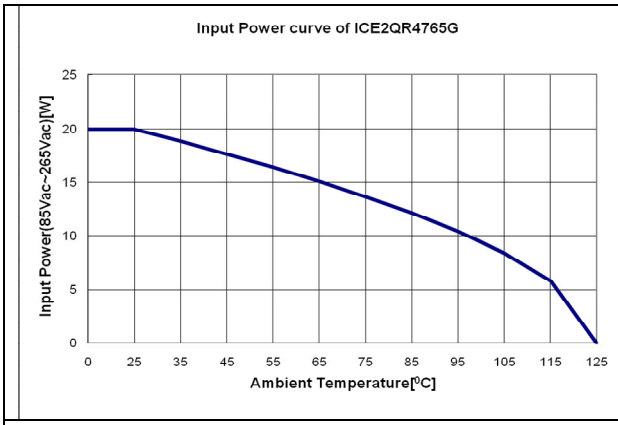


ICE2QR1765G: Vin=85Vac~265Vac

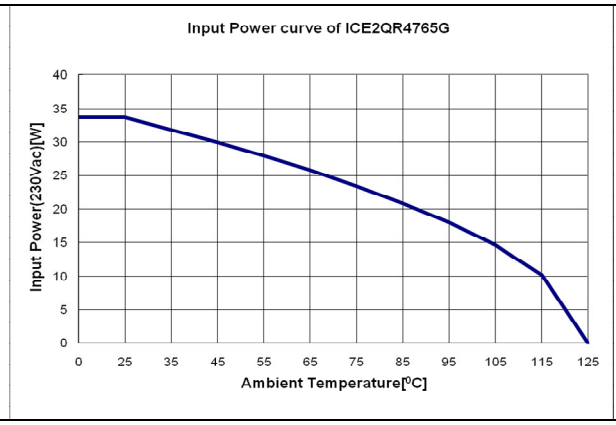


ICE2QR1765G: Vin=230Vac±15%

Figure 18 Input power curve for ICE2QR1765G

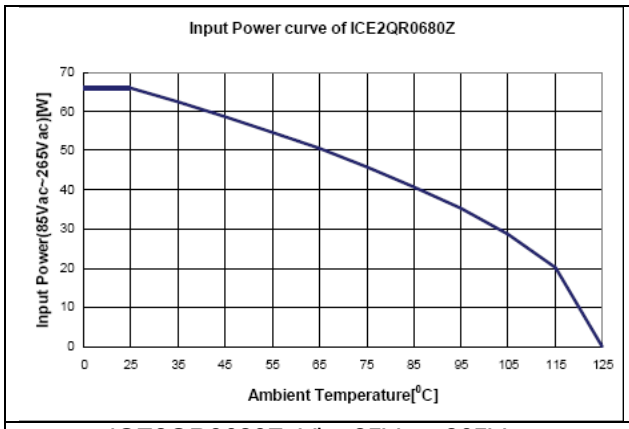


ICE2QR4765G: Vin=85Vac~265Vac

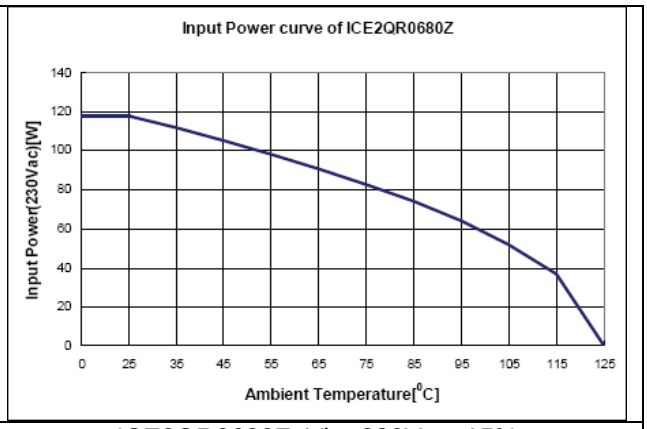


ICE2QR4765G: Vin=230Vac±15%

Figure 19 Input power curve for ICE2QR4765G

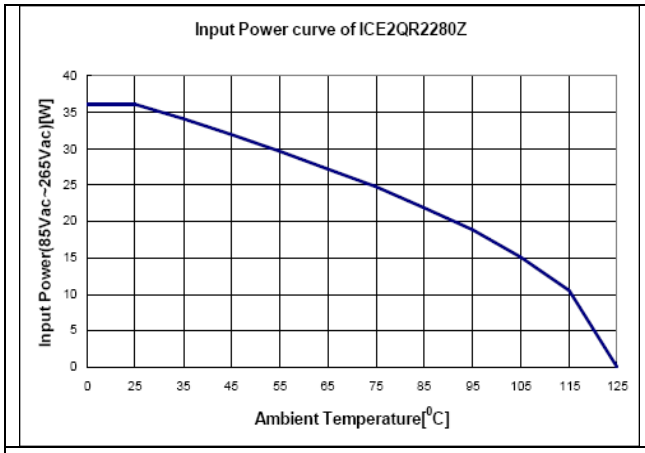


ICE2QR0680Z: Vin=85Vac~265Vac

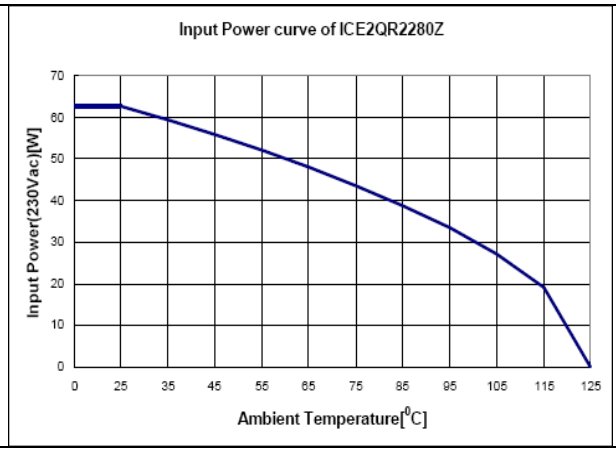


ICE2QR0680Z: Vin=230Vac±15%

Figure 20 Input power curve for ICE2QR0680Z

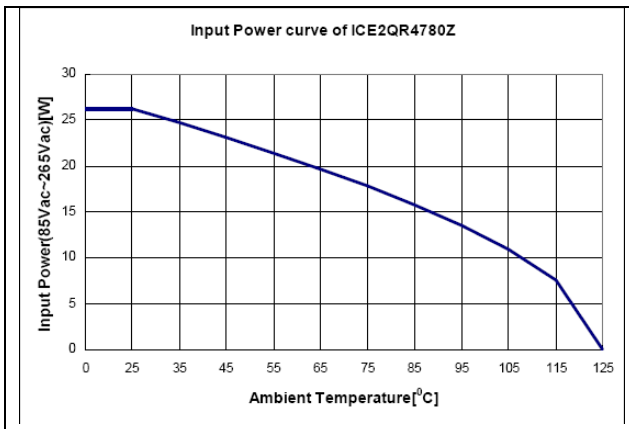


ICE2QR2280Z: Vin=85Vac~265Vac

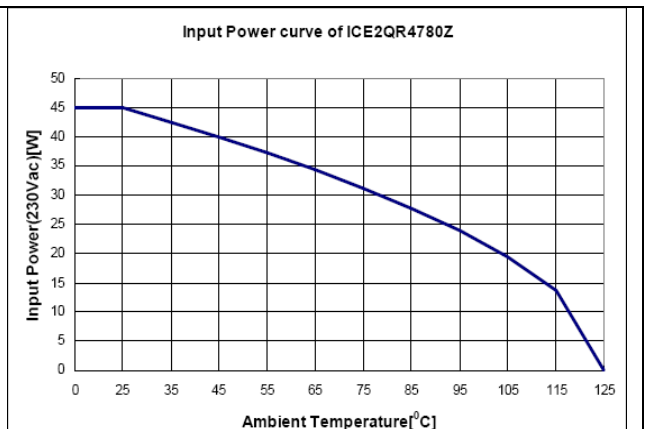


ICE2QR2280Z: Vin=230Vac±15%

Figure 21 Input power curve for ICE2QR2280Z

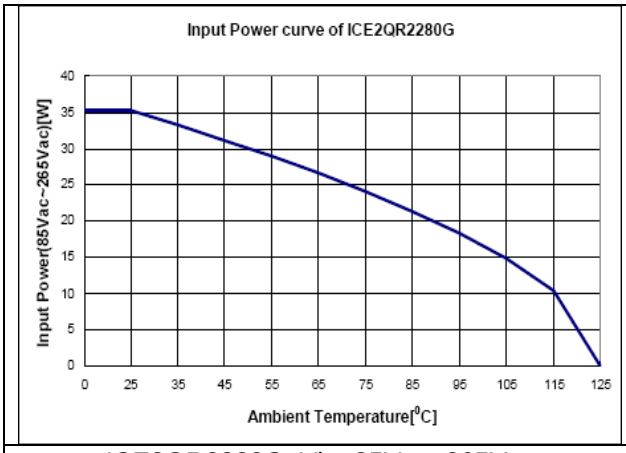


ICE2QR4780Z: Vin=85Vac~265Vac



ICE2QR4780Z: Vin=230Vac±15%

Figure 22 Input power curve for ICE2QR4780Z



ICE2QR2280G: Vin=85Vac~265Vac | ICE2QR2280G: Vin=230Vac±15%

Figure 23 Input power curve for ICE2QR2280G

The major assumption for the calculation is listed below.

1. Reflection voltage from secondary side to primary side is 115V for 650V CoolSET and 150V for 800V CoolSET.
2. The assumed maximum power for the device is when the junction temperature of the integrated CoolMOS® reaches 125°C. (With some margins to reach the over temperature protection of the device : 130°C). The maximum R_{dson} of the device at 125°C is taken for calculation.
3. For 650V DIP-8 CoolSET there is no copper area as heatsink and the R_{thja}=90K/W, for 650V DIP-7 CoolSET there is no copper area as heatsink and the R_{thja}=96K/W, for 650V DSO-12 CoolSET there is no copper area as heatsink and the R_{thja}=110K/W , for 800V DIP-7 CoolSET there is 232mm^2 copper area of 2oz PCB at drain pin for heatsink and the R_{thja}=80K/W and for 800V DSO12 CoolSET there is 232mm^2 copper area of 2oz PCB at drain pin for heatsink and the R_{thja}=85K/W.
4. Saturation current (I_{d_max} @ 125°C) of the MOSFET is considered which is showed in below table.
5. The typical resistance of the EMI filter is listed in the below table.
6. The voltage drop for the bridge rectifier is assumed to be 1V.

	Rdson_125°C (Ω)	I_{d_max} @125°C (A)	R_{EMI_filter} (Ω)	V_{F_bridge} (V)
ICE2QR0665x	1.58	9.95	2 * 0.56	2 * 1
ICE2QR1065x	2.22	6.47	2 * 0.56	2 * 1
ICE2QR1765x	4.12	4.03	2 * 1	2 * 1
ICE2QR4765x	12.5	1.67	2 * 3	2 * 1
ICE2QR0680x	1.58	12.60	2 * 0.56	2 * 1
ICE2QR2280x	5.80	2.87	2 * 2	2 * 1
ICE2QR4780x	11.50	1.45	2 * 3	2 * 1

7 PCB Layout Recommendation

In power supply system, PCB layout is a key point for a successful design. Following are some suggestions for this (refer to application circuit in Figure 9).

- Minimize the loop with pulse share current or voltage; examples are the loop formed by the bus voltage source, primary winding, main switch and current sensing resistor or the loop consisting of secondary winding, output diode and output capacitor, or the loop of VCC power supply.
- Good grounding of the CoolSET; as the CoolSET sees every signal to the reference point of the CoolSET ground which is also the ground of the VCC power supply, it is advisable that the ground of the CoolSET is connected to the bus voltage ground through a short and thick PCB track in a star structure. Note that ground of CoolSET is treated as small signal ground and the R_{CS} resistor ground and primary ground of auxiliary winding of the transformer are treasted as power loop ground. It needs to be separated before connected to the bulk capacitor ground.
- Good grounding of other parts/functions. This includes the CoolSET ground, FB loop ground, ZC loop ground and the VCC loop ground. It is advisable that all the above grounds connected to the CoolSET ground and then connected to the bus voltage ground using a star-structure.
- Power loop grounds can connect to bulk capacitor ground directly and separately; such as EMI filter return ground Y capacitor, C15, auxiliary winding ground of transformer and the R_{CS} resistor.
- The high voltage pins are connected to bus voltage in typical applications. During lightning surge test, the noise on bus voltage is high. It is suggested that the track to high voltage pin shall be kept away from other small signal tracks. The distance is better to be more than 3mm.

8 Product Portfolio Quasi Resonant CoolSET®

Type	Package	MOSFET V_{DS}	R_{DSon}[1]	Input power 230 V_{AC}	Input power (85-265) V_{AC}	Features[2]
ICE2QR0665	DIP-8	650V[3]	0.65 Ω	88W[4]	50W[4]	DFR, PPL
ICE2QR1765	DIP-8	650V[3]	1.7 Ω	56W[4]	33W[4]	DFR, PPL
ICE2QR4765	DIP-8	650V[3]	4.7 Ω	30W[4]	19W[4]	DFR, PPL
ICE2QR0665Z	DIP-7	650V[3]	0.65 Ω	79W[4]	45W[4]	DFR, PPL
ICE2QR1065Z	DIP-7	650V[3]	0.92Ω	71.6W[4]	41.0W[4]	DFR, PPL
ICE2QR1765Z	DIP-7	650V[3]	1.7 Ω	54.8W[4]	30.6W[4]	DFR, PPL
ICE2QR4765Z	DIP-7	650V[3]	4.7 Ω	31W[4]	18W[4]	DFR, PPL
ICE2QR0665G	DSO-12	650V[5]	0.65 Ω	79W[6]	45W[4]	DFR, PPL
ICE2QR1765G	DSO-12	650V[3]	1.7 Ω	49W[4]	28W[4]	DFR, PPL
ICE2QR4765G	DSO-12	650V[3]	4.7 Ω	29W[4]	17W[4]	DFR, PPL
ICE2QR0680Z	DIP-7	800V	0.65 Ω	102W[7]	57W[5]	DFR, PPL, 800V
ICE2QR2280Z	DIP-7	800V	2.2 Ω	53W[5]	30W[5]	DFR, PPL, 800V
ICE2QR4780Z	DIP-7	800V	4.7 Ω	39W[5]	22W[5]	DFR, PPL, 800V
ICE2QR2280G	DSO-12	800V	2.2 Ω	51W[5]	30W[5]	DFR, PPL, 800V

[1] Typical value @ T_j=25°C
[2] DFR=Digital Frequency Reduction; PPL= Peak Power Limitation
[3] T_j=110°C
[4] Calculated maximum input power in an open frame design at T_a=50°C, T_j=125°C and without copper area heat sink.
[5] T_j=110°C
[6] Calculated maximum input power in an open frame design at T_a=50°C, T_j=125°C and without copper area heat sink.
[7] Calculated maximum input power in an open frame design at T_a=50°C, T_j=125°C and with 232mm^2 2 oz copper area heat sink.

9 Design Equations

With reference to the typical application diagram in Figure 2, some useful design equations are tabulated as below (refer to symbols to datasheet):

Transformer Calculation (Quasi Resonant flyback)	
Input data	Vin_min=85V_{dc}, Vin_max=400V_{dc}, Vdc_max=515V for 650V MOSFET, 550V for 800V MOSFET
Turn ratio	$n = \frac{V_{ds\_max} - V_{in\_max}}{V_{out} + V_{diode}}$
Primary Inductance	$L_p \le \frac{1}{\left[\left(\frac{1}{V_{in\_min}} + \frac{1}{n \times V_{out}}\right) \times \sqrt{\frac{f_{sw\_LF} \times P_{out}}{\eta \times 0.5}} + \pi \times f_{sw\_LF} \times \sqrt{C_{DS}}\right]^2}$ f_{sw_LF} = switching frequency at low line full load; suggested : 40~65kHz C_{DS} = capacitance across Drain_Source of MOSFET (including $C_{o(er)}$ of MOSFET)
Primary peak current	$I_{pk\_P} = \sqrt{\frac{P_{out}}{\eta \times 0.5 \times L_p \times f_{sw\_LF}}}$
Primary turns	$N_p \ge \frac{L_p \times I_{p\_max}}{B_{max} \times A_{min}}$
Secondary turns	$N_s = \frac{N_p}{n}$
Auxiliary turns	$N_{aux} = \frac{V_{cc} + V_{diode}}{V_{out} + V_{diode}} \times N_s$
ICE2QRxx65/80x external component design	
Current sense resistor	$R_{CS} \le \frac{V_{CSth}}{I_{pk\_P}}$
VCC capacitor	$C_{VCC} = \frac{t_{startup} \times I_{VCCcharge2}}{V_{VCCon}}$ $t_{startup}$ = startup time of system; suggested C_{VCC} is ≥ 22µF
ZC resistors	$R_{ZC1} = \frac{V_{BUS\_S} \times N_{aux}}{0.5mA \times N_p}$; $R_{ZC2} = \frac{R_{ZC1}}{\frac{N_{aux}}{N_s} \times \frac{V_{out\_OVP} + V_{diode}}{V_{ZCOVP}} - 1}$ V_{out_OVP} = output OVP voltage; V_{BUS_S}=bulk capacitor voltage to maintain max. output power
ZC Capacitor	$C_{ZC} = \tan\left[2\pi \cdot \left(\frac{1}{4} - t_{delay} \cdot f_{osc2}\right)\right] \cdot \frac{R_{ZC1} + R_{ZC2}}{R_{ZC1} \cdot R_{ZC2}} \cdot \frac{1}{2\pi \cdot f_{osc2}}$ t_{delay} can be taken as 100ns; f_{osc2} = measured Drain oscillation frequency after secondary side current drops to 0A (refer to Figure 3)
Enter burst mode power	$P_{Burst\_enter} = 0.5 \times L_P \times \left(\frac{V_{FBEB} - V_{PWM}}{R_{CS} \times G_{PWM}}\right)^2 \times f_{sw\_bb}$ f_{sw_bb} = switching frequency before entering burst mode
Leave burst mode power	$P_{Burst\_leave} = 0.5 \times L_P \times \left(\frac{V_{CSB}}{R_{CS}}\right)^2 \times f_{sB}$ f_{sB} = switching frequency at burst mode

Please refer to the below references for some more useful calculation formulas.

10 References

[1] Design tips for flyback converters using the Quasi-Resonant PWM controller ICE2QS01, Infineon Technologies, 2006. [ANPS0005]

[2] Converter design using the quasi-resonant PWM controller ICE2QS01, application notes, Infineon Technologies, 2006. [ANPS0003]

[3] Determine the switching frequency of Quasi-Resonant flyback converters designed with ICE2QS01, Infineon Technologies, 2006. [ANPS0004]

[4] 12W 5V Evaluation Board with Quasi-Resonant PWM controller ICE2QR4780Z, Application notes, Infineon technologies 2011.

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