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Application Note

AN-Prod-Type-No

CoolSET™

ICE2AXXX for OFF – Line Switch Mode Power Supply (SMPS)

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http://www.infineon.com

Power Management & Supply

Never stop thinking

Contents:

Operating Principles

The **ICE2AXXX** is designed for a current-mode flyback configuration in **discontinous (DCM) or continous conduction (CCM)** mode.
The control circuit has a fixed frequency. The duty cycle (D) of the integrated CoolMOS™ Transistor is controlled to maintain a constant output voltage (V_{OUT}).
Fig. 1 shows the input voltage ($V_{DC\ IN}$), the primary current(I_{LPK}), and the secondary (I_{SEC}) transformer currentof the flyback converter depicted on p. 3
When the CoolMOS™ Transistor is swiched on, the initial state of all windings on the transformer is at positive potential.
The rectifier diode (D1) on the secondary side is reverse biased and therefore does not conduct. Consequently no current flows in the secondary winding. During this phase, energy is stored in the inductance of the primary winding and the transformer can be treated as a simple series inductor.
Fig. 1 shows that there is a linear increase of the primary current (I_{PRI}) while the CoolMOS Transistor is on.
When the CoolMOS Transistor is swiched off, the voltage reverses on all transformer windings (flyback action) until it is clamped by rectifier diode on the secondary side. Now the secondary rectifier diode (D1) is conducting, and the magnetizing energy stored in the transformer core is transferred to the secondary side during the reset interval.

In the **discontinous conduction mode DCM t**he secondary current (I_{SEC}) decreases from its peak value to zero (Fig. 1). During this period the whole energy stored in the primary inductance is transferred to the secondary side (neglecting losses and energy stored in the primary leakage inductance), then the next storage cycle starts. Taking into account the transformer turns ratio, the secondary voltage (V_{SEC}) is “reflected” back (V_R) to the primary winding and adds to the input voltage ($V_{DC\ IN} + V_R$). An additional transient voltage may appear on the primary winding due to energy stored in the uncoupled “leakage” inductance in the primary winding. This voltage is not clamped by the secondary side winding. If the flyback current (I_{LPK} and I_{SEC}) does not reach zero before the next “on” – cycle the converter is operating in **continous conduction mode** (Fig. 2).
Note:
When the system shifts to continous conduction operation, its transfer function is changed to a two pole system with low output impedance. In this case additional design rules have to be taken into account including different loop compensation and slope compensation on the primary side.

Voltage and current waveforms in **discontinous conduction mode** (DCM) operation:

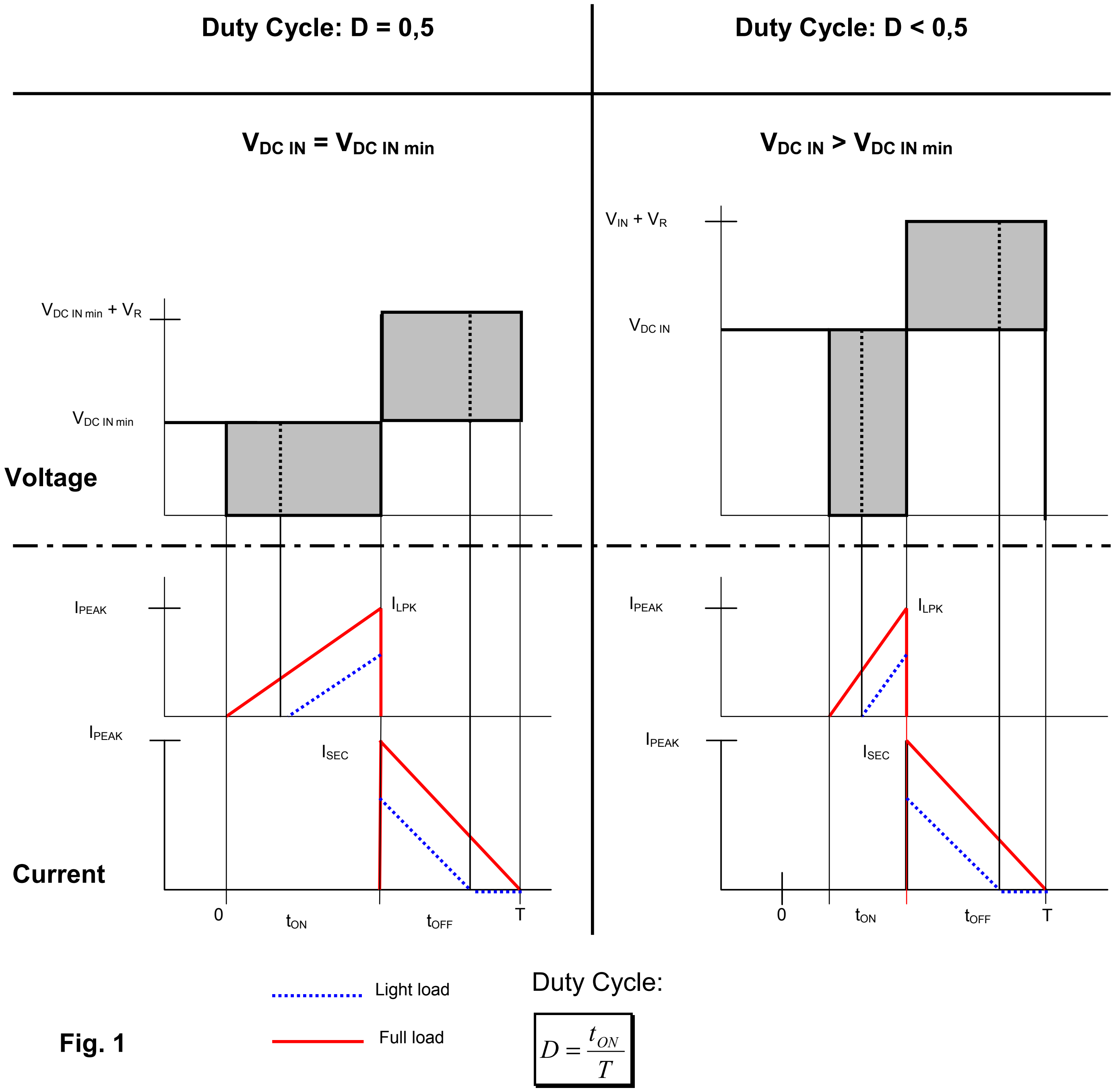

Fig. 1

Duty Cycle:

$$\boxed{D = \frac{t_{ON}}{T}}$$

Comparison of **continous conduction** (CCM) and **discontinous conduction** (DCM) mode.

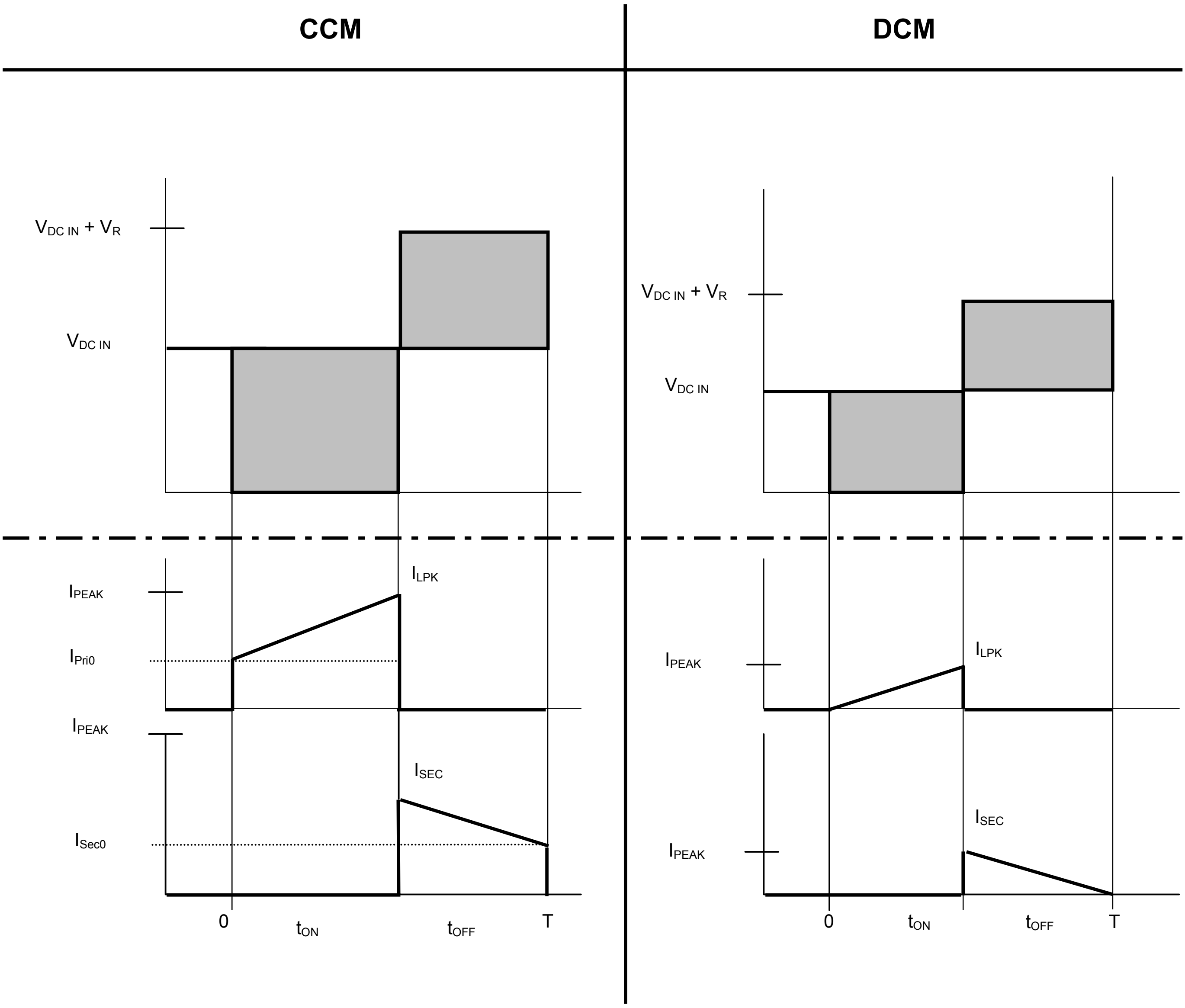

Fig. 2

Input stage

As shown in Fig. 3 the AC input power is rectified and filtered by the bridge rectifier (BR1) and the bulk capacitor C3. This create a DC high voltage bus which is connected to the primary winding of the transformer (TR1). The transformer is driven by the CoolSET™ integrated high voltage, avalanche rugged CoolMOS™ transistor, with an external sense resistor (R17) for precision current mesurement.

Output stage

The secondary winding power is rectified and filtered by a diode (D1), capacitors (C5, C9 and C20). The output LC-filter (L3, C23) reduces the output voltage ripple.

Other output voltages

Other output voltages can be realized by adjusting the transformer turn ratio and the output stage.

Chip supply

The current in the bias winding is rectified and filtered by a diode (D2) and a resistor (R8) in order to charge the the supply capacitor (C4). This creates a bias voltage that powers the CoolSET™ ICE 2AXXX. The resistors R6 and R7 charge the VCC Cap and supply the chip during startup. The Zener diode (D4) clamps the chip supply voltage (Vcc) in order to protect the chip in case of an over-voltage condition. Capacitor C13 filters high frequency ripples on the chip supply voltage (Vcc).

Soft-Start

A soft-start function is activated during start-up, and can be adjusted by capacitor C14. In addition to start-up, soft-start is activated at each restart attempt during auto-restart and when restarting after one of the several protection functions are activated. This effectively minimizes current and voltage stresses on the CoolMOS™ MOSFET, the snubber network, and the output rectifier during start-up. The soft-start feature further helps to minimize output overshoot and prevents saturation of the transformer during start-up.

Clamping network

The clamping network which consists of a diode (D3), a resistor (R10) and a capacitor (C12) clamps the voltage spike caused by the transformer leakage inductance to a safe value this limits the avalanche losses of the CoolMOS™ transistor.

Control Loop

The resistors R1 and R2 represent the voltage divider for the reference diode TL431CLP (IC2). R4 supplies the TL431CLP reference diode with a minimum current and R3 the LED of the optocoupler. The network which consists of capacitors C1 and C2 determines the corner frequencies fg1 and fg2. R5 sets the gain of the control loop.

Slope Compensation

The current mode controller becomes unstable whenever the steady – state duty cycle D is larger than 0.5. In order to realize a design with a duty cycle greater 0.5, the slope of the current needs to be compensated. The slope compensation is realized by the network consisting of capacitor C17, C18 and the resistor R19.

Ripple Reduction

Inductor L5 and capacitor C23 attenuate the differential – mode emission currents caused by the fundamental and harmonic frequencies of the primary current waveform.

SMPS Calculation Software FLYCAL

FLYCAL is an EXCEL spread sheet with all Equations needed for the easy calculaton of your SMPS. FLYCAL corresponds with the calculaton example in this application note. You only have to enter the main parameters of your application in FLYCAL and to follow step by step the principle outlined in the calculation example. FLYCAL contains all equations used in the example with the same consecutive numbering.

Circuit Diagram:

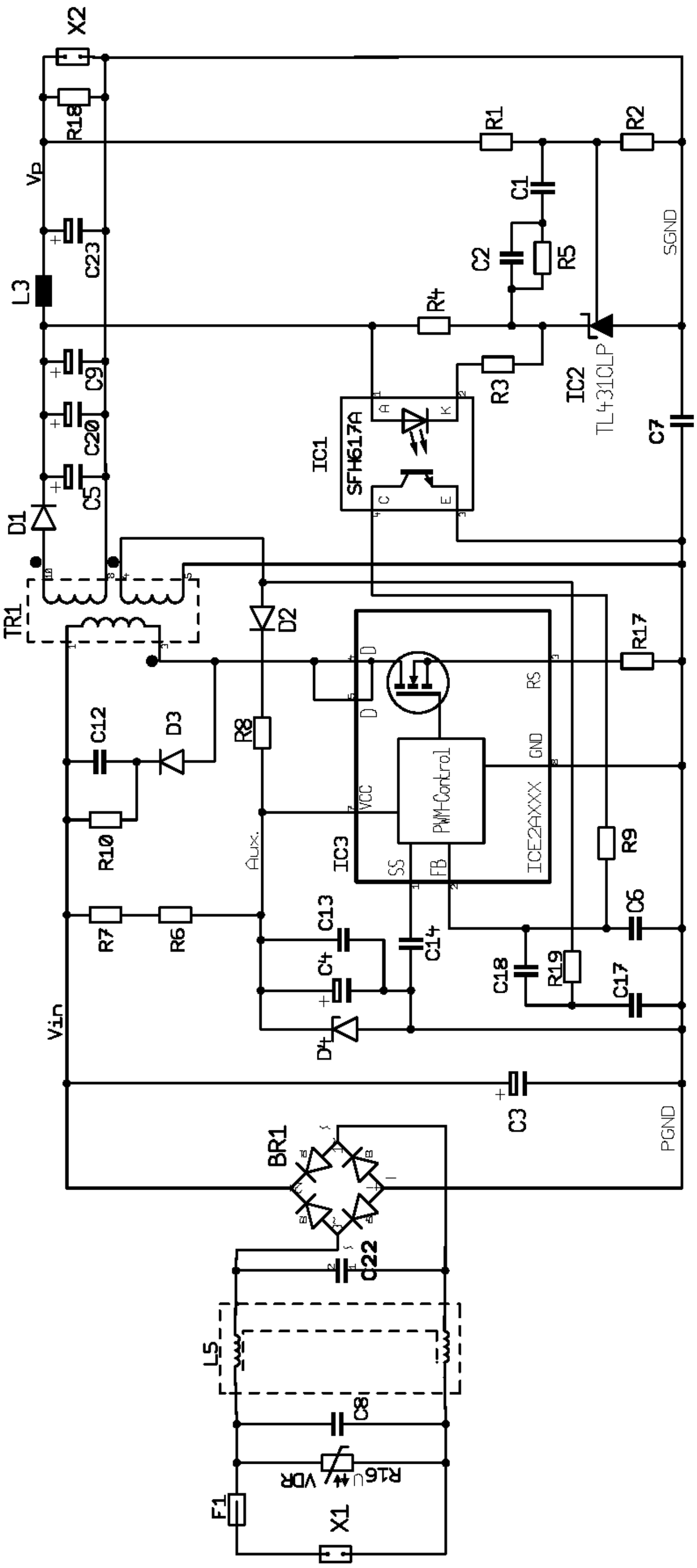

Fig. 3

Protection Functions

The block diagram displayed in Fig. 4 shows the interal functions of the protection unit. The comparators C1, C2, C3 and C4 compare the soft-start and feedback-pin voltages. Logic gates connected to the comparator outputs ensure the combination of the signals and enables the setting of the “Error-Latch”.

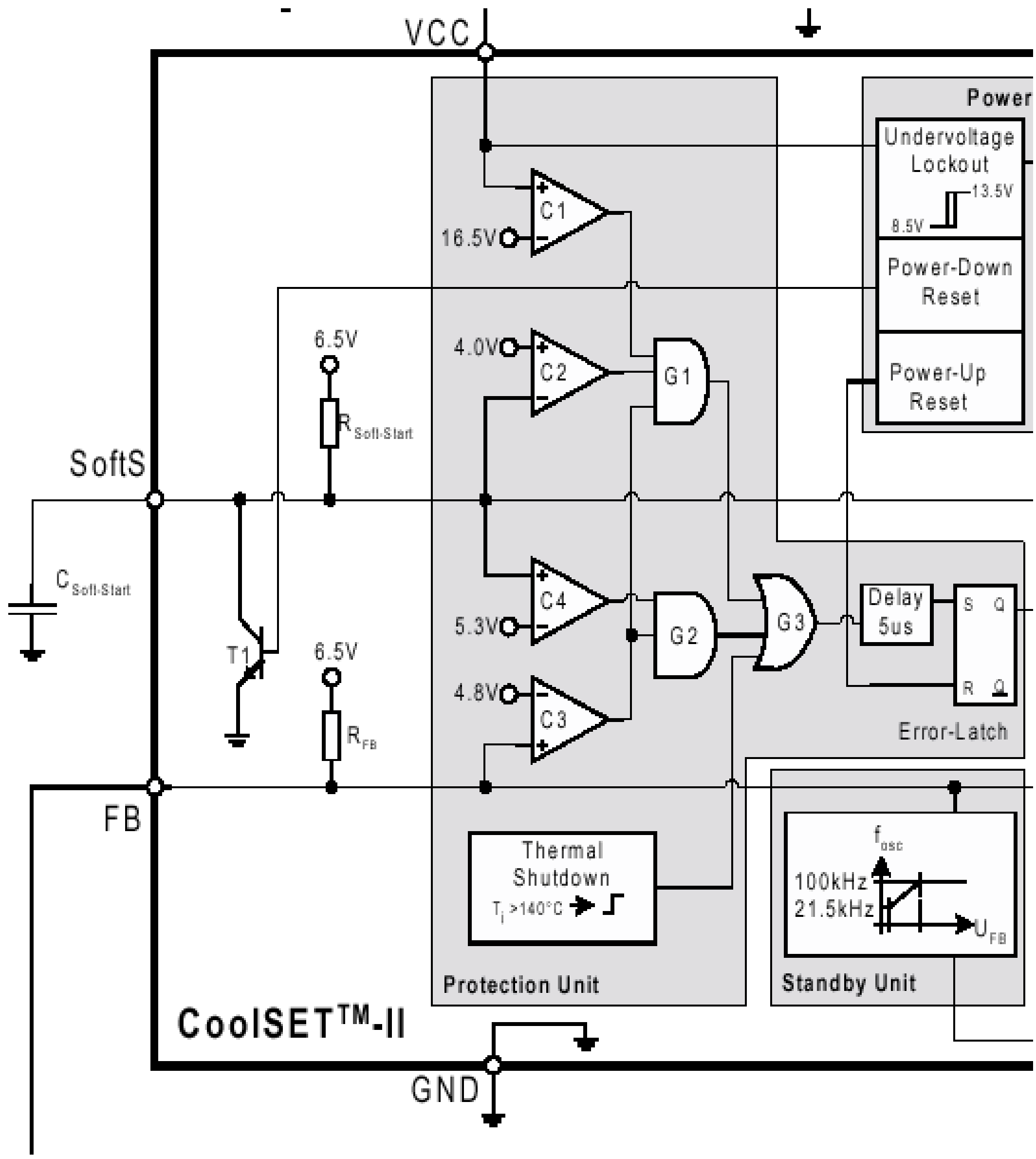

Fig. 4

Fig. 5 shows the relation between the voltages at the soft start (Vss) and the feedback pins (V_{FB}) of **ICE2AXXX**, as a function of the supply voltage (Vcc) during an overvoltage condition at CoolSET soft start.

Depending on the voltage levels at the inputs, the overvoltage and (Vcc – PIN 7) and overload (V_{FB} – PIN 2) protection functions are activated.

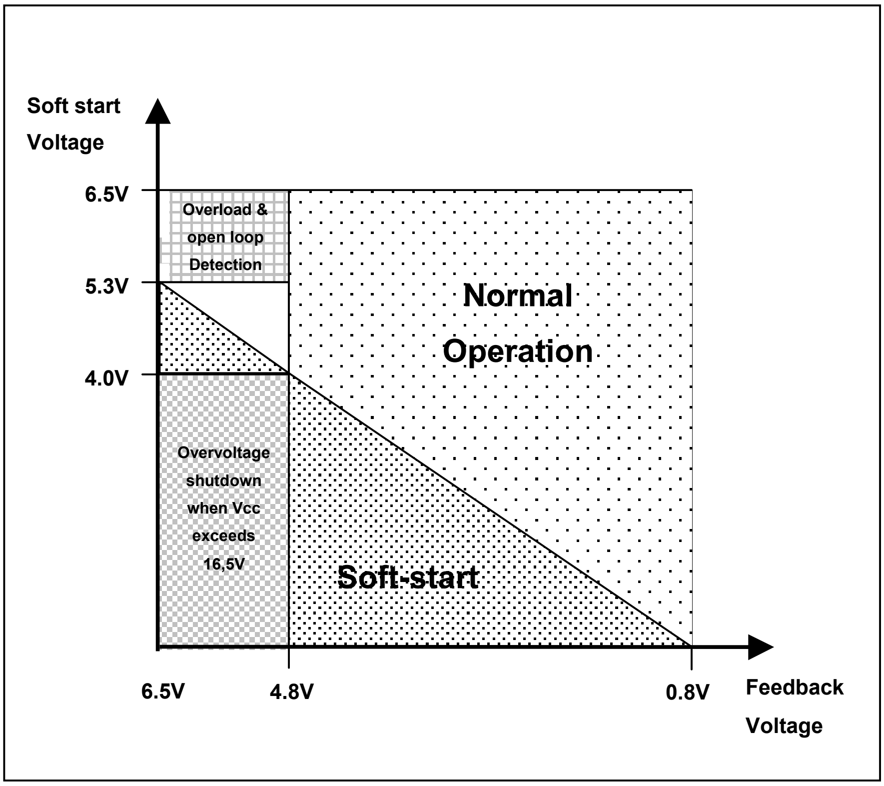

Fig. 5

Overload and Open-Loop Protection

- Feedback voltage **(VFB)** exceeds 4.8V and soft start voltage **(VSS)** is above 5.3V (soft start is completed) **(t1)**
- After a 5µs delay the **CoolMOS** is switched off **(t2)**
- Voltage at Vcc – Pin **(VCC)** decreases to 8.5V **(t2)**
- Control logic is switched off **(t3)**
- Start-up resistor charges Vcc capacitor **(t3)**
- Operation starts again with soft start after Vcc voltage has exceeded 13.5V **(t4)**

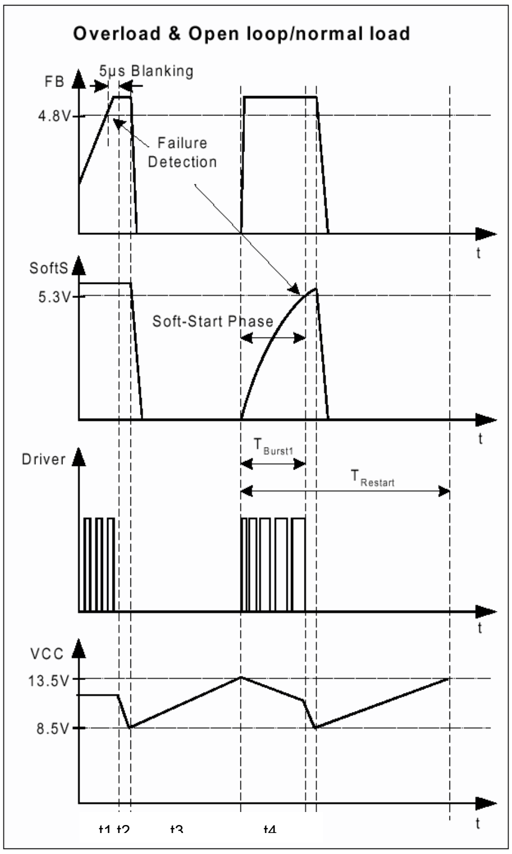

Fig. 6

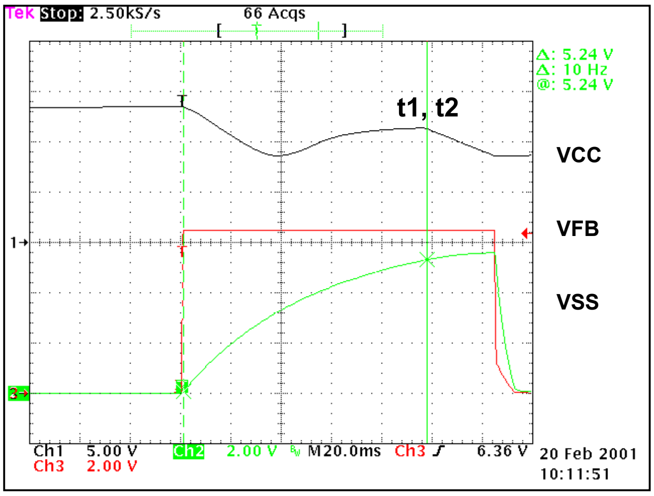

Fig. 7

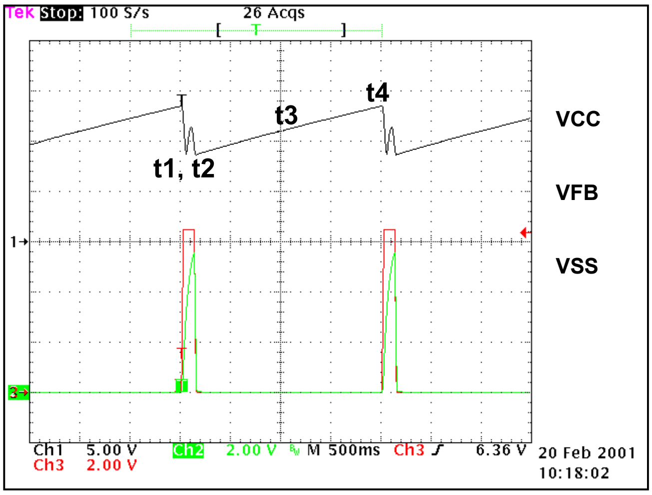

Fig. 8

Overvoltage Protection During Soft Start

- Feedback voltage **(VFB)** exceeds 4.8V <u>and</u> soft-start voltage **(VSS)** is below 4.0V (soft start phase) **(t1)**
- Voltage at Vcc pin **(VCC)** exceeds 16.5V **(t2)**
- CoolMOS transistor is immediately switched off **(t2)**
- Voltage at VCC pin decreases to 8.5V **(t3)**
- Control logic is switched off **(t3)**
- Start-up resistor charges VCC capacitor **(t4)**
- Operation starts again with soft start after VCC voltage has exceeded 13.5V **(t5)**

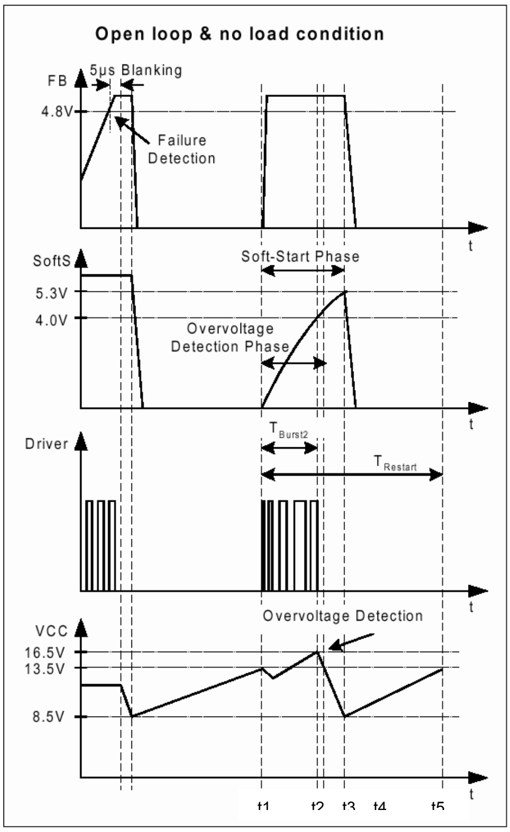

Fig. 9

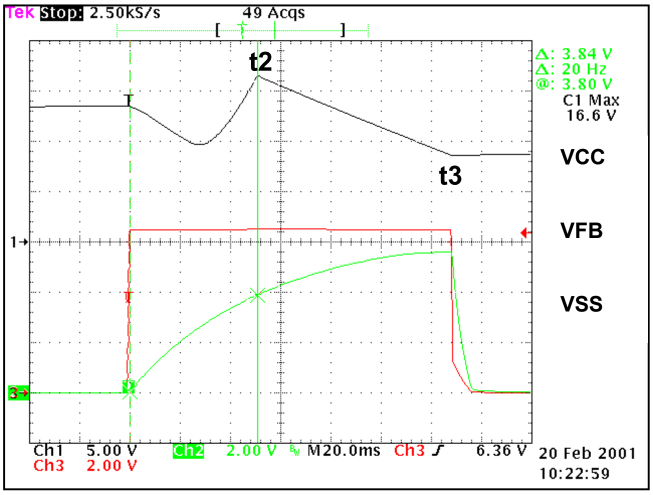

Fig. 10

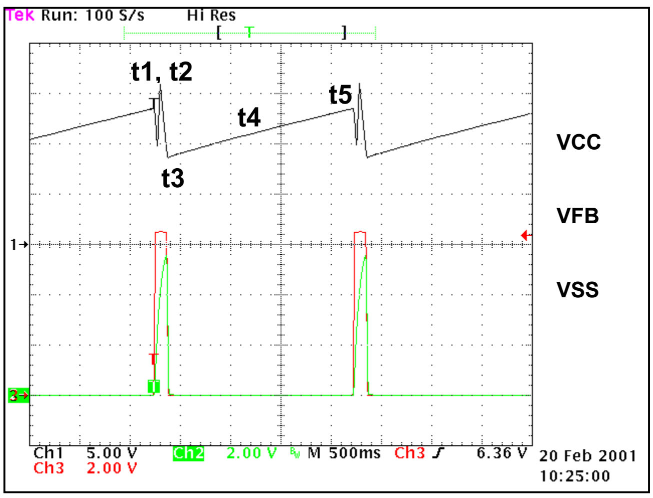

Fig. 11

Frequency Reduction

The frequency of the oscillator depends on the voltage at pin FB.

Below a voltage of typ. 1.75V the frequency decreases down to 21.5 kHz.

Due to this frequency reduction the power losses in low load condition can be reduced very effectively.

This dependency is shown in Fig. 12

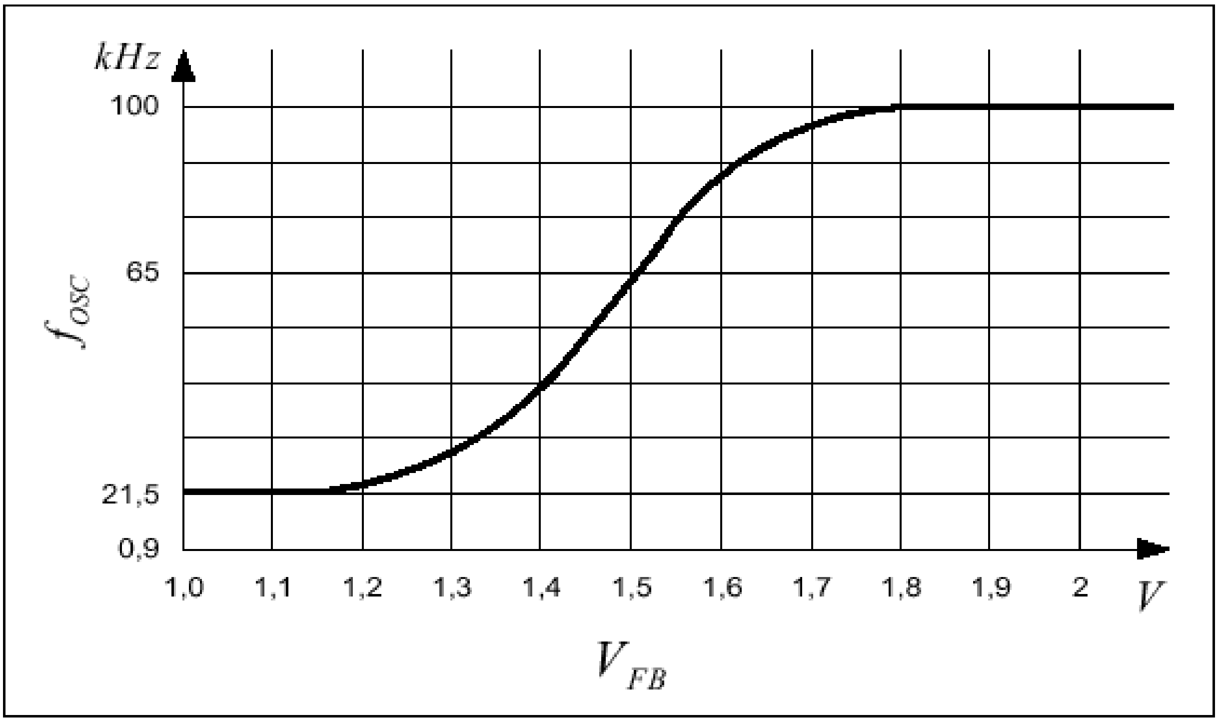

Fig. 12

Design Procedure

for fixed frequency Flyback Converter with **ICE2AXXX** operating in **discontinuous** current mode.

Procedure	Example

Define input Parameters:

Minimal AC input voltage:	$V_{AC\ min}$
Maximal AC input voltage:	$V_{AC\ max}$
Line frequency:	f_{AC}
Max. output power:	$P_{OUT\ max}$
Nom. output power:	$P_{OUT\ nom}$
Min. output power:	$P_{OUT\ min}$
Output voltage:	V_{OUT}
Output ripple voltage:	$V_{OUT\ Ripple}$
Reflection voltage:	V_{Rmax}
Estimated efficiency:	η
DC ripple voltage:	$V_{DC\ IN\ Ripple}$
Auxiliary voltage:	V_{Aux}

Input Diode Bridge (BR1):

$$I_{ACRMS} = \frac{P_{IN\,MAX}}{V_{AC\min} \cdot \cos\varphi} \quad \textbf{(Eq 2)}$$

$$I_{ACRMS} = \frac{59W}{90V \cdot 0{,}6} = 1{,}09A$$

Maximum DC IN voltage

$$V_{DC\max PK} = V_{AC\max} \cdot \sqrt{2} \quad \textbf{(Eq 3)}$$

$$V_{DC\max PK} = 264V \cdot \sqrt{2} = 373V$$

Determine Input Capacitor (C3):

Minimum peak input voltage at "no load" condition

$$V_{DC\min PK} = V_{AC\min} \cdot \sqrt{2} \quad \textbf{(Eq 4)}$$

$$V_{DC\min PK} = 90V \cdot \sqrt{2} = 127V$$

$$V_{DC\min} = V_{DC\min PK} - V_{Ripple} \quad \textbf{(Eq 5)}$$

we choose a ripple voltage of 30V

$$V_{DC\min} = 127V - 30V = 97V$$

Calculation of discharging time at each half-line cycle:

$$T_D = 5ms \cdot \left(1 + \frac{\arcsin \frac{V_{DC\min}}{V_{DC\min PK}}}{90} \right) \quad \textbf{(Eq 6)}$$

$$T_D = 5ms \cdot \left(1 + \frac{\arcsin \frac{97V}{127V}}{90} \right) = 7{,}7ms$$

Required energy at discharging time of C3:

$$W_{IN} = P_{IN\max} \cdot T_D \quad \textbf{(Eq 7)}$$

$$W_{IN} = 59W \cdot 7{,}7ms = 0{,}46Ws$$

Calculation of input capacitor value C_{IN}:

$$C_{IN} = \frac{2 \cdot W_{IN}}{V_{DC\min PK}^2 - V_{DC\min}^2} \quad \textbf{(Eq 8)}$$

$$C_{IN} = \frac{2 \cdot 0{,}46Ws}{16129V^2 - 9409V^2} = 136{,}9\mu F$$

Alternatively a rule of thumb for choosing C_{IN} can be applied:

Input voltage	C_{IN}
115V	2µF/W
230V	1µF/W
85V ...270V	2 ...3µF/W....................

$$59W \cdot 3\frac{\mu F}{W} = 177\mu F$$

Recalculation of input Capacitor:

Select a capacitor from the Epcos Databook of **Aluminium Electrolytic Capacitors**.

The following types are **preferred**:

For 85°C Applications:

Series	B43303-........	2000h life time
	B43501-........	10000h life time

For 105°C Applications:

Series	**B43504-........**	**3000h life time**
	B43505-........	5000h life time

We choose 150µF 400V (based on Eq 8)

$$V_{DC\min} = \sqrt{V_{DC\min PK}^2 - \frac{2 \cdot W_{IN}}{C_{IN}}} \qquad \textbf{(Eq 9)}$$

$$V_{DC\min} = \sqrt{16129V^2 - \frac{2 \cdot 0{,}46Ws}{150\mu F}} = 100V$$

Note that special requirements for hold up time, including cycle skip/dropout, or other factors which affect the resulting minimum DC input voltage and capacitor time should be considered at this point also.

Transformer Design (TR1):

Calculation of peak current of primary inductance:

$$D_{\max} = \frac{V_{R\max}}{V_{R\max} + V_{DC\min}} \quad \textbf{(Eq 10a)}$$

$$D_{\max} = \frac{120V}{120V + 100V} = 0{,}55$$

$$I_{LPK} = \frac{2 \cdot P_{IN\,MAX}}{V_{DC\min} \cdot D_{\max}} \quad \textbf{(Eq 10b)}$$

$$I_{LPK} = \frac{2 \cdot 59W}{100V \cdot 0{,}55} = 2{,}16A$$

$$I_{LRMS} = I_{LPK} \cdot \sqrt{\frac{D_{\max}}{3}} \quad \textbf{(Eq 11)}$$

$$I_{LRMS} = 2{,}16A \cdot \sqrt{\frac{0{,}55}{3}} = 0{,}92A$$

Calculation of primary inductance within the limit of **maximum Duty-Cycle** :

$$L_P = \frac{D_{\max} \cdot V_{DC\min}}{I_{LPK} \cdot f} \quad \textbf{(Eq 12)}$$

$$L_P = \frac{0{,}55 \cdot 100V}{2{,}16A \cdot 100 * 10^3\,Hz} = 253\mu H$$

Select core type and inductance factor (A_L) from **Epcos „Ferrite Databook“ or CD-ROM „Passive Components“**.

Fix maximum flux density:

$B_{max} \approx$ 0,2T ...0,3T for ferrite cores depending on core material.

We choose 0,2T for material N27

Selected core: **E 25/13/7**

Material = N27

A_L = 111 nH

s = 0,75 mm

A_e = 52 mm^2

A_N = 61 mm^2

l_N = 57,5 mm

The number of primary turns can be calculated as:

$$N_P = \sqrt{\frac{L_P}{A_L}} \quad \textbf{(Eq 13)}$$

$$N_P = \sqrt{\frac{253\mu H}{111nH}} = 47{,}7 \quad \text{turns}$$

we choose Np = 46 turns

The number of secondary turns can be calculated as:

$$Ns = \frac{N_P \cdot (V_{OUT} + V_{FDIODE})}{V_{R\max}} \quad \textbf{(Eq 14)}$$

$$Ns = \frac{46 \cdot (16V + 0{,}8V)}{120V} = 6{,}46$$

we choose N_S = 7 turns

The number of auxiliary turns can be calculated as:

$$N_{Aux} = \frac{Ns \cdot (V_{Aux} + V_{FDIODE})}{V_{R\max}} \quad \textbf{(Eq 15)}$$

$$Ns = \frac{46 \cdot (12V + 0{,}7V)}{120V} = 5{,}6$$

we choose N_{Aux} = 5 turns

Verification of primary inductance, primary peak current, max. duty cycle, flux density and gap:

$$L_P = N_P^2 \cdot A_l \qquad \textbf{(Eq 16)}$$

$$L_P = 46^2 \cdot 111nH = 235\mu H$$

$$I_{LPK} = \sqrt{\frac{P_{IN\max}}{0{,}5 \cdot Lp \cdot f}} \qquad \textbf{(Eq 17)}$$

$$I_{LPK} = \sqrt{\frac{59W}{0{,}5 \cdot 235\mu H \cdot 100 * 10^3\,Hz}} = 2{,}24A$$

$$V_R = \frac{(V_{OUT} + V_{FDIODE}) \cdot N_P}{Ns} \qquad \textbf{(Eq 18)}$$

$$V_R = \frac{(16V + 0{,}8V) \cdot 46}{7} = 110V$$

$$D_{\max} = \frac{L_P \cdot I_{LPK} \cdot f}{V_{DC\min}} \qquad \textbf{(Eq 19)}$$

$$D_{\max} = \frac{235\mu H \cdot 2{,}24A \cdot 100kHz}{100V} = 0{,}53$$

$$D'_{\max} = \frac{L_P \cdot I_{LPK} \cdot f}{V_R} \qquad \textbf{(Eq 20)}$$

$$D'_{\max} = \frac{235\mu H \cdot 2{,}24A \cdot 100kHz}{110V} = 0{,}47$$

$$B_{\max} = \frac{L_P \cdot I_{LPK}}{N_P \cdot A_e} \qquad \textbf{(Eq 21)}$$

$$B_{\max} = \frac{235\mu H \cdot 2{,}24A}{46 \cdot 52mm^2} = 210mT$$

$$s = \frac{4 \cdot \pi \cdot 10^{-7} \cdot N_P^2 \cdot A_e}{L_P} \qquad \textbf{(Eq 22)}$$

$$s = \frac{4 \cdot \pi \cdot 10^{-7} \cdot 46^2 \cdot 52mm^2}{235\mu H} = 0{,}588mm$$

Sense resistor

The sense resistance R_{Sense} can be used to individually define the maximum peak current and thus the maximum power transmitted.

Caution:

When calculating the maximum peak current, short term peaks in output-power must also be taken into consideration.

Vcsth = 1.0V typ. (taken from data sheet)

$$R_{Sense} = \frac{V_{csth}}{I_{LPK}} \qquad \textbf{(Eq23)}$$

$$R_{Sense} = \frac{1{,}0V}{2{,}24A} = 0{,}45\Omega$$

we select 0,43Ω $\Rightarrow$ I_{LPK} = 2,33A

P_{OUTmax} = 54W

Winding Design:

see also page 38

Transformer Construction

The primary winding of 46 turns has to be divided into 23+23 turns in order to get the best coupling between primary and secondary winding.

From bobbin datasheet E25/13/7: BW = 15,6mm

Margin determined: M = 0mm

⇒ **we use triple insulated wire for secondary winding**

The effective bobbin width and winding cross section can be calculated as:

$$BW_e = BW - 2 \cdot M \qquad \textbf{(Eq 24)}$$

$$BW_e = 15{,}6mm$$

$$A_{Ne} = \frac{A_N \cdot BW_e}{BW} \qquad \textbf{(Eq 25)}$$

$$A_{Ne} = 61mm^2$$

Calculate copper section for **primary and secondary** winding:

The winding cross section A_N has to be subdivided according to the number of windings.

Primary winding	0,5
Secondary winding	0,45
Auxiliary winding	0,05

Copper space factor f_{Cu} :0,2 0,4

We calculate the **available area** for each winding:

Used for calculation: f_{Cu} =0,3

$$A_P = \frac{0{,}5 \cdot A_N \cdot f_{Cu} \cdot BW_e}{N_P \cdot BW} \qquad \textbf{(Eq 26)}$$

$$A_P = \frac{0{,}5 \cdot 61mm^2 \cdot 0{,}3}{46} = 0{,}2mm^2$$

$$AWG = 9{,}97 \cdot (1{,}8277 - (2 \cdot \log(d))) \qquad \textbf{(Eq 27)}$$

⇒ diameter dp ≈ 0,5mm ⇒ **25 AWG**

$$A_s = \frac{0{,}45 \cdot A_N \cdot f_{Cu} \cdot BW_e}{N_s \cdot BW} \quad \textbf{(Eq 28)}$$

$$A_s = \frac{0{,}45 \cdot 61mm^2 \cdot 0{,}3}{7} = 1{,}18mm^2$$

$\Rightarrow$ diameter ds 2 x 0,8mm $\Rightarrow$ **2 x 20 AWG**

$$A_{aux} = \frac{0{,}05 \cdot A_N \cdot f_{Cu} \cdot BW_e}{N_{aux} \cdot BW} \quad \textbf{(Eq 29)}$$

$$A_{aux} = \frac{0{,}05 \cdot 61mm^2 \cdot 0{,}3}{5} = 0{,}18mm^2$$

$\Rightarrow$ diameter da $\approx$ 0,5mm $\Rightarrow$ **25 AWG**

With the effective bobbin width we check the number of turns per layer:

$$N_P = \frac{BWe}{d_P} \quad \textbf{(Eq 30)}$$

Primary:

$N_P = \dfrac{15{,}6mm}{0{,}46mm} = 31$ turns per layer

$\Rightarrow$ **2 layer needed**

Secondary:

$N_S = \dfrac{15{,}6mm}{2 \cdot 1{,}21mm} = 6$ turns per layer

$\Rightarrow$ **2 layer needed**

Auxiliary: **1 layer !**

Output Rectifier (D1):

The output rectifier diodes in flyback converters are subjected to a large PEAK and RMS current stress. The values depend on the load and operating mode. The voltage requirements depend on the output voltage and the transformer winding ratio.

Calculation of the maximum reverse voltage:

$$V_{RDiode} = V_{OUT} + \left(V_{DC\max PK} \cdot \frac{N_S}{N_P} \right) \quad \textbf{(Eq 31)}$$

$$V_{RDiode} = 16V + \left(373V \cdot \frac{7}{46} \right) = 72{,}8V$$

Calculation of the maximum current on secondary side:

$$I_{SPK} = I_{LPK} \cdot \frac{N_P}{N_S} \quad \textbf{(Eq 32)}$$

$$I_{SPK} = 2{,}33A \cdot \frac{46}{7} = 15{,}3A$$

$$I_{SRMS} = I_{SPK} \cdot \sqrt{\tfrac{1}{3} \cdot D'_{\max}} \quad \textbf{(Eq 33)}$$

$$I_{SRMS} = 15{,}3A \cdot \sqrt{\tfrac{1}{3} \cdot 0{,}47} = 5{,}9A$$

Output Capacitors (C5, C9):

Output capacitors are highly stressed in flyback converters. Normally the capacitor will be selected for **3 major parameters: capacitance value, low ESR and ripple current rating.**

Max. voltage overshoot: ΔV_{OUT}

Number of clock periods: n_{CP}

$$C_{OUT} = \frac{I_{OUT\max} \cdot n_{CP}}{\Delta V_{OUT} \cdot f} \quad \textbf{(Eq 34)}$$

$$I_{OUT} = \frac{P_{OUT\max}}{V_{OUT}} \quad \textbf{(Eq 34a)}$$

$$I_{Ripple} = \sqrt{I_{SRMS}{}^2 - I_{OUT}{}^2} \quad \textbf{(Eq 34b)}$$

Select a capacitor out of **Epcos** Databook for **Aluminium Electrolytic Capacitors**.

The following types are **preferred**:

For 105°C Applications low impedance:
Series B41856-........ 4000h life time

For 105°C Applications lowest impedance:
Series B41859-........ 4000h life time

To calculate the output capacitor, it is necessary to set the maximum voltage overshoot in case of switching off @ maximum load condition.
After switching off the load, the control loop needs about 10...20 internal clock periods to reduce the duty cycle.

$$\Delta V_{OUT} = 0{,}5V$$

$n_{CP} = 20$

$$C_{OUT} = \frac{3{,}1A \cdot 20}{0{,}5V \cdot 100 * 10^3\,Hz} = 1250\mu F$$

$$I_{OUT} = \frac{50W}{16V} = 3{,}1A$$

$$I_{Ripple} = \sqrt{5{,}9A^2 - 3{,}1A^2} = 5{,}0A$$

We select 1000µF 35V (based on Eq 34):

B41859-F7108-M

ESR ≈ Zmax = 0,034Ω @ 100kHz

Iac_R = 1,94A

⇒ **we need 2 capacitors in parallel**

Output Filter (L3, C23):

The output filter consists of one capacitor (C23) and one inductor (L3) in a L-C filter topology.

Zero frequency of output capacitor (C5,C9, C20) and associated ESR:

$$f_{ZCOUT} = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{OUT}}$$ **(Eq 35)**

$$f_{ZCOUT} = \frac{1}{2 \cdot \pi \cdot 0{,}034\Omega \cdot 1000\mu F} = 4{,}7kHz$$

Calculation of the inductance (L3) needed for the substitution of the zero caused by the output capacitors:

We use C_{LC} (C23) 470uF

$$L_{OUT} = \frac{(C_{OUT} \cdot R_{ESR})^2}{C_{LC}}$$ **(Eq 36)**

$$L_{OUT} = \frac{(1000uF \cdot 0{,}034\Omega)^2}{470uF} = 2{,}5uH$$

RC-Filter at Feedback Pin

(C6, R9)

The RC Filter at the Feedback pin is designed to supress any noise which may be coupled in on this track.

Typical values:
C6 : 1...4,7nF
R9 : 22 Ohm

Note that the value of C6 interacts with the internal pullup (3,7k typical) to create a filter.

Soft-start capacitor

(C14)

The voltage at the soft-start pin together with feedback voltage controls the overvoltage, open loop and overcurrent protection functions.

The softstart capacitor must be calculated in such a way that the output voltage and thus the feedback voltage is within the working range (V_{FB} < 4.8V) before the over-current threshold (typ. 5.3V) is reached.

$$t_{Sstart} = Vo^2 \cdot \frac{C_{out}}{P_{OUT\max} - P_{OUTnom}} \qquad \textbf{(Eq37)}$$

$$C_{SS} = t_{Sstart} \cdot \frac{1}{-R_{Soft-Start} \cdot \ln(1 - \frac{V_{Soft-Start1}}{V_{REF}})} \qquad \textbf{(Eq38)}$$

$R_{soft\ start}$ = 50kΩ typ (from datasheet).

$$t_{Sstart} = 16V^2 \cdot \frac{2470uF}{54W - 40W} = 45ms$$

$$C_{SS} = 45ms \cdot \frac{1}{-50k\Omega \cdot \ln(1 - \frac{5{,}1V}{6{,}5V})} = 586nF$$

choose 560nF

VCC Capacitor:

(C4, C13)

The VCC capacitor needs to ensure the power supply of the IC until the power can be provided by the auxiliary winding.
In parallel with the VCC Capacitor it is recommended to use a 100nF ceramic capacitor very close between pin 7 & 8. Alternatively, an HF type electrolytic with low ESR and ESL may be used.

$$C_{VCC} = \frac{I_{VCC3} \cdot t_{softstart}}{V_{CCHY}} * \frac{2}{3} \quad \textbf{(Eq 39)}$$

$$C_{VCC} = \frac{8{,}2mA \cdot 45ms}{5V} * \frac{2}{3} = 49uF$$

we choose 47uF

Start-up Resistor (R6, R7):

I_{VCC1} = max. quiescent current (Control IC)
I_{LoadC} = VCC-Capacitor load-current (C4)
C_{VCC} = Value of VCC-capacitor (C4)

I_{CCLmax} = 55µA
I_{LoadC} = 70µA

$$R_{Start} = \frac{V_{DC\,\min}}{I_{VCC1} + I_{LoadC}} \quad \textbf{(Eq 40)}$$

$$R_{Start} = \frac{100V}{(55+70)\mu A} = 801k\Omega$$

R6 = R7 =1/2 R_{Start} = 400kΩ

Choose 2 with value: 390kΩ

Start up Time t_{Start}:

$$t_{Start} = \frac{C_{VCC} \cdot V_{CCon}}{I_{LoadC}} \quad \textbf{(Eq 41)}$$

$$t_{Start} = \frac{47\mu F \cdot 13{,}5V}{73\mu A} = 8{,}7s$$

Note:
Before the IC can be plugged into the application board, the VCC capacitor must be always <u>discharged</u>!

Clamping Network:

(R10/C12/D3)

$$V_{Clamp} = V_{(BR)DSS} - V_{DC\max} - V_R \qquad \textbf{(Eq 42)}$$

For calculating the clamping network it is necessary to know the leakage inductance. The most common way is to have the value of the leakage inductance (L_{LK}) given in percentage of the primary inductance (Lp). If it is known that the transformer construction is very consistent, measuring the primary leakage inductance by shorting the secondary windings will give an exact number (assuming the availability of a good LCR analyser).

$$L_{LK} = Lp \cdot x\%$$

$$C_{Clamp} = \frac{I_{LPK}{}^2 \cdot L_{LK}}{\left(V_R + V_{Clamp}\right) \cdot V_{Clamp}} \qquad \textbf{(Eq 43)}$$

$$R_{Clamp} = \frac{\left(V_{Clamp} + V_R\right)^2 - V_R^2}{0{,}5 \cdot L_{LK} \cdot I_{LPK}{}^2 \cdot f} \qquad \textbf{(Eq 44)}$$

$$V_{Clamp} = 650V - 373V - 110V = 166V$$

In our example we choose 5% of the primary inductance for leakage inductance.

$$L_{LK} = 235\mu H \cdot 5\% = 11{,}8\mu H$$

$$C_{Clamp} = \frac{(2{,}24A)^2 \cdot 11{,}8\mu H}{\left(110V + 166V\right) \cdot 166V} = 1{,}2nF \approx$$

we choose 1,5nF

$$R_{Clamp} = \frac{\left(166V + 110V\right)^2 - 110V^2}{0{,}5 \cdot 11{,}8\mu H \cdot (2{,}24A)^2 \cdot 100 * 10^3 Hz} = 23{,}9k\Omega$$

we choose 22kΩ

Calculation of Losses:

Input diode bridge (BR1):

$$P_{DIN} = I_{ACRMS} \cdot V_F \cdot 2 \qquad \textbf{(Eq 45)}$$

$$P_{DIN} = 1{,}1A \cdot 1V \cdot 2 = 2{,}2W$$

Calculation of copper resistance R_{Cu}:

Copper resistivity p_{100} @ 100°C = 0,0172Ωmm²/m

$$R_{PCu} = \frac{l_N \cdot N_P \cdot p_{100}}{A_P} \qquad \textbf{(Eq 46)}$$

$$R_{PCu} = \frac{0{,}0644m \cdot 46 \cdot 17{,}2m\Omega mm^2 / m}{0{,}46mm^2} = 277{,}1m\Omega$$

$$R_{SCu} = \frac{0{,}0644m \cdot 7 \cdot 17{,}2m\Omega mm^2 / m}{2{,}10mm^2} = 6{,}6m\Omega$$

Calculation of copper losses (TR1):

$$P_{PCu} = I_{LPK}^2 \cdot D_{MAX} \cdot {}^1\!/_3 \cdot R_{PCu} \qquad \textbf{(Eq 47)}$$

$$P_{SCu} = I_{SPK}^2 \cdot D'_{MAX} \cdot {}^1\!/_3 \cdot R_{SCu}$$

$$P_{PCu} = (2{,}33A)^2 \cdot 0{,}53 \cdot {}^1\!/_3 \cdot 277{,}1m\Omega = 225{,}7mW$$

$$P_{SCu} = (15{,}3A)^2 \cdot 0{,}47 \cdot {}^1\!/_3 \cdot 2{,}01m\Omega = 227{,}4mW$$

$$\sum P_{Cu} = 225{,}7mW + 227{,}4mW = 453{,}1mW$$

Output rectifier diode (D1):

$$P_{DDIODE} = I_{SPK} \cdot \sqrt{\frac{D'_{\max}}{3}} \cdot V_{FDIODE} \qquad \textbf{(Eq 48)}$$

$$P_{DDIODE} = 15{,}3A \cdot \sqrt{\frac{0{,}47}{3}} \cdot 0{,}8V = 5W$$

COOLMOS TRANSISTOR:

ICE2A365 $C_{o(er)}$ = 30pF

Calculated @ V_{DCmin} = 100V

$C_O \approx$ 80pF ($C_O = C_{O(er)} + C_{Extern}$)

R_{DSON} = 1,1Ω (@ 125°C)

Switching losses:

(see also ICE2AXXX Data Sheet)

$$P_{SON} = \frac{1}{2} \cdot C_O \cdot V_{DC\min}^2 \cdot f$$ **(Eq 49)**

$$P_{SON} = \frac{1}{2} \cdot 80pF \cdot 100V^2 \cdot 100*10^3\,Hz = 40mW$$

Conduction losses:

$$P_D = \frac{1}{3} \cdot R_{DSON} \cdot I_{LPK}^2 \cdot D_{\max}$$ **(Eq 50)**

$$P_D = \frac{1}{3} \cdot 1\Omega \cdot (2{,}33A)^2 \cdot 0{,}53 = 0{,}95W$$

Summary of Losses:

$$P_{Losses} = P_{SON} + P_D$$ **(Eq 51)**

$$P_{Losses} = 40mW + 950mW = 0{,}99W$$

Thermal Calculation:

Table of typical thermal Resistance [$\frac{K}{W}$]:

Heatsink	DIP8	DIP7	TO220
No	90	96	74
3 cm²	64	72	
6 cm²	56	65	

$$dT = P_{Losses} * R_{th}$$ **(Eq 52)**

$$dT = 0{,}99W * 56\frac{K}{W} = 55{,}4K$$

$$Tj = dT + Ta$$ **(Eq 53)**

$$Tj = 55{,}4K + 50°C = 115{,}4°C$$

Regulation Loop:

Reference: TL431 (IC2)

V_{REF} =2,5V

I_{KAmin}=1mA

Optocoupler: SFH617-3 (IC1)

Gc = 1 ...2 ≡ CTR 100% ...200%

V_{FD} = 1,2V

I_{Fmax} =20mA (maximum current limit)

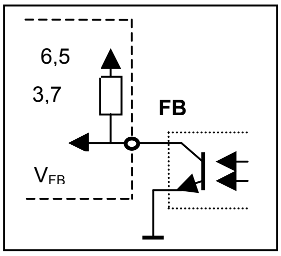

Fig. 13

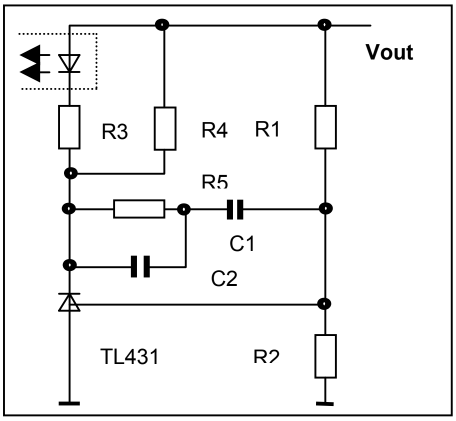

Fig. 14

Primary side:

Feedback voltage:

Values from **ICE2AXXX** datasheet

$V_{Ref\ int}$ = 6,5V typ.

V_{FBmax} = 4,5V

Av = 3,65

R_{FB} = 3,7k typ.

$$I_{FB\max} = \frac{V_{Ref\,int}}{R_{FB}} \qquad \textbf{(Eq 54)}$$

$$I_{FB\max} = \frac{6{,}5V}{3{,}7k\Omega} = 1{,}76mA$$

$$I_{FB\min} = \frac{V_{Ref\,int} - V_{FB\max}}{R_{FB}} \qquad \textbf{(Eq 55)}$$

$$I_{FB\min} = \frac{6{,}5V - 4{,}6V}{3{,}7k\Omega} = 0{,}5mA$$

Secondary side:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right) \qquad \textbf{(Eq 56)}$$

$$R_1 = 4{,}3k \cdot \left(\frac{16V}{2{,}5V} - 1\right) = 23{,}22k$$

the value of R2 can be fixed at 4,3k

$$R_3 \geq \frac{(V_{OUT} - (V_{FD} + V_{REF}))}{I_{F\max}} \qquad \textbf{(Eq 57)}$$

$$R_3 \geq \frac{(16V - (1{,}2V + 2{,}5V))}{20mA} = 0{,}74k \approx 0{,}75\text{k}$$

$$R_4 \leq \frac{V_{FD} + \left(R_3 \cdot \frac{I_{FB\min}}{Gc}\right)}{I_{KA\min}} \qquad \textbf{(Eq 58)}$$

$$R_4 \leq \frac{1{,}2V + 0{,}75k \cdot \left(\frac{0{,}5mA}{1}\right)}{1mA} = 1{,}58k \approx 1{,}5\text{k}$$

Regulation Loop Elements:

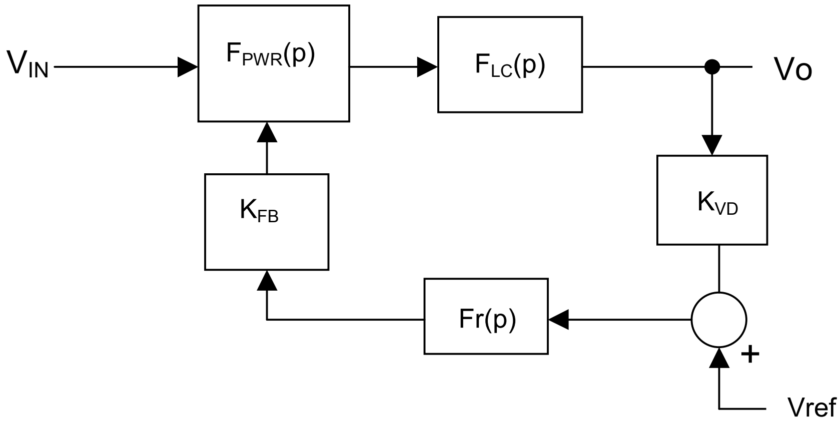

Fig. 15

Transfer Characteristics of Regulation Loop Elements:

$$K_{FB} = \frac{G_C \cdot 3k7}{R3}$$ **(Eq 59) Feedback**

$$K_{VD} = \frac{R2}{R1+R2} = \frac{V_{REF}}{V_{OUT}}$$ **(Eq 60) VoltageDivider**

$$F_{PWR}(p) = \frac{1}{Z_{PWM}} \cdot \sqrt{\frac{R_L \cdot L_P \cdot f \cdot \eta}{2}} \cdot \left(\frac{(1 + p \cdot R_{ESR} \cdot C_5)}{\left(1 + p \cdot \left(\frac{R_L}{2} + R_{ESR}\right) \cdot C_5\right)} \right)$$ **(Eq 61) Powerstage**

Z_{PWM} = Transimpedance $\Delta V_{FB}/\Delta I_D$

$$F_{LC}(p) = \frac{1 + p \cdot R_{ESR} \cdot C_9}{1 + p \cdot R_{ESR} \cdot C_9 + p^2 \cdot L \cdot C_9}$$ **(Eq 62) Output filter**

$$Fr(p) = \frac{1 + p \cdot R5 \cdot (C1 + C2)}{p \cdot \frac{R1 \cdot R2}{R1 + R2} \cdot C1 \cdot (1 + p \cdot R5 \cdot C2)}$$ **(Eq 63) Regulator**

Zeros and Poles of transfer characteristics:

Poles of powerstage @ min. and max. load:

$$R_{LH} = \frac{V_{OUT}^{2}}{P_{OUT\,max}} = \frac{16V^{2}}{54W} = 4{,}9\Omega \quad \textbf{(Eq 64)} \qquad R_{LL} = \frac{V_{OUT}^{2}}{P_{OUT\,min}} = \frac{16V^{2}}{0{,}5W} = 512\Omega \quad \textbf{(Eq 65)}$$

$$f_{OH} = \frac{1}{\pi \cdot R_{LH} \cdot C5} \qquad f_{OH} = \frac{1}{\pi \cdot 4{,}9\Omega \cdot 2000\mu F} = 31{,}1Hz \quad \textbf{(Eq 66)}$$

$$f_{OL} = \frac{1}{\pi \cdot R_{LL} \cdot C5} \qquad f_{OL} = \frac{1}{\pi \cdot 512\Omega \cdot 2000\mu F} = 0{,}31Hz \quad \textbf{(Eq 67)}$$

We use the gain (Gc) of the optocoupler stage K_{FB} and the voltage divider K_{VD} as a constant.

$$K_{FB} = \frac{G_C \cdot 3k7}{R3} \qquad K_{FB} = 4{,}9 \qquad \Rightarrow \mathbf{G_{FB} = 13{,}9db}$$

$$K_{VD} = \frac{R2}{R1 + R2} = \frac{V_{REF}}{V_{OUT}} \qquad K_{VD} = 0{,}15 \qquad \Rightarrow \mathbf{G_{VD} = -16{,}4db}$$

With adjustment of the transfer characteristics of the regulator we want to reach equal gain within the operating range and to compensate the pole **fo** of the powerstage $F_{PWR}(\omega)$.

Because of the compensation of the output capacitor‘s zero (see page 22 Eq35, Eq36) we neglect it as well as the LC-Filter pole.

Consequently the transfer characteristic of the power stage is reduced to a single-pole response.

In order to calculate the gain of the open loop we have to select the cross-over frequency.

We calculate the gain of the Power-Stage with max. output power at the selected cross-over frequency
fg = 3kHz:

Calculation of transient impedance Z_{PWM} of ICE2AXXX

The transient impedance defines the direct relationship between the level of the peak current and the feedback pin voltage. It is required for the calculation of the power stage amplification.
PWM-Op gain -Av = 3,65 (according to datasheet)

$$Z_{PWM} = \frac{\Delta V_{FB}}{\Delta I_{pk}} = A_v \cdot \frac{R_{sense}}{V_{csth}} \tag{Eq 68}$$

$$Z_{PWM} = \frac{\Delta V_{FB}}{\Delta I_{pk}} = 3{,}65 \cdot \frac{0{,}43\Omega}{1{,}00V} = 1{,}57\frac{V}{A}$$

Gain @ crossover frequency:

$$\left|F_{PWR}(fg)\right| = \frac{1}{Z_{PWM}} \cdot \sqrt{\frac{R_L \cdot L_p \cdot f \cdot \eta}{2}} \cdot \left(\frac{1}{\sqrt{1+\left(\frac{fg}{fo}\right)^2}} \right) \tag{Eq 69}$$

$$\left|F_{PWR}(3kHz)\right| = \frac{1}{1{,}7} \cdot \sqrt{\frac{5{,}1R \cdot 235\mu H \cdot 100kHz \cdot 0{,}8}{2}} \cdot \left(\frac{1}{\sqrt{1+\left(\frac{3000}{31{,}1}\right)^2}} \right) = 0{,}05$$

⇒ G_{PWR}(3kHz) = **-26,2db**

Transfer characteristics:

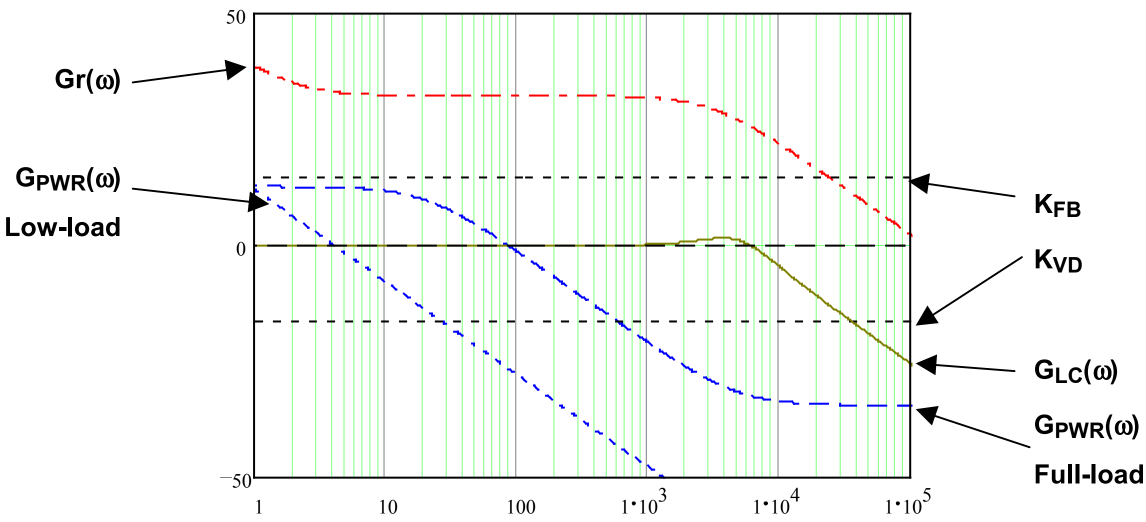

Fig. 16

At the crossover frequency (fg) we calculate the open loop gain:

$G_{ol}(\omega) = Gs\ (\omega) + Gr\ (\omega) = 0.$

With the equations for the transfer characteristics we calculate the gain of the regulation loop @ fg.

For the gain of the regulation loop we calculate:

$Gs = G_{FB} + G_{PWR} + G_{VD}$ = 13,9db – 26,2db – 16,4db

Gs = -28,7db

We calculate the separate components of the regulator:

Gs (ω) + Gr (ω) = 0 $\Rightarrow$ Gr = 0 – (-28,7db) = **28,7db**

$$Fr(p) = \frac{1 + p \cdot R5 \cdot (C1 + C2))}{p \cdot \frac{R1 \cdot R2}{R1 + R2} \cdot C1 \cdot (1 + p \cdot R5 \cdot C2)}$$

$$Gr = 20 \cdot \log \frac{R5 \cdot (R1 + R2)}{R1 \cdot R2} \qquad \Rightarrow \quad R5 = 10^{\frac{Gr}{20}} \cdot \frac{R1 \cdot R2}{R1 + R2}$$

$$R5 = 10^{\frac{32,2}{20}} \cdot 3,65k = 99,15k \approx \mathbf{100k} \qquad \textbf{(Eq 70)}$$

$$fp = \frac{1}{2 \cdot \pi \cdot R5 \cdot C2} \qquad \Rightarrow \quad C2 = \frac{1}{2 \cdot \pi \cdot R5 \cdot fg}$$

$$C2 = \frac{1}{2 \cdot \pi \cdot 100k \cdot 3kHz} = 530\,pF \approx \mathbf{560pF} \qquad \textbf{(Eq 71)}$$

In order to have enough phase margin @ low load condition we select the zero frequency of the compensation network to be at the middle between the min. and max. load poles of the power stage.

$$f_{om} = f_{oh} \cdot 10^{0,5 \cdot \log \frac{f_{ol}}{f_{oh}}} \qquad f_{om} = 31,1Hz \cdot 10^{0,5 \cdot \log \frac{0,15}{31,1}} = 3,2Hz$$

$$fz = \frac{1}{2 \cdot \pi \cdot R5 \cdot (C1 + C2)} \qquad \Rightarrow \quad C1 = \frac{1}{2 \cdot \pi \cdot R5 \cdot fom} - C2$$

$$C1 = \frac{1}{2 \cdot \pi \cdot 100k \cdot 3,2Hz} - 560\,pF = 492nF \approx \mathbf{470nF} \qquad \textbf{(Eq 72)}$$

Open Loop Gain

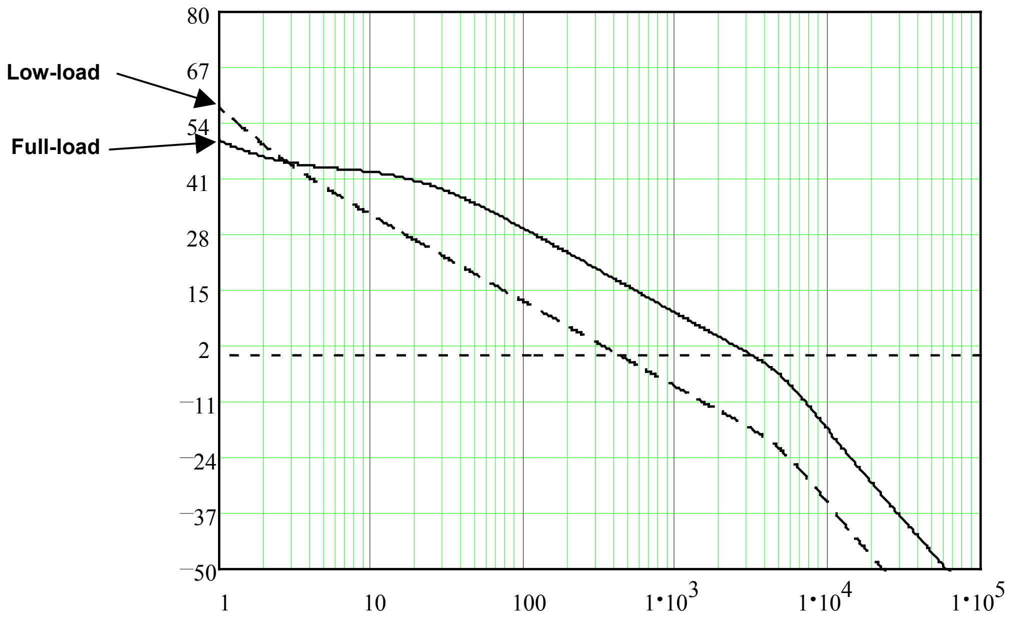

Fig. 17

Open Loop Phase

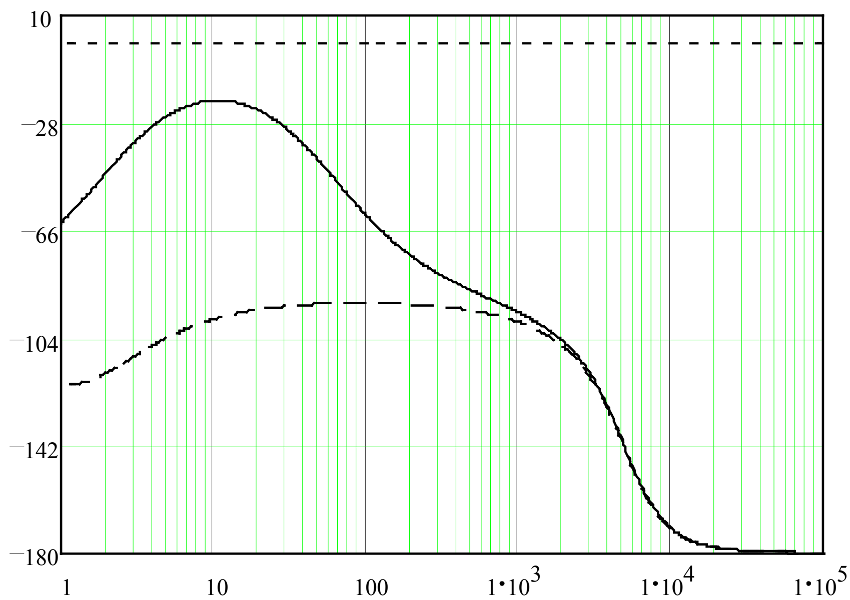

Fig. 18

Continuous Conduction Mode (CCM)

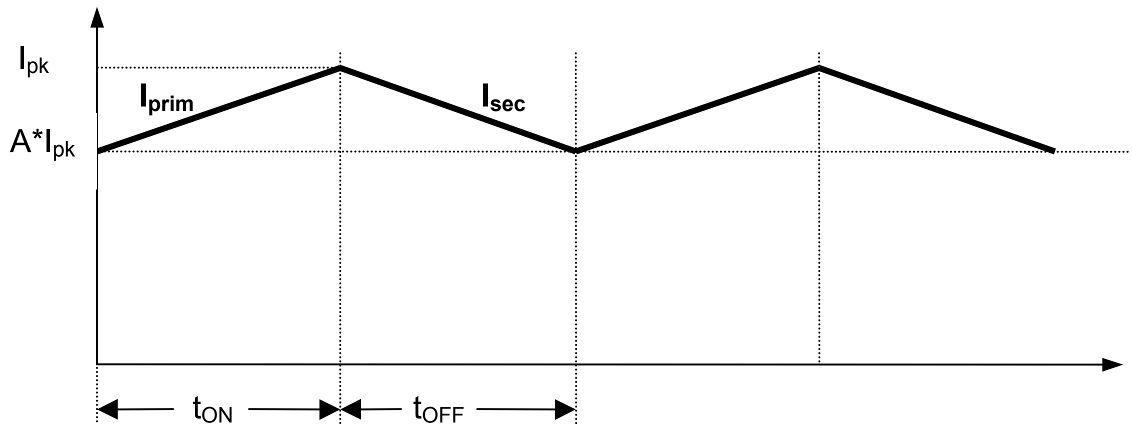

Fig. 19

Transformer calculation:

The transformer is calculated in such a way that DCM operation is just barely reached (A=0) at minimum output power P_{Omin}.

Po_{min} = 2W

Po_{max} = 10W

D_{max} = 0,6

$$p = \frac{Po_{\max}}{Po_{\min}}$$

$$Ipk = \frac{Po_{\min} + Po_{\max}}{D_{\max} \cdot V_{dc\min} \cdot \eta}$$

$$Lp = \frac{Po_{\max} \cdot (p+1)^2 * D_{\max}}{Ipk^2 \cdot f \cdot p}$$

$$p = \frac{10W}{2W} = 5$$

$$Ipk = \frac{2W + 10W}{0{,}6 \cdot 100V \cdot 0{,}8} = 0{,}25A$$

$$Lp = \frac{10W \cdot (5+1)^2 * 0{,}6}{0{,}25^2 \cdot 100kHz \cdot 5} = 6{,}91mH$$

Slope Compensation

Slope compensation is necessary for stable regulator operation in **Continuous Conduction Mode (CCM)**, up to and beyond a duty cycle of 0.5 (see also [4]).

An simple method of slope compensation using the components R19, C17 and C18 is illustrated in the circuit diagram on page 3 .

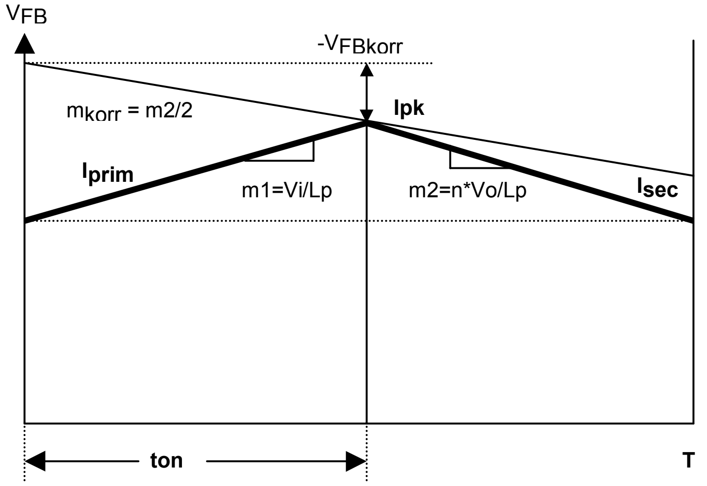

Fig. 20

$$V_R = n \cdot Vo \qquad n = \frac{n_p}{n_s}$$

$$m2 = \frac{n \cdot Vo}{L_p} = \frac{V_R}{L_p} \qquad m_{korr} = \frac{m2}{2} = \frac{V_R}{2 \cdot L_p}$$

For duty cycle = 0,5 applies:

$$m_{korr} = \frac{V_{FBkorr}}{5us} \Rightarrow \qquad V_{FBkorr} = \left(\frac{V_R \cdot 5us}{2 \cdot L_p}\right) \cdot Z_{PWM}$$

C_{Comp} (C17) is selected at 10nF.

C18 is selected at 100nF.

R_{Comp} (R19):

$$R_{Comp} = -\frac{t}{\ln\left(1 - \frac{V_{FBkorr}}{VCC}\right) \cdot C_{Comp}}$$

Transformer Construction

The winding topology has a considerable influence on the performance and reliability of the transformer.
In order to reduce leakage inductance and proximity to acceptable limits, the use of a sandwich construction is recommended.
In order to meet international safety requirements a transformer for Off - Line power supply must have adequate insulation between primary and secondary windings.
This can be achieved by using a margin-wound construction or by using triple insulated wire for the secondary winding.
The creepage distance for the universal input voltage range is typically 8mm. This results in a minimum margin width (as a half of the creepage distance) of 4mm. Additionally the neccesary insulation between primary and secondary winding is provided using three layers of basic insulation tape.

Example of winding topology for margin wound transformers:

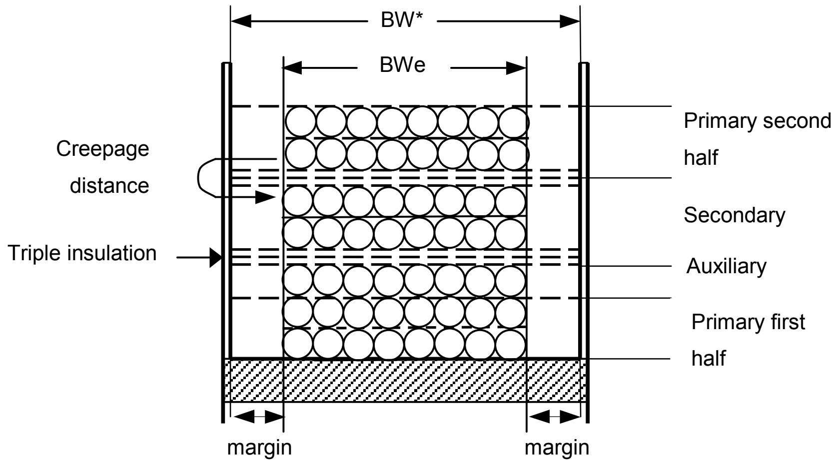

Fig. 21

Example of winding topology with triple insulated wire for secondary winding:

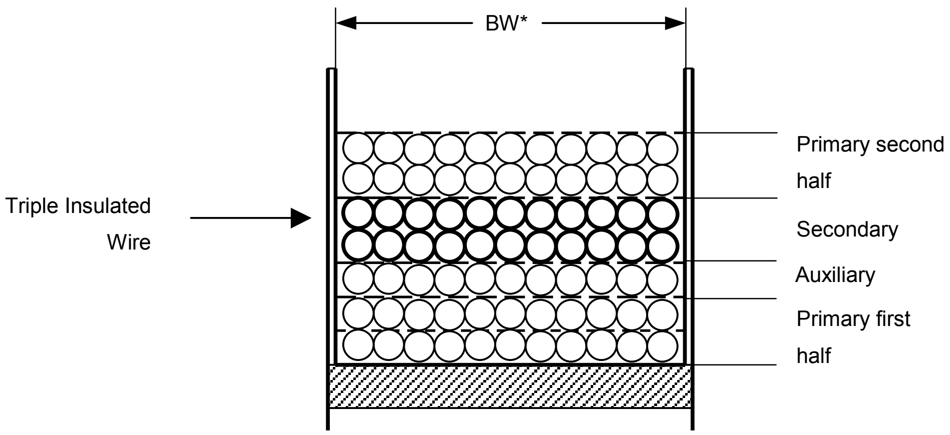

Fig. 22

BW* : value from bobbin datasheet

Layout Recommendation:

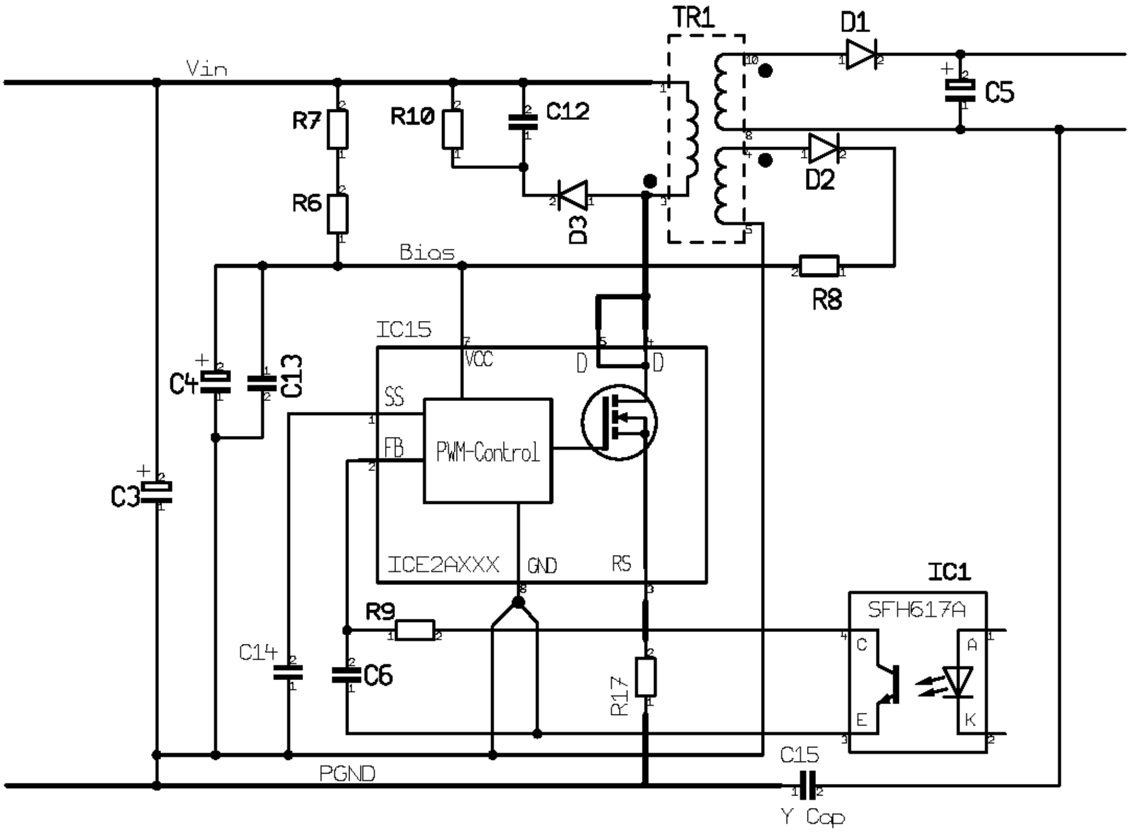

Fig. 23

In order to avoid crosstalk on the board between power and signal path we have to use care regarding the track layout when designing the PCB.

The power path (see Fig. 23) has to be as short as possible and needs to be separated from the VCC Path and the feedback path. All GND paths have to be connected together at pin 8 (star ground) of ICE2AXX.

CoolSET Table

DevICE	Package	Current A	Rdson Ω	Pout @ 190Vacin Ta=75°C / Tj = 125°C	Pout @ 85Vacin Ta=75°C / Tj = 125°C	Heatsink	Frequency KHz
V_{DS}=650V							
ICE2A0565	DIP8	0.5	6.0	23	13	6 cm²	100
ICE2A0565Z	DIP7	0.5	6.0	21	12	6 cm²	100
ICE2A165	DIP8	1.0	3.0	31	18	6 cm²	100
ICE2B165	DIP8	1.0	3.0	31	18	6 cm²	67
ICE2A265	DIP8	2.0	0.9	52	32	6 cm²	100
ICE2B265	DIP8	2.0	0.9	52	32	6 cm²	67
ICE2A365	DIP8	3.0	0.45	67	45	6 cm²	100
ICE2B365	DIP8	3.0	0.45	73	45	6 cm²	67
ICE2A765P	TO220	7.0	0.5	240	130	2.7 k/W	100
ICE2B765P	TO220	7.0	0.5	240	130	2.7 k/W	67
V_{DS}=800V							
ICE2A180	DIP8	1.0	3.0	31	18	6 cm²	100
ICE2A180Z	DIP7	1.0	3.0	29	17	6 cm²	100
ICE2A280	DIP8	2.0	0.8	54	34	6 cm²	100
ICE2A280Z	DIP7	2.0	0.8	50	31	6 cm²	100

Output Power Notes:

The output power was created using the equations of this application note (see „Calculation of Losses“ on page 27). It shows the maximum practical continuous power @ Ta = 75 °C and Tj = 125 °C with the recommended heatsink as a copper area on PCB for DIP7 / 8 and PDSO14 packages.

Summary of used Nomenclature

B_{max} Magnetic Inductance
BW Bobbin Width
BWe Effective Bobbin Width
C_{IN} Capacitance of Bulk Capacitor
C_{OUT} Output Capacitance
C_{OSS} Output Capacitance of **CoolMOS™**
C_{Extern} Output Capacitance of external Components
C_{Clamp} Capacitance of Clamping – Capacitor
C_{VCC} Capacitance of VCC – Capacitor
D Duty Cycle
D_{max} Maximum Duty Cycle
f Operating Frequency of **CoolSET™** (f = 100kHz)
f_{AC} Line Frequency (Germany F_{AC} = 50Hz)
f_g Crossover Frequency
f_{Cu} Copper Space Factor (0,2 ... 0,4)
f_{OH} Frequency Open Loop (High)
f_{Om} Frequency Open Loop (middle)
f_{OL} Frequency Open Loop (Low)
f_{ZCOUT} Zero Frequency of output Capacitor
G_C Optocoupler Gain
I_{FBmax} Maximum Feedback Current
I_{FBmin} Minimum Feedback Current
I_{Fmax} Maximum Current (Optocoupler)
I_{KAmin} Minimum Current (TL431)
I_{LoadC} VCC – Capacitor Load – Current
I_{LPK} Peak Current through the primary Inductance
I_{ACRMS} Root Mean Square Current through the primary Inductance
I_{ACRMS} Root Mean Square Current through the Bridge Rectifier
I_{PRI} Primary Current @ time t
I_{SEC} Secondary Current @ time t
I_{SPK} Peak Current through the secondary diode
I_{SRMS} RMS Current through the secondary diode
I_{VCC1} Maximum quiescent Current of CoolSET™ (Control IC)
L_{OUT} Inductance output Filter
L_P Primary Inductance
L_{LK} Leakage Inductance
M Margin (of Transformer)
n_{CP} Number of Clock Periods
n_{pCOUT} Number of parallel output Capacitors
N_P Number of primary Turns
N_S Number of secondary Turns
N_{Aux} Number of auxiliary Turns
P_{Cu} Power losses of Copper Resistor
P_D Conduction losses
P_{DIN} Power losses input Diode
P_{DDIODE} Power losses rectifier Diode (secondary side)
$P_{IN\,MAX}$ Maximum Input Power
$P_{OUT\,max}$ Maximum Output Power
$P_{OUT\,min}$ Minimum Output Power
P_{PCu} Power losses of Copper Resistor (primary Inductance)
P_{SCu} Power losses of Copper Resistor (secondary Inductance)
P_{SOFF} Switching losses of **CoolMOS™** Transistor (Off – Operation)
P_{SON} Switching losses of **CoolMOS™** Transistor (On – Operation)

R_{Cu} Copper Resistor (Transformer)
R_{DSON} Resistance of switching **CoolMOS™** Transistor (On – Operation)
R_L Load - Resistance
R_{LH} Maximum Load
R_{LL} Minimum Load (defined by Designer)
R_{FB} Internal Feedback Resistor (CoolSET™)
R_{PCu} Copper Resistor of primary Inductance
R_{SCu} Copper Resistor of secondary Inductance
R_{Clamp} Clamping Resistor
R_{Start} Start up Resistor
T Time of one Period
T_D Discharging Time of Input Capacitor C3
t_{ON} On Time (**CoolMOS™**)
t_{OFF} Off Time (**CoolMOS™**)
t_r Rising Time (Voltage)
t_{Start} Start up Time
$V_{AC\,min}$ Minimal AC Input Voltage
$V_{AC\,max}$ Maximal AC Input Voltage
V_{Aux} Auxiliary Voltage
$V_{(BR)DSS}$ Drain Source Breakdown Voltage
V_{CCon} Turn On Threshold for **CoolSET™** @ Vcc - Pin
$V_{DC\,IN}$ DC Input Voltage
$V_{DC\,IN\,max}$ Maximum DC Input Voltage
$V_{DC\,IN\,min}$ Minimum DC Input Voltage
$V_{DC\,max\,PK}$ Maximum DC Input Voltage Peak
$V_{DC\,min\,PK}$ Minimum DC Input Voltage Peak
$V_{DC\,min}$ Minimum DC Input Voltage @ maximum load
V_{DDIODE} Reverse Voltage rectifier Diode (secondary side)
V_{FBmax} Maximum Feedback Voltage (**CoolSET™**)
V_{FDIODE} Output Diode Forward Voltage
V_{FD} Forward Diode Voltage (Optocoupler)
V_{OUT} Output Voltage (secondary Side)
$V_{OUT\,Ripple}$ Output Ripple Voltage (secondary Side)
V_R Reflected Voltage (from secondary side to primary side)
V_{RDiode} Reverse Voltage Diode
V_{Refint} Internal Reference Voltage (**CoolSET™**)
V_{REF} Reference Voltage TL431
V_{Ripple} DC Ripple Voltage (on primary Side)
V_{SEC} Voltage on Sekondary Inductor
V_{Clamp} Maximum Voltage overshoot @ clamping network
W_{IN} Discharging Energie Input Capacitor
Z_{PWM} Transimpedanz

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44	----------	Second Issue
40	-------------	CoolSET Table Update

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