# AN-8024

## Applying Fairchild Power Switch (FPS™) FSBH-series to Standby Auxiliary Power Supply

### 1. Introduction

The highly integrated FSBH-series consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche-rugged 700V SenseFET. It is specifically designed for high-performance offline Switch-Mode Power Supplies (SMPS) with minimal external components.

The integrated PWM controller features include a proprietary green-mode function that provides off-time modulation to linearly decrease the switching frequency at light-load conditions to minimize standby power consumption. The PWM controller is manufactured using the BiCMOS process to further reduce power consumption. The green and burst modes function with a low operating current (2.5mA in green mode) to maximize the light load efficiency so that the power supply can meet stringent standby power regulations.

The FSBH-series has built-in synchronized slope compensation to achieve stable peak-current-mode control. The proprietary external line compensation ensures constant output power limit over a wide AC input voltage range, from $90V_{AC}$ to $264V_{AC}$ and helps optimize the power stage.

Many protection functions, such as open-loop / overload protection (OLP), over-voltage protection (OVP), brownout protection, and over-temperature protection (OTP); are fully integrated into FSBH-series, which improves the SMPS reliability without increasing the system cost.

This application note presents design consideration to apply FSBH-series to a standby auxiliary power supply with single output. It covers designing the transformer, selecting the components, feedback loop design, and design tips to maximize efficiency. For multi-output applications, refer to Fairchild application note AN-4137.

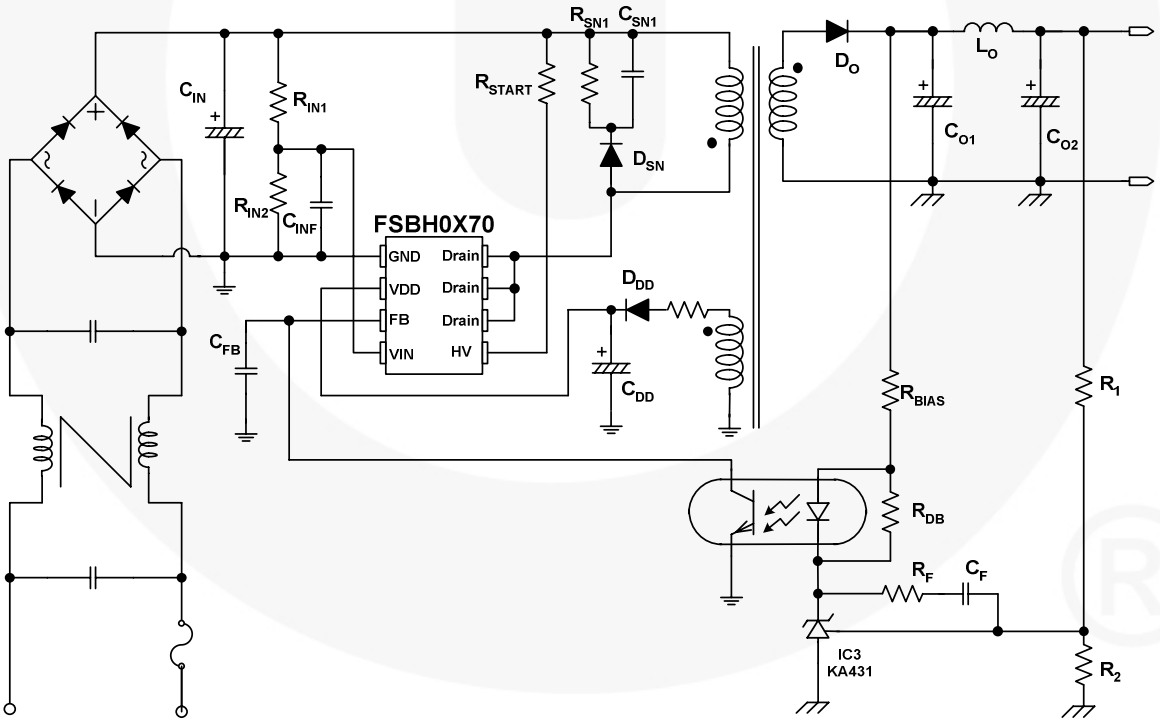


**Figure 1. Typical Application Circuit**

## 2. Design Considerations

Flyback converters have two kinds of operation modes; Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). CCM and DCM each has advantages and disadvantages. In general, DCM provides better switching conditions for the rectifier diodes, since the diodes are operating at zero current just before becoming reverse biased and the reverse recovery loss is minimized. The transformer size can be reduced using DCM because the average energy storage is low compared to CCM. However, DCM inherently causes high RMS current, which increases the conduction loss of the MOSFET severely for low line condition. Thus, especially for standby auxiliary power supply applications with low output voltage where Schottky diode without reverse recovery can be used; it is typical to design the converter such that the converter operates in CCM to maximize efficiency.

In this section, a design procedure is presented using Figure 1 as a reference. An offline SMPS with 20W/5V nominal output power has been selected as a design example.

### [STEP-1] Define the System Specifications

When designing a power supply with peak load current profile, the following specifications should be determined:

- ■`Line voltage range ($V_{LINE}^{MIN}$ and $V_{LINE}^{MAX}$)
- ■`Line frequency ($f_L$)
- ■`Nominal output power ($P_O$)
- ■`Estimated efficiencies for nominal load ($\eta$): The power conversion efficiency must be estimated to calculate the input powers for nominal load condition. If no reference data is available, set $\eta$ = 0.7~0.75 for low-voltage output applications and $\eta$ = 0.8~0.85 for high-voltage output applications.

With the estimated efficiency, the input power for peak load condition is given by:

$$P_{IN} = \frac{P_O}{\eta} \quad (1)$$

**(Design Example)** The specifications of the target system are:

- $V_{LINE}^{MIN}$ =90$V_{AC}$ and $V_{LINE}^{MAX}$ =264VAC
- Line frequency $f_L$ = 60Hz (90$V_{AC}$) and 50Hz (264$V_{AC}$)
- Nominal output power $P_O$ = 20W (5V/4A)
- Estimated efficiency: $\eta$ = 0.77

$$P_{IN} = \frac{P_O}{\eta} = \frac{20}{0.77} = 26W$$

### [STEP-2] Determine the Input Capacitor ($C_{IN}$) and the Input Voltage Range

It is typical to select the input capacitor as 2~3μF per watt of peak input power for universal input range (85-265$V_{AC}$) and 1μF per watt of peak input power for European input range (195V-265$V_{AC}$). With the input capacitor chosen, the minimum input capacitor voltage at nominal load condition is obtained as:

$$V_{IN}^{MIN} = \sqrt{2 \cdot (V_{LINE}^{MIN})^2 - \frac{P_{IN} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}} \quad (2)$$

where $D_{CH}$ is the input capacitor charging duty ratio defined as shown in Figure 2, which is typically about 0.2.

The maximum input capacitor voltage is given as:

$$V_{IN}^{MAX} = \sqrt{2} V_{LINE}^{MAX} \quad (3)$$

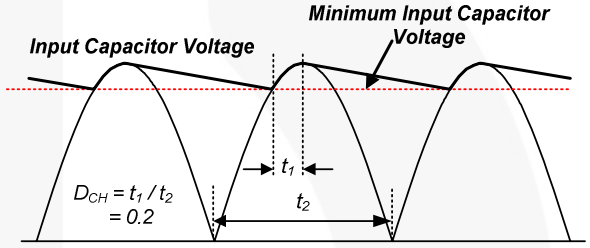


**Figure 2. Input Capacitor Voltage Waveform**

**(Design Example)** By choosing 100μF capacitor for input capacitor, the minimum input voltages for nominal load is obtained as:

$$V_{IN}^{MIN} = \sqrt{2 \cdot (V_{LINE}^{MIN})^2 - \frac{P_{IN} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{26 \cdot (1 - 0.2)}{100 \times 10^{-6} \cdot 60}} = 113V$$

The maximum input voltage is obtained as:

$$V_{IN}^{MAX} = \sqrt{2} \cdot V_{LINE}^{MAX} = \sqrt{2} \cdot 264 = 373V$$

### [STEP-3] Determine the Reflected Output Voltage ($V_{RO}$)

When the MOSFET is turned off, the input voltage ($V_{IN}$), together with the output voltage reflected to the primary ($V_{RO}$), are imposed across the MOSFET, as shown in 0. With a given $V_{RO}$, the maximum duty cycle ($D_{MAX}$), and the maximum nominal MOSFET voltage ($V_{DS}^{NOM}$) are obtained as:

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{IN}^{MIN}} \quad (4)$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} \quad (5)$$

$$V_{DO}^{NOM} = \frac{V_{IN}^{MAX} \cdot (V_O + V_F)}{V_{RO}} + V_O \quad (6)$$

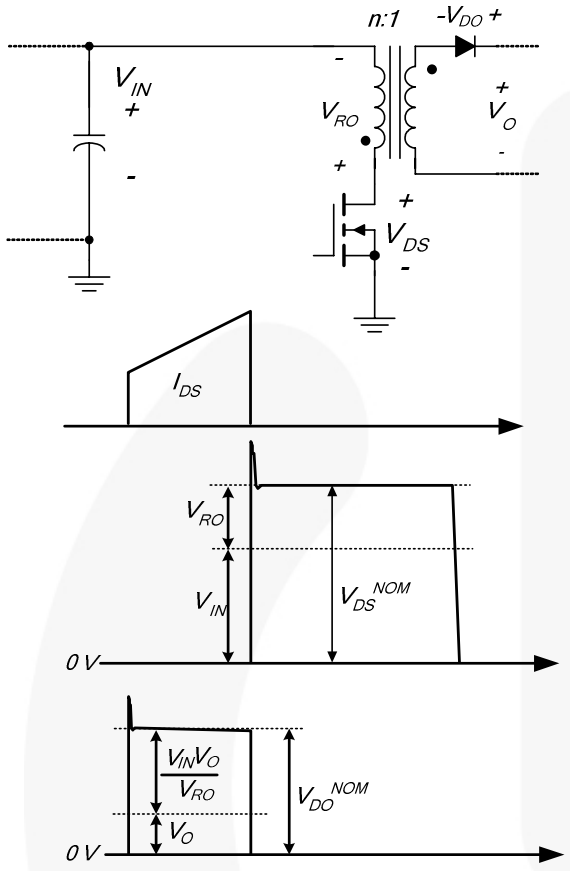


**Figure 3. Output Voltage Reflected to the Primary**

As can be seen in Equation (5), the voltage stress across MOSFET can be reduced by reducing $V_{RO}$. This, however, increases the voltage stresses on the rectifier diodes in the secondary side, as shown in Equation (6). Therefore, $V_{RO}$ should be determined by a trade-off between the voltage stresses of MOSFET and diode. Especially for low output voltage application, the rectifier diode forward-voltage drop is a dominant factor determining the power supply efficiency. Therefore, the reflected output voltage should be determined such that rectifier diode forward voltage can be minimized. Table 1 shows the forward-voltage drops for Schottky diodes with different voltage ratings.

Because the actual drain voltage and diode voltage rise above the nominal voltage due to the leakage inductance of the transformer, as shown in 0, it is typical to set $V_{RO}$ such that $V_{DS}^{NOM}$ and $V_{DO}^{NOM}$ are 60~70% of voltage ratings of MOSFET and diode, respectively.

**Table 1. Diode Forward-Voltage Drop for Different Voltage Ratings (3A Schottky Diode)**

| Part Name | $V_{RRM}$ | $V_F$ |
|---|---|---|
| SB320 | 20V | 0.5V |
| SB330 | 30V | |
| SB340 | 40V | |
| SB350 | 50V | 0.74V |
| SB360 | 60V | |
| SB380 | 80V | 0.85V |
| SB3100 | 100V | |

**(Design Example)** As can be seen in Table 1, it is necessary to use a rectifier diode with 40V voltage rating to maximize efficiency. Assuming that the nominal voltages of MOSFET and diode are less than 68% of their voltage rating, the reflected output voltage is given as:

$$V_{DO}^{NOM} = \frac{V_{IN}^{MAX} \cdot (V_O + V_F)}{V_{RO}} + V_O$$

$$= \frac{373 \cdot (5 + 0.5)}{V_{RO}} + 5 < 0.68 \cdot 40 = 27.2$$

$$\Rightarrow V_{RO} > \frac{373 \cdot (5 + 0.5)}{22.2} = 92.4V$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} < 0.68 \cdot 700 = 476$$

$$\Rightarrow V_{RO} < 476 - 373 < 103V$$

By determining $V_{RO}$ as 100V,

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{IN}^{MIN}} = \frac{100}{100 + 113} = 0.47$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} = 373 + 100 = 473V$$

$$V_{DO}^{NOM} = \frac{V_{IN}^{MAX} \cdot (V_O + V_F)}{V_{RO}} + V_O$$

$$= \frac{373 \cdot (5 + 0.5)}{100} + 5 = 25.5V$$

**[STEP-4] Determine the Transformer Primary-Side Inductance ($L_M$)**

The transformer primary-side inductance is determined for the minimum input voltage and nominal load condition. With the $D_{MAX}$ from step 3, the primary-side inductance ($L_M$) of the transformer is obtained as:

$$L_M = \frac{(V_{IN}^{MIN} \cdot D_{MAX})^2}{2P_{IN} f_{SW} K_{RF}} \quad (7)$$

where $f_{SW}$ is the switching frequency and $K_{RF}$ is the ripple factor at minimum input voltage and nominal load condition, defined as shown in Figure 4. The ripple factor is closely related with the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced by reducing the ripple factor, too small a ripple factor forces an increase in

transformer size. From a practical point of view, it is reasonable to set $K_{RF}$ = 0.3~0.6 for the universal input range and $K_{RF}$ = 0.4~0.8 for the European input range.

Once $L_M$ is calculated by determining $K_{RF}$ from Equation (7), the peak current and RMS current of the MOSFET for minimum input voltage and nominal load condition are obtained as:

$$I_{DS}^{PK} = I_{EDC} + \frac{\Delta I}{2} \quad (8)$$

$$I_{DS}^{RMS} = \sqrt{\left[3(I_{EDC})^2 + (\frac{\Delta I}{2})^2\right]\frac{D_{MAX}}{3}} \quad (9)$$

where $$I_{EDC} = \frac{P_{IN}}{V_{IN}^{MIN} \cdot D_{MAX}} \quad (10)$$

and $$\Delta I = \frac{V_{IN}^{MIN} D_{MAX}}{L_M f_{SW}} \quad (11)$$

$$K_{RF} = \frac{\Delta I}{2I_{EDC}}$$

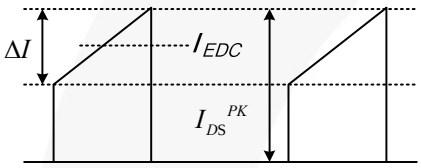


**Figure 4. MOSFET Current and Ripple Factor ($K_{RF}$)**

**(Design Example)** Determining the ripple factor as 0.6:

$$L_M = \frac{(V_{IN}^{MIN} \cdot D_{MAX})^2}{2P_{IN} f_{SW} K_{RF}} = \frac{(113 \cdot 0.47)^2}{2 \cdot 26 \cdot 100 \times 10^3 \cdot 0.6}$$

$$= 900\mu H$$

$$I_{EDC} = \frac{P_{IN}}{V_{IN}^{MIN} \cdot D_{MAX}} = \frac{26}{113 \cdot 0.47} = 0.49A$$

$$\Delta I = \frac{V_{IN}^{MIN} D_{MAX}}{L_M f_{SW}} = \frac{113 \cdot 0.47}{900 \times 10^{-6} \cdot 100 \times 10^3} = 0.59A$$

$$I_{DS}^{PK} = I_{EDC} + \frac{\Delta I}{2} = 0.49 + 0.295 = 0.78A$$

$$I_{DS}^{RMS} = \sqrt{\left[3(I_{EDC})^2 + (\frac{\Delta I}{2})^2\right]\frac{D_{MAX}}{3}}$$

$$= \sqrt{\left[3(0.49)^2 + (0.295)^2\right]\frac{0.47}{3}} = 0.36A$$

**[STEP-5] Choose the Proper FPS, Considering Input Power and Peak Drain Current**

With the resulting maximum peak drain current of the MOSFET ($I_{DS}^{PK}$) from Equation (8), choose the proper FPS for which the pulse-by-pulse current limit level ($I_{LIM}$) is higher than $I_{DS}^{PK}$. Since FPS has ±10% tolerance of $I_{LIM}$, there should be some margin when choosing the proper FPS device. The FSBH-series lineup with power ratings is summarized in Table 2.

**Table 2. Lineup of FSBH-Series with Power Ratings**

| Product | $I_{LIM}$ | Maximum Output Power for Universal Input Range and Open Frame |
|---|---|---|
| FSBH0F70 | 0.73A | 8W |
| FSBH0170 | 0.80A | 13W |
| FSBH0270 | 1.00A | 16W |
| FSBH0370 | 1.20A | 19W |

**(Design Example)** FSBH0370 is selected.

**[STEP-6] Determine the Minimum Primary Turns**

With a given core, the minimum number of turns for the transformer primary side to avoid core saturation is given by:

$$N_P^{\min} = \frac{L_M I_{LIM}}{B_{SAT} A_e} \times 10^6 \quad (12)$$

where $A_e$ is the cross-sectional area of the core in mm$^2$, $I_{LIM}$ is the pulse-by-pulse current limit level, and $B_{SAT}$ is the saturation flux density in Tesla.

The pulse-by-pulse current limit level is included in Equation (12) because the inductor current reaches the pulse-by-pulse current limit level during the load transient or overload condition. **Error! Reference source not found.** shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density ($B_{SAT}$) decreases as the temperature increases, the high temperature characteristics should be considered. If there is no reference data, use $B_{MAX}$ =0.3 T.

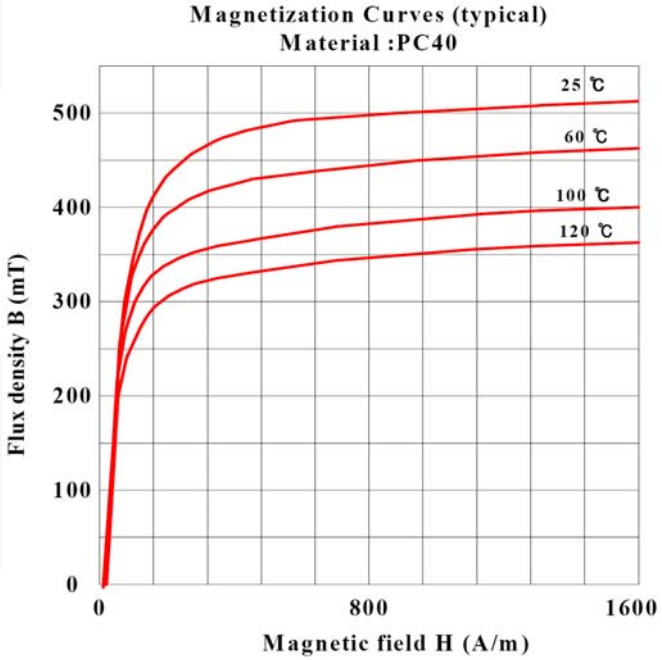


**Figure 5. Typical B-H Characteristics of Ferrite Core (TDK/PC40)**

**(Design Example)** EEL-19 core is selected, whose effective cross-sectional area is 25mm$^2$. Choosing the saturation flux density as 0.3 T, the minimum number of turns for the primary side is obtained as:

$$N_P{}^{\min} = \frac{L_M \cdot I_{LIM}}{B_{SAT} A_e} \times 10^6$$

$$= \frac{900 \times 10^{-6} \cdot 1.2}{0.3 \cdot 25} \times 10^6 = 144$$

**[STEP-7] Determine the Number of Turns for Each Winding**

Figure 6 shows the simplified diagram of the transformer. First, calculate the turn ratio (n) between the primary side and the secondary side from the reflected output voltage, determined in step 3, as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} \quad (13)$$

where $N_P$ and $N_S$ are the number of turns for primary side and secondary side, respectively; $V_O$ is the output voltage; and $V_F$ is the diode ($D_O$) forward-voltage drop. Then, determine the proper integer for $N_S$, such that the resulting $N_P$ is larger than $N_P{}^{min}$ obtained from Equation (12).

The number of turns for the auxiliary winding for $V_{DD}$ supply is determined as:

$$N_A = \frac{V_{DD}{}^* + V_{FA}}{V_O + V_F} \cdot N_{S1} \quad (14)$$

where $V_{DD}{}^*$ is the nominal value of the supply voltage and $V_{FA}$ is the forward-voltage drop of $D_{DD}$ as defined in Figure 6. Since $V_{DD}$ increases as the output load increases, it is proper to set $V_{DD}$ at 3~5V higher than $V_{DD}$ UVLO level (8V) to avoid the over-voltage protection condition during the peak load operation.

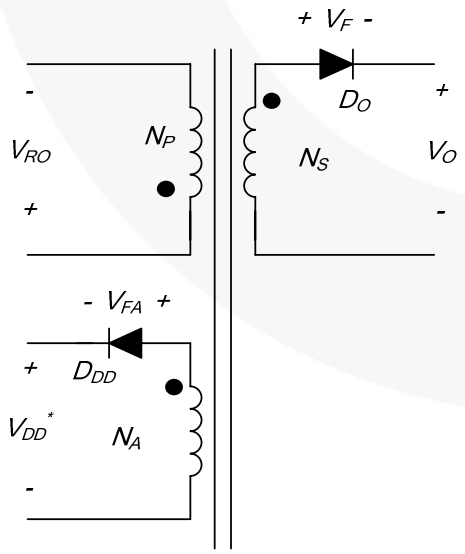


**Figure 6. Simplified Transformer Diagram**

**(Design Example)** Assuming the diode forward-voltage drop is 0.5V, the turn ratio is obtained as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} = \frac{100}{5 + 0.5} = 18.18$$

Then, determine the proper integer for $N_S$, such that the resulting $N_P$ is larger than $N_P{}^{min}$ as:

$N_S = 8$, $N_P = n \cdot N_S = 146 > N_P{}^{\min}$

Setting $V_{DD}{}^*$ as 15V, the number of turns for the auxiliary winding is obtained as:

$$N_A = \frac{V_{DD}{}^* + V_{FA}}{V_O + V_F} \cdot N_S = \frac{15 + 1.2}{5 + 0.5} \cdot 8 = 24$$

**[STEP-8] Determine the Wire Diameter for Each Winding Based on the RMS Current of Winding**

The maximum RMS current of the secondary winding is obtained as:

$$I_{SEC}{}^{RMS} = n \cdot I_{DS}{}^{RMS} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}} \quad (15)$$

The current density is typically 3~5A/mm$^2$ when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 5~10A/mm$^2$ is also acceptable. Avoid using wire with a diameter larger than 1mm to avoid severe eddy current losses as well as to make winding easier. For high-current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect.

**(Design Example)** The RMS current of primary-side winding is obtained from step 4 as 0.36A. The RMS current of secondary-side winding is calculated as:

$$I_{SEC}{}^{RMS} = n \cdot I_{DS}{}^{RMS} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}}$$

$$= 18.18 \cdot 0.36 \sqrt{\frac{1 - 0.47}{0.47}} = 6.9A$$

0.3mm (5A/mm$^2$) and 0.65mm×2 (10A/mm$^2$) diameter wires are selected for primary and secondary windings, respectively.

**[STEP-9] Choose the Rectifier Diode in the Secondary Side Based on the Voltage and Current Ratings**

The maximum reverse voltage and the RMS current of the rectifier diode are obtained as:

$$V_{DO} = V_O + \frac{V_{IN}{}^{MAX}}{n} \quad (16)$$

$$I_{DO}{}^{RMS} = n \cdot I_{DS}{}^{RMS} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}} \quad (17)$$

The typical voltage and current margins for the rectifier diode are:

$$V_{RRM} > 1.3 \cdot V_{DO} \quad (18)$$

$$I_F > 1.5 \cdot I_{DO}^{RMS} \quad (19)$$

where $V_{RRM}$ is the maximum reverse voltage and $I_F$ is the current rating of the diode.

**(Design Example)** The diode voltage and current are calculated as:

$$V_{DO} = V_O + \frac{V_{IN}^{MAX}}{n} = 5 + \frac{373}{18.18} = 25.5V$$

$$I_{DO}^{RMS} = n \cdot I_{DS}^{RMS} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}}$$

$$= 18.18 \cdot 0.36 \sqrt{\frac{1 - 0.47}{0.47}} = 6.9A$$

Two 5A and 40V diodes in parallel are selected for the rectifier diode.

### [STEP-10] Feedback Circuit Configuration

Since FSBH-series employs current-mode control, the feedback loop can be implemented with a one-pole and one-zero compensation circuit.

The current control factor of FPS, $K$ is defined as:

$$K = \frac{I_{LIM}}{V_{FB}^{SAT}} = \frac{I_{LIM}}{3.2} \quad (20)$$

where $I_{LIM}$ is the pulse-by-pulse current limit and $V_{FB}^{SAT}$ is the feedback saturation voltage. which is typically 3.2V.

As described in step 4, it is typical to design the flyback converter to operate in CCM for heavy load condition. For CCM operation, the control-to-output transfer function of a flyback converter using current mode control is given by:

$$G_{vc} = \frac{\hat{v}_o}{\hat{v}_{FB}} = \frac{K \cdot R_L \cdot V_{IN} (N_P / N_S)}{2V_{RO} + V_{IN}} \cdot \frac{(1 + s/\omega_Z)(1 - s/\omega_{RZ})}{(1 + s/\omega_P)} \quad (21)$$

where $R_L$ is the load resistance and the pole and zeros of Equation (21) are obtained as:

$$\omega_Z = \frac{1}{R_C C_O}, \quad \omega_{RZ} = \frac{R_L (1 - D)^2}{D L_M (N_S / N_P)^2} \quad and \quad \omega_P = \frac{(1 + D)}{R_L C_O}$$

where $D$ is the duty cycle of the FPS and $R_C$ is the ESR of $C_O$.

Notice that there is a right half plane (RHP) zero ($\omega_{RZ}$) in the control-to-output transfer function of Equation (21). Because the RHP zero reduces the phase by 90 degrees, the crossover frequency should be placed below the RHP zero.

Figure 7 shows the variation of a CCM flyback converter control-to-output transfer function for different input voltages. This figure shows the system poles and zeros together with the DC gain change for different input voltages. The gain is highest at the high input voltage condition and the RHP zero is lowest at the low input voltage condition.

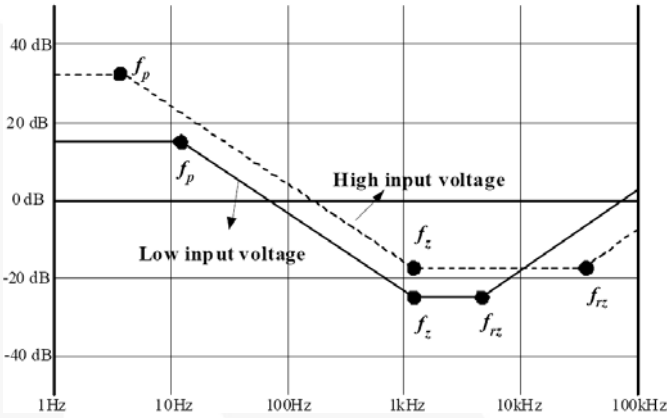


**Figure 7. CCM Flyback Converter Control-to Output Transfer Function Variation for Different Input Voltages**

Figure 8 shows the variation of a CCM flyback converter control-to-output transfer function for different loads. This figure shows that the low frequency gain does not change for different loads and the RHP zero is lowest at the full load condition.

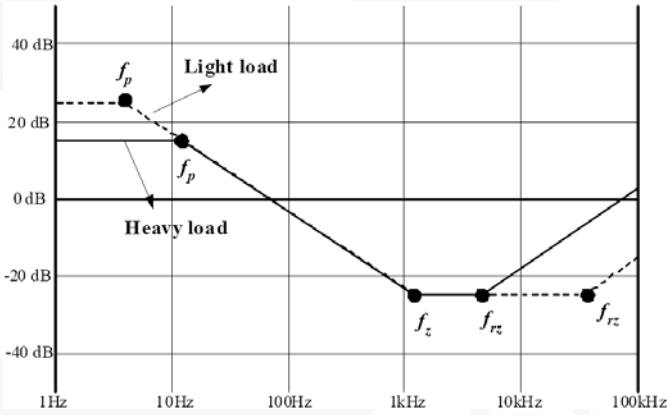


**Figure 8. CCM Flyback Converter Control-to Output Transfer Function Variation for Different Loads**

When the input voltage and the load current vary over a wide range, it is not easy to determine the worst case for the feedback loop design. The gain, together with zeros and poles, vary according to the operating conditions. Moreover, even though the converter is designed to operate in CCM or at the boundary of DCM and CCM in the minimum input voltage and full load condition, the converter enters into DCM,

changing the system transfer functions as the load current decreases and/or input voltage increases.

One simple and practical way to address this problem is designing the feedback loop for low input voltage and full load condition with enough phase and gain margin. When the converter operates in CCM, the RHP zero is lowest in low input voltage and full load condition. The gain increases only about 6dB as the operating condition is changed from the lowest input voltage to the highest input voltage condition under universal input condition. When the operating mode changes from CCM to DCM, the RHP zero disappears, making the system stable. Therefore, by designing the feedback loop with more than 45 degrees phase margin in low input voltage and full load condition, the stability over all the operating ranges can be guaranteed.

Figure 9 is a typical feedback circuit mainly consisting of a shunt regulator and a photo-coupler. $R_1$ and $R_2$ form a voltage divider for output voltage regulation. $R_F$ and $C_F$ are adjusted for control-loop compensation. The maximum source current of the FB pin is about 1mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of $R_D$, is determined as:

$$\frac{V_O - V_{OPD} - V_{KA}}{R_D} \cdot CTR > I_{FB} \quad (22)$$

where $V_{OPD}$ is the drop voltage of the photodiode, about 1.2V; $V_{KA}$ is the minimum cathode to anode voltage of KA431 (2.5V); and CTR is the current transfer rate of the opto-coupler.

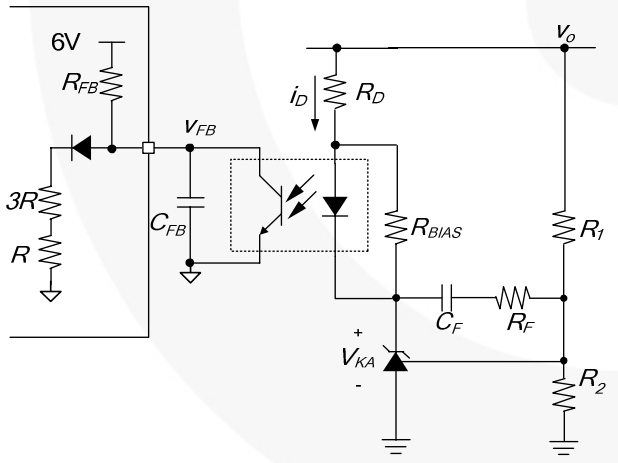


**Figure 9. Feedback Circuit**

The feedback compensation network transfer function of Figure 9 is obtained as:

$$\frac{\hat{v}_{FB}}{\hat{v}_o} = -\frac{\omega_I}{s} \cdot \frac{1 + s/\omega_{ZC}}{1 + s/\omega_{PC}} \quad (23)$$

where $\omega_I = \frac{R_{FB}}{R_1 R_D C_F}$, $\omega_{ZC} = \frac{1}{(R_F + R_1)C_F}$, and $\omega_{PC} = \frac{1}{R_{FB} C_{FB}}$.

and $R_{FB}$ is the equivalent feedback bias resistor of FSBH-series (5kΩ); and $R_1$, $R_D$, $R_F$, $C_F$ and $C_{FB}$ are shown in Figure 10.

**(Design Example)** Assuming CTR is 100%,

$$\frac{V_O - V_{OPD} - V_{KA}}{R_D} \cdot CTR > 1 \times 10^{-3}$$

$$R_D < \frac{V_O - V_{OPD} - V_{KA}}{1 \times 10^{-3}} = \frac{5 - 1.2 - 2.5}{1 \times 10^{-3}} = 1.3k\Omega$$

The minimum cathode current for KA431 is 1mA.

$$R_{BIAS} < \frac{V_{OPD}}{1 \times 10^{-3}} = 1.2k\Omega$$

1kΩ resistor is selected for $R_{BIAS}$.

The voltage divider resistors $R_1$ and $R_2$ for $V_O$ sensing are selected as 20kΩ and 20kΩ.

**[STEP-11] Design Input Voltage Sensing Circuit**

Figure 10 shows a resistive voltage divider with low-pass filter for line-voltage detection of the VIN pin. The $V_{IN}$ voltage is used for brownout protection, which triggers when the $V_{IN}$ voltage drops below 0.6V. A 500ms debounce time is introduced for brownout protection to prevent false triggering by the voltage ripple on the input capacitor. FSBH-series devices start up when the $V_{IN}$ voltage reaches 1.1V. It is typical to use 100:1 voltage divider for $V_{IN}$ level.

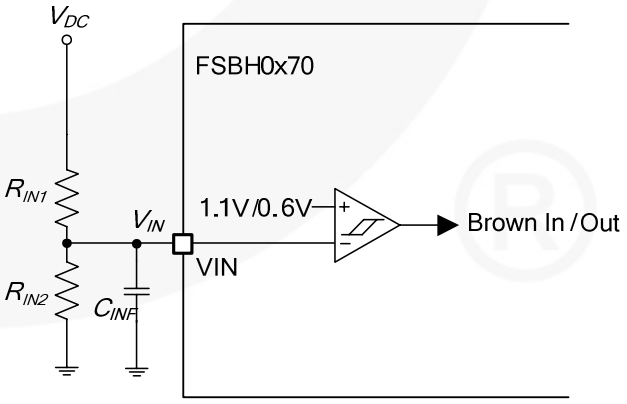


**Figure 10.Input Voltage Sensing**

## Design Summary

Figure 11 shows the final schematic of the 20W power supply of the design example.

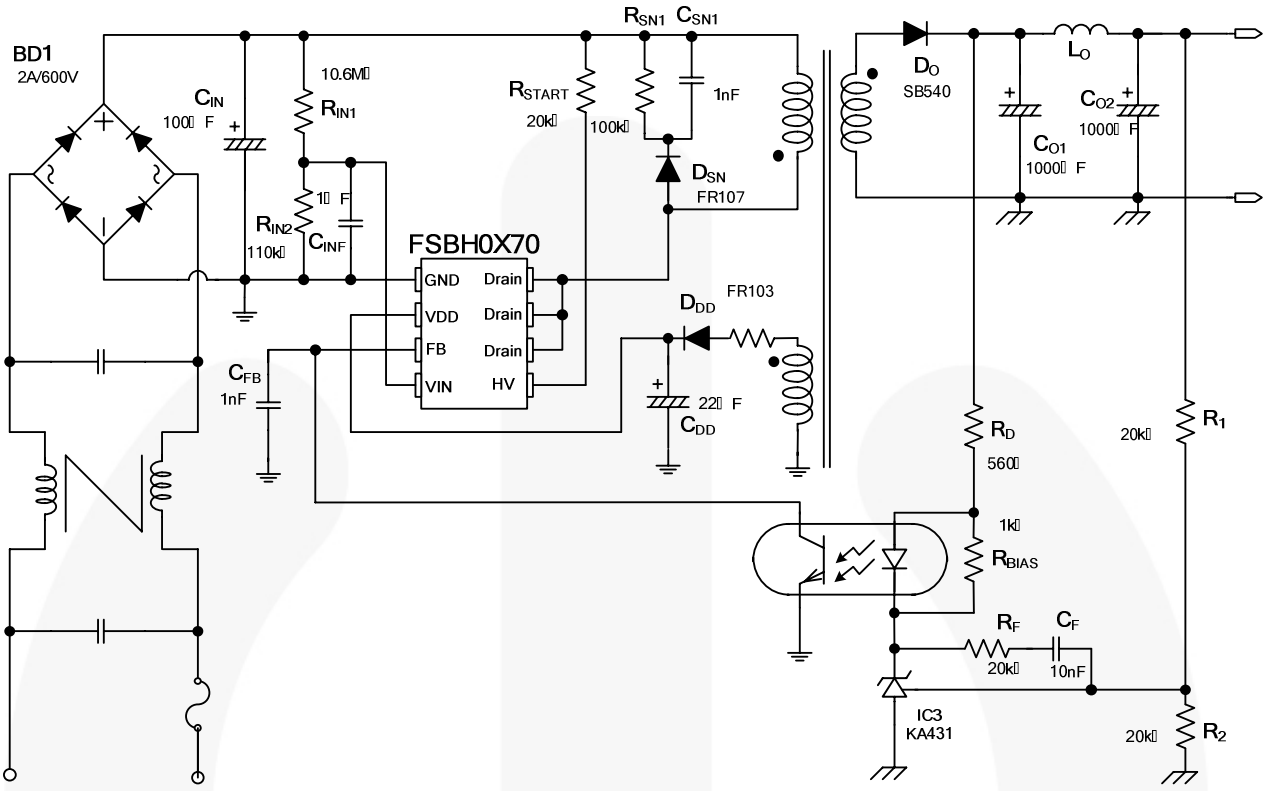


**Figure 11. Final Schematic of Design Example**

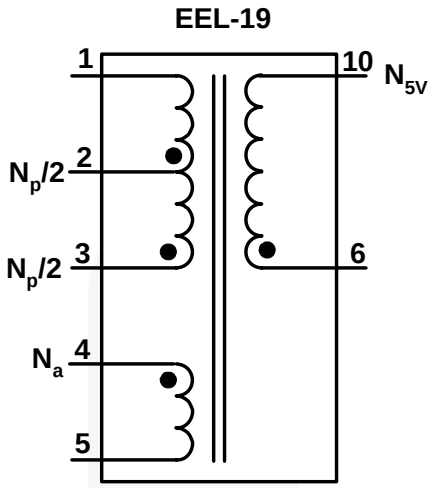


**Figure 12.Transformer Specification**

Core: EEL-19 (Ae=25mm$^2$)
Bobbin: EEL-19

| | Pin (S → F) | Wire | Turns | Winding Method |
|---|---|---|---|---|
| $N_a$ | 4 → 5 | 0.3φ×1 | 24 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 1 Layer | | | | |
| $N_p/2$ | 3 → 2 | 0.3φ×1 | 73 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | |
| $N_{5V}$ | 6 → 10 | 0.65φ×3 | 8 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | |
| $N_p/2$ | 2 → 1 | 0.3φ×1 | 73 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 2 Layers | | | | |

| | Pin | Specifications | Remark |
|---|---|---|---|
| Inductance | 1−3 | 900μH ± 10% | 100 kHz, 1 V |
| Leakage | 1−3 | < 30 μH Max. | Short All Other Pins |

## Related Datasheets

*FSBH0F70A, FSBH0170/A, FSBH0270/A, FSBH0370 — Green Mode Fairchild Power Switch (FPS™)*