



ADVANCED TRANSITION-MODE PFC CONTROLLER

PRELIMINARY DATA

1 MAIN FEATURES

- TRANSITION-MODE CONTROL OF PFC PRE-REGULATORS
- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- TRACKING BOOST FUNCTION
- PROTECTION AGAINST FEEDBACK LOOP FAILURE (LATCHED SHUTDOWN)
- INTERFACE FOR CASCADED CONVERTER'S PWM CONTROLLER
- INPUT VOLTAGE FEEDFORWARD ($1/V^2$)
- REMOTE ON/OFF CONTROL
- LOW ($\leq 90\mu\text{A}$) START-UP CURRENT
- 5 mA MAX. QUIESCENT CURRENT
- 1.5% (@ $T_j = 25^\circ\text{C}$) INTERNAL REFERENCE VOLTAGE
- -600/+800 mA TOTEM POLE GATE DRIVER WITH ACTIVE PULL-DOWN DURING UVLO
- SO14 PACKAGE

1.1 APPLICATIONS

PFC PRE-REGULATORS FOR:

- HI-END AC-DC ADAPTER/CHARGER

Figure 1. Package

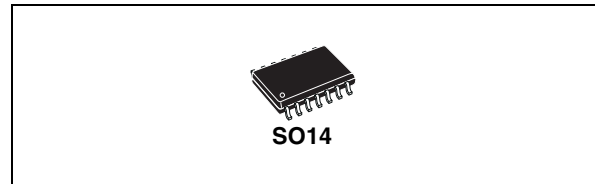


Table 1. Order Codes

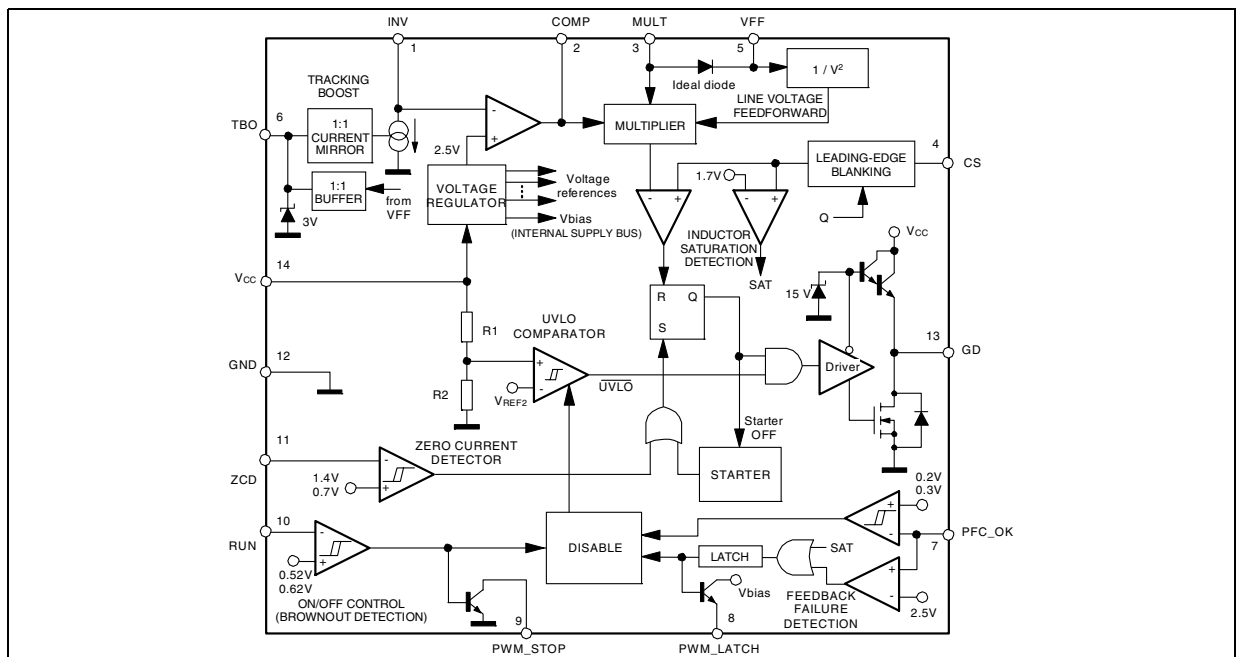
Part Number	Package
L6563	SO14
L6563TR	SO14 in Tape & Reel

- DESKTOP PC, SERVER, WEB SERVER
- IEC61000-3-2 OR JEIDA-MITI COMPLIANT SMPS, IN EXCESS OF 250W

2 DESCRIPTION

The device is a current-mode PFC controller operating in Transition Mode (TM). Based on the core of a standard TM PFC controller, it offers improved performance and additional functions.

Figure 2. Block Diagram



2 DESCRIPTION (continued)

The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide-range-mains operation with an extremely low THD even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and a precise (1.5% @ $T_j = 25^\circ\text{C}$) internal voltage reference. The stability of the loop and the transient response to sudden mains voltage changes are improved by the voltage feedforward function ($1/V^2$ correction).

Additionally, the IC provides the option for tracking boost operation (where the output voltage is changed tracking the mains voltage). The device features extremely low consumption ($\leq 90 \mu\text{A}$ before start-up and $\leq 5 \text{ mA}$ running).

An interface with the PWM controller of the DC-DC converter supplied by the PFC pre-regulator is provided: the purpose is to stop the operation of the converter in case of anomalous conditions for the PFC stage (feedback loop failure, boost inductor's core saturation) and to disable the PFC stage in case of light load for the DC-DC converter, so as to make it easier to comply with energy saving norms (Blue Angel, EnergyStar, Energy2000, etc.). The device includes disable functions suitable for remote ON/OFF control both in systems where the PFC pre-regulator works as a master and in those where it works as a slave.

In addition to an effective two-step OVP that handles normal operation overvoltages, the IC provides also a protection against feedback loop failures or erroneous output voltage setting.

Table 2. Absolute Maximum Ratings

Symbol	Pin	Parameter	Value	Unit
Vcc	14	IC Supply voltage ($I_{cc} = 20 \text{ mA}$)	self-limited	V
---	2, 4 to 6, 8 to 10	Analog Inputs & Outputs	-0.3 to 8	V
---	1, 3, 7	Max. pin voltage ($I_{pin} = 1 \text{ mA}$)	Self-limited	V
IPWM_STOP	10	Max. sink current	3	mA
I _{ZCD}	11	Zero Current Detector Max. Current	-10 (source) 10 (sink)	mA
P _{tot}		Power Dissipation @ $T_{amb} = 50^\circ\text{C}$	0.75	W
T _j		Junction Temperature Operating range	-25 to 150	$^\circ\text{C}$
T _{stg}		Storage Temperature	-55 to 150	$^\circ\text{C}$

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
R _{th j-amb}	Thermal Resistance, Junction-to-ambient Max.	120	$^\circ\text{C}/\text{W}$

Figure 3. Pin Connection (Top view)

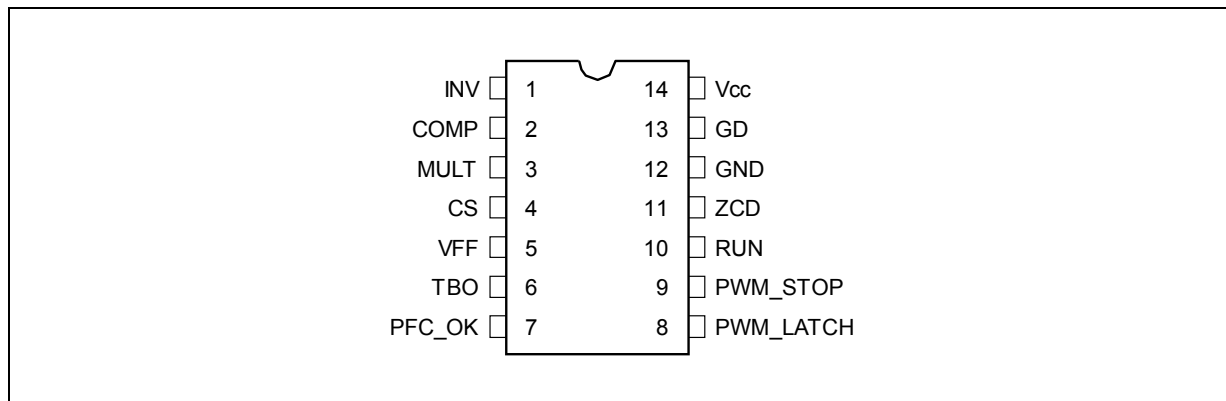


Table 4. Pin Description

Pin #	Pin Name	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin normally features high impedance but, if the tracking boost function is used, an internal current generator programmed by TBO (pin #6) is activated. It sinks current from the pin to change the output voltage so that it tracks the mains voltage.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin #1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop. The voltage on this pin is used also to derive the information on the RMS mains voltage.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. A second comparison level at 1.7V detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, shuts down the IC, reduces its consumption almost to the start-up level and asserts PWM_LATCH (pin #8) high.
5	VFF	Second input to the multiplier for $1/V^2$ function. A capacitor and a parallel resistor must be connected from the pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a DC level equal to the peak voltage at pin MULT (#3), compensates the control loop gain dependence on the mains voltage. Never connect the pin directly to GND.
6	TBO	Tracking Boost function. This pin provides a buffered VFF voltage. A resistor connected between this pin and GND defines a current that is sunk from pin INV (#1). In this way, the output voltage is changed proportionally to the mains voltage (tracking boost). If this function is not used leave this pin open.
7	PFC_OK	PFC pre-regulator output voltage monitoring/disable function. This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage at the pin exceeds 2.5V the IC is shut down, its consumption goes almost to the start-up level and this condition is latched. PWM_LATCH pin is asserted high. Normal operation can be resumed only by cycling the Vcc. This function is used for protection in case the feedback loop fails. If the voltage on this pin is brought below 0.2V the IC is shut down and its consumption is considerably reduced. To restart the IC the voltage on the pin must go above 0.26V. If these functions are not needed, tie the pin to a voltage between 0.26 and 2.5 V.
8	PWM_LATCH	Output pin for fault signaling. During normal operation this pin features high impedance. If either a voltage above 2.5V at PFC_OK (pin #7) or a voltage above 1.7V on CS (pin #4) is detected the pin is asserted high. Normally, this pin is used to stop the operation of the DC-DC converter supplied by the PFC pre-regulator by invoking a latched disable of its PWM controller. If not used, the pin will be left floating.
9	PWM_STOP	Output pin for fault signaling. During normal operation this pin features high impedance. If the IC is disabled by a voltage below 0.5V on RUN (pin #10) the voltage at the pin is pulled to ground. Normally, this pin is used to temporarily stop the operation of the DC-DC converter supplied by the PFC pre-regulator by disabling its PWM controller. If not used, the pin will be left floating.
10	RUN	Remote ON/OFF control. A voltage below 0.52V shuts down (not latched) the IC and brings its consumption to a considerably lower level. PWM_STOP is asserted low. The IC restarts as the voltage at the pin goes above 0.6V. Connect this pin to VFF (pin #5) either directly or through a resistor divider to use this function as brownout (AC mains undervoltage) protection, tie to INV (pin #1) if the function is not used.
11	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
12	GND	Ground. Current return for both the signal part of the IC and the gate driver.
13	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages.
14	Vcc	Supply Voltage of both the signal part of the IC and the gate driver.

Figure 4. Typical System Block Diagram

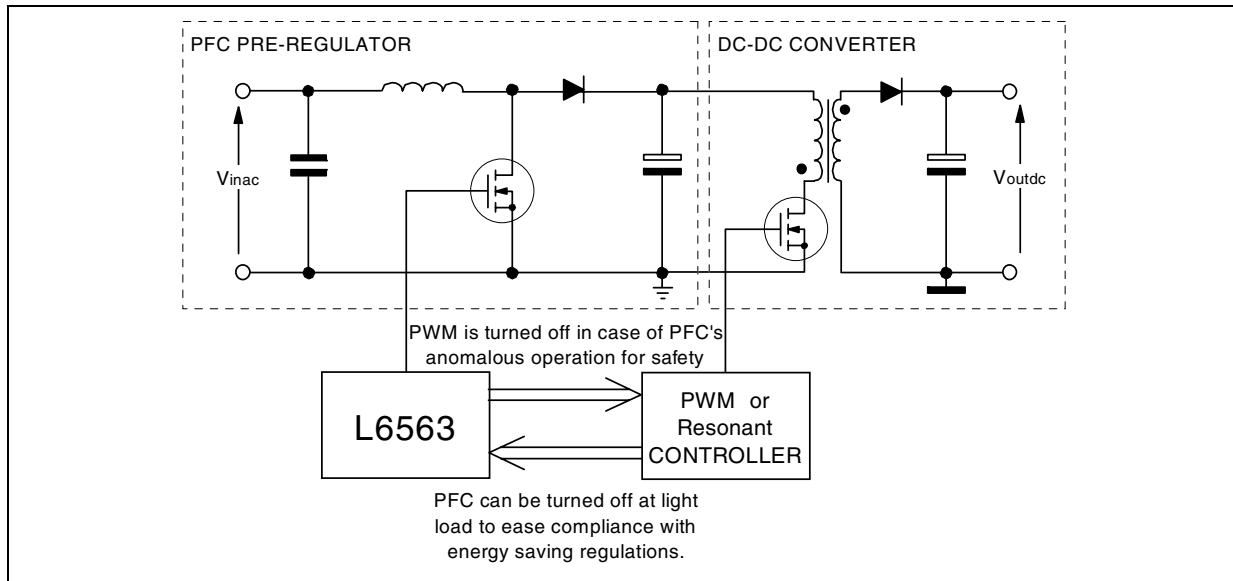


Table 5. Electrical Characteristics

($T_j = -25$ to 125°C , $V_{CC} = 12$, $C_o = 1$ nF between pin GD and GND, $C_{FF} = 1\mu\text{F}$ between pin V_{FF} and GND; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V_{CC}	Operating range	After turn-on	10.3		22	V
V_{CCOn}	Turn-on threshold	(1)	11	12	13	V
V_{CCOff}	Turn-off threshold	(1)	8.7	9.5	10.3	V
Hys	Hysteresis		2.3		2.7	V
V_Z	Zener Voltage	$I_{CC} = 20$ mA	22	25	28	V
SUPPLY CURRENT						
$I_{start-up}$	Start-up Current	Before turn-on, $V_{CC} = 10V$		50	90	μA
I_q	Quiescent Current	After turn-on		3	5	mA
I_{CC}	Operating Supply Current	@ 70 kHz		3.8	5.5	mA
I_{qdis}	Idle state quiescent Current	Latched by $PFC_OK > V_{th1}$ or $V_{CS} > V_{CSdis}$		180	250	μA
		Disabled by $PFC_OK < V_{th}$ or $RUN < V_{DIS}$		1.5	2.2	mA
I_q	Quiescent Current	During static/dynamic OVP		2	3	mA
MULTIPLIER INPUT						
I_{MULT}	Input Bias Current	$V_{MULT} = 0$ to 3 V		-0.2	-1	μA
V_{MULT}	Linear Operation Range		0 to 3			V
V_{CLAMP}	Internal clamp level	$I_{MULT} = 1$ mA	9	9.5		V
$\frac{\Delta V_{cs}}{\Delta V_{MULT}}$	Output Max. Slope	$V_{MULT} = 0$ to $0.5V$, $V_{FF} = 0.8V$ $V_{COMP} =$ Upper clamp	2.2	2.34		V/V
K_M	Gain (3)	$V_{MULT} = 1$ V, $V_{COMP} = 4$ V, $V_{VFF} = V_{MULT}$	0.375	0.45	0.525	1/V

Table 5. Electrical Characteristics (continued)

($T_j = -25$ to 125°C , $V_{CC} = 12$, $C_o = 1$ nF between pin GD and GND, $C_{FF} = 1\mu\text{F}$ between pin VFF and GND; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER						
V_{INV}	Voltage Feedback Input Threshold	$T_j = 25^\circ\text{C}$	2.465	2.5	2.535	V
		$10.3\text{ V} < V_{CC} < 22\text{ V}$ (2)	2.44		2.56	
	Line Regulation	$V_{CC} = 10.3\text{ V}$ to 22 V		2	5	mV
I_{INV}	Input Bias Current	TBO open, $V_{INV} = 0$ to 4 V		-0.2	-1	μA
$V_{INVCLAMP}$	Internal clamp level	$I_{INV} = 1\text{ mA}$	9	9.5		V
G_v	Voltage Gain	Open loop	60	80		dB
GB	Gain-Bandwidth Product			1		MHz
I_{COMP}	Source Current	$V_{COMP} = 4\text{ V}$, $V_{INV} = 2.4\text{ V}$	-2	-3.5	-5	mA
	Sink Current	$V_{COMP} = 4\text{ V}$, $V_{INV} = 2.6\text{ V}$	2.5	4.5		mA
V_{COMP}	Upper Clamp Voltage	$I_{SOURCE} = 0.5\text{ mA}$	5.7	6.2	6.7	V
	Lower Clamp Voltage	$I_{SINK} = 0.5\text{ mA}$ (2)	2.1	2.25	2.4	V
CURRENT SENSE COMPARATOR						
I_{CS}	Input Bias Current	$V_{CS} = 0$			-1	μA
t_{LEB}	Leading Edge Blanking		100	200	300	ns
$t_{d(H-L)}$	Delay to Output			120		ns
$V_{CSclamp}$	Current sense reference clamp	$V_{COMP} = \text{Upper clamp}$, $V_{VFF} = V_{MULT} = 0.5\text{ V}$	1.0	1.08	1.16	V
$V_{CSoffset}$	Current sense offset	$V_{MULT} = 0$, $V_{VFF} = 3\text{ V}$		25		mV
		$V_{MULT} = 3\text{ V}$, $V_{VFF} = 3\text{ V}$		5		
V_{CSdis}	IC disable level	(2)	1.6	1.7	1.8	V
OUTPUT OVERVOLTAGE						
I_{OVP}	Dynamic OVP triggering current		17	20	23	μA
Hys	Hysteresis	(4)		15		μA
	Static OVP threshold	(2)	2.1	2.25	2.4	V
VOLTAGE FEEDFORWARD						
V_{VFF}	Linear operation range	$R_{FF} = 47\text{ k}\Omega$ to GND	0.5		3	V
ΔV	Dropout $V_{MULTpk} - V_{VFF}$				10	mV
ZERO CURRENT DETECTOR						
V_{ZCDH}	Upper Clamp Voltage	$I_{ZCD} = 2.5\text{ mA}$	5.0	5.7		V
V_{ZCDL}	Lower Clamp Voltage	$I_{ZCD} = -2.5\text{ mA}$	-0.3	0	0.3	V
V_{ZCDA}	Arming Voltage (positive-going edge)	(4)		1.4		V
V_{ZCDT}	Triggering Voltage (negative-going edge)	(4)		0.7		V
I_{ZCdb}	Input Bias Current	$V_{ZCD} = 1$ to 4.5 V			1	μA
I_{ZCDsrc}	Source Current Capability		-2.5			mA
I_{ZCDsnk}	Sink Current Capability		2.5			mA
TRACKING BOOST FUNCTION						
ΔV	Dropout voltage $V_{VFF} - V_{TBO}$	$I_{TBO} = 0.25\text{ mA}$			10	mV
I_{TBO}	Linear operation		0		0.25	mA

Table 5. Electrical Characteristics (continued)

($T_j = -25$ to 125°C , $V_{CC} = 12$, $C_o = 1$ nF between pin GD and GND, $C_{FF} = 1\mu\text{F}$ between pin V_{FF} and GND; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	$I_{INV-I_{TBO}}$ current mismatch	$I_{TBO} = 25 \mu\text{A}$ to 0.25 mA	-3.5		3.5	%
$V_{TBOclamp}$	Clamp voltage	(2) $V_{VFF} = 4\text{V}$	2.9	3	3.1	V
PFC_OK						
V_{thl}	Latch-off threshold	(2) voltage rising	2.4	2.5	2.6	V
V_{th}	Disable threshold	(2) voltage falling		0.2		V
V_{EN}	Enable threshold	(2) voltage rising		0.26		V
I_{PFC_OK}	Input Bias Current	$V_{PFC_OK} = 0$ to 2.5V		-0.1	-1	μA
V_{clamp}	Clamp voltage	$I_{PFC_OK} = 1 \text{ mA}$	9	9.5		V
PWM_LATCH						
I_{leak}	Low level leakage current	$V_{PWM_LATCH} = 0$			-1	μA
V_H	High level	$I_{PWM_LATCH} = -0.5 \text{ mA}$	3.7			V
PWM_STOP						
I_{leak}	High level leakage current	$V_{PWM_STOP} = 6\text{V}$			1	μA
V_L	Low level	$I_{PWM_STOP} = 0.5 \text{ mA}$			1	V
V_{clamp}	Clamp voltage	$I_{PFC_OK} = 2 \text{ mA}$	9	9.5		V
RUN FUNCTION						
I_{RUN}	Input Bias Current	$V_{RUN} = 0$ to 3 V			-1	μA
V_{DIS}	Disable threshold	(2) voltage falling	0.5	0.52	0.54	V
V_{EN}	Enable threshold	(2) voltage rising	0.57	0.6	0.63	V
START TIMER						
t_{START}	Start Timer period		75	150	300	μs
GATE DRIVER						
V_{OHdrop}	Dropout Voltage	$I_{GDsource} = 20 \text{ mA}$		2	2.6	V
		$I_{GDsource} = 200 \text{ mA}$		2.5	3	V
V_{OLdrop}		$I_{GDsink} = 200 \text{ mA}$		1	2	V
t_f	Current Fall Time			30	70	ns
t_r	Current Rise Time			40	80	ns
V_{Oclamp}	Output clamp voltage	$I_{GDsource} = 5\text{mA}$; $V_{CC} = 20\text{V}$	10	12	15	V
	UVLO saturation	$V_{CC} = 0$ to V_{CCOn} , $I_{sink} = 10\text{mA}$			1.1	V

(1), (2) Parameters tracking each other

(3) The multiplier output is given by: $V_{CS} = K_M \cdot \frac{V_{MULT} \cdot (V_{COMP} - 2.5)}{V_{VFF}^2}$

(4) Parameters guaranteed by design, functionality tested in production.

3 TYPICAL ELECTRICAL PERFORMANCE

Figure 5. Supply current vs. Supply voltage

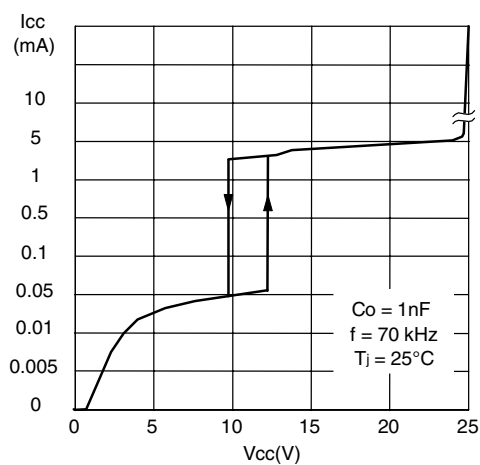


Figure 8. Vcc Zener voltage vs. Tj

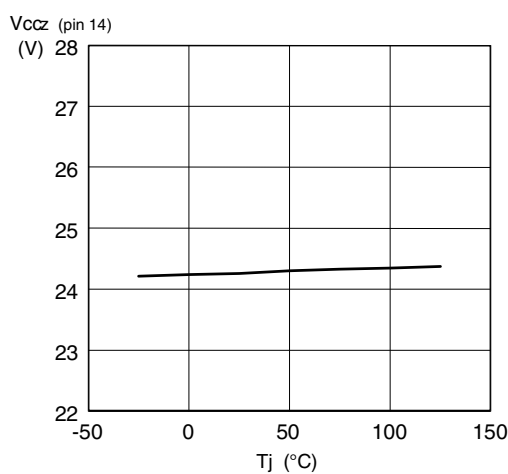


Figure 6. IC consumption vs. Tj

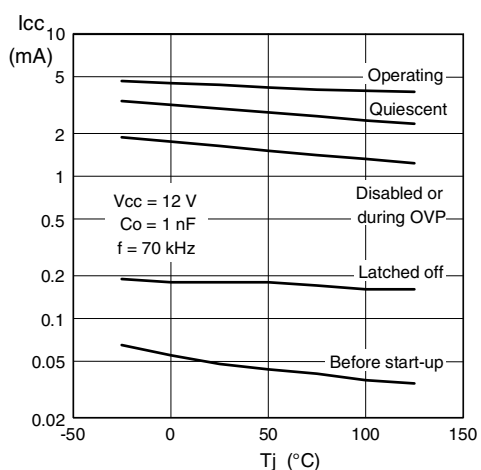


Figure 9. Feedback reference vs. Tj

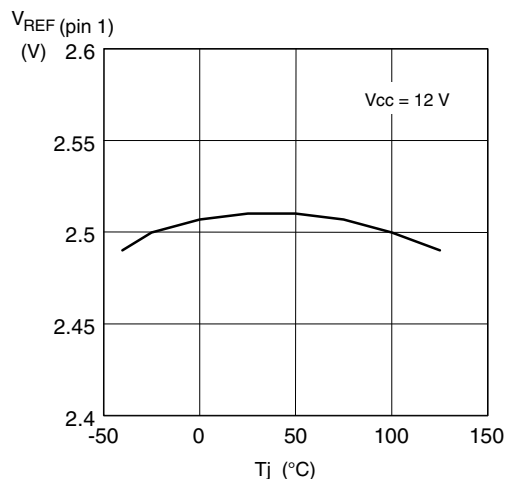


Figure 7. Start-up & UVLO vs. Tj

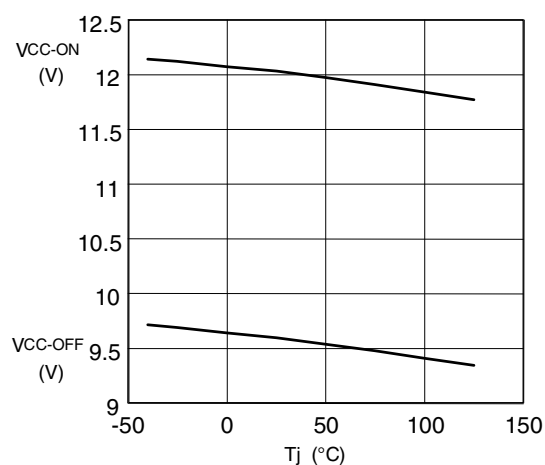


Figure 10. E/A output clamp levels vs. Tj

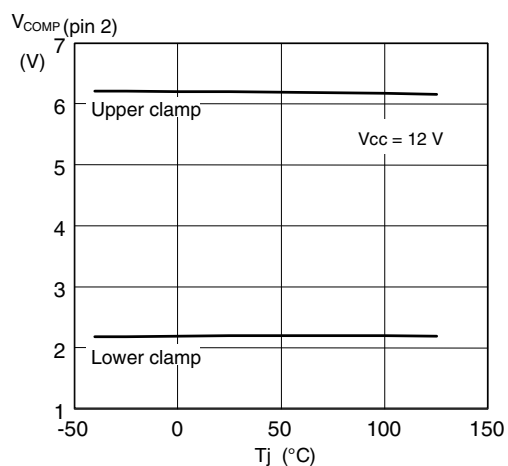


Figure 11. Static OVP level vs. Tj

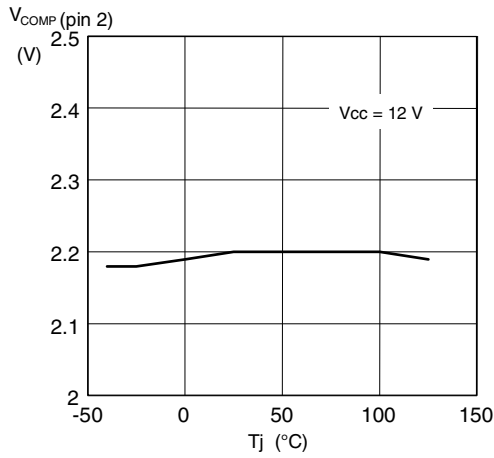


Figure 14. Vcs clamp vs. Tj

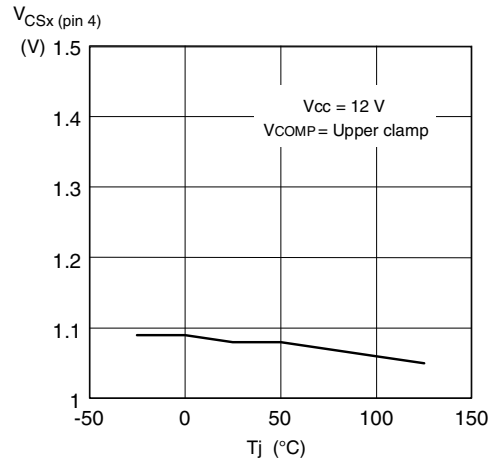


Figure 12. Dynamic OVP current vs. Tj (normalized value)

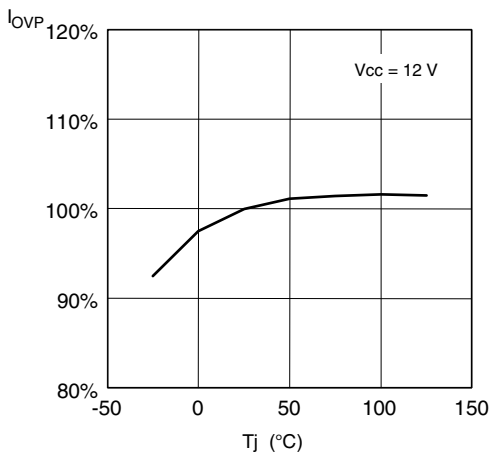


Figure 15. Current-sense offset vs. mains voltage phase angle

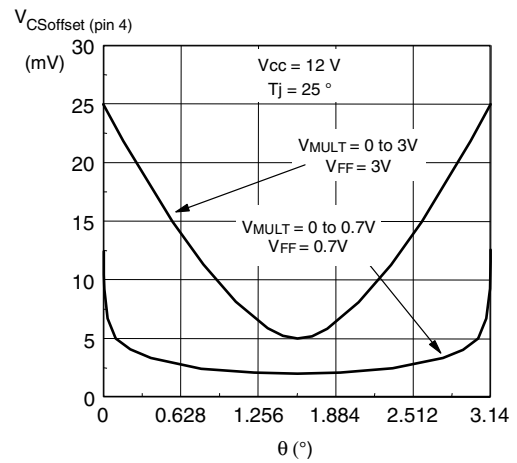


Figure 13. Delay-to-output vs. Tj

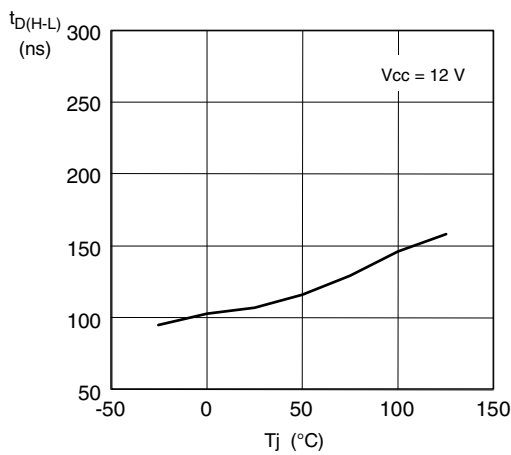


Figure 16. IC disable level on current sense vs. Tj

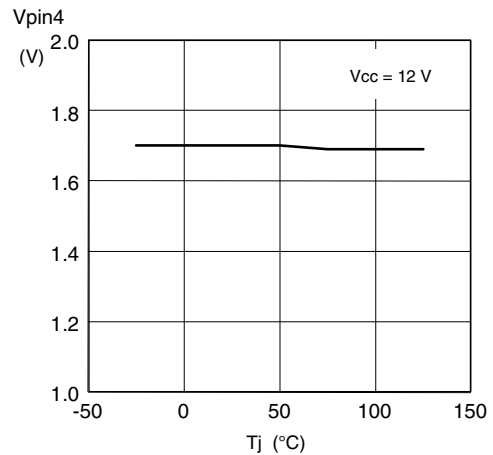


Figure 17. Multiplier characteristics @ VFF=1V

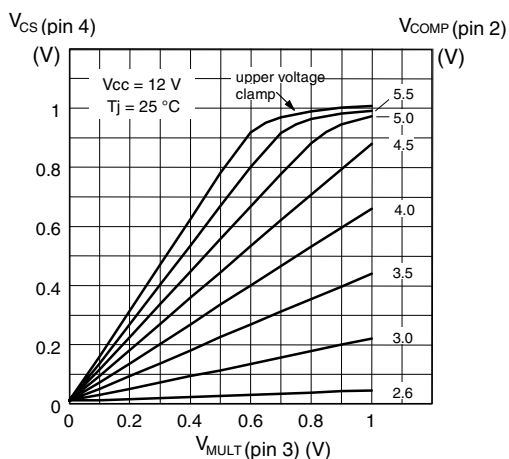


Figure 20. ZCD clamp levels vs. Tj

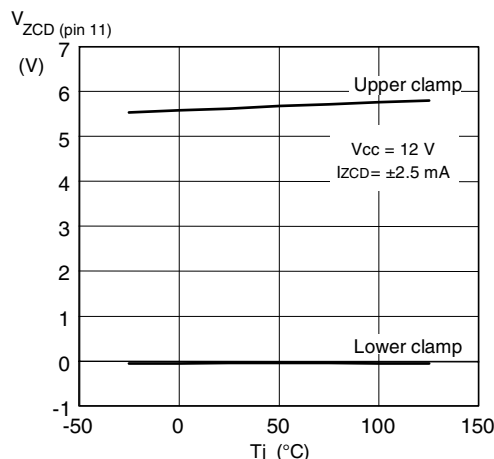


Figure 18. Multiplier characteristics @ VFF=3V

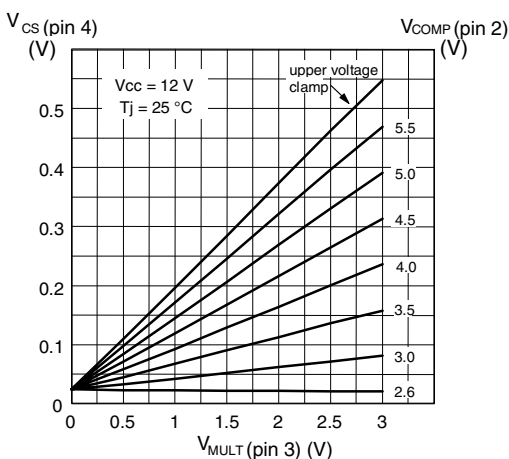


Figure 21. ZCD source capability vs. Tj

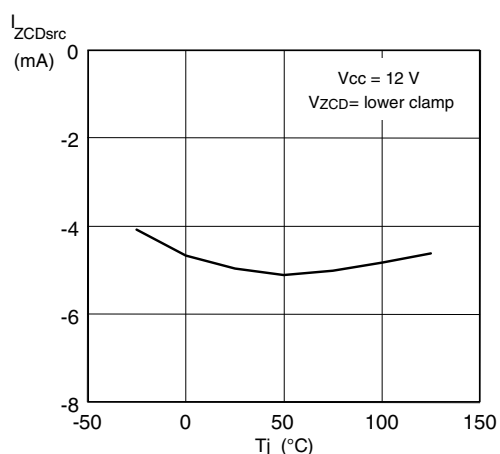


Figure 19. Multiplier gain vs. Tj

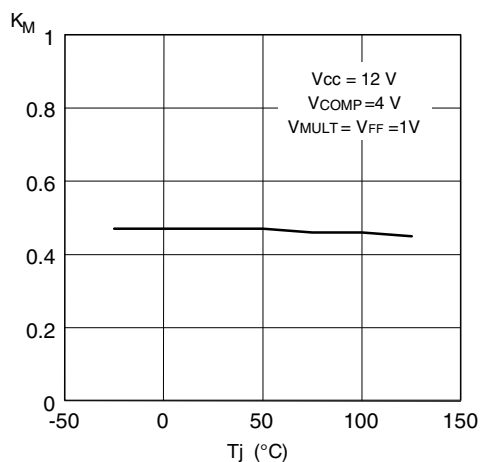


Figure 22. VFF & TBO dropouts vs. Tj

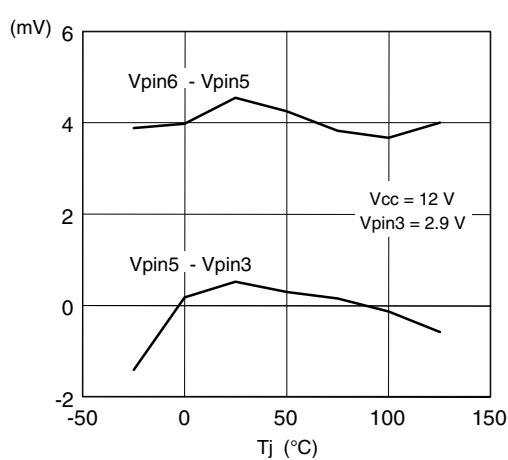


Figure 23. TBO current mismatch vs. Tj

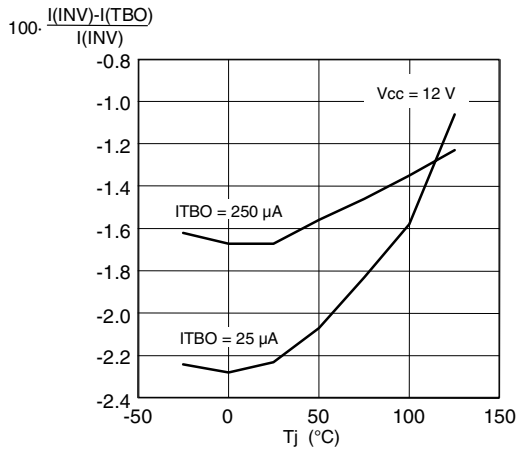


Figure 26. RUN thresholds vs. Tj

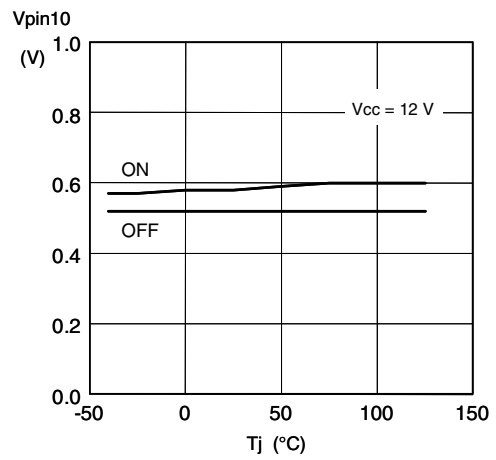


Figure 24. TBO-INV current mismatch vs. TBO currents

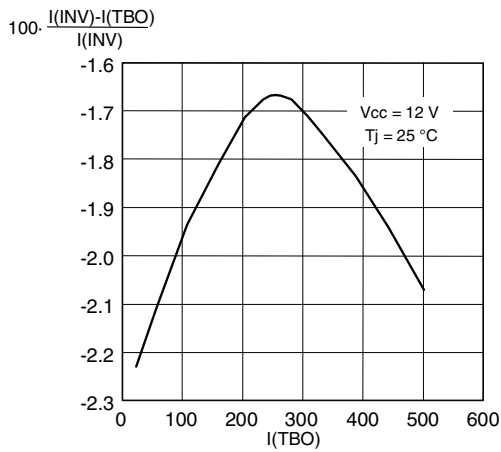


Figure 27. PWM_LATCH high saturation vs. Tj

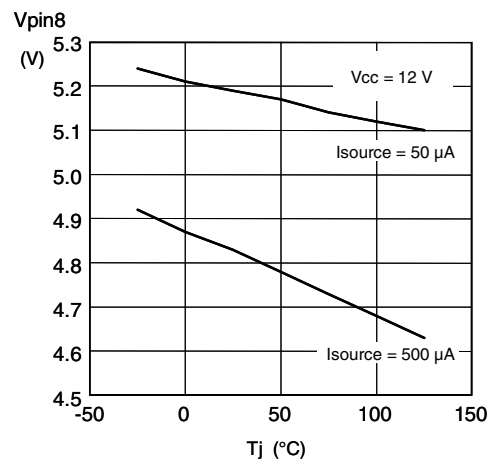


Figure 25. TBO clamp vs. Tj

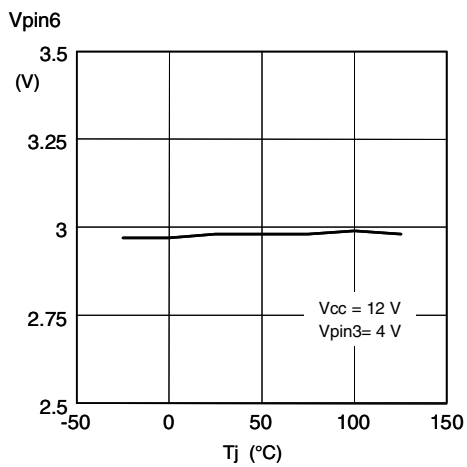


Figure 28. PWM_STOP low saturation vs. Tj

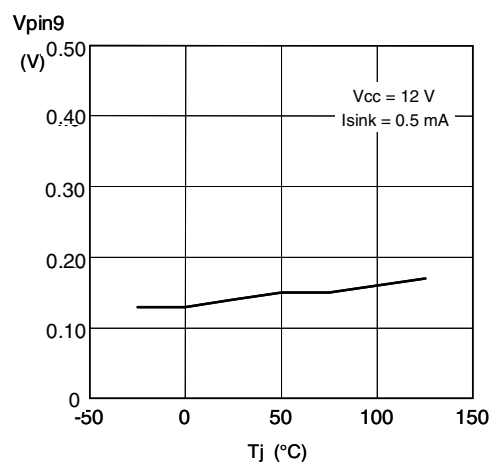


Figure 29. PFC_OK thresholds vs. Tj

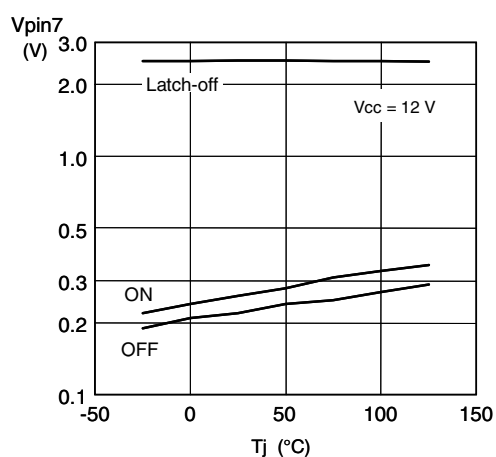


Figure 32. UVLO saturation vs. Tj

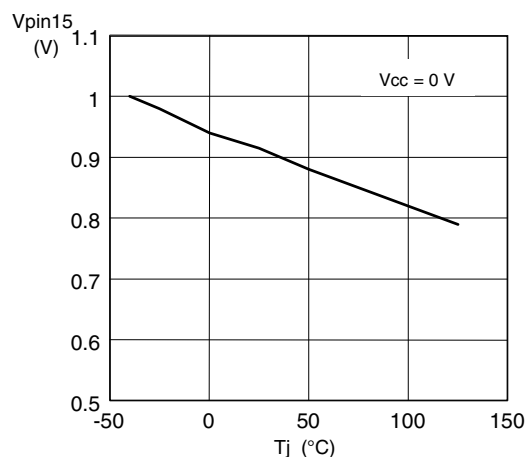


Figure 30. Start-up timer vs. Tj

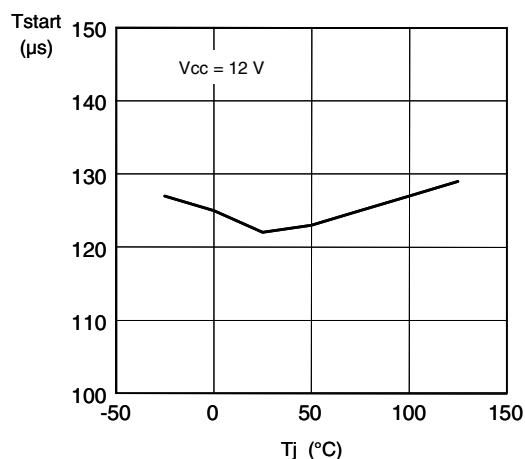


Figure 33. Gate-drive output low saturation

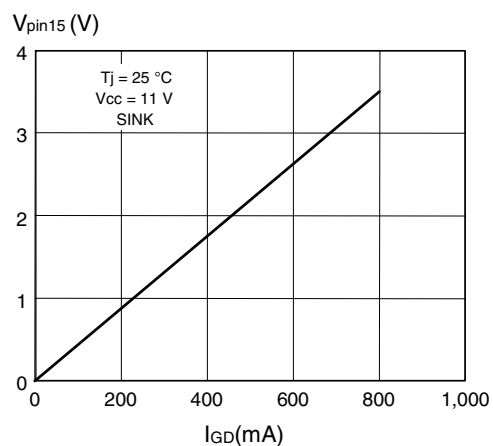


Figure 31. Gate-drive clamp vs. Tj

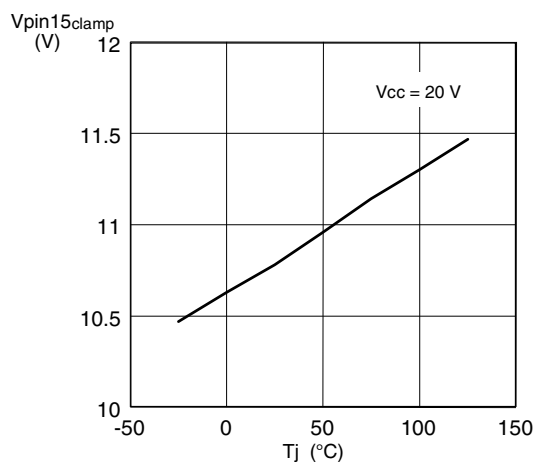
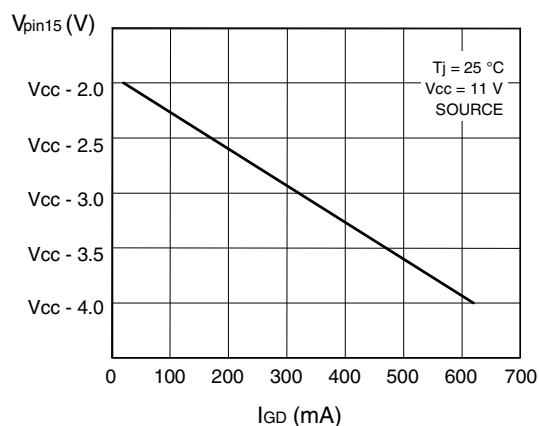


Figure 34. Gate-drive output high saturation



4 APPLICATION INFORMATION

4.1 Overvoltage protection

Normally, the voltage control loop keeps the output voltage V_o of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors R1 and R2 of the output divider. Neglecting the ripple components, under steady state conditions the current through R1 equals that through R2. Considering that the non-inverting input of the error amplifier is internally biased at 2.5V, the voltage at pin INV will be 2.5V as well, then:

$$I_{R2} = I_{R1} = \frac{2.5}{R2} = \frac{V_o - 2.5}{R1}$$

If the output voltage experiences an abrupt change ΔV_o the voltage at pin INV is kept at 2.5V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant. Then the current through R2 remains equal to $2.5/R2$ but that through R1 becomes:

$$I'_{R1} = \frac{V_o - 2.5 + \Delta V_o}{R1}$$

The difference current $\Delta I_{R1} = I'_{R1} - I_{R1} = \Delta V_o/R1$ will flow through the compensation network and enter the error amplifier (pin COMP). This current is monitored inside the IC and when it reaches about $18 \mu A$ the output voltage of the multiplier is forced to decrease, thus reducing the energy drawn from the mains. If the current exceeds $20 \mu A$, the OVP is triggered (Dynamic OVP), and the external power transistor is switched off until the current falls approximately below $5 \mu A$. However, if the overvoltage persists (e.g. in case the load is completely disconnected), the error amplifier will eventually saturate low hence triggering an internal comparator (Static OVP) that will keep the external power switch turned off until the output voltage comes back close to the regulated value. The output overvoltage that is able to trigger the OVP function is then:

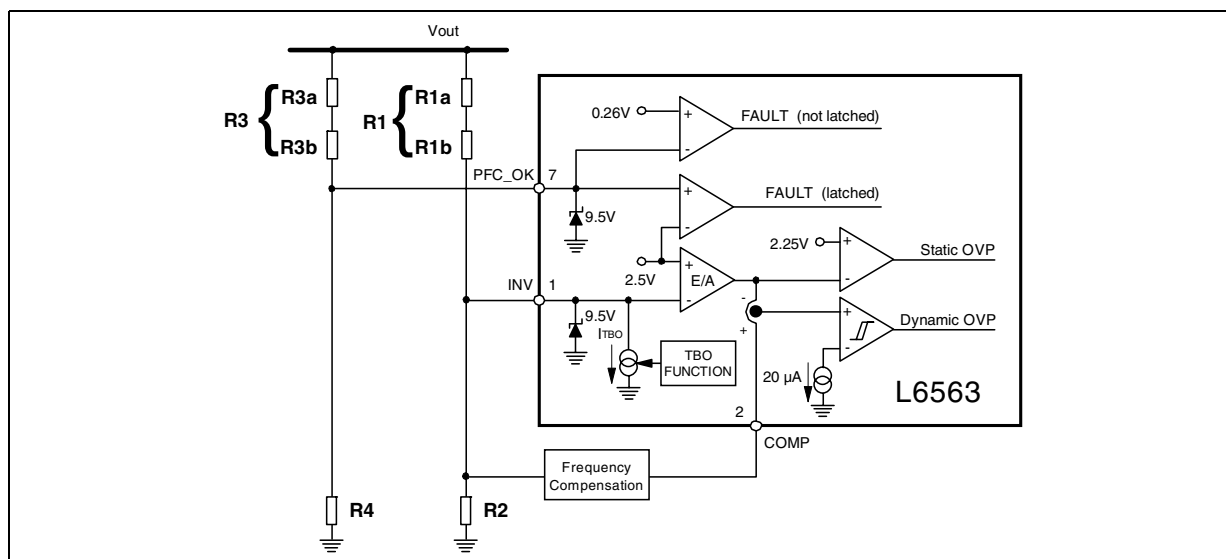
$$\Delta V_o = R1 \cdot 20 \cdot 10^{-6}$$

An important advantage of this technique is that the overvoltage level can be set independently of the regulated output voltage: the latter depends on the ratio of R1 to R2, the former on the individual value of R1. Another advantage is the precision: the tolerance of the detection current is 15%, which means 15% tolerance on the ΔV_o . Since it is usually much smaller than V_o , the tolerance on the absolute value will be proportionally reduced.

Example: $V_o=400V$, $\Delta V_o=40V$. Then: $R1=40V/20\mu A=2M\Omega$; $R2=2.5 \cdot 2M\Omega / (400-2.5)=12.58k\Omega$. The tolerance on the OVP level due to the L6563 will be $40 \cdot 0.15=6V$, that is $\pm 1.36\%$.

When either OVP is activated the quiescent consumption is reduced to minimize the discharge of the V_{cc} capacitor.

Figure 35. Output voltage setting, OVP and FFP functions: internal block diagram



4.2 Feedback failure protection (FFP)

The OVP function above described is able to handle "normal" overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at start-up. It cannot handle the overvoltage generated, for instance, when the upper resistor of the output divider (R1) fails open: the voltage loop can no longer read the information on the output voltage and will force the PFC pre-regulator to work at maximum ON-time, causing the output voltage to rise with no control.

A pin of the device (PFC_OK) has been dedicated to provide an additional monitoring of the output voltage with a separate resistor divider (R3 high, R4 low, see [Figure 35](#)). This divider is selected so that the voltage at the pin reaches 2.5V if the output voltage exceeds a preset value, usually larger than the maximum V_o that can be expected, also including worst-case load/line transients.

Example: $V_o = 400\text{ V}$, $V_{ox} = 475\text{ V}$. Select: $R_3 = 3\text{M}\Omega$; then: $R_4 = 3\text{M}\Omega \cdot 2.5 / (475 - 2.5) = 15.87\text{k}\Omega$.

When this function is triggered, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below $250\ \mu\text{A}$ and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. At the same time the pin PWM_LATCH is asserted high. PWM_LATCH is an open source output able to deliver 3.7V min. with 0.5 mA load, intended for tripping a latched shutdown function of the PWM controller IC in the cascaded DC-DC converter, so that the entire unit is latched off. To restart the system it is necessary to recycle the input power, so that the V_{cc} voltages of both the L6563 and the PWM controller go below their respective UVLO thresholds.

The PFC_OK pin doubles its function as a not-latched IC disable: a voltage below 0.2V will shut down the IC, reducing its consumption below 1 mA . In this case both PWM_STOP and PWM_LATCH keep their high impedance status. To restart the IC simply let the voltage at the pin go above 0.26 V .

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating will result in shutting down the IC and stopping the pre-regulator.

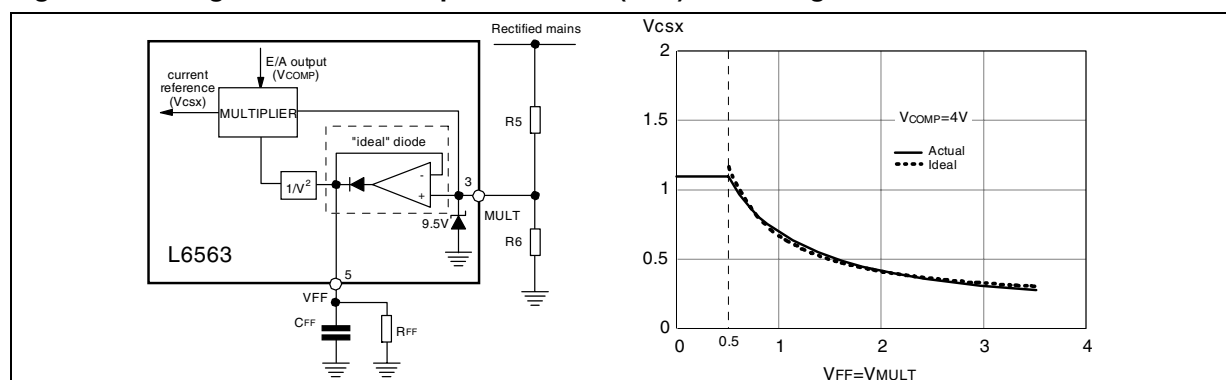
4.3 Voltage Feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency f_c of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design.

For example, setting the gain of the error amplifier to get $f_c = 20\text{ Hz}$ @ 264 Vac means having $f_c \cong 4\text{ Hz}$ @ 88 Vac , resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage Feedforward can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (see [Figure 36](#)).

Figure 36. Voltage feedforward: squarer-divider ($1/V^2$) block diagram and transfer characteristic



In this way a change of the line voltage will cause an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier output will be halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain will be constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

Actually, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated will be affected by a considerable amount of ripple at twice the mains frequency that will cause distortion of the current reference (resulting in high THD and poor PF); if it is too large there will be a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off is required.

The L6563 realizes Voltage Feedforward with a technique that makes use of just two external parts and that limits the feedforward time constant trade-off issue to only one direction. A capacitor C_{FF} and a resistor R_{FF} , both connected from the V_{FF} (#5) pin to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (#3). R_{FF} provides a means to discharge C_{FF} when the line voltage decreases (see [Figure 36](#)). In this way, in case of sudden line voltage rise, C_{FF} will be rapidly charged through the low impedance of the internal diode and no appreciable overshoot will be visible at the pre-regulator's output; in case of line voltage drop C_{FF} will be discharged with the time constant $R_{FF} \cdot C_{FF}$, which can be in the hundred ms to achieve an acceptably low steady-state ripple and have low current distortion; consequently the output voltage can experience a considerable undershoot, like in systems with no feedforward compensation.

The twice-mains-frequency ($2 \cdot f_L$) ripple appearing across C_{FF} is triangular with a peak-to-peak amplitude that, with good approximation, is given by:

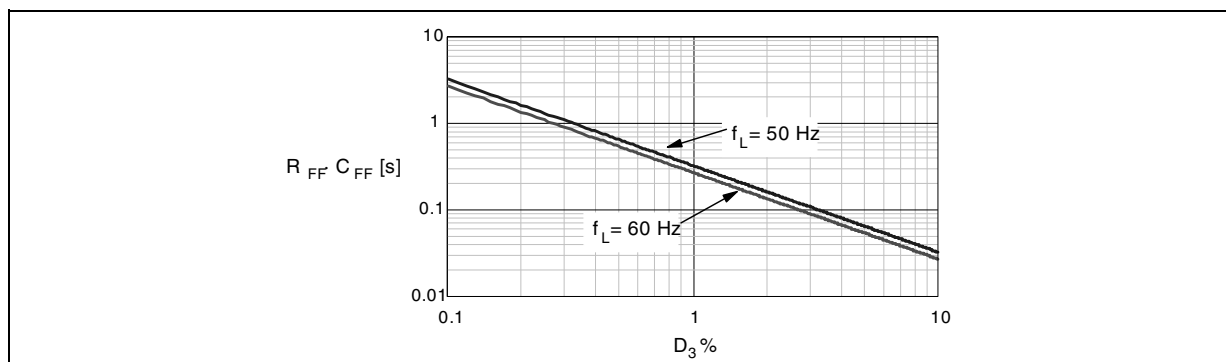
$$\Delta V_{FF} = \frac{2V_{MULTpk}}{1 + 4f_L R_{FF} C_{FF}},$$

where f_L is the line frequency. The amount of 3rd harmonic distortion introduced by this ripple, related to the amplitude of its $2 \cdot f_L$ component, will be:

$$D_3\% = \frac{100}{2\pi f_L R_{FF} C_{FF}}$$

[Figure 37](#) shows a diagram that helps choose the time constant $R_{FF} \cdot C_{FF}$ based on the amount of maximum desired 3rd harmonic distortion. Always connect R_{FF} and C_{FF} to the pin, the IC will not work properly if the pin is either left floating or connected directly to ground.

Figure 37. $R_{FF} \cdot C_{FF}$ as a function of 3rd harmonic distortion introduced in the input current



The dynamics of the voltage feedforward input is limited downwards at 0.5V (see [Figure 36](#)), that is the output of the multiplier will not increase any more if the voltage on the V_{FF} pin is below 0.5V. This helps to prevent excessive power flow when the line voltage is lower than the minimum specified value

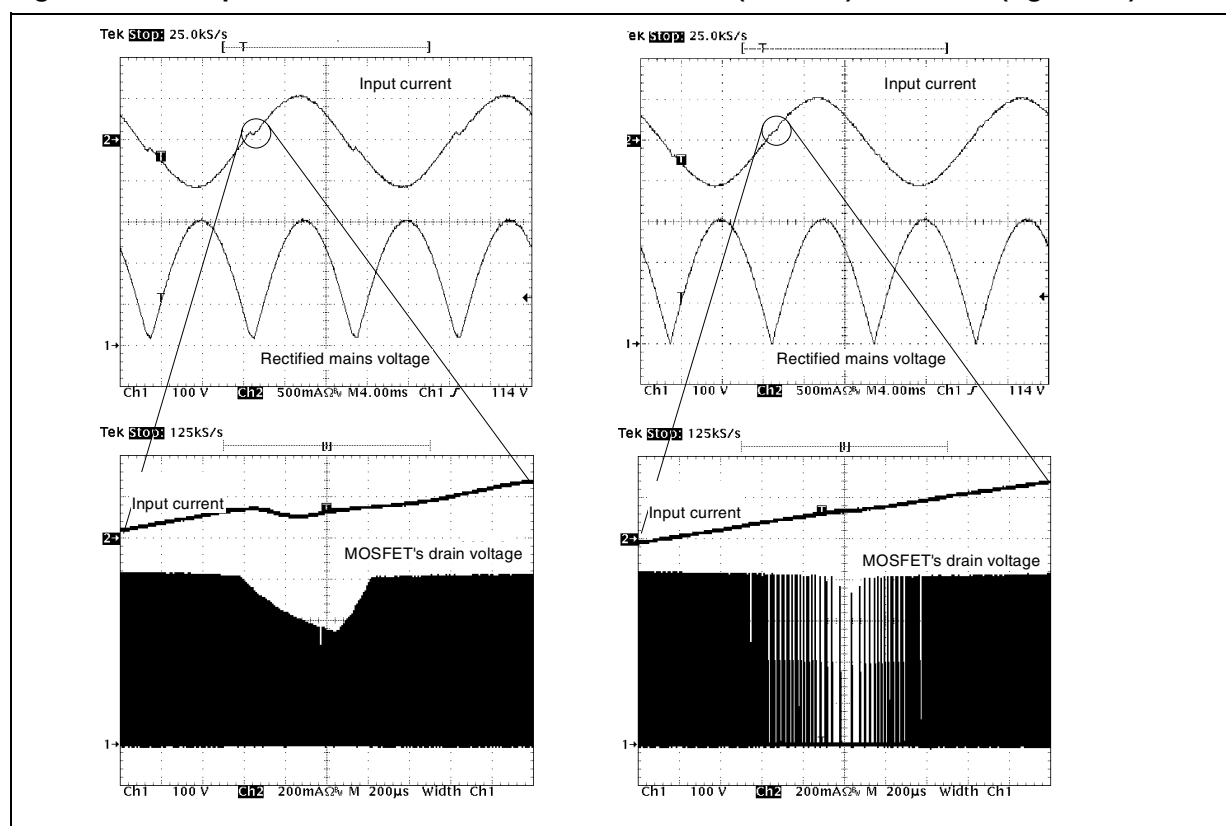
4.4 THD optimizer circuit

The L6563 is provided with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge.

Figure 38. THD optimization: standard TM PFC controller (left side) and L6563 (right side)



Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore the offset is modulated by the voltage on the V_{FF} pin (see [Voltage Feed-forward](#) section) so as to have little offset at low line, where energy transfer at zero crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

The effect of the circuit is shown in [Figure 38](#), where the key waveforms of a standard TM PFC controller are compared to those of this chip.

To take maximum benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus reducing the effectiveness of the optimizer circuit.

4.5 Tracking boost function

In some applications it may be advantageous to regulate the output voltage of the PFC pre-regulator so that it tracks the RMS input voltage rather than at a fixed value like in conventional boost pre-regulators. This is commonly referred to as "tracking boost" or "follower boost" approach.

With the L6563 this can be realized by connecting a resistor (R_T) between the TBO pin and ground. The TBO pin presents a DC level equal to the peak of the MULT pin voltage and is then representative of the mains RMS voltage. The resistor defines a current, equal to $V(\text{TBO})/R_T$, that is internally 1:1 mirrored and sunk from pin INV (#1) input of the L6563's error amplifier. In this way, when the mains voltage increases the voltage at TBO pin will increase as well and so will do the current flowing through the resistor connected between TBO and GND. Then a larger current will be sunk by INV pin and the output voltage of the PFC pre-regulator will be forced to get higher. Obviously, the output voltage will move in the opposite direction if the input voltage decreases.

To avoid undesired output voltage rise should the mains voltage exceed the maximum specified value, the voltage at the TBO pin is clamped at 3V. By properly selecting the multiplier bias it is possible to set the maximum input voltage above which input-to-output tracking ends and the output voltage becomes constant. If this function is not used, leave the pin open: the device will regulate a fixed output voltage.

Starting from the following data:

- V_{in1} = minimum specified input RMS voltage;
- V_{in2} = maximum specified input RMS voltage;
- V_{o1} = regulated output voltage @ $V_{in} = V_{in1}$;
- V_{o2} = regulated output voltage @ $V_{in} = V_{in2}$;
- V_{ox} = absolute maximum limit for the regulated output voltage;
- ΔV_o = OVP threshold,

to set the output voltage at the desired values use the following design procedure:

- 1) Determine the input RMS voltage $V_{in_{clamp}}$ that produces $V_o = V_{ox}$:

$$V_{in_{clamp}} = \frac{V_{ox} - V_{o1}}{V_{o2} - V_{o1}} \cdot V_{in2} - \frac{V_{ox} - V_{o2}}{V_{o2} - V_{o1}} \cdot V_{in1}$$

and choose a value V_{in_x} such that $V_{in2} = V_{in_x} < V_{in_{clamp}}$. This will result in a limitation of the output voltage range below V_{ox} (it will equal V_{ox} if one chooses $V_{in_x} = V_{in_{clamp}}$)

- 2) Determine the divider ratio of the MULT pin (#3) bias:

$$k = \frac{3}{\sqrt{2} \cdot V_{in_x}}$$

and check that at minimum mains voltage V_{in1} the peak voltage on pin 3 is greater than 0.65V.

- 3) Determine R_1 , the upper resistor of the output divider:

$$R_1 = \frac{\Delta V_o}{20} \cdot 10^6$$

- 4) Calculate the lower resistor R_2 of the output divider and the adjustment resistor R_T :

$$\begin{cases} R_2 = 2.5 \cdot R_1 \cdot \frac{V_{in2} - V_{in1}}{(V_{o1} - 2.5) \cdot V_{in2} - (V_{o2} - 2.5) \cdot V_{in1}} \\ R_T = \sqrt{2} \cdot k \cdot R_1 \cdot \frac{V_{in2} - V_{in1}}{V_{o2} - V_{o1}} \end{cases}$$

- 5) Check that the maximum current sourced by the TBO pin (#6) does not exceed the maximum specified (0.25 mA):

$$I_{TBO_{max}} = \frac{3}{R_T} \leq 0.25 \cdot 10^{-3}$$

In the following Mathcad® sheet, as an example, the calculation is shown for the circuit illustrated in [Figure 39](#). [Figure 40](#) shows the internal block diagram of the tracking boost function.

Design Data

$$\begin{aligned} V_{in1} &= 88V & V_{o1} &= 200V \\ V_{in2} &= 264V & V_{o2} &= 385V \\ V_{ox} &= 400V \\ \Delta V_o &= 40V \end{aligned}$$

Step 1

$$V_{in_{clamp}} = \frac{V_{ox} - V_{o1}}{V_{o2} - V_{o1}} \cdot V_{in2} - \frac{V_{ox} - V_{o2}}{V_{o2} - V_{o1}} \cdot V_{in1} \quad V_{in_{clamp}} = 278.27V$$

$$\text{choose: } V_{in_x} = 270V$$

Step 2

$$k = \frac{3}{\sqrt{2} \cdot V_{in_x}} \quad k = 7.857 \times 10^{-3}$$

Step 3

$$R1 = \frac{\Delta V_o}{20} \cdot 10^6 \quad R1 = 2 \times 10^6 \Omega$$

Step 4

$$R2 = 2.5 \cdot R1 \cdot \frac{V_{in2} - V_{in1}}{(V_{o1} - 2.5) \cdot V_{in2} - (V_{o2} - 2.5) \cdot V_{in1}} \quad R2 = 4.762 \times 10^4 \Omega$$

$$R_T = k \cdot \sqrt{2} \cdot R1 \cdot \frac{V_{in2} - V_{in1}}{V_{o2} - V_{o1}} \quad R_T = 2.114 \times 10^4 \Omega$$

Step 5

$$I_{TBO_{max}} = \frac{3}{R_T} \cdot 10^3 \quad I_{TBO_{max}} = 0.142 \text{ mA}$$

$$V_o(V_i) = \begin{cases} V_{MULTpk} \leftarrow k \cdot \sqrt{2} \cdot V_i & V_o(V_{in1}) = 200 \text{ V} \\ V_{TBO} \leftarrow \text{if}(V_{MULTpk} < 3, V_{MULTpk}, 3) & V_o(V_{in2}) = 385 \text{ V} \\ 2.5 \cdot \left(1 + \frac{R1}{R2}\right) + V_{TBO} \cdot \frac{R1}{R_T} & V_o(V_{in_x}) = 391.307 \text{ V} \end{cases}$$

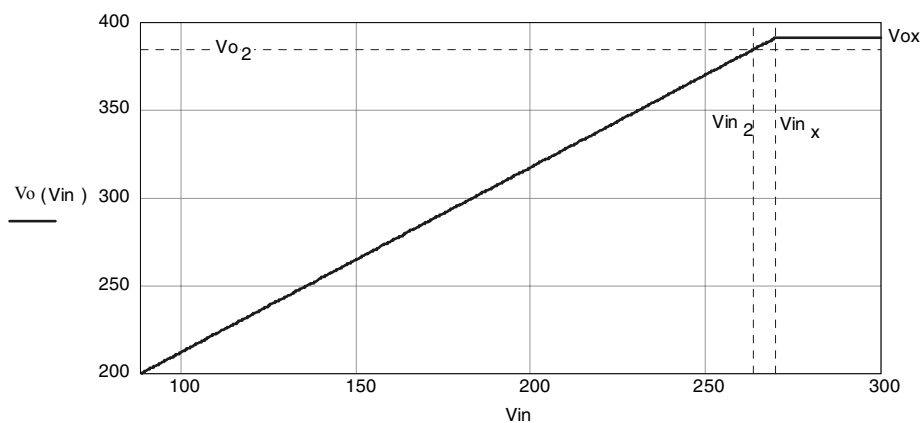


Figure 39. 80W, wide-range-mains PFC pre-regulator with tracking boost function active

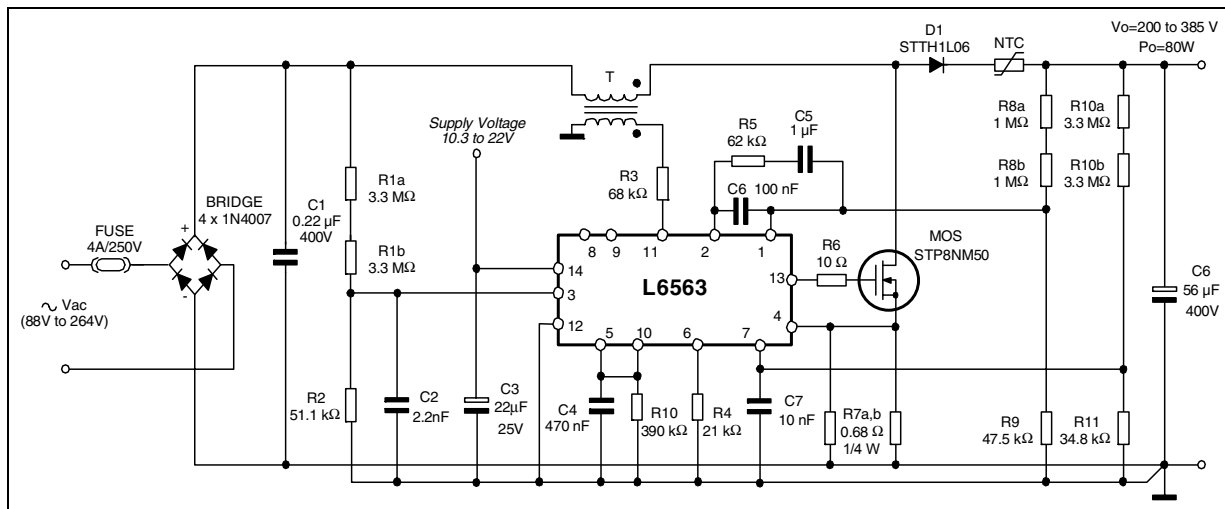
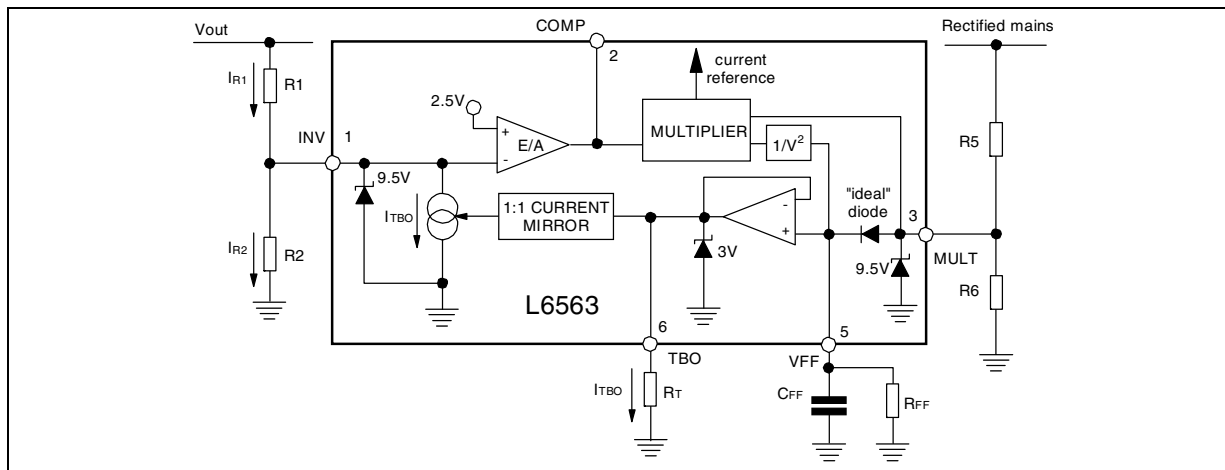


Figure 40. Tracking boost and Voltage Feedforward blocks

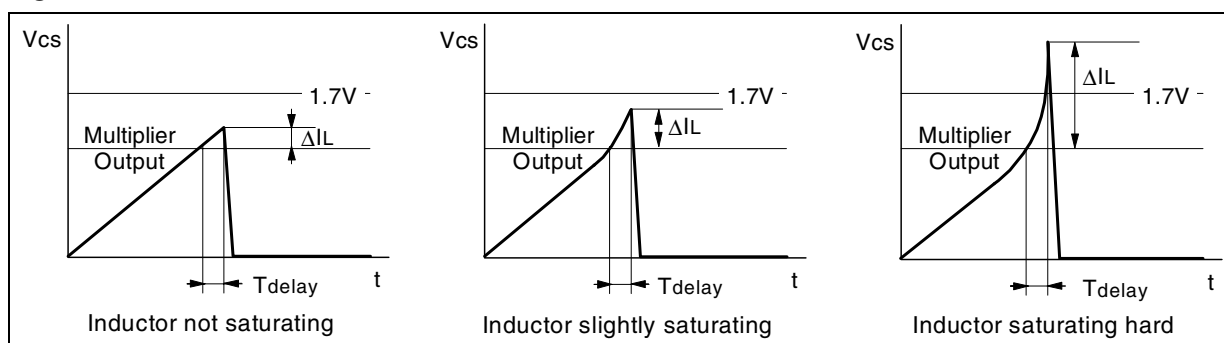


4.6 Inductor saturation detection

Boost inductor's hard saturation may be a fatal event for a PFC pre-regulator: the current upslope becomes so large (50-100 times steeper, see [Figure 41](#)) that during the current sense propagation delay the current may reach abnormally high values. The voltage drop caused by this abnormal current on the sense resistor reduces the gate-to-source voltage, so that the MOSFET may work in the active region and dissipate a huge amount of power, which leads to a catastrophic failure after few switching cycles.

A well-designed boost inductor must not saturate even under the worst-case operating conditions, that is at power-up with maximum load and minimum line voltage, when the error amplifier saturates high and commands the maximum peak current (defined by the current reference clamp, $V_{CSclamp}$, and the sense resistor) for some line cycles. However, especially in the development stage, inductor saturation may be encountered and a protection able to prevent the application from blowing up can be very useful.

The device is provided with a second comparator on the current sense pin (CS, #4) that stops and latches off the IC if the voltage on the pin, normally limited within 1.1V, exceeds 1.7V. Also the cascaded DC-DC converter can be stopped via the PWM_LATCH pin that is asserted high. In this way there can be abnormal current only for one cycle, after that the system is stopped and enabled to restart only after recycling the input power, that is when the V_{cc} voltages of the IC and the PWM controller go below their respective UVLO thresholds. System safety will be considerably increased.

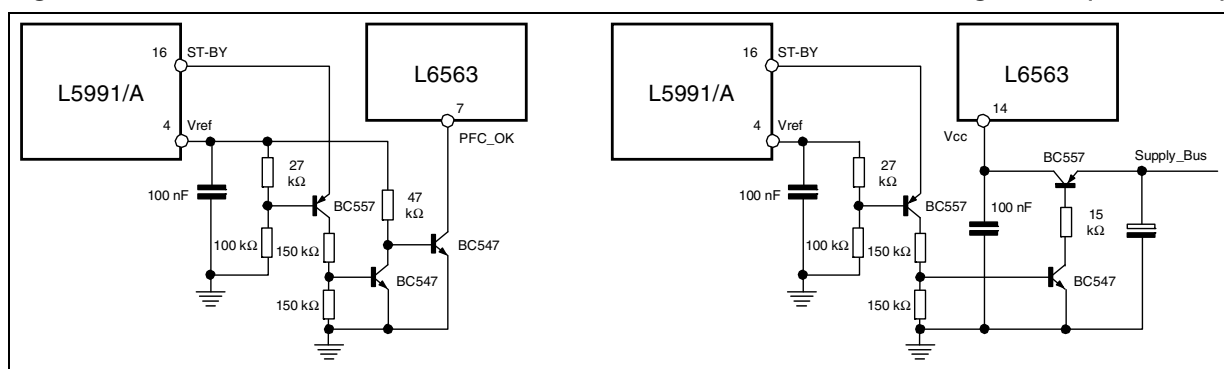
Figure 41. Effect of boost inductor saturation on the MOSFET current and detection method

4.7 Power management/housekeeping functions

A special feature of this IC is that it facilitates the implementation of the "housekeeping" circuitry needed to coordinate the operation of the PFC stage to that of the cascaded DC-DC converter. The functions realized by the housekeeping circuitry ensure that transient conditions like power-up or power down sequencing or failures of either power stage be properly handled.

This device provides some pins to do that. As already mentioned, one communication line between the IC and the PWM controller of the cascaded DC-DC converter is the PWM_LATCH pin, which is normally open when the PFC works properly and goes high if it loses control of the output voltage (because of a failure of the control loop) or if the boost inductor saturates, with the aim of latching off the PWM controller of the cascaded DC-DC converter as well ([Feedback failure protection \(FFP\)](#) for more details).

A second communication line can be established via the disable function included in the PFC_OK pin ([Feedback failure protection \(FFP\)](#) for more details). Typically this line is used to allow the PWM controller of the cascaded DC-DC converter to shut down the L6563 in case of light load, to minimize the no-load input consumption. Should the residual consumption of the chip be an issue, it is also possible to cut down the supply voltage. Interface circuits like those shown in [Figure 42](#), where the L6563 works along with the L5991, PWM controller with standby function, can be used. Needless to say, this operation assumes that the cascaded DC-DC converter stage works as the master and the PFC stage as the slave or, in other words, that the DC-DC stage starts first, it powers both controllers and enables/disables the operation of the PFC stage.

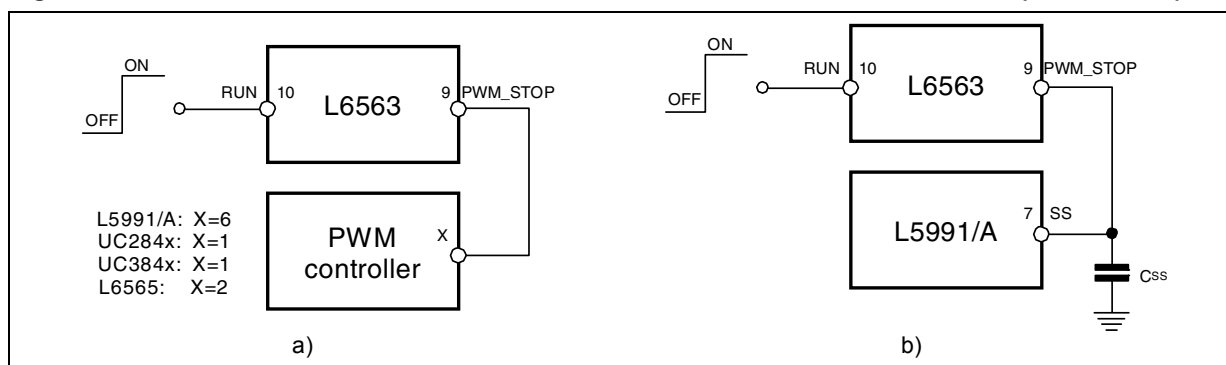
Figure 42. Interface circuits that let the L5991/ L5991A disable the L6563 at light load (slave PFC)

The third communication line is the PWM_STOP pin (#9), which works in conjunction with the RUN pin (#10). The purpose of the PWM_STOP pin is to inhibit the PWM activity of both the PFC stage and the cascaded DC-DC converter. The pin is an open collector, normally open, that goes low if the device is disabled by a voltage lower than 0.52V on the RUN pin. It is important to point out that this function works correctly in systems where the PFC stage is the master and the cascaded DC-DC converter is the slave or, in other words, where the PFC stage starts first, powers both controllers and enables/disables the op-

eration of the DC-DC stage.

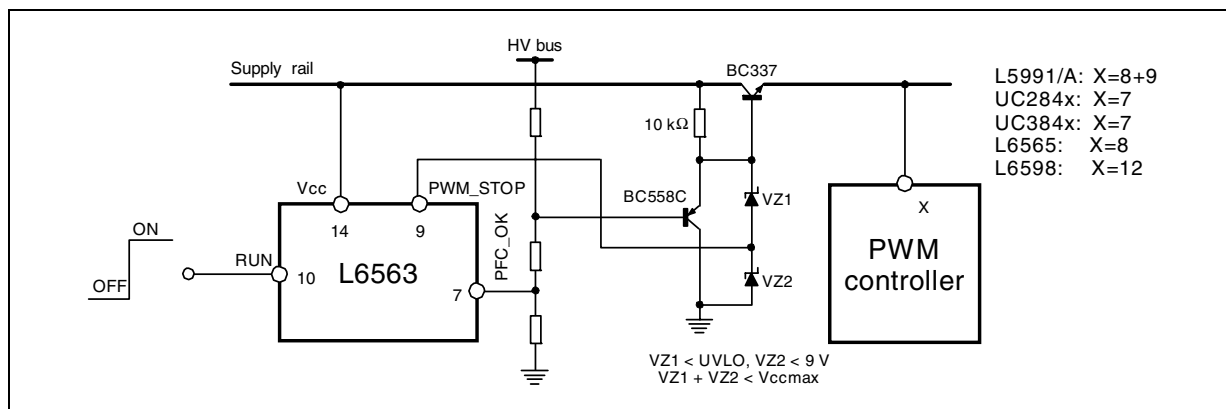
This function is quite flexible and can be used in different ways. In systems comprising an auxiliary converter and a main converter (e.g. desktop PC's silver box or hi-end LCD-TV), where the auxiliary converter also powers the controllers of the main converter, the pin RUN can be used to start and stop the main converter. In the simplest case, to enable/disable the PWM controller the PWM_STOP pin can be connected to either the output of the error amplifier (Figure 43 a) or, if the chip is provided with it, to its soft-start pin (Figure 43 b). The use of the soft-start pin allows the designer to delay the start-up of the DC-DC stage with respect to that of the PFC stage, which is often desired. An underlying assumption in order for that to work properly is that the UVLO thresholds of the PWM controller are certainly higher than those of the L6563.

Figure 43. Interface circuits that let the L6563 switch on or off a PWM controller (master PFC)



If this is not the case or it is not possible to achieve a start-up delay long enough (because this prevents the DC-DC stage from starting up correctly) or, simply, the PWM controller is devoid of soft start, the arrangement of Figure 44 lets the DC-DC converter start-up when the voltage generated by the PFC stage reaches a preset value. The technique relies on the UVLO thresholds of the PWM controller.

Figure 44. Interface circuits for actual power-up sequencing (master PFC)



Another possible use of the RUN and PWM_STOP pins (again, in systems where the PFC stage is the master) is brownout protection, thanks to the hysteresis provided.

Brownout protection is basically a not-latched device shutdown function that must be activated when a condition of mains undervoltage is detected. This condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also cause the PFC pre-regulator to work open loop and this could be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power down and that cause the output voltage of the converter not to decay to zero monotonically. For these reasons it is usually preferable to shutdown the unit in case of brownout.

IC shutdown upon brownout can be easily realized as shown in *Figure 45*. The scheme on the left is of general use, the one on the right can be used if the bias levels of the multiplier and the $R_{FF} \cdot C_{FF}$ time constant are compatible with the specified brownout level and with the specified holdup time respectively.

In *Table 6* it is possible to find a summary of all of the above mentioned working conditions that cause the device to stop operating.

Figure 45. Brownout protection (master PFC)

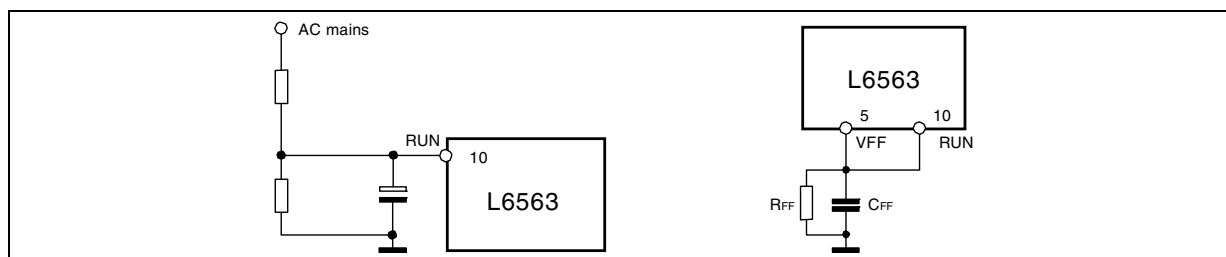


Table 6. Summary of L6563 idle states

CONDITION	CAUSED OR REVEALED BY	PWM_LATCH (pin 8)	PWM_STOP (pin9)	TYPICAL IC CONSUMPTION	IC behavior
UVLO	$V_{cc} < 8.7\text{ V}$	Open	Open	50 μA	Auto-restart
Feedback disconnected	$\text{PFC_OK} > 2.5\text{ V}$	Active (high)	Open	180 μA	Latched
Saturated Boost Inductor	$V_{cs} > 1.7\text{ V}$	Active (high)	Open	180 μA	Latched
AC Brownout	$\text{RUN} < 0.52\text{ V}$	Open	Active (low)	1.5 mA	Auto-restart
Standby	$\text{PFC_OK} < 0.2\text{ V}$	Open	Open	1.5 mA	Auto-restart

5 APPLICATION EXAMPLES AND IDEAS

Figure 46. 250W, wide-range-mains PFC pre-regulator with fixed output voltage

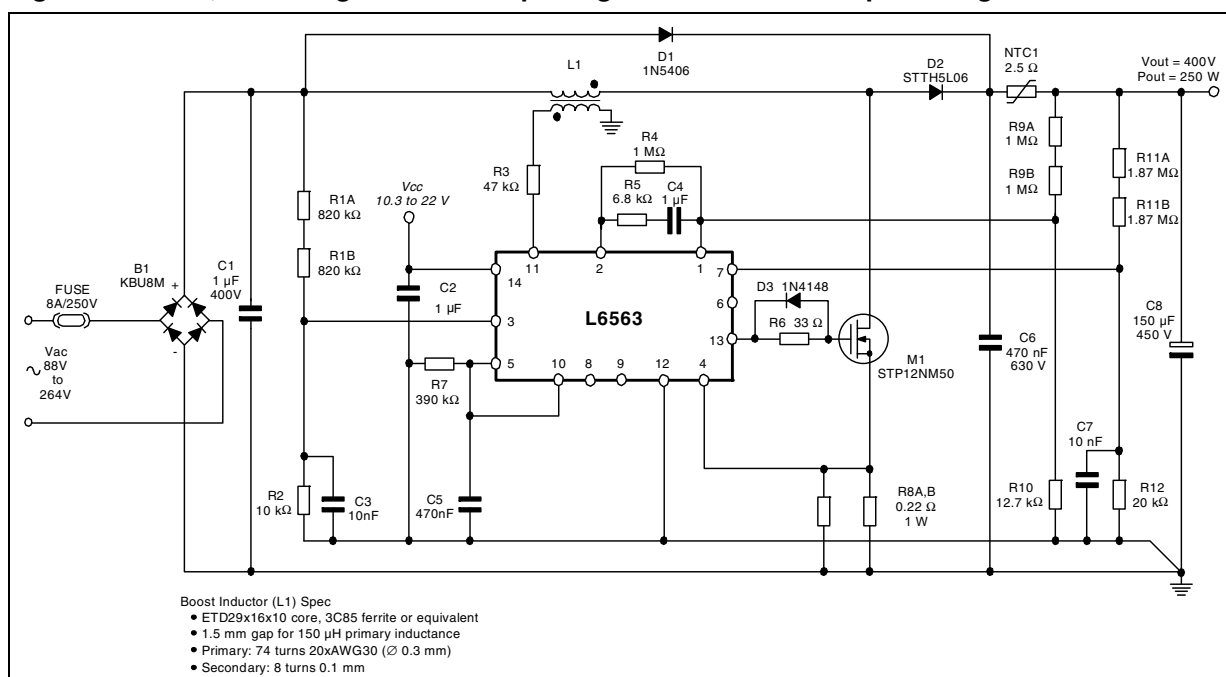
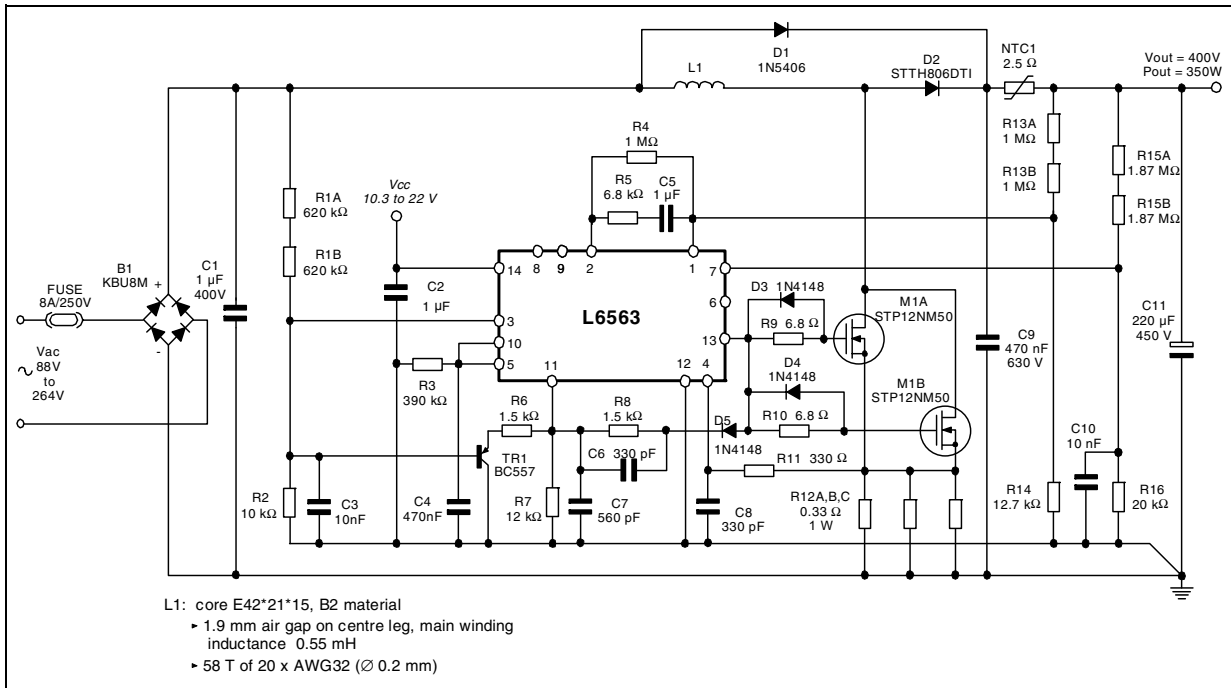
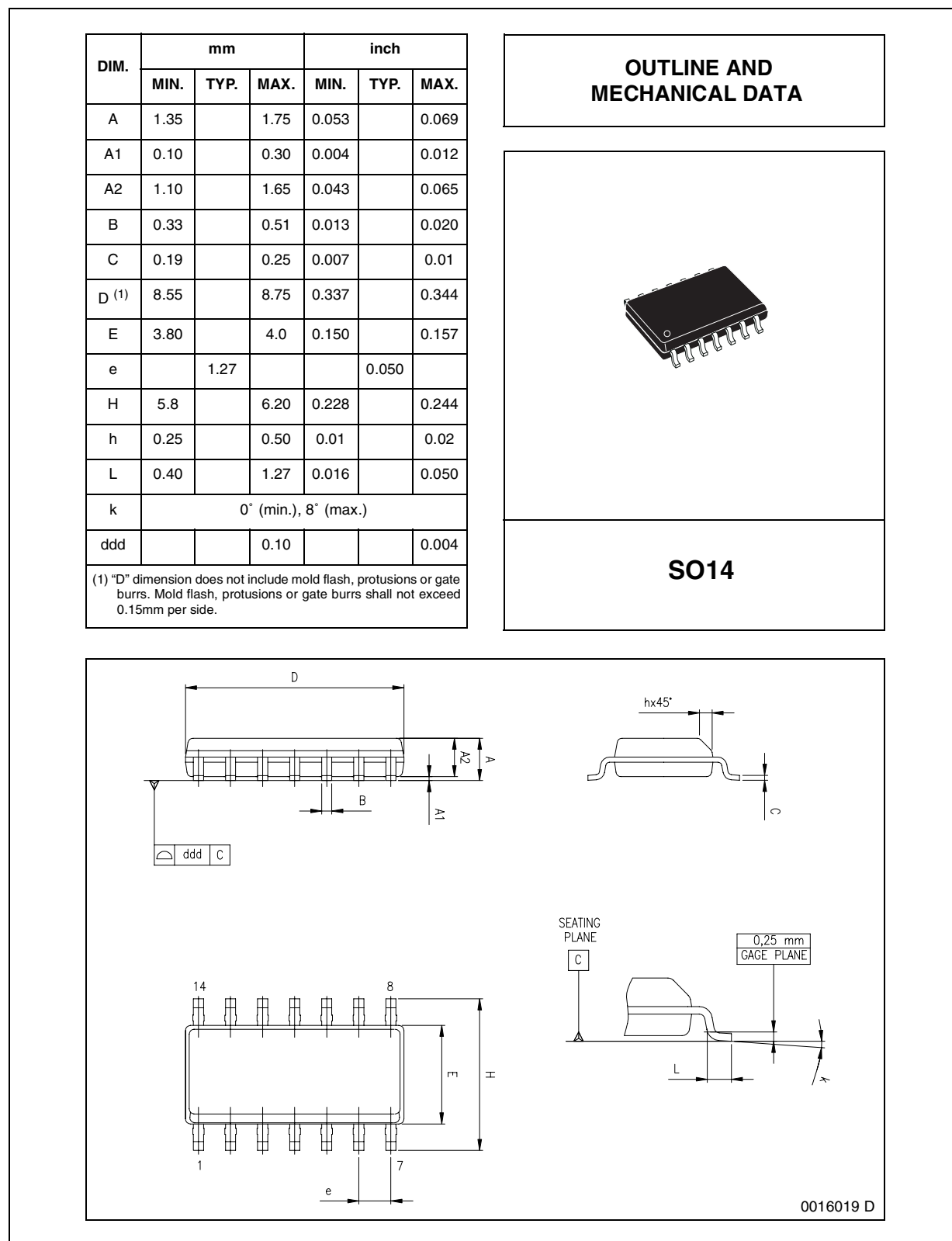


Figure 47. 350W, wide-range-mains PFC pre-regulator with fixed output voltage and FOT control



6 PACKAGE INFORMATION

Figure 48. SO14 Mechanical Data & Package Dimensions



7 REVISION HISTORY

Table 7. Revision History

Date	Revision	Description of Changes
November 2004	1	First Issue

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