

绿色环保模式反激式控制器

 查询样品: **UCC28610**

特性

- 共发-共基放大器配置可实现完全集成的电流控制方案, 无需使用外部检测电阻器
- 利用共发-共基放大器配置 (**cascode configuration**) 实现了快速启动和低待机功耗
- 用于在整个工作范围内实现最优效率的频率及峰值电流调制
- 绿色环保模式 (**GM**) 突发开关脉冲群改善了无负载时的效率
- 高级过流保护功能可限制 **RMS** 输入及输出电流
- 热关断
- 具有重试或锁断响应的定时过载
- 可编程无光耦输出过压保护 (**Opto-Less Output Overvoltage Protection**)
- 快速闭锁故障恢复
- **8** 引脚 **SOIC** 封装和 **8** 引脚 **PDIF** 无铅型封装

应用

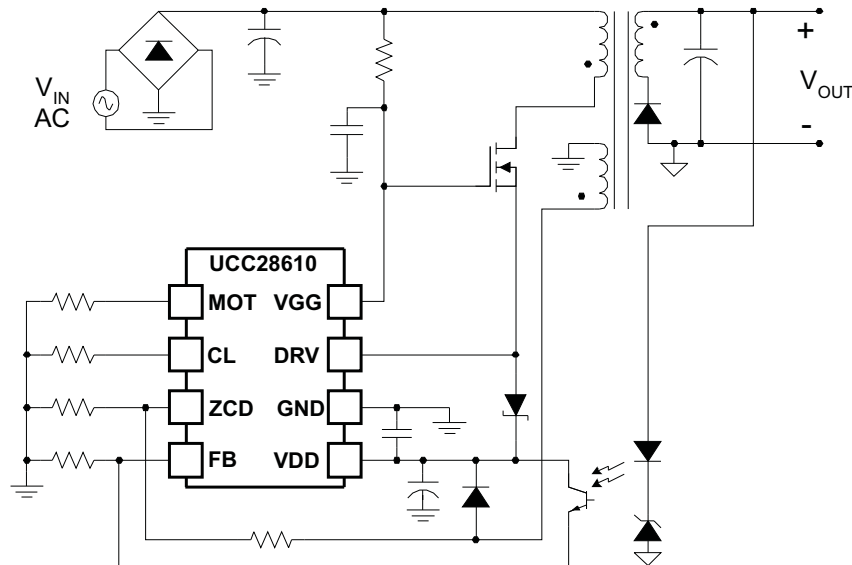
- 通用输入 **AC / DC** 适配器 (输出功率范围为 **12W** 至 **65W**)
- 高效率内务处理及辅助电源
- 离线式电池充电器
- 消费电子产品 (DVD 播放机、机顶盒、**DTV**、游戏、打印机等)

说明

UCC28610 使 AC / DC 消费产品电源解决方案的性能和可靠性达到了一个新的水平。

一种 PWM 调制算法用于调整开关频率和初级电流 (primary current), 并在整个工作范围内保持不连续或转换模式操作。通过与一种共发-共基放大器架构相结合, 这些创新较之传统的反激式架构在效率、可靠性及系统成本方面实现了改进。

UCC28610 提供了一个可预知的最大功率阈值和一个针对过载的定时响应, 从而实现了浪涌功率要求的安全处理。过载故障响应可由用户设置为“重试”或“锁断”模式。其他保护功能还包括输出过压检测、可编程最大导通时间和热关断。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

ORDERING INFORMATION

OPERATING TEMPERATURE RANGE, T _A	PINS	PACKAGE	PACKAGE LEAD	TRANSPORT MEDIA	UNITS	ORDERABLE PART NUMBER
-40°C to 125°C	8	Plastic Small Outline SOIC	D	Tape and Reel	2500	UCC28610DR
	8	Plastic Dual In-Line PDIP	P	Tube	50	UCC28610P

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

All voltages are with respect to GND, -40°C < T_J = T_A < 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted)

		UCC28610	UNIT
Input voltage range	VDD	-0.5 to +25	V
	DRV, during conduction	-0.5 to +2.0	
	DRV, during non-conduction	20	
	VGG ⁽²⁾	-0.5 to +16	
	ZCD, MOT, CL ⁽³⁾	-0.5 to +7	
	FB ⁽³⁾	-0.5 to +1.0	
	VDD – VGG	-7 to +10	
Continuous input current	I _{VGG} ⁽²⁾	10	mA
Input current range	I _{ZCD} , I _{MOT} , I _{CL} , I _{FB} ⁽³⁾	-3 to +1	
Peak output current	DRV	-5	A
	DRV, pulsed 200ns, 2% duty cycle	-5 to +1.5	
T _J	Operating junction temperature range	-40 to +150	°C
T _{stg}	Storage temperature range	-65 to +150	
	Lead Temperature (soldering, 10 sec.)	+260	

- (1) These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability
- (2) Voltage on VGG is internally clamped. The clamp level varies with operating conditions. In normal use, VGG is current fed with the voltage internally limited
- (3) In normal use, MOT, CL, ZCD, and FB are connected to resistors to GND and internally limited in voltage swing

PACKAGE DISSIPATION RATINGS^{(1) (2)}

PACKAGE	θ _{JA} , THERMAL IMPEDANCE JUNCTION TO AMBIENT, NO AIRFLOW (°C/W) ⁽¹⁾	θ _{JB} , THERMAL IMPEDANCE JUNCTION TO BOARD, NO AIRFLOW (°C/W) ⁽²⁾	T _A = 25°C POWER RATING (mW) ⁽³⁾	T _A = 85°C POWER RATING (mW) ⁽³⁾	T _B = 85°C POWER RATING (mW) ^{(2) (3)}
SOIC-8 (D)	165	55	606	242	730
PDIP-8 (P)	110	37	909	364	1080

- (1) Tested per JEDEC EIA/JESD51-1. Thermal resistance is a function of board construction and layout. Air flow reduces thermal resistance. This number is included only as a general guideline; see TI document ([SPRA953](#)) IC Package Thermal Metrics.
- (2) Thermal resistance to the circuit board is lower. Measured with standard single-sided PCB construction. Board temperature, T_B, measured approximately 1 cm from the lead to board interface. This number is provided only as a general guideline.
- (3) Maximum junction temperature, T_J, equal to 125°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, all voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$. Components reference, 图 1.

		MIN	MAX	UNIT	
VDD	Input voltage	9	20	V	
VGG	Input voltage from low-impedance source	9	13		
I _{VGG}	Input current from a high impedance source	10	2000	μA	
R _{MOT}	Resistor to GND	Shutdown/Retry mode	25	100	kΩ
		Latch-off mode	150	750	
R _{CL}	Resistor to GND	24.3	100		
R _{ZCD1}	Resistor to auxiliary winding	50	200		
C _{VGG}	VGG capacitor	33	200	nF	
C _{BP}	VDD bypass capacitor, ceramic	0.1	1	μF	

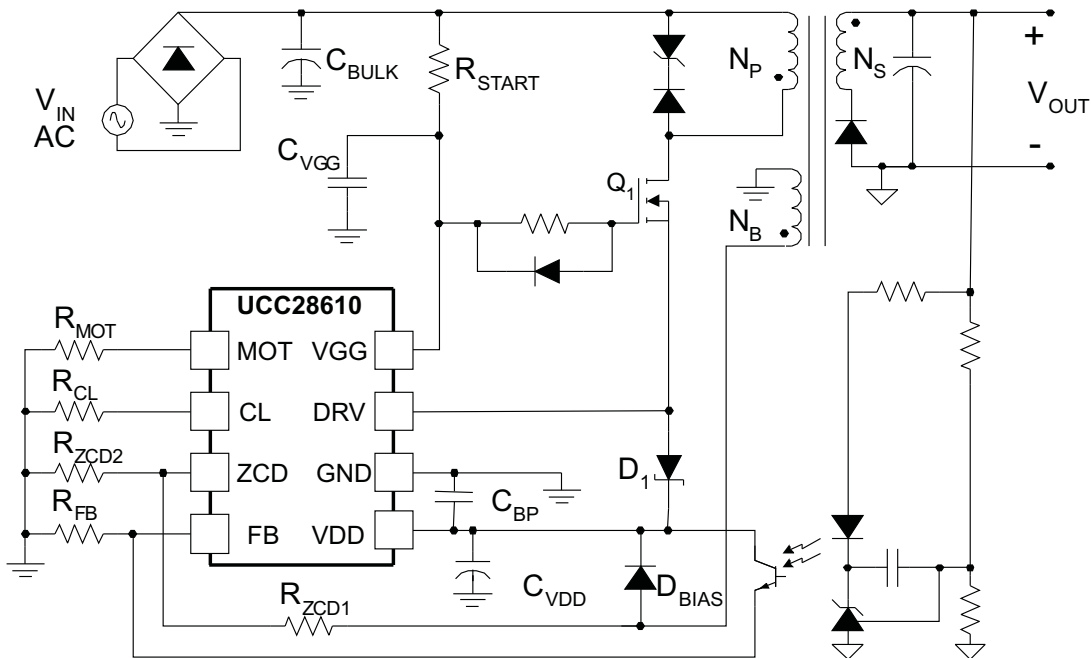


图 1. Recommended Operating Conditions Application

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

over operating free-air temperature range (unless otherwise noted)

	MAX	UNIT
ESD Rating, Human Body Model (HBM)	2	kV
ESD Rating, Charged Device Model (CDM)	500	V

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: VDD = 12 V, VGG=12 V, ZCD = 1 V, FB = 0 V, GND = 0 V, a 0.1- μ F capacitor between VDD and GND, a 0.1- μ F capacitor between VGG and GND, R_{CL} = 33.2 k Ω , R_{MOT} = 380 k Ω , -40°C < T_A < +125°C, T_J = T_A

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS			
VDD and VGG SUPPLY								
VGG _(OPERATING)	VGG voltage, operating	VDD = 14 V, I _{VGG} = 2.0 mA			13	14	15	V
VGG _(DISABLED)	VGG voltage, PWM disabled	VDD = 12 V, I _{VGG} = 15 μ A, I _{FB} = 350 μ A			15	16	17	
Δ VGG	Rise in VGG clamping voltage during UVLO, GM, or Fault	VGG _(DISABLED) – VGG _(OPERATING)			1.75	2.00	2.15	
I _{VGG(SREG)}	VGG shunt regulator current	VGG = VGG _(DISABLED) – 100 mV, VDD = 12 V				6	10	μ A
Δ VGG _(SREG)	VGG shunt load regulation	10 μ A \leq I _{VGG} \leq 5 mA, I _{FB} = 350 μ A				125	200	mV
VGG _(LREG)	VGG LDO regulation voltage	VDD = 20 V, I _{VGG} = – 2 mA				13		
VGG _(LREG, DO)	VGG LDO Dropout Voltage	VDD – VGG, VDD = 11 V, I _{VGG} = – 2 mA			1.5	2	2.5	V
VDD _(ON)	UVLO turn-on threshold		9.7	10.2	10.7			
VDD _(OFF)	UVLO turn-off threshold		7.55	8	8.5			
Δ VDD _(UVLO)	UVLO hysteresis		1.9	2.2	2.5			
I _{VDD(OPERATING)}	Operating current	VDD = 20 V			2.5	3	3.7	mA
I _{VDD(GM)}	Idle current between bursts	I _{FB} = 350 μ A				550	900	μ A
I _{VDD(UVLO)}	Current for VDD < UVLO	VDD = VDD _(ON) – 100 mV, increasing				225	310	
R _{DS,ON(VDD)}	VDD Switch on resistance, DRV to VDD	VGG = 12 V, VDD = 7V, I _{DRV} = 50 mA				4	10	Ω
VDD _(FAULT RESET)	VDD for fault latch reset		5.6	6	6.4	V		
MODULATION								
t _{S(HF)} ⁽¹⁾	Minimum switching period, frequency modulation (FM) mode	I _{FB} = 0 μ A, ⁽¹⁾			7.125	7.5	7.875	μ s
t _{S(LF)} ⁽¹⁾	Maximum switching period, reached at end of FM modulation range	I _{FB} = I _{FB, CNR3} – 20 μ A, ⁽¹⁾			31	34	38	
I _{DRVpk(max)}	Maximum peak driver current over amplitude modulation(AM) range	I _{FB} = 0 μ A, R _{CL} = 33.2 k Ω			2.85	3	3.15	A
		I _{FB} = 0 μ A, R _{CL} = 100 k Ω			0.80	0.90	1.0	
I _{DRVpk(min)}	Minimum peak driver current reached at end of AM modulation range	I _{FB, CNR2} + 10 μ A, R _{CL} = 33.2 k Ω			0.7	0.85	1.1	A
		I _{FB, CNR2} + 10 μ A, R _{CL} = 100 k Ω			0.2	0.33	0.5	
K _P	Maximum power constant	For I _{DRVpk(max)} = 3 A			0.54	0.60	0.66	W/ μ H
I _{DRVpk(absmin)}	Minimum peak driver independent of R _{CL} or AM control	R _{CL} = OPEN			0.3	0.45	0.6	A
t _{BLANK(Ilim)}	Leading edge current limit blanking time	I _{FB} = 0 μ A, R _{CL} = 100 k Ω , 1.2-A pull-up on DRV			120	220	450	ns
V _{CL}	Voltage of CL pin	I _{FB} = 0 μ A			2.94	3	3.06	V
		I _{FB} = (I _{FB, CNR3} – 20 μ A) ⁽¹⁾			0.95	1	1.05	
I _{FB, CNR1} ⁽²⁾	I _{FB} range for FM modulation	I _{FB} increasing, t _S = t _{S(LF)} , I _{DRVpk} = I _{DRVpk(max)}			145	165	195	μ A
I _{FB, CNR2} – I _{FB, CNR1} ⁽²⁾	I _{FB} range for AM modulation	t _S = t _{S(LF)} , I _{DRVpk} ranges from I _{DRVpk(max)} to I _{DRVpk(min)}			35	45	65	
I _{FB, CNR3} – I _{FB, CNR2} ⁽²⁾	I _{FB} range for Green Mode (GM) modulation	I _{FB} increasing until PWM action is disabled entering a burst-off state			50	70	90	
I _{FB, GM-HYST} ⁽²⁾	I _{FB} hysteresis during GM modulation to enter burst on and off states	I _{FB} decreasing from above I _{FB, CNR3}			10	25	40	
V _{FB}	Voltage of FB pin	I _{FB} = 10 μ A			0.34	0.7	0.84	V

(1) t_S sets a minimum switching period. Following the starting edge of a PWM on time, under normal conditions, the next on time is initiated following the first zero crossing at ZCD after t_S. The value of t_S is modulated by I_{FB} between a minimum of t_{S(HF)} and a maximum of t_{S(LF)}. In normal operation, t_{S(HF)} sets the maximum operating frequency of the power supply and t_{S(LF)} sets the minimum operating frequency of the power supply.

(2) Refer to [Figure 2](#).

ELECTRICAL CHARACTERISTICS (接下页)

Unless otherwise stated: VDD = 12 V, VGG=12 V, ZCD = 1 V, FB = 0 V, GND = 0 V, a 0.1-μF capacitor between VDD and GND, a 0.1-μF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, -40°C < T_A < +125°C, T_J = T_A

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ZERO CROSSING DETECTION						
ZCD _(TH)	ZCD zero crossing threshold	ZCD high to low generates switching period (t _S has expired)	5	20	50	mV
ZCD _(CLAMP)	ZCD low clamp voltage	I _{ZCD} = -10 μA	-200	-160	-100	mV
ZCD _(START)	ZCD voltage threshold to enable the internal start timer	Driver switching periods generated at start timer rate	0.1	0.15	0.2	V
t _{DLY(ZCD)}	Delay from zero crossing to Driver turn-on	150-Ω pull-up to 12-V on DRV		150		ns
t _{WAIT(ZCD)}	Wait time for zero crossing detection	Driver turn-on edge generated following t _S with previous zero crossing detected	2	2.4	2.8	μs
t _{ST}	Starter time-out period	ZCD = 0 V	150	240	300	
DRIVER						
R _{DS(on)(DRV)}	Driver on-resistance	I _{DRV} = 4.0 A		90	190	mΩ
I _{DRV(OFF)}	Driver off-leakage current	DRV = 12 V		1.5	20	μA
R _{DS(on)(HSDRV)}	High-side driver on-resistance	I _{DRV} = -50 mA		6	11	Ω
I _{DRV(DSCH)}	DRV bulk discharge current	VDD open, DRV= 12 V, Fault latch set	2	2.8	3.6	mA
OVERVOLTAGE FAULT						
ZCD _(OVP)	Overvoltage fault threshold at ZCD	Fault latch set	4.85	5	5.15	V
t _{BLANK(OVP)}	ZCD blanking and OVP sample time from the turn-off edge of DRV		0.6	1	1.7	μs
I _{ZCD(bias)}	ZCD Input bias current	ZCD = 5 V	-0.1	-0.05	0.1	μA
OVERLOAD FAULT						
I _{FB(OL)}	Current to trigger overload delay timer		0	1.5	3	μA
t _{OL}	Delay to overload fault	I _{FB} = 0 A continuously	200	250	325	
t _{RETRY}	Retry delay in retry mode or after shutdown command	R _{MOT} = 76 kΩ		750		ms
R _{MOT(TH)}	Boundary R _{MOT} between latch-off and retry modes	See ⁽³⁾	100	120	150	
SHUTDOWN THRESHOLD						
MOT _(SR)	Shutdown-Retry threshold	MOT high to low	0.7	1	1.3	V
I _{MOT}	MOT current when MOT is pulled low	MOT = 1 V	-600	-450	-300	μA
MAXIMUM ON TIME						
t _{MOT}	Latch-OFF	R _{MOT} = 383 kΩ	3.43	3.83	4.23	μs
	Shutdown-retry	R _{MOT} = 76 kΩ	3.4	3.8	4.2	
MOT	MOT voltage		2.7	3	3.3	V
THERMAL SHUTDOWN						
T _{SD} ⁽⁴⁾	Shutdown temperature	T _J , temperature rising ⁽⁴⁾		165		°C
T _{SD_HYS} ⁽⁴⁾	Hysteresis	T _J ⁽⁴⁾ , temperature falling, degrees below T _{SD}		15		

(3) A latch-off or a shutdown and retry fault response to a sustained overload is selected by the range of R_{MOT}.

To select the latch-off mode, R_{MOT} should be greater than 150 kΩ and t_{MOT} is given by R_{MOT} × (1.0 × 10⁻¹¹).

To select the shutdown-retry mode, R_{MOT} should be less than 100 kΩ and t_{MOT} is given by R_{MOT} × (5.0 × 10⁻¹¹).

(4) Thermal shutdown occurs at temperatures higher than the normal operating range. Device performance at or near thermal shutdown temperature is not specified or assured.

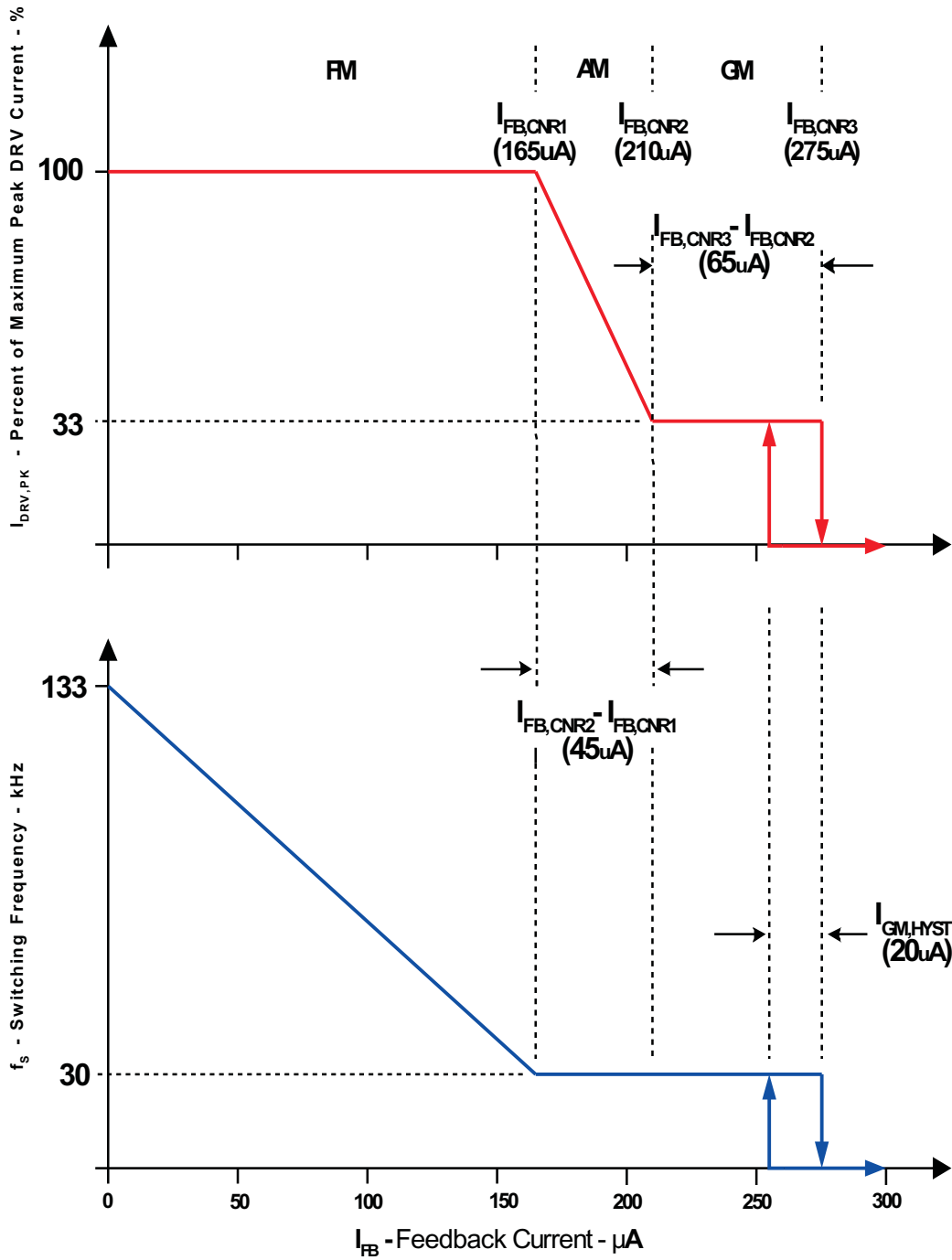
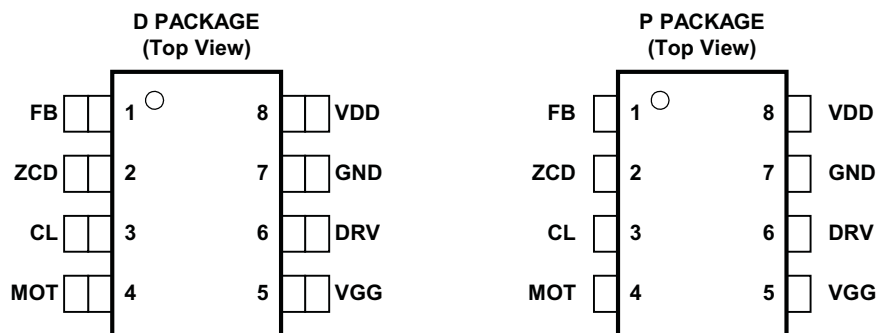


图 2. FB Electrical Condition Detail

DEVICE INFORMATION
PIN CONFIGURATION

PIN DESCRIPTIONS

NAME	PIN	I/O	DESCRIPTION
CL	3	I	(Current Limit) This pin programs the peak primary inductor current that is reached each switching cycle. Program with a resistor between CL and GND.
DRV	6	O	(DRiVe) This pin drives the source of an external high voltage power MOSFET. The DRV pin carries the full primary current of the converter. Connect a Schottky diode between DRV and VDD to provide initial bias at start up.
FB	1	I	(FeedBack) The FB current, I_{FB} , commands the operating mode of the UCC28610. The FB voltage is always 0.7 V. This pin only detects current.
GND	7	—	(Ground) This pin is the current return terminal for both the analog and power signals in the UCC28610. This terminal carries the full primary current of the converter. Separate the return path of the bulk capacitor from the return path of FB, ZCD, MOT, and CL.
MOT	4	I	(Maximum On Time) This pin has three functions: <ol style="list-style-type: none"> MOT programs the allowed maximum on-time, t_{MOT}, of the internal driver. MOT programs the converter's reaction to overload and power input under-voltage conditions with either a shutdown/retry response or a latch-off response. MOT can be used to externally shut down the power supply by pulling MOT to GND. When the pin is released, the converter will start after a restart delay, t_{RETRY}. Functions 1 and 2 are programmed with a resistor between MOT and GND.
VDD	8	—	This is the bias supply pin for the UCC28610. It can be derived from an external source or an auxiliary winding. This pin must be decoupled with a 0.1- μ F ceramic capacitor placed between VDD and GND, as close to the device as possible.
VGG	5	—	This pin provides a DC voltage for the gate of the external high voltage MOSFET. This pin must be decoupled with a 0.1- μ F ceramic capacitor placed between VGG and GND, as close to the device as possible. This pin also initiates start-up bias through a large value resistor that is connected to the input bulk voltage.
ZCD	2	I	(Zero Current Detection) This pin has two functions: <ol style="list-style-type: none"> ZCD senses the transformer reset based on a valid zero current detection signal. ZCD programs the output Over Voltage Protection (OVP) feature using a resistive divider on the primary side bias winding of the Flyback transformer.

TYPICAL CHARACTERISTICS

Unless otherwise stated: VDD = 12V, VGG = 12V, ZCD = 1 V, FB = 0 V, GND = 0 V, a 0.1-μF capacitor between VDD and GND, a 0.1-μF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, -40°C < T_A < +125°C, T_J = T_A

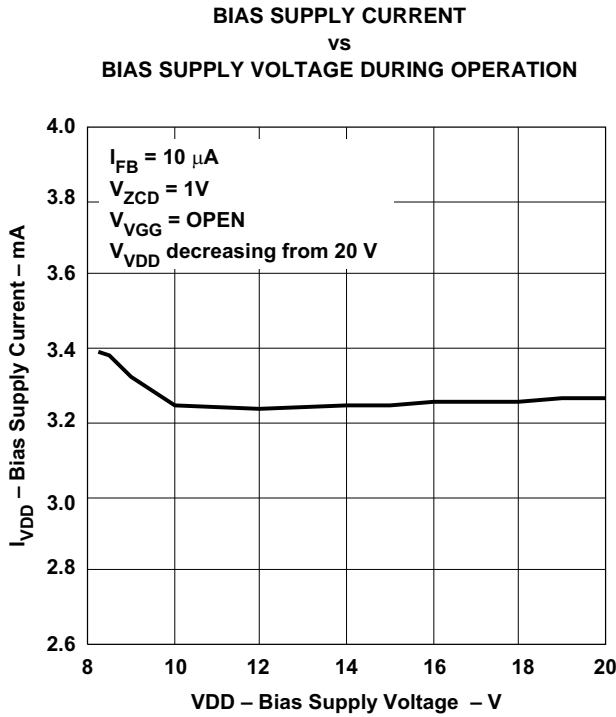


图 3.

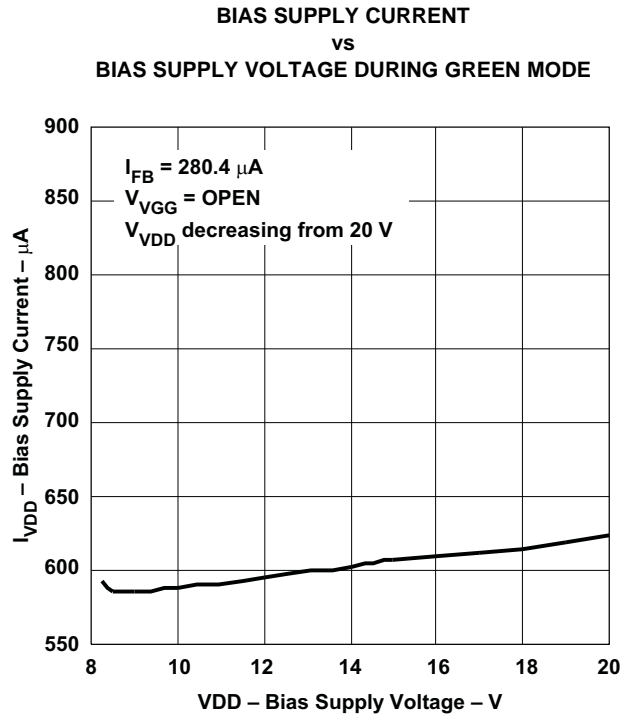


图 4.

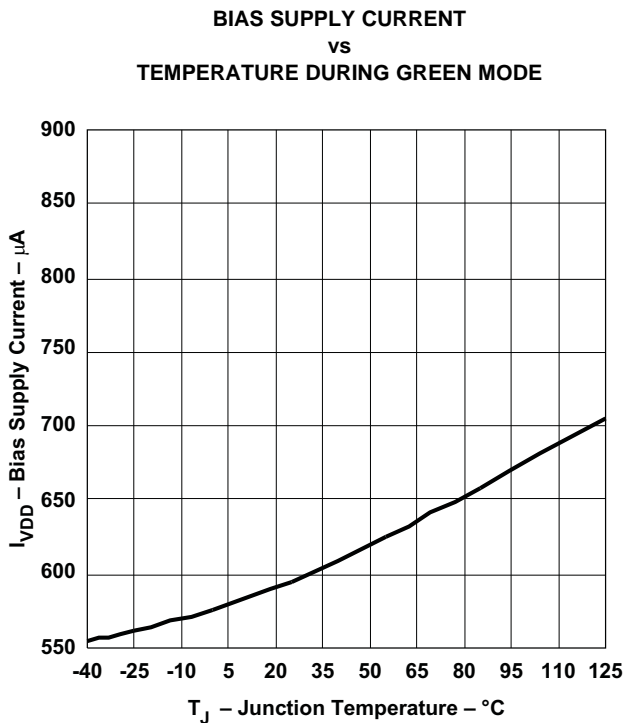


图 5.

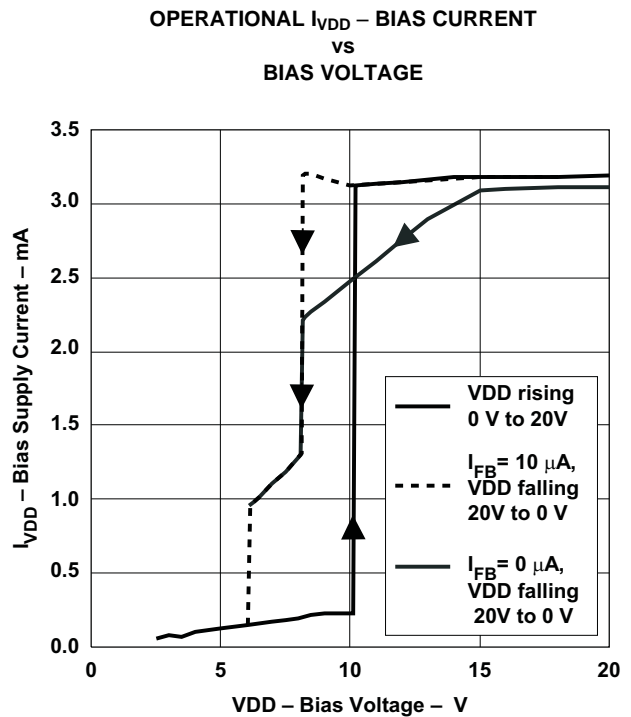


图 6.

TYPICAL CHARACTERISTICS (接下页)

Unless otherwise stated: VDD = 12V, VGG = 12V, ZCD = 1 V, FB = 0 V, GND = 0 V, a 0.1- μ F capacitor between VDD and GND, a 0.1- μ F capacitor between VGG and GND, R_{CL} = 33.2 k Ω , R_{MOT} = 380 k Ω , -40°C < T_A < +125°C, T_J = T_A

OSCILLATOR FREQUENCY

vs
FEEDBACK CURRENT

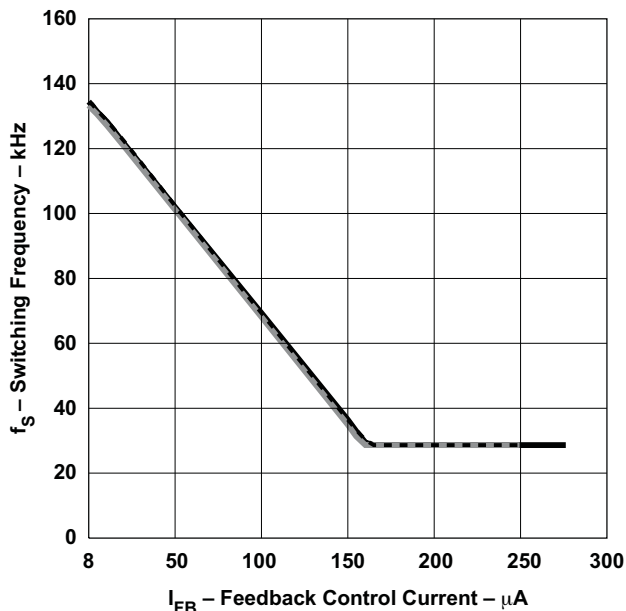


图 7.

MINIMUM SWITCHING PERIOD

vs
TEMPERATURE

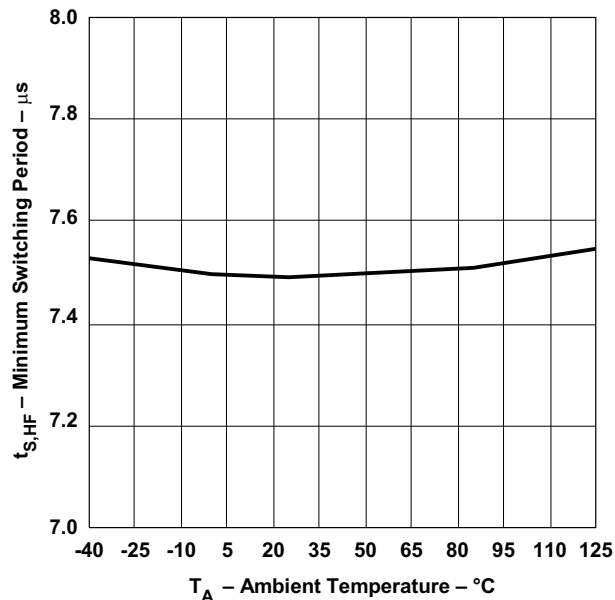


图 8.

SWITCHING PERIOD DURING AMPLITUDE MODULATION

vs
AMBIENT TEMPERATURE

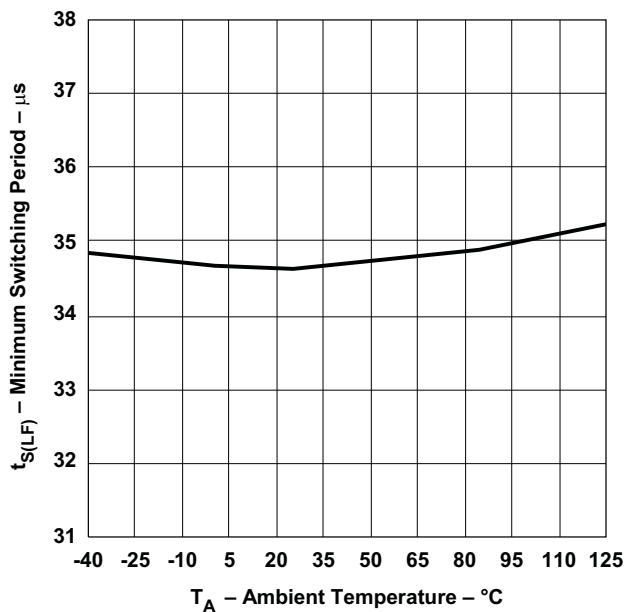


图 9.

PEAK DRV CURRENT

vs
FEEDBACK CURRENT

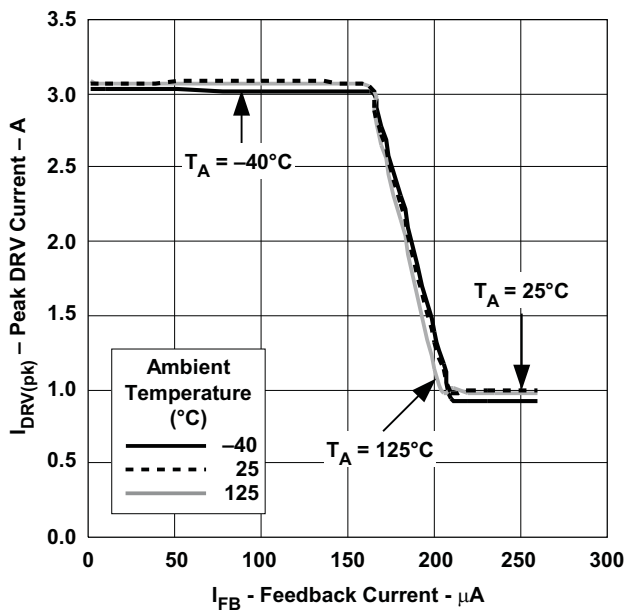


图 10.

TYPICAL CHARACTERISTICS (接下页)

Unless otherwise stated: VDD = 12V, VGG = 12V, ZCD = 1 V, FB = 0 V, GND = 0 V, a 0.1-μF capacitor between VDD and GND, a 0.1-μF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, -40°C < T_A < +125°C, T_J = T_A

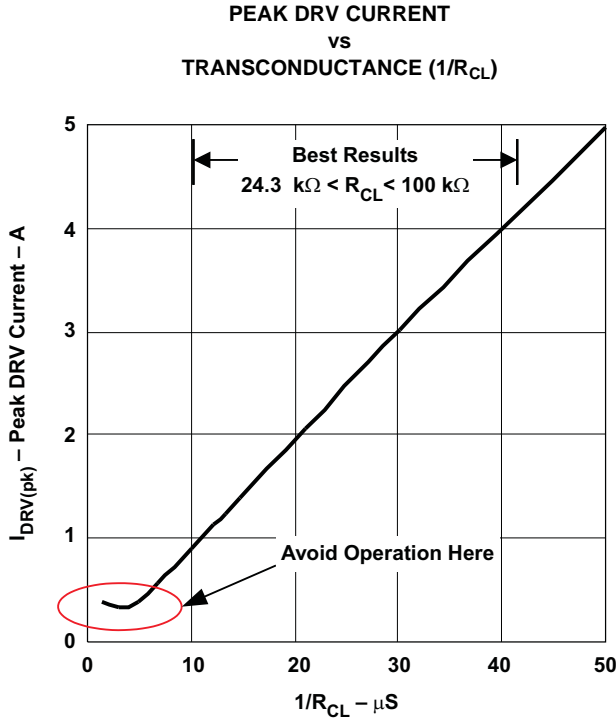


图 11.

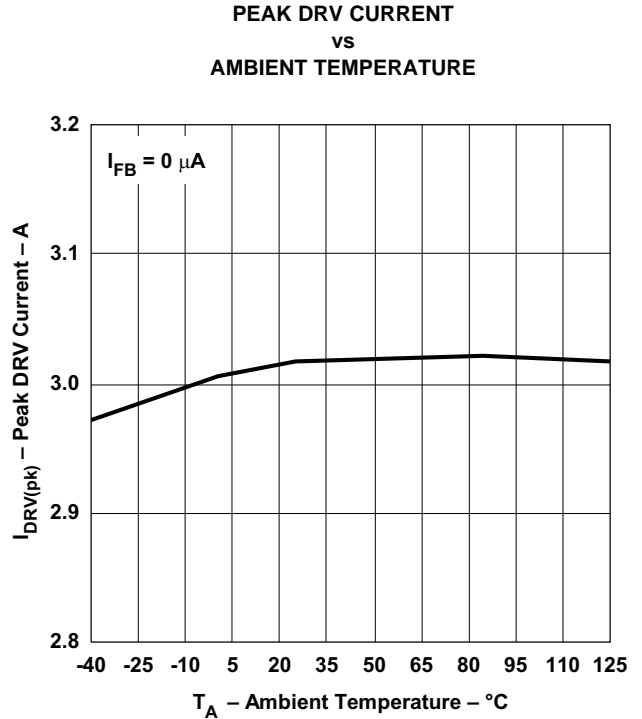


图 12.

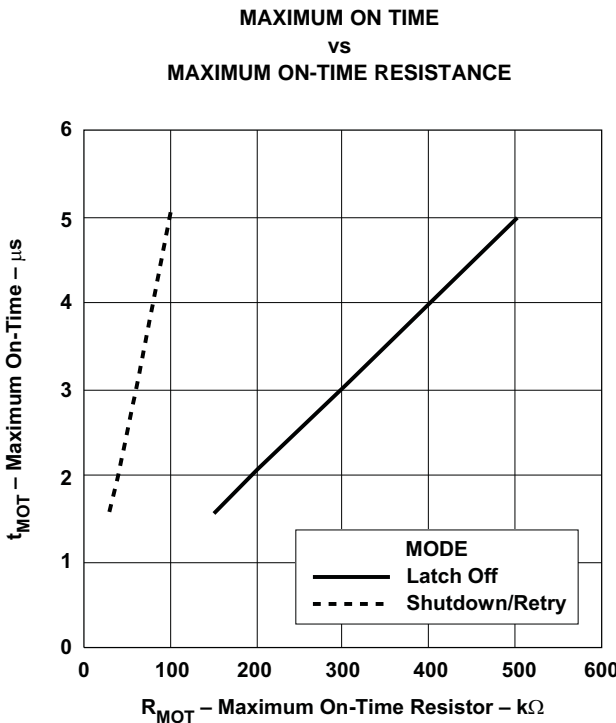


图 13.

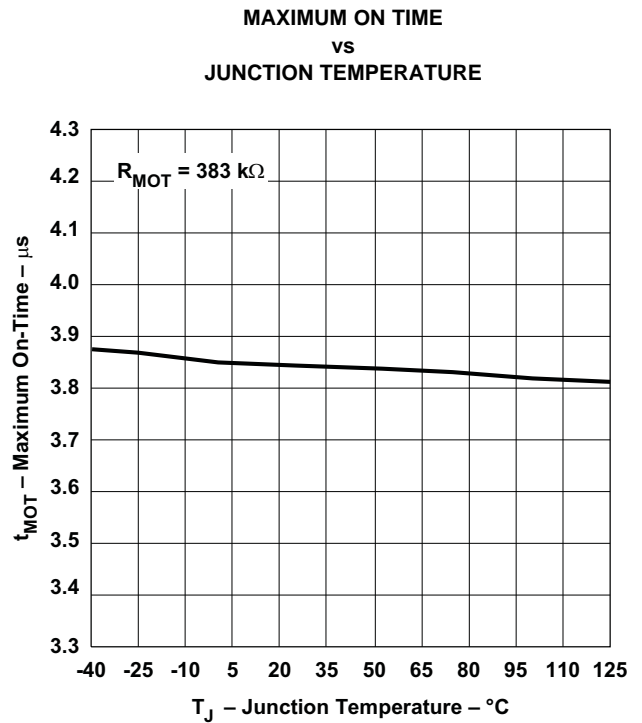


图 14.

TYPICAL CHARACTERISTICS (接下页)

Unless otherwise stated: VDD = 12V, VGG = 12V, ZCD = 1 V, FB = 0 V, GND = 0 V, a 0.1-μF capacitor between VDD and GND, a 0.1-μF capacitor between VGG and GND, R_{CL} = 33.2 kΩ, R_{MOT} = 380 kΩ, -40°C < T_A < +125°C, T_J = T_A

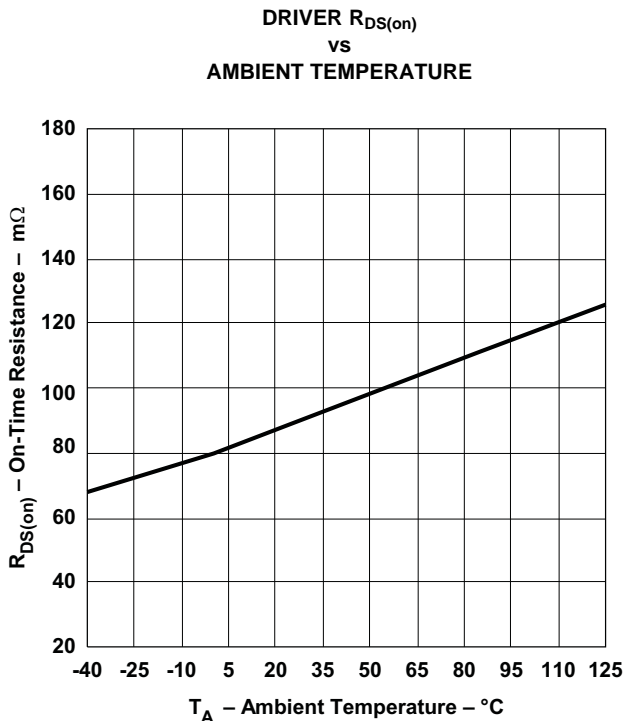


图 15.

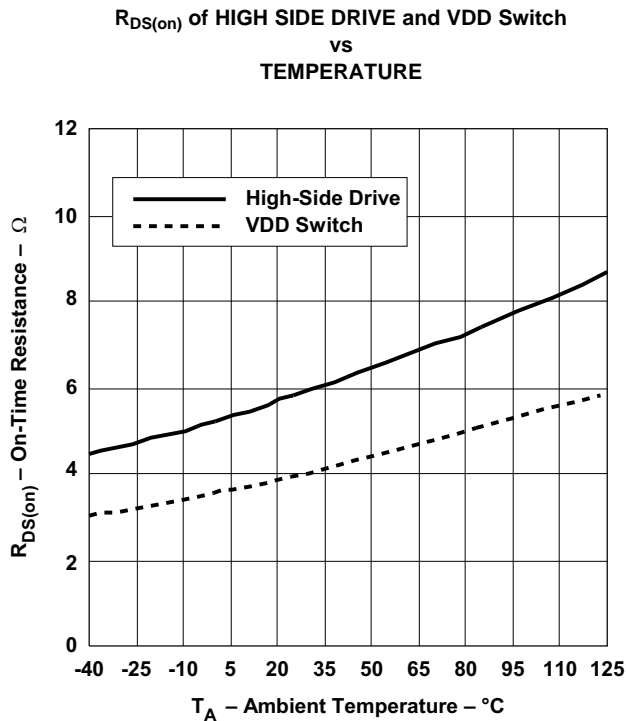


图 16.

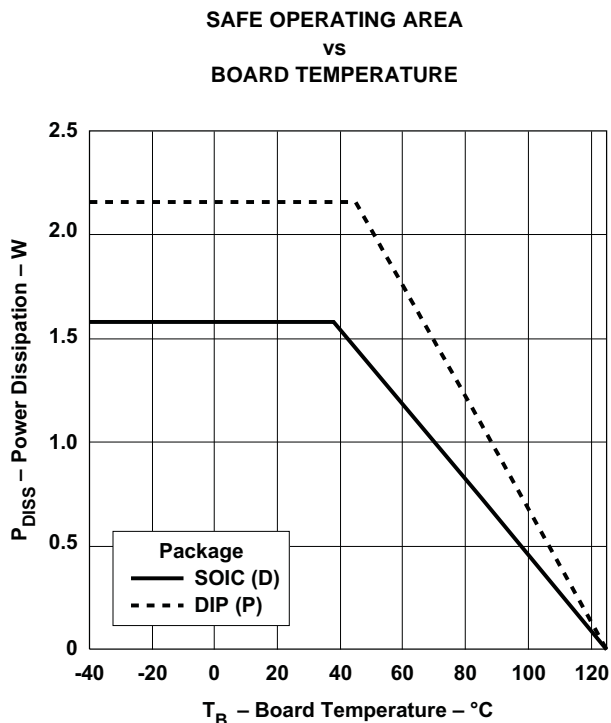


图 17.

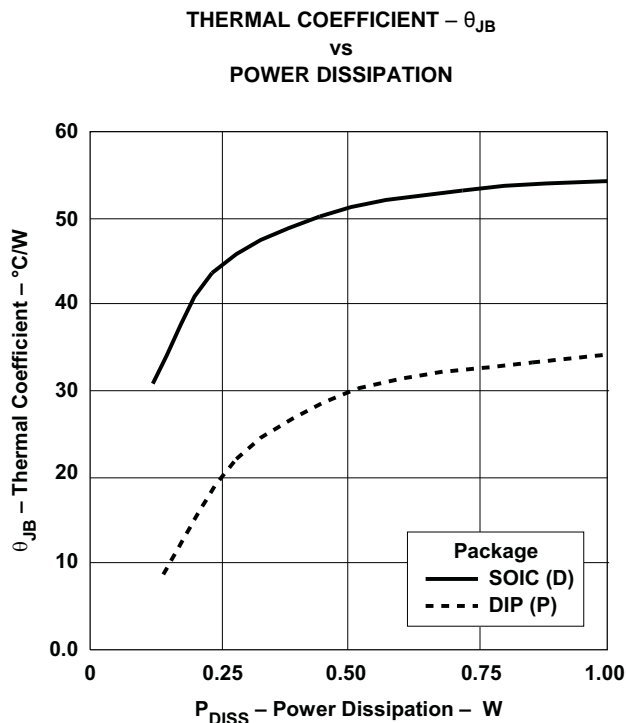


图 18.

Block Diagram

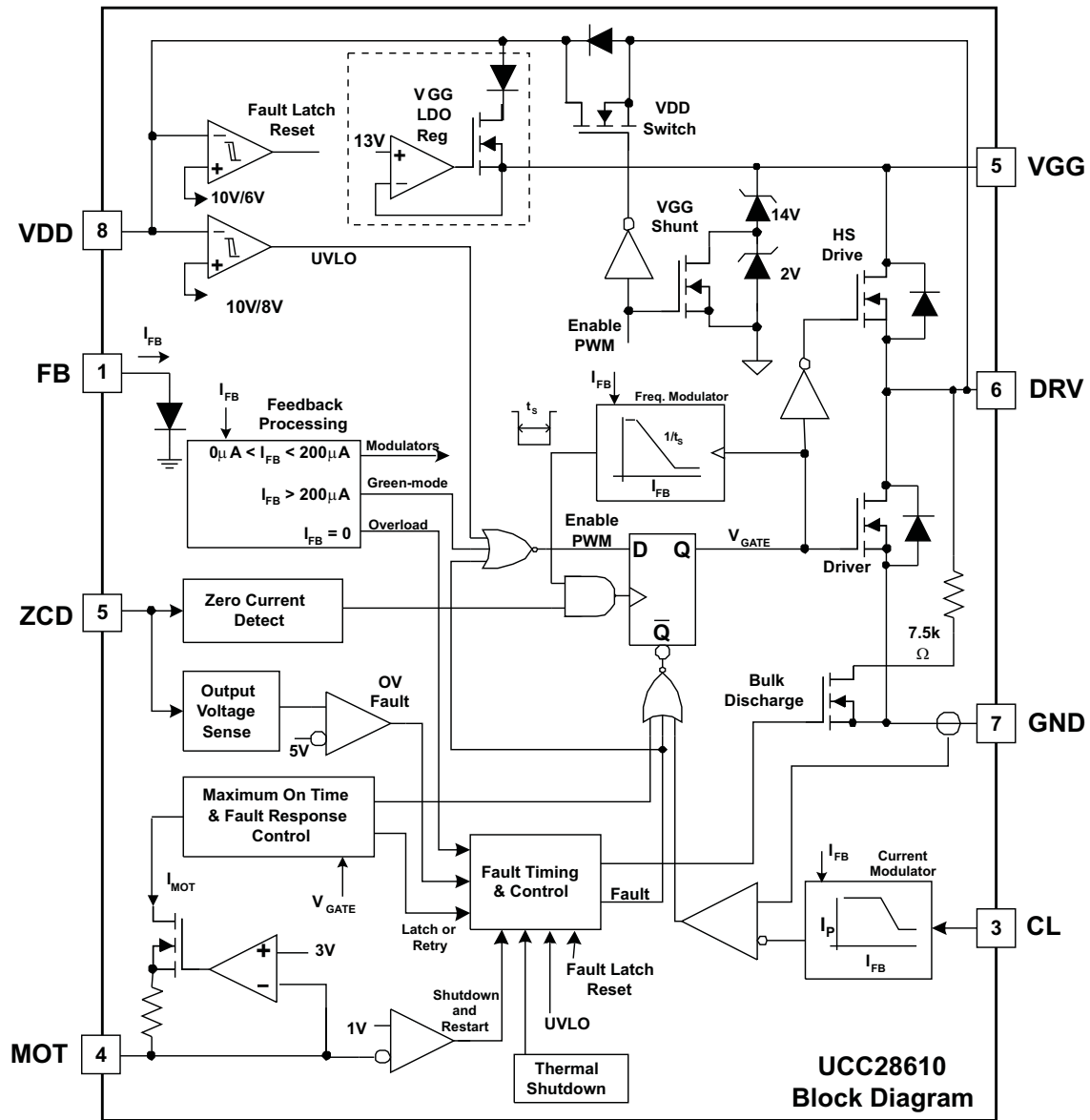


图 19. Simplified Block Diagram

APPLICATION INFORMATION

General Operation

The flyback converter is attractive for low power AC/DC applications because it provides output isolation and wide input operating abilities using a minimum number of components. Operation of the flyback converter in Discontinuous Conduction Mode (DCM) is especially attractive because it eliminates reverse recovery losses in the output rectifier and it simplifies control.

The UCC28610 is a flyback controller for 12-W to 65-W, peak AC/DC power supply applications that require both low AC line power during no-load operation and high average efficiency. This controller limits the converter to DCM operation. It does not allow Continuous Conduction Mode (CCM) operation. Forced DCM operation results in a uniquely safe current limit characteristic that is insensitive to AC line variations. The peak current mode modulator does not need slope compensation because the converter operates in DCM.

The operation of the UCC28610 is facilitated by driving the external high voltage MOSFET through the source. This configuration is called a cascode driver. It features fast start-up and low input power under no-load conditions without having high voltage connections to the control device. The cascode driver has no effect on the general operation of the flyback converter.

The feedback pin uses current rather than voltage. This unique feature minimizes primary side power consumption during no-load operation by avoiding external resistive conversion from opto-coupler current to voltage.

Average efficiency is optimized by the UCC28610 between peak power and 22% peak power with constant peak current, variable off-time modulation. This modulation tends to make the efficiency constant between 22% and 100% peak load, eliminating the need to over-design to meet average efficiency levels that are required by EnergyStar™.

Transformer Selection

To begin a power supply design, the power supply designer needs to know the peak power to be delivered by the converter, the input voltage range, the output voltage, and an estimate of the maximum allowable bulk voltage ripple. Select the maximum allowable stress voltage for the external power MOSFET. The stress voltage, V_{DS} , determines the reflected secondary voltage that resets the flyback transformer and the turn ratio between primary and secondary. A simplified diagram of the converter and its waveforms are shown in 图 20.

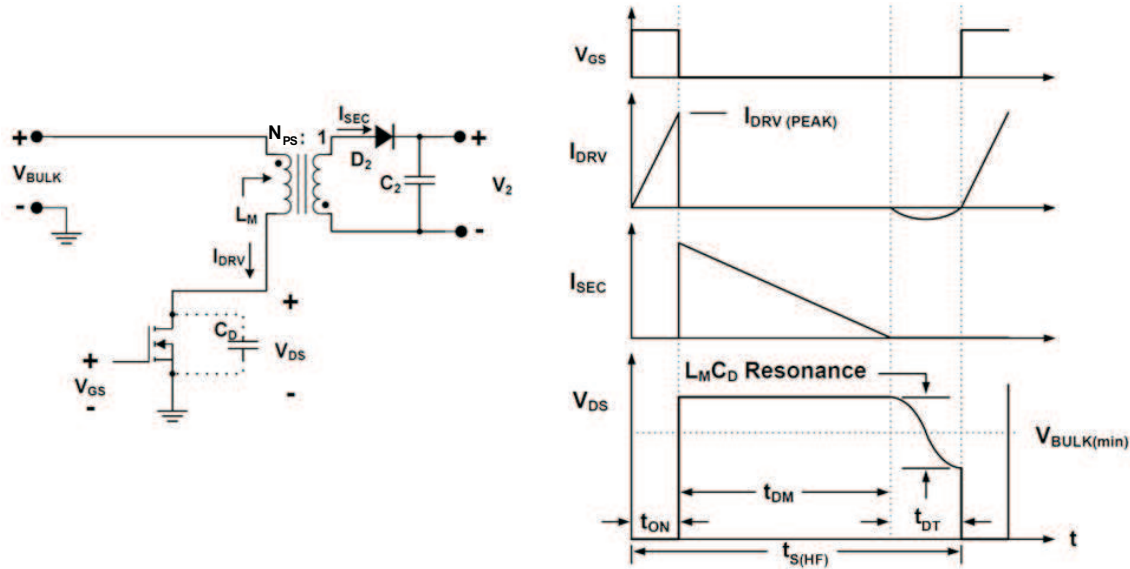


图 20. Basic Flyback Converter and Waveforms at Peak Load and Minimum V_{BULK} Voltage

Peak power is the maximum power level that must be regulated by the converter control system. Loads that last longer than the control loop time constant (100 μ s - 300 μ s) are directly considered “peak power”. Loads lasting less than the control loop time constant can be averaged over the control loop time constant.

The minimum switching period is when the converter is operating in the Frequency Modulation (FM) mode, referred to as $t_{S(HF)}$. This switching period must equal the sum of the switching intervals at minimum input voltage, maximum load, as shown in 图 20 and described in 公式 1. The switching intervals are t_{ON} , the conduction time of the MOSFET; t_{DM} the demagnetization time of the transformer and t_{DT} , the duration of the deadtime, equal to half of the resonant cycle, after the transformer is de-energized.

$$t_{S(HF)} = t_{ON} + t_{DM} + t_{DT} \quad (1)$$

Solve for the primary to secondary turn ratio, N_{PS} , using the maximum allowable V_{DS} , the maximum input line voltage, the predicted voltage spike due to leakage inductance and the desired regulated output voltage of the converter, V_{OUT} .

$$N_{PS} = \frac{V_{DS} - \sqrt{2} V_{IN(max)} - V_{leakage_spike}}{V_{OUT}} \quad (2)$$

Assume a deadtime, t_{DT} , of 5% of the total minimum switching period to allow for variations in the output capacitance of the HVMOSFET and the leakage inductance value:

$$t_{DT} = 0.05 \times t_{S(HF)} \quad (3)$$

Using volt-seconds balance, set the volt-seconds on equal to the volt-seconds for demagnetizing and solve for the on-time:

$$V_{BULK(min)} \times t_{ON} = V_{OUT} \times N_{PS} \times t_{DM} \quad (4)$$

$$t_{DM} = t_{S(HF)} - t_{ON} - t_{DT} \quad (5)$$

$$t_{ON} = \frac{V_{OUT} \times N_{PS} \times (t_{S(HF)} - t_{DT})}{V_{BULK(min)} + (V_{OUT} \times N_{PS})} \quad (6)$$

The maximum input power, P_{IN} , to the converter, in addition to being equal to the output power divided by the overall efficiency, is always equal to:

$$P_{IN} = \frac{P_{OUT}}{\text{efficiency}} = \frac{(V_{BULK(min)} \times t_{ON})^2}{2 \times L_M \times t_{S(HF)}} \quad (7)$$

Solve for the primary inductance value:

$$L_M = \frac{(V_{BULK(min)} \times t_{ON})^2}{2 \times P_{IN} \times t_{S(HF)}} \quad (8)$$

This equation is an approximation of the primary inductance value that is the best choice to minimize the primary side RMS current. In the actual circuit, when the resonance and delay due to leakage inductance can be measured, the magnetizing inductance value may need to be iterated for optimized low voltage switching.

Select the CL resistor, R_{CL} , based upon the maximum power constant of the controller, K_P . The tolerance of L_M should be considered (such as 10% lower for a typical inductor) and the minimum value of L_M should be used to calculate the value of the CL resistor.

To avoid tripping the overload protection feature of the controller during the normal operating range, use the minimum value of K_P from the Electrical Characteristics Table:

$$R_{CL} = 33.2k\Omega \times \sqrt{\frac{K_P \times L_M}{P_{IN}}} \quad (9)$$

Once R_{CL} is selected, the peak DRV current is calculated using Equation 10:

$$I_{DRV(PK)} = \frac{100kV}{R_{CL}} \quad (10)$$

For high efficiency, the bias winding turn ratio, N_{PB} , should be designed to maintain the VDD voltage above the VGG clamp, which is equal to $VGG_{(DISABLED)}$, when the converter is in burst mode. If VDD discharges below this value, minus the threshold voltage of the HVMOSFET, the HVMOSFET will turn on and linearly supply the VDD current from the high voltage rail instead of from the bias windings. Adding a zener diode on VDD will protect VDD from exceeding its absolute maximum rating in the event of a spike due to excess leakage inductance.

Cascode Bias and Start-Up

The UCC28610 uses a cascode drive and bias to control the high voltage power MOSFET and provide initial bias at start-up. Thus, the external high voltage power MOSFET provides the start-up function in addition to the power switching function during converter operation. The cascode architecture utilizes a low voltage switch operating between ground and the source of a high voltage MOSFET (HVMOSFET) configured in a common gate configuration, as shown in 图 21. There are some key points to note.

1. The gate of the external HVMOSFET is held at a DC voltage.
2. The HVMOSFET is driven through the source, not the gate.
3. The entire primary winding current passes through the internal low voltage Driver MOSFET (both DRV and GND pins).

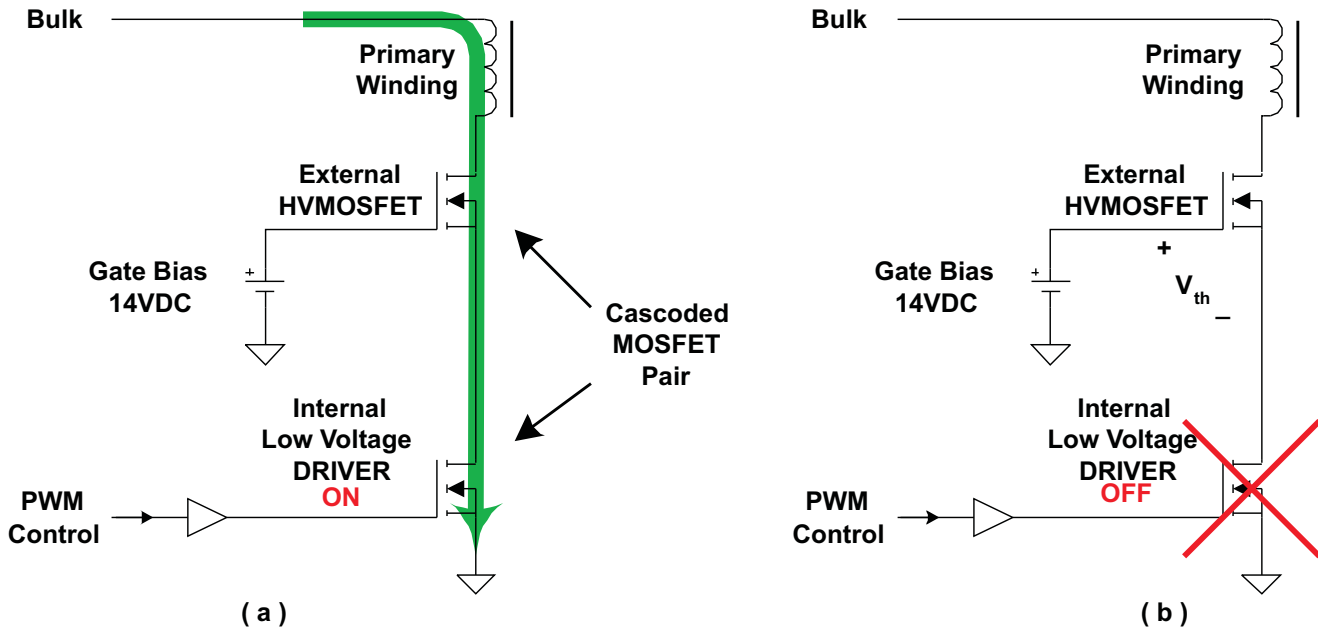


图 21. Cascoded Architecture

The UCC28610 integrates the low voltage switch in the form of a 90-mΩ FET along with all associated current sensing and drive. The HV MOSFET is forced to track the fast internal low voltage driver. The drain-gate charge in the HV MOSFET does not affect the turn-off speed because the gate is connected to a low impedance DC source. The cascode configuration results in very fast turn-off of the HV MOSFET, which keeps MOSFET switching losses low.

Cascode drive circuits are well known for high speed voltage gain. This topology can have small signal bandwidth over 100 MHz and it can exhibit high frequency ringing. High frequency ringing can cause EMI problems and become destructive in some situations. The sub-intervals during and immediately following the turn-on and turn-off transients are particularly susceptible to oscillation. For avoidance or solutions, see the application section, Solving High Frequency Ringing.

The cascode configuration permits a unique start-up sequence that is fast yet low-loss. Start-up bias uses a low level bleed current from either the AC line or the rectified and filtered AC line, or bulk voltage (via R_{START}) as shown in Figure 22. This current charges a small VGG capacitor, C_{VGG} , raising the HV MOSFET gate. The VGG pin will typically draw approximately 6 μA ($I_{VGG(SREG)}$) during this time, allowing the bulk bias current to be small and still charge the VGG capacitor. The HV MOSFET acts as a source follower once VGG reaches the threshold voltage of the HV MOSFET. Then, the HV MOSFET will bring up the DRV voltage as VGG continues to rise. During this time the UCC28610 is in UVLO and the Enable PWM signal is low. This turns on the VDD switch connecting VDD to DRV, allowing VDD to rise with the source of the HV MOSFET and charging C_{VDD} . An external Schottky diode, D1, is required between DRV and VDD. This diode passes potentially high switching currents that could otherwise flow through the body diode of the internal VDD Switch.

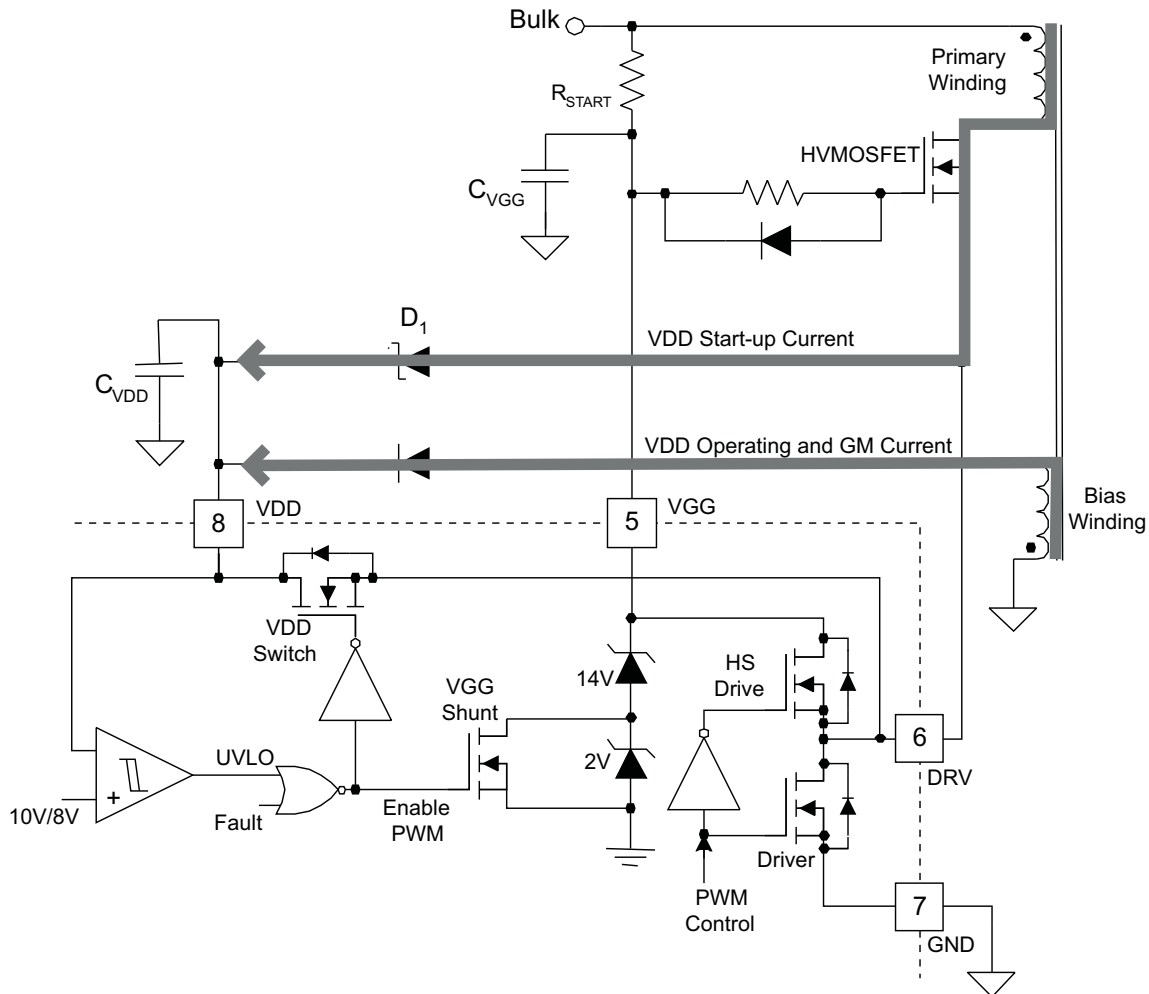


图 22. Start-Up Currents for the Cascode Architecture.

In order to achieve the lowest possible no-load power, select the number of turns in the bias winding so that VDD is higher than $16\text{ V} - V_{\text{TH}}$ of the HVMOSFET. A bias winding voltage between 17 V and 20 V usually achieves minimum loss. The bias winding often tracks the primary leakage inductance turn-off voltage spike. Place a 20-V Zener diode between VDD and GND in applications where heavy loads cause excessive VDD voltage.

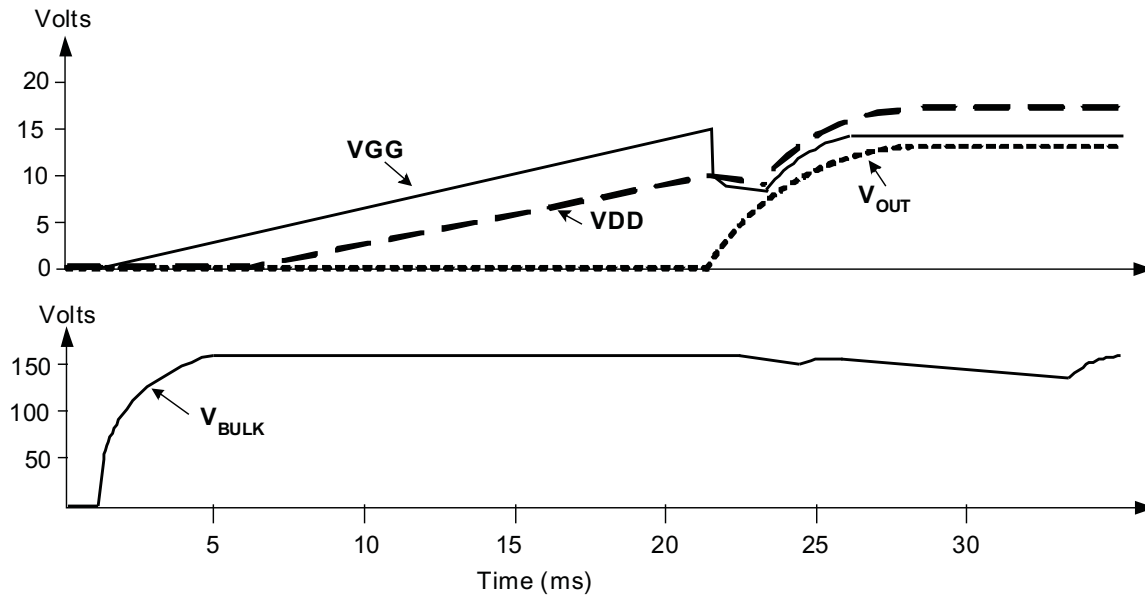


图 23. Typical Start-Up Waveforms for a 17-V Bias Winding Voltage

Typical start-up waveforms are shown in 图 23. As VGG rises, VDD will follow, minus the threshold voltage of the HVMOSFET. When VDD reaches approximately 10 V, the UCC28610 initiates switching. The bias supply current, I_{VDD} , rises to its operating level and it is supplied from the VDD capacitor. Start-up times can be kept under 200 ms by selecting the VGG capacitor in the range of 33 nF to 1000 nF and selecting R_{START} to have a current of 15 μA at the minimum AC line voltage. Select capacitor C_{VDD} to have enough capacitance to provide operating bias current to the controller for the time it takes the auxiliary winding to take over. No-load burst operation may impose a requirement for additional C_{VDD} capacitance.

The voltage on VGG is shunt regulated to 16 V whenever the PWM action is disabled. This is reduced to 14 V during switching to limit voltage stress on the gate of the external HVMOSFET. The external HVMOSFET should have a threshold voltage of less than 6 V in order to permit proper starting.

Feedback Function

Modulation and modes are controlled by applying current to the FB pin. The FB pin is usually used to feed back the output error signal to the modulator. The UCC28610 uses internal current mirrors to apply the FB current to the Feedback Processing block, and then to the Frequency Modulator and Current Modulator blocks. The voltage of the FB pin is a constant 0.7 V. AC filtering of the output of the opto-coupler must be applied to the emitter of the opto-coupler, as shown in 图 24. The corner frequency of the filter in 图 24 should be at least a decade above the maximum switching frequency of the converter, as given in 公式 11. A 100-kΩ resistor, R_{FB} , between the FB pin and GND prevents ground noise from resetting the overload timer by biasing the FB pin with a negative current. An opto-coupler with a low Current Transfer Ratio (CTR) often gives better no-load performance than a high CTR device due to the bias current of the secondary reference. The low CTR also offers better noise immunity than a high CTR device.

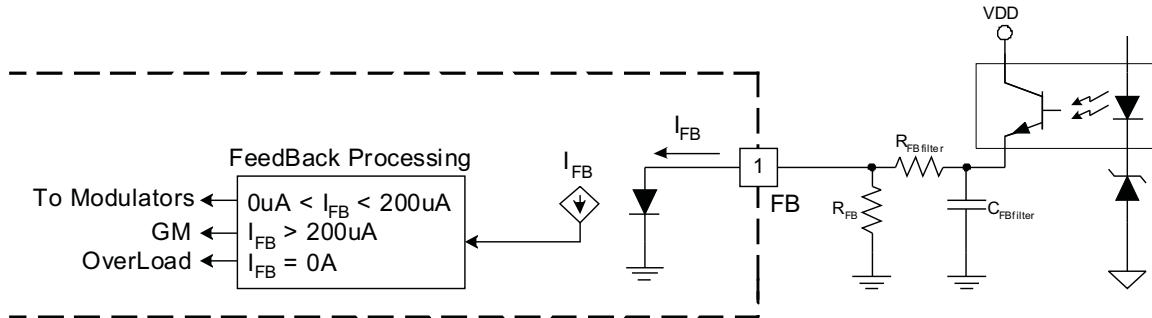


图 24. FB Details

$$f_{FB} = \frac{1}{2 \times \pi \times R_{FBfilter} \times C_{FBfilter}}$$

(11)

Modulation Modes

Under normal operating conditions, the FB current commands the operating mode of the UCC28610, as shown in 图 25 and 图 26. The FB current commands the UCC28610 to operate the converter in one of three modes: Frequency Modulation (FM) mode, Amplitude Modulation (AM) mode, and Green Mode (GM).

The converter operates in FM mode with a large power load (22% to 100% the peak regulated power). The peak HV MOSFET current reaches its maximum programmed value and FB current regulates the output voltage by varying the switching frequency, which is inversely proportional to t_s . The switching frequency is modulated from 30 kHz (22% peak power) to 133 kHz (100% peak power), the on time is constant, and the I_{DRV} peak current is constant. The maximum programmable HV MOSFET current, $I_{DRV,PK(max)}$, is set by a resistor on the CL pin, as described in 公式 10.

The converter operates in AM mode at moderate power levels (2.5% to 22% of the peak regulated power). The FB current regulates the output voltage by modulating the amplitude of the peak HV MOSFET current from 33% to 100% of the maximum programmed value while the switching frequency is fixed at approximately 30 kHz. The UCC28610 modulates the voltage on the CL pin from 3 V to 1 V to vary the commanded peak current, as shown in 图 25 and 图 26.

The converter operates in GM at light load (0% to 2.5% of the peak regulated power). The FB current regulates the output voltage in the Green Mode with hysteretic bursts of pulses using FB current thresholds. The peak HV MOSFET current is 33% of the maximum programmed value. The switching frequency within a burst of pulses is approximately 30 kHz. The duration between bursts is regulated by the power supply control dynamics and the FB hysteresis. The UCC28610 reduces internal bias power between bursts in order to conserve energy during light-load and no-load conditions.

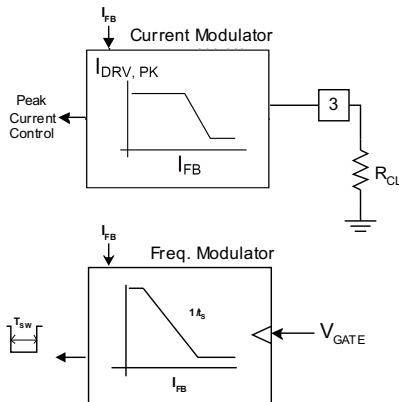


图 25. Modulation Control Blocks

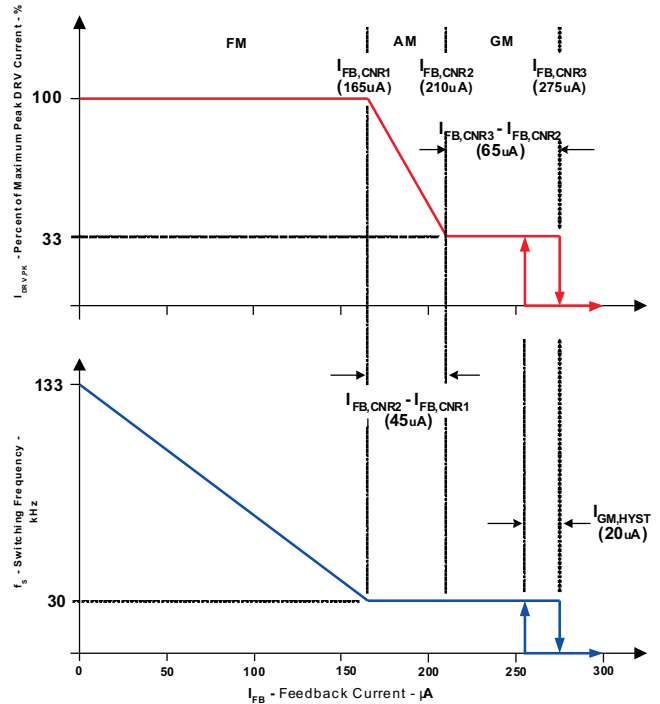


图 26. Control Diagram with Operating Modes

Primary Current Sense

The UCC28610 uses a current mirror technique to sense primary current in the Current Modulator. See [Figure 27](#) for details. All of the primary current passes into the DRV pin, through the Driver MOSFET and out of the GND pin. The Driver MOSFET current is scaled and reflected to the PWM Comparator where it is compared with the CL current. At the beginning of each switching cycle a blanking pulse, $t_{BLANK,(Ilim)}$, of approximately 220 ns is applied to the internal current limiter to allow the driver to turn on without false limiting on the leading edge capacitive discharge currents normally present in the circuit.

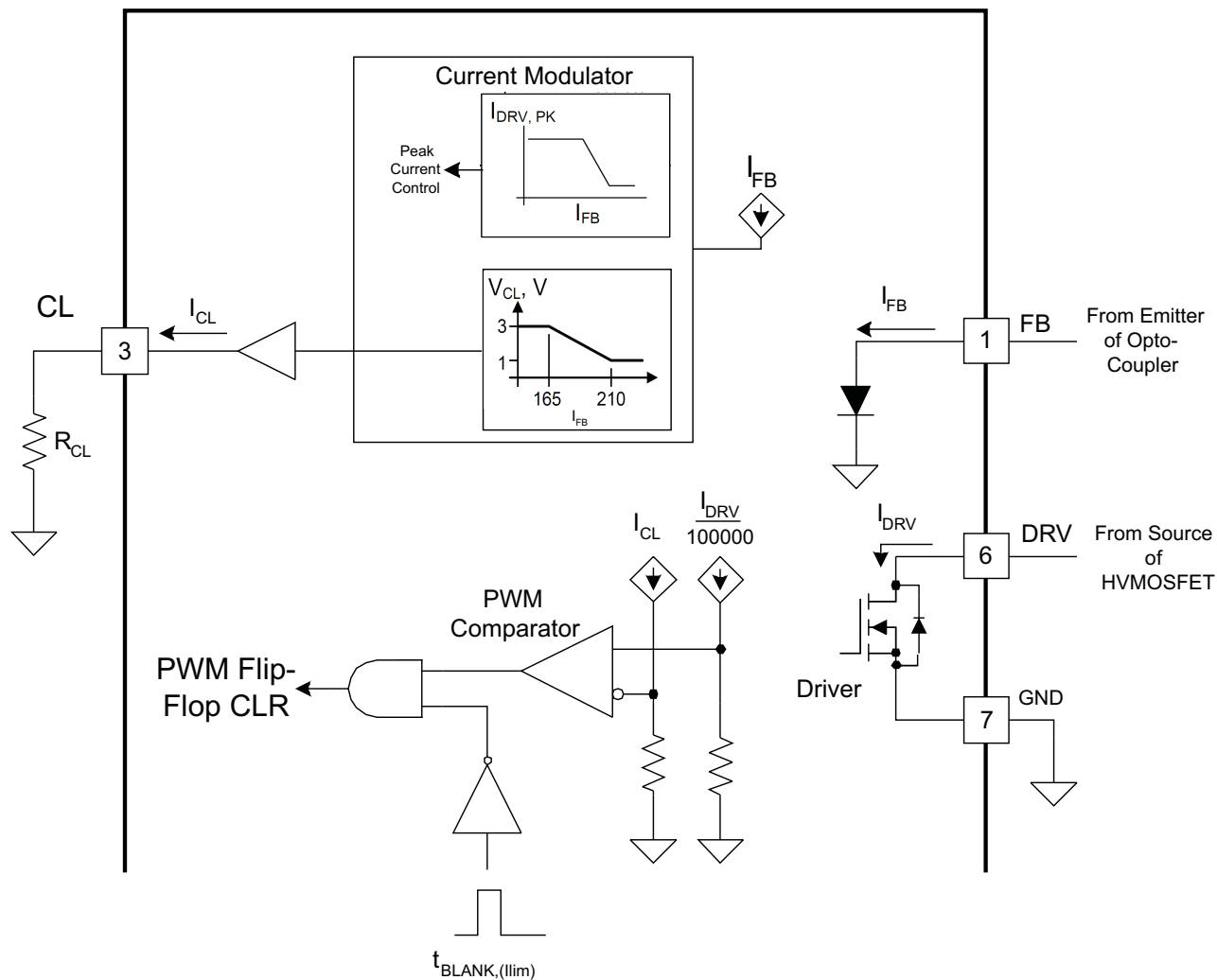


图 27. CL pin and DRV Current Sense

Zero Crossing Detection

The modulator requires three conditions in order to initiate the next switching cycle:

1. The time since the last turn-on edge must be equal to or greater than the time that is requested by the Feedback Processor as determined by the feedback current, I_{FB} .
2. The time since the last turn-on edge must be longer than the minimum period that is built into the UCC28610 (nominally $7.5 \mu\text{s}$ which equals 133 kHz).
3. Immediately following a high-to-low zero crossing of the ZCD voltage. Or, it has been longer than $t_{WAIT,ZCD}$ ($\sim 2.4 \mu\text{s}$) since the last zero crossing has been detected.

Every switching cycle is preceded by at least one zero crossing detection by the ZCD pin. The modulator allows the resonant ring to damp between pulses if the period needs to exceed the damping limit, allowing long pauses between pulses during no-load operation.

The switching frequency is not allowed to exceed 133 kHz (nominally). This sets the maximum power limit so that it will be constant for all bulk voltages that exceed the minimum line voltage value.

图 28 illustrates a set of switching cycle waveforms over a range of operating conditions. The UCC28610 is designed to always keep the inductor current discontinuous. This prevents current tailing during start-up or short circuit conditions and accommodates control of the maximum power delivered.

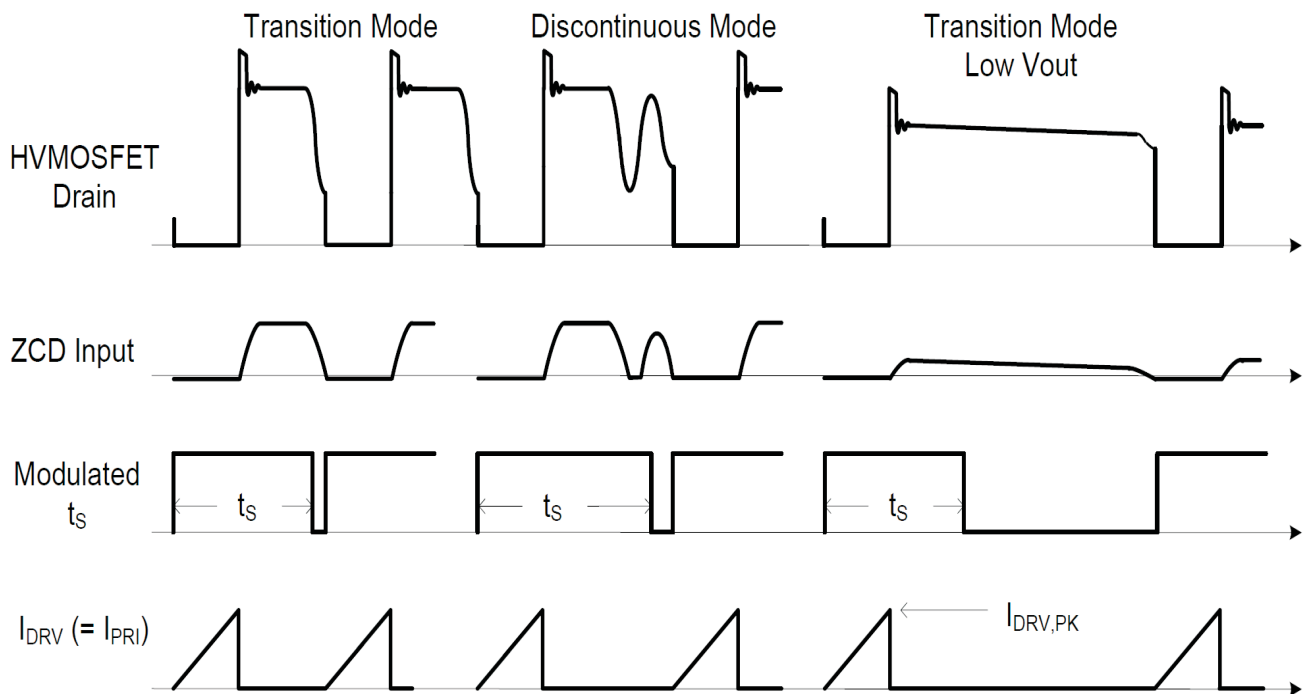


图 28. Switching Cycle Waveforms

Zero crossing is detected using a resistive divider across the bias winding, as shown in 图 29. The bias winding operates in phase with the output winding. The ZCD function detects transformer demagnetization when the ZCD voltage has a high to low crossing of the 20-mV ZCD threshold, ZCD_{TH} . The voltage at the ZCD pin is internally clamped to contain negative excursions at -160mV (ZCD_{CLAMP}). A small delay, 50 ns to 200 ns, can be added with C_{ZCD} to align the turn-on of the primary switch with the resonant valley of the primary winding waveform.

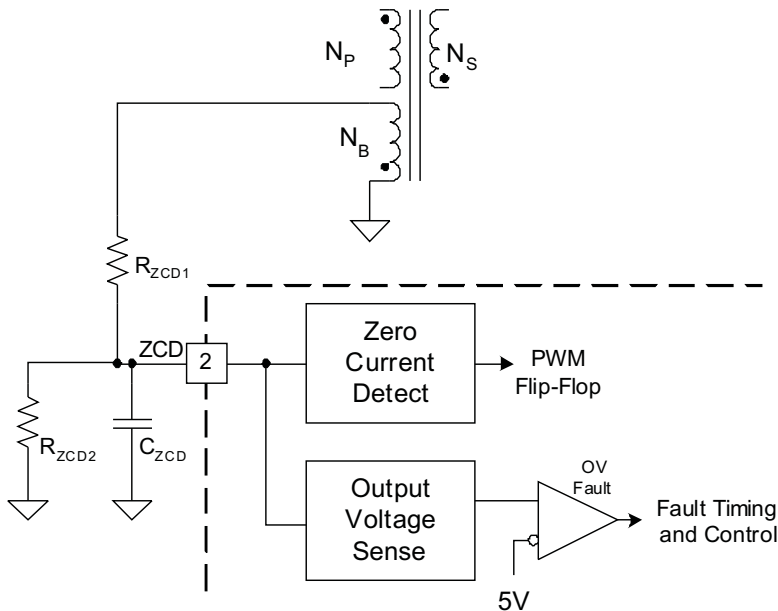


图 29. Zero Crossing Detection.

$$R_{ZCD1} = \frac{V_{OUT} + V_F}{100\mu A} \times \frac{N_B}{N_S} \quad (12)$$

$$R_{ZCD2} = \frac{ZCD_{(ovp)} \times R_{ZCD1}}{\left(V_{OUT(pk)} \times \frac{N_B}{N_S} \right) - ZCD_{(ovp)}} \quad (13)$$

Green Mode Operation

During light load operation the UCC28610 cycles between two states: GM-on and GM-off. The details are shown in 图 30. During the GM-on state, the controller is active while the modulator issues a burst of one or more pulses. During the GM-off state the controller reduces its operating current and switching action is inhibited. The rate and duration of the on and off states are controlled by the current into the FB pin as it cycles between the two hysteretic thresholds separated by I_{FB, GM_HYST} , the load current, the output filter capacitor, and the details of the feedback circuit.

During the GM-off state the VDD supply current is reduced to approximately 550 μA , $I_{VDD(GM)}$. The Enable PWM signal goes low which inhibits switching, sets the VGG shunt regulation to $\sim 16\text{ V}$, $V_{GG(DISABLED)}$, and turns on the VDD switch. The VGG node quickly charges to 16V and the low VDD current is supplied from the VDD capacitor.

During the GM-on state the UCC28610 controls the peak primary current to 33% of $I_{DRV,PK(max)}$, at a 30-kHz rate. When switching, the VGG shunt regulator pulls the VGG voltage down to $\sim 14\text{ V}$. VDD is charged by the auxiliary winding during this time as long as VDD does not discharge below 14 V. The converter's output voltage is charged until the feedback network forces the FB current to the GM off threshold, $I_{FB,CNR3}$, and puts the controller back into the GM off state.

At very light loads the time between PWM bursts can be long. To obtain the lowest no-load power, it is important that VDD not discharge below 16 V by more than the threshold voltage of the HV MOSFET or the HV MOSFET will turn-on and linearly supply the VDD current from the high-voltage bulk rail. The VDD voltage can be extended by increasing the C_{VDD} capacitance without significant impact on start-up time.

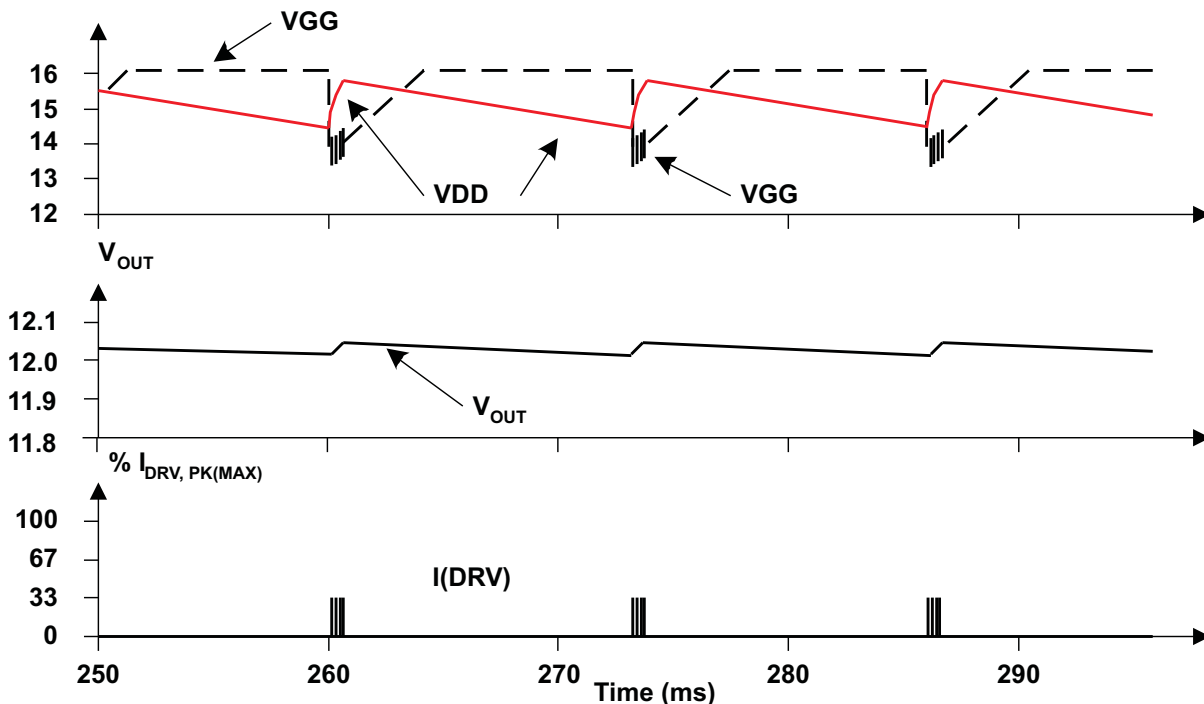


图 30. Green Mode Operation

Maximum Converter Power Limitation

The suggested peak power range of the UCC28610 is 12 W to 65 W based on a universal AC line converter (90-VAC to 265-VAC input line voltage), using an external high voltage MOSFET with a voltage rating of 600 V. This power range may depend on application and external MOSFET stress voltage. Ultimately, the peak primary current is the limiting factor because this current must pass through the UCC28610. The limit on the peak primary current imposes a limit on the peak primary power. The peak power must be less than 65 W, not the average power. The peak power is defined as the highest power level where the controller must maintain regulation.

At all power levels, program the UCC28610 to control the power limit with the primary inductance, peak current and maximum switching frequency (133 kHz). The maximum peak input power level is given by 公式 14. The accuracy of the power limit is twice as sensitive to $I_{DRV(PK)}$ errors than L_M errors and $f_{S(max)}$ errors. If the load demands more power than the programmed level, the power supply output voltage sags and the overload timer is initiated.

$$P_{IN(max)} = \frac{L_m \times I_{DRV(pk)}^2 \times f_{S(max)}}{2} \tag{14}$$

Minimum Converter Power Limitation

The dynamics of the DRV current sense imposes the 12-W minimum power level limit for this controller. The power level limits are found from DRV current estimates for typical universal AC adapters that use a 600-V MOSFET. The power range and its associated peak current range are given in 公式 15.

$$\begin{aligned} P_{IN} &\geq 12W \\ I_{DRV,PK(min)} &\geq 1A \end{aligned} \tag{15}$$

The minimum power level is due to a loss of linearity of the current mirror, as shown in 图 31. A programmed $I_{DRV,PK}$ level between 0.66 A and 1 A (by using $100\text{ k}\Omega \leq R_{CL} \leq 150\text{ k}\Omega$) allows only a 2:1 amplitude modulation range of the peak DRV current. The amplitude of I_{DRV} modulates linearly if $I_{DRV,PK}$ is programmed within its recommended operating range ($1.0\text{ A} < I_{DRV,PK} < 4.1\text{ A}$, corresponding to $100\text{ k}\Omega > R_{CL} > 24.3\text{ k}\Omega$ respectively).

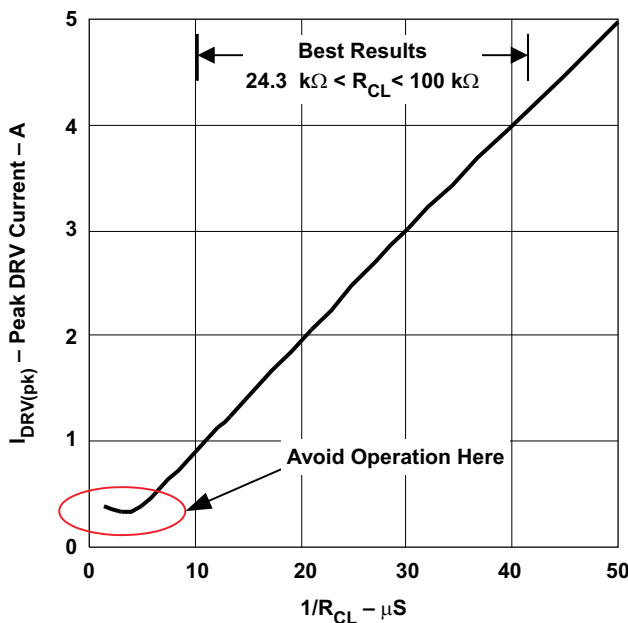


图 31. Dynamic Operating Range

Fault Recovery

The UCC28610 reacts with the programmed overload response if the overload lasts longer than t_{OL} (nominally 250 ms). The overload fault responses are either (1) latch-off or (2) shutdown/retry after a retry delay of 750 ms. The overload response is programmed with the MOT pin. The forced DCM feature prevents transformer saturation and limits the average and RMS output currents of the secondary winding of the transformer. Even under short circuit load conditions, the output current of the transformer is limited to the levels that are shown in 公式 16, where N_{PS} is the primary-to-secondary turns ratio. Typical behavior for a shorted load is shown in 图 32.

$$I_{SECONDARY,AVG(SHORTEDLOAD)} = \frac{N_{PS} \times I_{DRV(PEAK)}}{2}$$

$$I_{SECONDARY,RMS(SHORTEDLOAD)} = \frac{N_{PS} \times I_{DRV(PEAK)}}{\sqrt{3}}$$

(16)

In shutdown/retry mode switching will be re-enabled after the 750-ms retry delay. In latch-off mode, a 7.5-kΩ load is activated at the DRV pin upon the activation by a fault condition. The internal 7.5-kΩ load draws current from the bulk capacitor through the HV MOSFET and the transformer primary winding. The bias voltage, VDD, is also regulated by the HV MOSFET during the latch-off state. Once the AC line is removed, a 2.8-mA current, $I_{DRV,DSCH}$, will discharge the bulk capacitor. Ultimately, VDD will discharge when the bulk voltage becomes sufficiently low. A normal start-up cycle can occur if the input voltage is applied after VDD falls below the fault reset level, $V_{DD(Fault\ Reset)}$, which is approximately equal to 6 V.

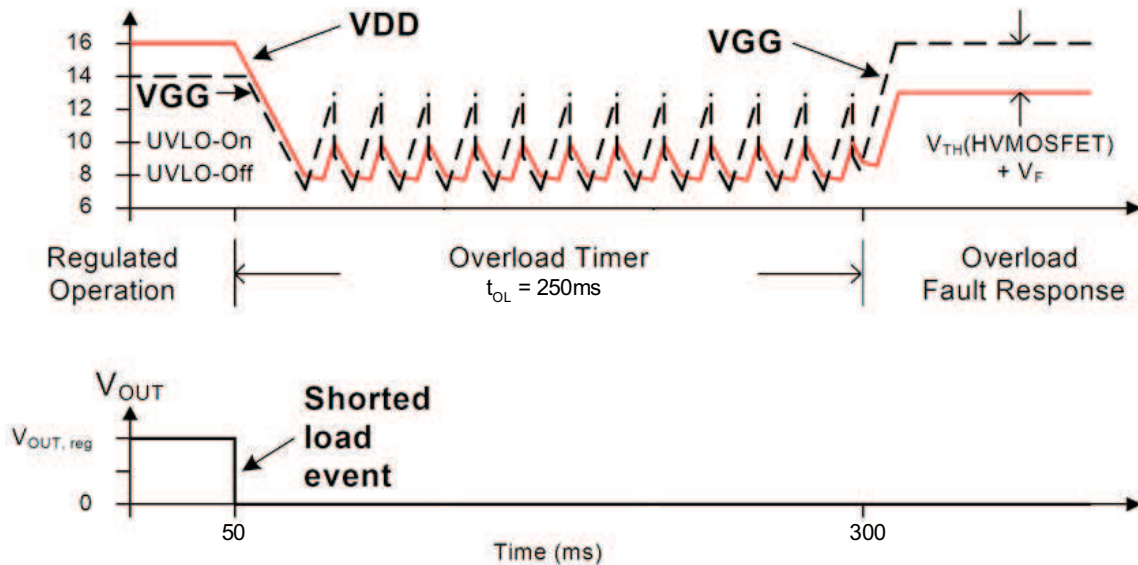


图 32. Overload Behavior with a Shorted Output

Maximum On-Time and Brown Out

The forced DCM feature provides protection against excessive primary currents in the event that the input voltage becomes very low. The highest possible secondary currents can be described by 公式 16. The UCC28610 adds further protection by allowing the user to program the maximum on-time.

The Maximum On-Time (MOT) function causes the converter to react as if there is an overload condition if the load is sufficiently large during a line sag condition. During low line conditions the MOT function limits the on-time of the primary switch which limits the peak current in the primary power stage. 图 33 shows how the MOT period, t_{MOT} , is programmed over the range of 1.5 μ s to 5 μ s for either range of programming resistors. The resistor range determines the controller's response to a sustained overload fault – to either Latch-off or to Shutdown/Retry, which is the same response for a line-sag, or brown out, condition.

External Shutdown Using the MOT Pin

Many applications require the ability to shutdown the power supply with external means. This feature is easily implemented by connecting the collector and emitter of an NPN transistor between MOT and GND, respectively. The NPN transistor can be the photo-transistor of an opto-isolator for isolated applications.

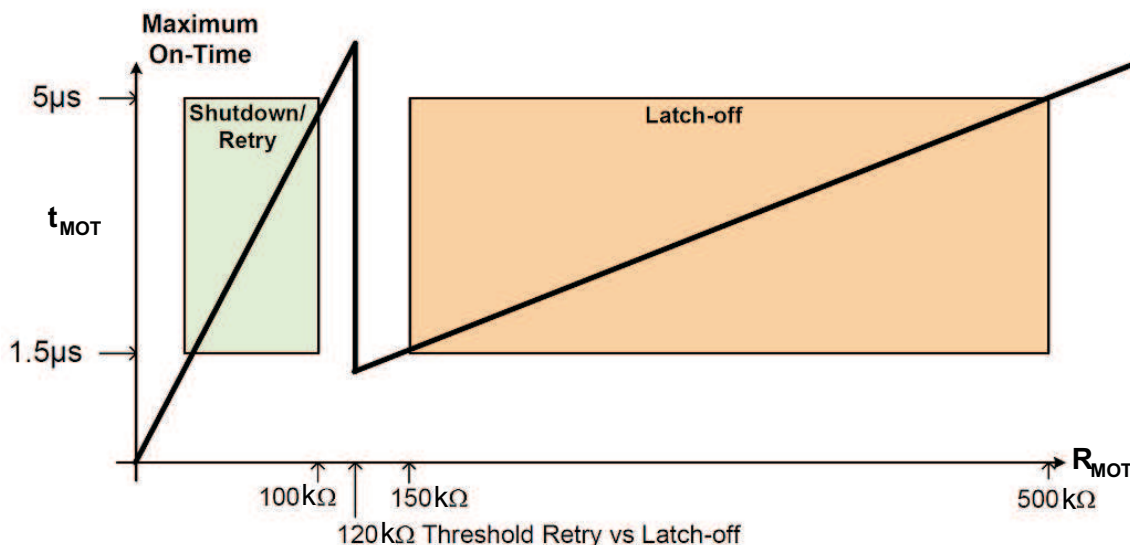


图 33. Programming MOT and Overload Fault Response

For latch-off response to over-current or brownout:

$$R_{MOT} = t_{MOT} \times \left(1 \times 10^{11} \frac{\Omega}{s} \right) \quad (17)$$

where:

$$\begin{aligned} 150 \text{ k}\Omega &\leq R_{MOT} \leq 500 \text{ k}\Omega \\ 1.5 \text{ }\mu\text{s} &\leq t_{MOT} \leq 5 \text{ }\mu\text{s} \end{aligned} \quad (18)$$

For shut-down/retry response to over-current or brownout:

$$R_{MOT} = t_{MOT} \times \left(2 \times 10^{10} \frac{\Omega}{s} \right) \quad (19)$$

where:

$$\begin{aligned} 25 \text{ k}\Omega &\leq R_{MOT} \leq 100 \text{ k}\Omega \\ 1.5 \text{ }\mu\text{s} &\leq t_{MOT} \leq 5 \text{ }\mu\text{s} \end{aligned} \quad (20)$$

Over Voltage Detection

The UCC28610 controller monitors the output voltage by sampling the voltage at the auxiliary winding. The sampling time has a fixed delay of $1\ \mu\text{s}$, $t_{\text{BLANK,OV}}$, after the internal driver turns off. This allows the auxiliary winding to be sampled after the bias winding voltage settles from the transient. This same delay is used to blank the ZCD input to avoid unintended zero crossing detection should the ringing be large enough to cross the ZCD zero crossing threshold.

The output over-voltage (OV) threshold is set using the turn ratio of the auxiliary winding to the output secondary and a resistive divider into the ZCD input pin. The UCC28610 will always enter a latched-off state if it detects an OV condition. The VDD supply must cycle below the fault reset threshold to re-start in order to recover. The functionality of the over-voltage detection function is shown in [图 34](#).

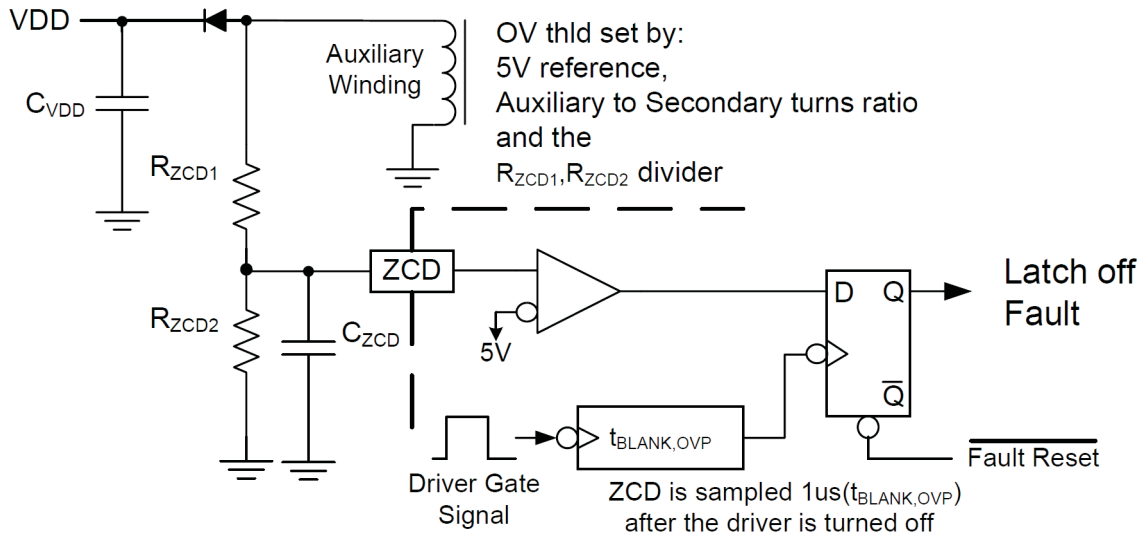


图 34. Output Over-Voltage Protection with ZCD Pin

Solving for High Frequency Ringing

Cascode drive circuits are well known for high speed voltage gain. This topology can have small signal bandwidth well over 100 MHz and it can exhibit high frequency ringing. The internal HS Drive MOSFET shorts the gate to source of the external HV MOSFET during the turn-off interval of the switch cycle. This prevents the HV MOSFET from undesirably exciting the LC resonant circuit in the converter (the magnetizing inductance of the transformer and the stray drain capacitance). High frequency ringing can appear within the built-in dead-time between the turn-off of DRV and the turn-on of the HS Drive. A large amount of energy is transferred through the power components during this dead-time. Excessive high frequency ringing can cause EMI problems and become destructive in some situations.

Identification of High Frequency Ringing

The high frequency ringing is the result of stray capacitances ringing with the stray inductance between the source of the HV MOSFET and the DRV pin. Low threshold voltage of the high voltage MOSFET and large peak DRV current can make the ringing worse. In destructive ringing situations, the converter may easily power up and attain regulation the first time, never to start-up again.

The ringing can be observed in either or both of the following conditions:

- The very first HV MOSFET turn-off event during a cold start of the converter ($V_{\text{GG}} > V_{\text{DD}}$).
- HV MOSFET turn-off edge under steady state, where the converter switches the HV MOSFET at the programmed $I_{\text{DRV,PK}}$ level ($V_{\text{DD}} > V_{\text{GG}}$).

Avoid HF Ringing

High frequency ringing problems with cascode MOSFET drives can often be avoided. Many converters will not have this problem because they use an HV MOSFET with a large V_{th} , large $R_{DS(on)}$, low transconductance gain, or operate at low current. Ringing problems can also be avoided by minimizing stray inductance. The trace between the HV MOSFET source and the DRV pin must be kept very short, less than 1 cm. Do not add current probe loops to the source lead of the HV MOSFET. Do not place ferrite beads on the source lead of the HV MOSFET.

If ringing cannot be avoided, the most efficient and effective methods to solve ringing during switching transients are:

1. A ferrite chip or bead connected to the gate of the HV MOSFET,
2. A small capacitor connected from DRV to GND and
3. A gate turn-off resistor. These three techniques can be used separately or combined, as shown in [图 35](#).

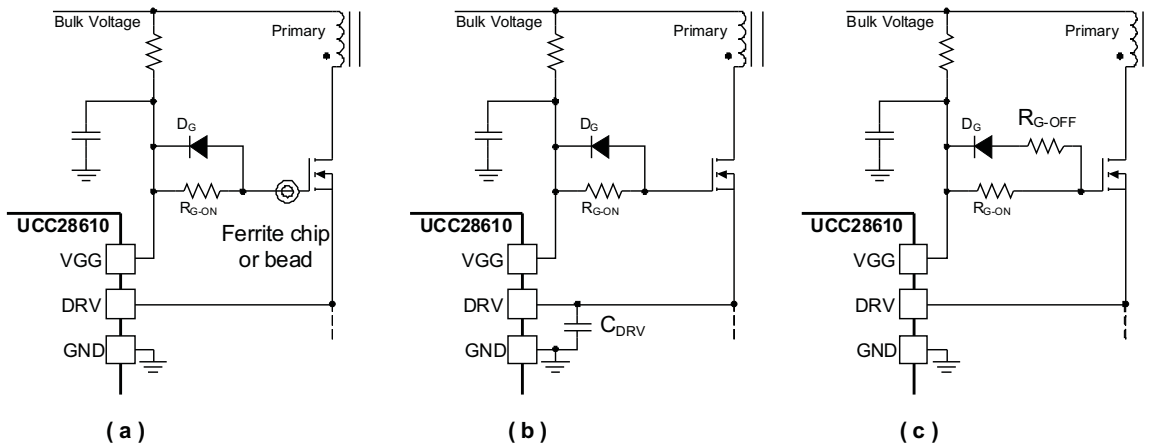


图 35. High Frequency Ringing Solutions, (a) ferrite chip, (b) CDRV and (c) RG-OFF

Ferrite Chip or Bead Solution

The ferrite chip or bead connected to the gate of the HVMOSFET provides the best result because it suppresses ringing in the gate, source, and drain circuits of the HVMOSFET with minimal added losses. Select the ferrite chip for its resistance value in the ringing frequency range (for example, 60 Ω at 100 MHz). The peak current rating of the ferrite chip or bead must be sufficient for the drain – gate discharge current that occurs during the turn-off transient. Excessively large bead reactance can result in low frequency surges of VGG at peak load. Normally, good results can be achieved with a 0603 ferrite chip device.

DRV Capacitor Solution

A capacitor between DRV and GND can reduce ringing on VGG. Select the DRV capacitor experimentally by observing the effect on the VGG pin during the first turn-off edge and during the turn-off edge at full load operation. The capacitor should be less than 3.3 nF so that it does not significantly reduce efficiency. Use a capacitor with a low Q, such as one with Y5V dielectric. This technique will not completely damp the ringing yet it can provide sufficient protection against stray inductance between the source of the HVMOSFET and the DRV pin.

Gate Turn-Off Resistor Solution

A gate turn-off resistor in the range $0 \Omega < R_{G-OFF} < 5 \Omega$ can damp ringing. The turn-off resistance is limited in order to prevent the stray source inductance of the HVMOSFET from over charging VGG through the body diode of the HS Drive MOSFET, in addition to any peak current error problems that would be caused by additional delay. The damping effect of the gate resistor works better in applications with low current and small source inductance.

A much larger resistance can be tolerated during the HVMOSFET turn-on transition due to DCM operation. The recommended turn-on resistance range is $0 \Omega < R_{G-ON} < 200 \Omega$ in order to prevent the turn-on delay from interfering with valley switching.

Thermal Shutdown

The UCC28610 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown point, T_{SD} , the UCC28610 initiates a shutdown event and permits retry after the retry time, t_{RETRY} . Shutdown/Retry cycles continue if the junction temperature is not less than T_{SD} minus T_{SD_HYST} .

Typical Schematic and Layout

It is possible to design a power supply on a single layer board using the UCC28610. 图 36 and 图 37 show an example of a typical layout and design, respectively. Proper use of ground planes can solve EMI and thermal problems. For best results, create a quiet ground plane for the components associated with pins 1 through 4. This offers shielding for the control signals. Also, do not extend the ground plane under heat sinks, thermistors or snubbers so that these components do not heat the UCC28610.

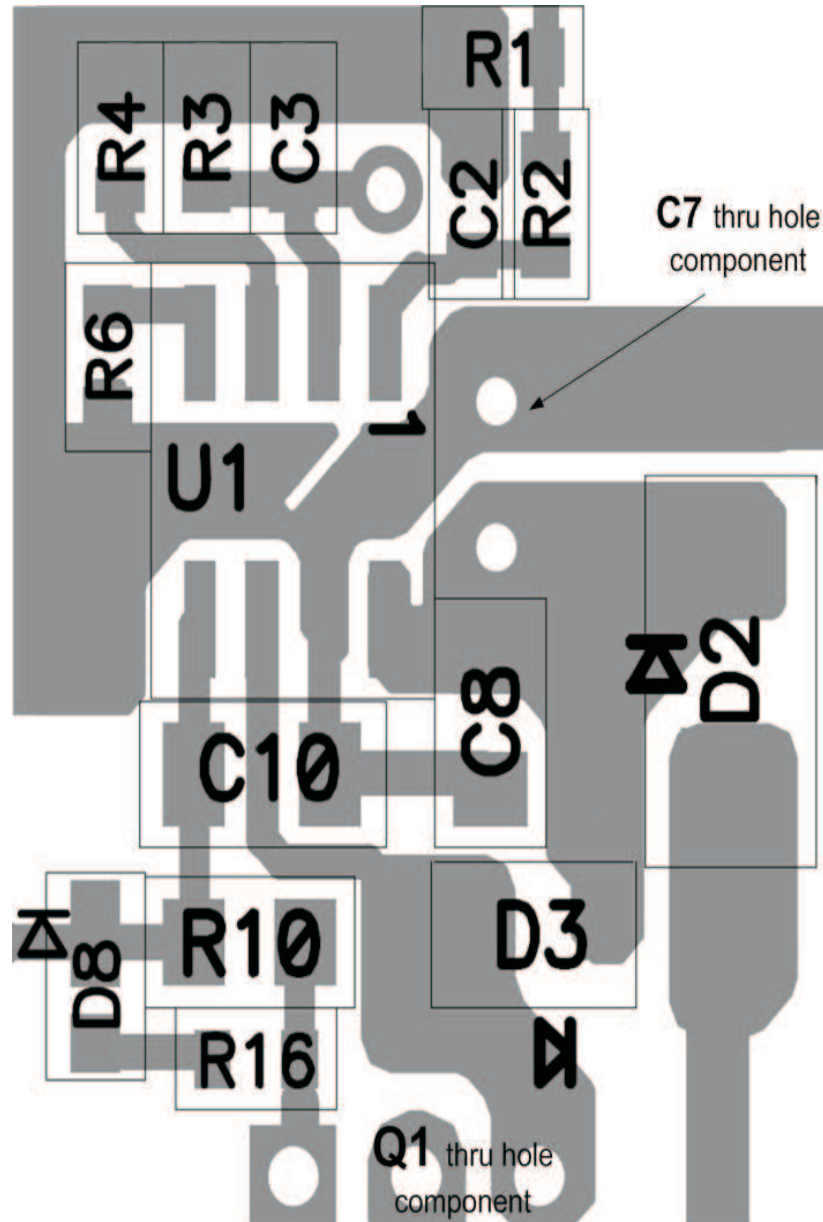
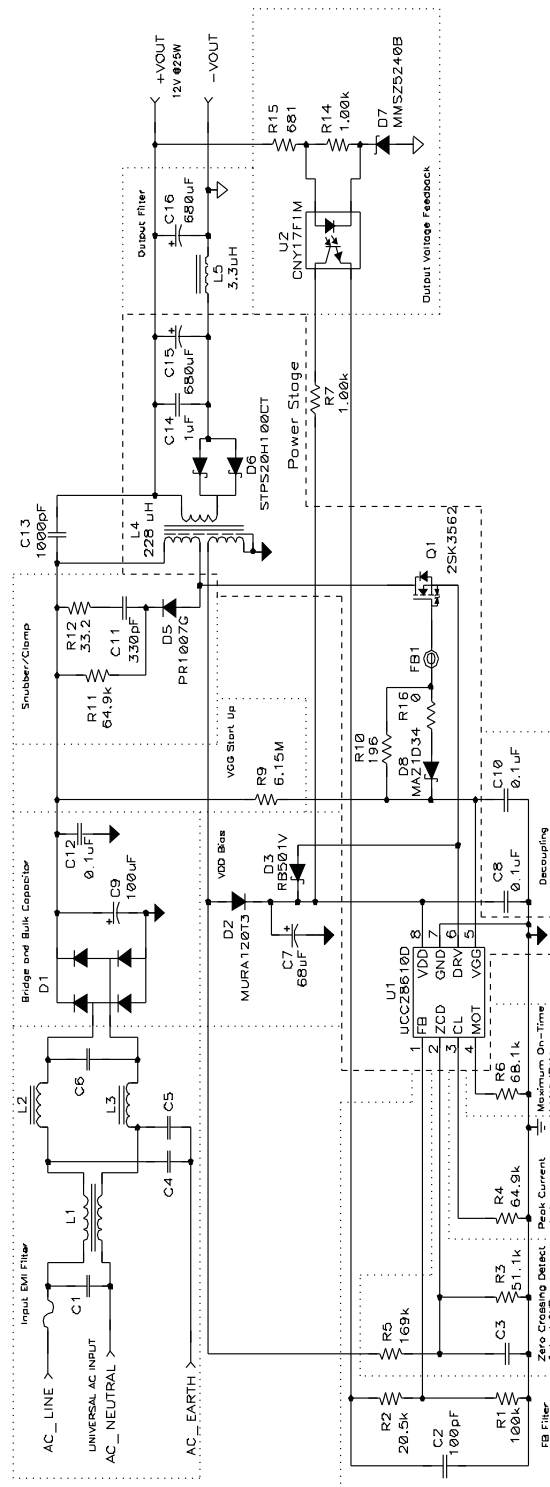


图 36. Typical Layout of the Device on a Single Layer PCB

注

The reference designators correspond to the components shown in the schematic of 图 37.



37. Typical Design Schematic

Terminal Components

For reference designators refer to [图 1](#).

表 1. Terminal Components

NAME	TERMINAL	DESCRIPTION
CL	3	$R_{CL} = 33.2k\Omega \times \sqrt{\frac{K_P \times L_M}{P_{IN}}}$ $I_{DRV(PK)} = \frac{100 \text{ kV}}{R_{CL}}$ <p>Where $K_P = 0.54W/\mu H$ L_M is the minimum value of the primary inductance $P_{IN} = P_{OUT}/\eta$ η = efficiency</p>
DRV	6	Q_1 , power MOSFET with adequate voltage and current ratings, V_{VGS} must have at least 20-V static rating. D_1 , Schottky diode, rated for at least 30 V, placed between DRV and VDD
FB	1	$R_{FB} = 100 \text{ k}\Omega$
GND	7	Bypass capacitor to VDD, $C_{BP} = 0.1\text{-}\mu\text{F}$, ceramic
MOT	4	<p>For latch-off response to overcurrent faults: t_{MOT} = user programmable maximum on-time after 250-ms delay.</p> $R_{MOT} = t_{MOT} \times \left(1 \times 10^{11} \frac{\Omega}{s} \right)$ <p>where</p> <ul style="list-style-type: none"> $150 \text{ k}\Omega \leq R_{MOT} \leq 500 \text{ k}\Omega$ <p>For shutdown-retry response to overcurrent faults:</p> $R_{MOT} = t_{MOT} \times \left(2 \times 10^{10} \frac{\Omega}{s} \right)$ <ul style="list-style-type: none"> $25 \text{ k}\Omega \leq R_{MOT} \leq 100 \text{ k}\Omega$ and $t_{MOT} \leq 5 \mu\text{s}$
VDD	8	$C_{VDD} = \frac{I_{VDD(GM)} \times t_{BURST}}{\Delta V_{DD(BURST)}}$ <p>where: $\Delta V_{DD(BURST)}$ is the allowed VDD ripple during burst operation t_{BURST} is the estimated burst period, The typical C_{VDD} value is approximately 47 μF D_{BIAS} must have a voltage rating greater than:</p> $V_{DBIAS} \geq V_{OUT} \frac{N_{PS}}{N_{PB}} + \frac{V_{BULK(max)}}{N_{PB}}$ <p>where: V_{DBIAS} is the reverse voltage rating of diode D_2 $V_{BULK(max)}$ is the maximum rectified voltage of C_{BULK} at the highest line voltage</p>
VGG	5	minimize the length of the C_{VGG} connection to GND $C_{VGG} =$ at least 10x C_{GS} of HV MOSFET, usually $C_{VGG} = 0.1 \mu\text{F}$.

表 1. Terminal Components (接下页)

NAME	TERMINAL	DESCRIPTION
ZCD	2	$R_{ZCD1} = \frac{V_{OUT} + V_F}{100 \mu A} \times \frac{N_{PS}}{N_{PB}}$ $R_{ZCD2} = \frac{ZCD_{(ovp)} \times R_{ZCD1}}{\left(V_{OUT(pk)} \times \frac{N_{PS}}{N_{PB}} \right) - ZCD_{(ovp)}}$
		<p>where:</p> <p>ZCD_(ovp) is the overvoltage fault threshold at ZCD</p> <p>N_{PS} is the primary to secondary turns ratio</p> <p>N_{PB} is the primary to bias turns ratio</p> <p>V_{OUT} is the average output voltage of the secondary</p> <p>V_F is the forward bias voltage of the secondary rectifier</p> <p>V_{OUT,PEAK} is the desired output overvoltage fault level</p>
<p>Note 1. Refer to the <i>Electrical Characteristics</i> table for all constants and measured values, unless otherwise noted.</p> <p>Note 2. Refer to 图 1 for all component locations in the 表 1.</p>		

Revision History

Changes from Revision C (January, 2009) to Revision D	Page
• Deleted 公式 2	14

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28610DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28610DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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