2.5A 隔离式绝缘栅双极型晶体管 (IGBT)，金属氧化物半导体场效应晶体管 (MOSFET) 栅极驱动器

查询样品: **ISO5500**

特性

- 最大峰值输出电流 **2.5A**
- 驱动 **IGBT** 高达 **I_C=150A**，**V_{CE}=1200V**
- 电容隔离式故障反馈
- **CMOS/TTL** 兼容输入
- **300nS** 最大传播延迟
- **IGBT** 软关闭
- 集成故障安全 **IGBT** 保护
  - 高 **V_{CE}(DESAT)** 保护
  - 具有滞后的欠电压锁定 **(UVLO)** 保护
- 用户可配置函数
  - 反向、同向输入
  - 自动复位
  - 自动关断
- 宽 **V_{CC1}**范围：**3V** 至 **5.5V**
- 宽 **V_{CC2}**范围：**15V** 至 **30V**
- 运行温度：**-40°C** 至 **125°C**
- 宽体小外形尺寸 **(SO)-16** 封装
- **±50kV/μs** 典型瞬态抗扰度
- **6000V$_{峰值}$**隔离
- 管理批准：经 **UL1577** 批准；**CSA**，**DIN EN 60747-5-2**，**IEC 60950-1** 和 **61010-1** 等待审批中

应用范围

- 隔离式 **IGBT** 和 **MOSFET** 驱动输入
  - 电机控制
  - 运动控制
  - 工业变频器
  - 开关模式电源

说明

ISO5500 是一款用于 IGBT 和 MOSFET 的隔离式栅极驱动器，额定功率高达 I_C=150A 和 V_{CE}=1200V。输入 TTL 逻辑和输出功率级由一个电容、二氧化硅 (SiO_2)，隔离栅隔离开来。 当与隔离式电源配合使用时，这些器件可以阻止高电压、隔离接地，并防止噪声电流进入本地接地和干扰或损坏敏感的电路。

在一个欠压闭锁电路 (UVLO) 监视输出电源的同时，此器件为 IGBT 和 MOSFET 提供过流保护 (DESAT) 功能以保证足够的栅极驱动电压。 如果输出电源电压下降至低于 12V，通过将栅极驱动输出驱动至一个逻辑低电平状态，UVLO 将功率晶体管关闭。

对于一个 DESAT 故障，在防止较大 di/dt 感应电压尖峰出现的同时，ISO5500 启动一个软关断过程来将 IGBT/MOSFET 电流缓慢减少至零。 然后穿过隔离隔栅发送一个故障信号，有效驱动开漏$\overline{\text{FAULT}}$输出低电平并且禁用器件输入。 输入在 $\overline{\text{FAULT}}$引脚为低电平的时间内被阻断。 在输入针对一个输出低电平状态进行配置之前，$\overline{\text{FAULT}}$保持低电平，随后是一个$\overline{\text{RESET}}$引脚上的逻辑低电平输入。

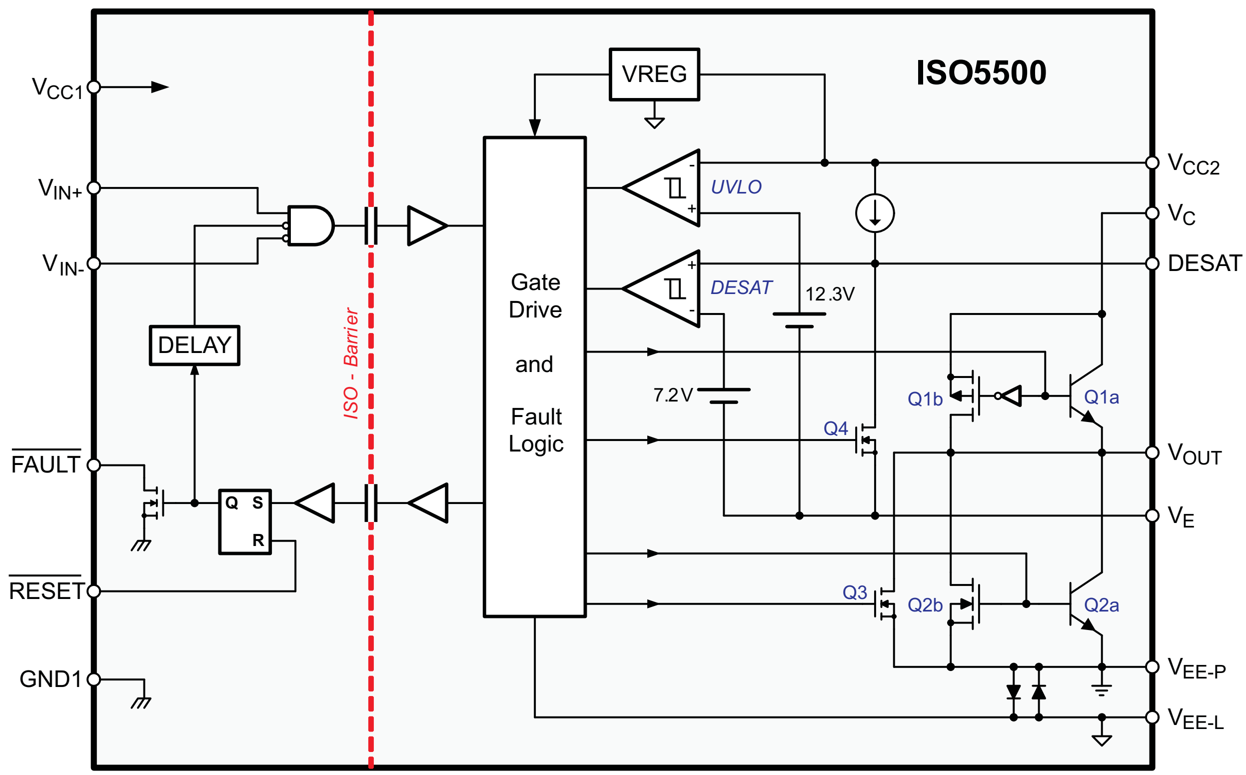
ISO5500 采用一个 16 引脚小外形尺寸集成电路 (SOIC) 封装，额定运行温度范围为 -40°C 至 125°C。

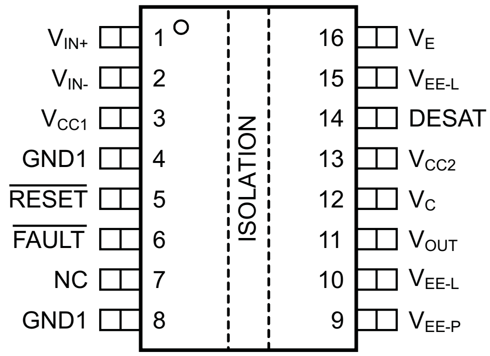
English Data Sheet: SLLSE64

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM





PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1	V_{IN+}	Non-inverting gate drive voltage control input
2	V_{IN-}	Inverting gate drive voltage control input
3	V_{CC1}	Positive input supply (3 V to 5.5 V)
4,8	GND1	Input ground
5	$\overline{\text{RESET}}$	$\overline{\text{FAULT}}$ reset input
6	$\overline{\text{FAULT}}$	Open-drain output. Connect to 3.3k pull-up resistor
7	NC	Not connected
9	V_{EE-P}	Most negative output-supply potential of the power output. Connect externally to pin 10.
10, 15	V_{EE-L}	Most negative output-supply potential of the logic circuitry. Pin 10 and 15 are internally connected. Connect at least pin 10 externally to pin 9. Pin 15 can be floating.
11	V_{OUT}	Gate drive output voltage
12	V_C	Gate driver supply. Connect to V_{CC2}.
13	V_{CC2}	Most positive output supply potential
14	DESAT	Desaturation voltage input
16	V_E	Gate drive common. Connect to IGBT Emitter.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

				VALUE MIN	VALUE MAX	UNIT
Supply voltage, V_{CC1}				–0.5	6	V
Total output supply voltage, $V_{OUT(total)}$		$(V_{CC2} – V_{EE-P})$		–0.5	35	V
Positive output supply Voltage, V_{OUT+}		$(V_{CC2} – V_E)$		–0.5	35 – $(V_E – V_{EE-P})$	V
Negative output supply voltage, V_{OUT-}		$(V_E – V_{EE-P})$		–0.5	V_{CC2}	V
Voltage at		DESAT		V_E – 0.5	V_{CC2}	
		V_{IN+}, $V_{IN–}$, $\overline{\text{RESET}}$		–0.5	6	V
Peak gate drive output voltage		$V_{o(peak)}$		–0.5	V_{CC2}	V
Collector voltage, V_C				–0.5	V_{CC2}	V
Output current , I_O (1)					±2.8	A
$\overline{\text{FAULT}}$ output current, I_{FL}					±20	mA
Electrostatic Discharge, ESD	Human Body Model	ESDA / JEDEC JS-001-2012	All pins		±4	kV
	Charged Device Model	JEDEC JESD22-C101E			±1.5	kV
	Machine Model	JEDEC JESD22-A115-A			±200	V
Maximum junction temperature, T_J					170	°C
Maximum storage temperature, T_{STG}				-65	150	°C

(1) Maximum pulse width = 10 μs, maximum duty cycle = 0.2%.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC1}	Supply voltage	3		5.5	V
$V_{OUT(total)}$	Total output supply voltage $(V_{CC2} – V_{EE-P})$	15		30	V
V_{OUT+}	Positive output supply voltage $(V_{CC2} – V_E)$	15		30V – $(V_E – V_{EE-P})$	V
$V_{OUT–}$	Negative output supply voltage $(V_E – V_{EE-P})$	0		15	V
V_C	Collector voltage	V_{EE-P} + 8		V_{CC2}	V
t_{ui}	Input pulse width	0.1			μs
t_{uiR}	$\overline{\text{RESET}}$ Input pulse width	0.1			μs
V_{IH}	High-level input voltage (V_{IN+}, $V_{IN–}$, $\overline{\text{RESET}}$)	2		V_{CC}	V
V_{IL}	Low-level input voltage (V_{IN+}, $V_{IN–}$, $\overline{\text{RESET}}$)	0		0.8	V
f_{INP}	Input frequency			520 (1)	kHz
V_{SUP_SR}	Supply Slew Rate (V_{CC1} or $V_{CC2} – V_{EE-P}$) (2)			75	V/ms
T_J	Junction temperature	–40		150	°C
T_A	Ambient temperature	-40	25	125	°C

(1) If T_A = 125°C, V_{CC1}= 5.5 V, V_{CC2} = 30 V, R_G = 10 Ω, C_L = 1 nF
(2) If V_{CC1} skew is faster than 75 V/ms (especially for the falling edge) then V_{CC2} must be powered up after V_{CC1} and powered down before V_{CC1} to avoid output glitches.

ELECTRICAL CHARACTERISTICS

All typical values are at T_A = 25°C, V_{CC1} = 5 V, $V_{CC2} – V_E$ = 30 V, $V_E – V_{EE-P}$ = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current	Quiescent	$V_I = V_{CC1}$ or 0 V, No load, See Figure 1, Figure 2, Figure 28, and Figure 29		5.5	8.5	mA
		300 kHz			5.7	8.7	
I_{CC2}	Supply current	Quiescent	$V_I = V_{CC1}$ or 0 V, No load, See Figure 3 through Figure 5, Figure 30, and Figure 31		8.4	12	mA
		300 kHz			9	14	
I_{CH}	High-level collector current		I_{OUT} = 0, See Figure 27 and Figure 30			1.3	mA
			I_{OUT} = –650 µA, See Figure 27 and Figure 30			1.9	
I_{CL}	Low-level collector current		See Figure 27 and Figure 31			0.4	mA
I_{EH}	V_E High-level supply current		See Figure 6 and Figure 40	–0.5	–0.3		mA
I_{EL}	V_E Low-level supply current		See Figure 6 and Figure 41	–0.8	–0.53		mA
I_{IH}	High-level input leakage		IN from 0 to V_{CC}			10	µA
I_{IL}	Low-level input leakage			–10			
I_{FH}	High-level $\overline{FAULT}$ pin output current		$V_{\overline{FAULT}} = V_{CC1}$, no pull-up, See Figure 33	–10		10	µA
I_{FL}	Low-level $\overline{FAULT}$ pin output current		$V_{\overline{FAULT}}$ = 0.4 V, no pull-up, See Figure 34	5	12		mA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage		See Figure 32	11.6	12.3	13.5	V
$V_{IT–(UVLO)}$	Negative-going UVLO threshold voltage				11.1	12.4	
$V_{HYS\ (UVLO)}$	UVLO Hysteresis voltage ($V_{IT+} – V_{IT–}$)			0.7	1.2		
I_{OH}	High-level output current		$V_{OUT} = V_{CC2}$ – 4 V(1), See Figure 7 and Figure 35	–1	–1.6		A
			$V_{OUT} = V_{CC2}$ – 15 V(2), See Figure 7 and Figure 35	–2.5			
I_{OL}	Low-level output current		$V_{OUT} = V_{EE-P}$ + 2.5 V(1), See Figure 8 and Figure 36	1	1.8		A
			$V_{OUT} = V_{EE-P}$ + 15 V(2), See Figure 8 and Figure 36	2.5			
I_{OF}	Output-low fault current		$V_{OUT} – V_{EE-P}$ = 14 V, See Figure 9 and Figure 37	90	140	230	mA
V_{OH}	High-level output voltage		I_{OUT} = –100 mA, See Figure 10, Figure 11 and Figure 38	V_C-1.5	V_C-0.8		V
			I_{OUT} = –650 µA, See Figure 10, Figure 11 and Figure 38	V_C-0.15	V_C-0.05		
V_{OL}	Low-level output voltage		I_{OUT} = 100 mA, See Figure 12, Figure 13 and Figure 39		0.2	0.5	V
I_{CHG}	Blanking capacitor charging current		V_{DESAT} = 0 V to 6 V, See Figure 14 and Figure 42	–180	–270	–380	µA
I_{DSCHG}	Blanking capacitor discharge current		V_{DESAT} = 8 V, See Figure 42	20	45		mA
V_{DSTH}	DESAT threshold voltage		($V_{CC2} – V_E$) > $V_{TH-(UVLO)}$, See Figure 15 and Figure 42	6.7	7.2	7.7	V
CMTI	Common mode transient immunity		$V_I = V_{CC1}$ or 0 V, V_{CM} at 1500 V, See Figure 43 though Figure 46	25	50		kV/µS

(1) Maximum pulse width is 50 µs, maximum duty cycle is 0.5%
(2) Maximum pulse width is 10 µs, maximum duty cycle is 0.2%

SWITCHING CHARACTERISTICS

All typical values are at T_A = 25°C, V_{CC1} = 5 V, $V_{CC2} – V_E$ = 30 V, $V_E – V_{EE-P}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation Delay	R_G = 10 Ω, C_G = 10 nF, 50 % duty cycle, 10 kHz input, $V_{CC2} – V_{EE}$ = 30 V, $V_E – V_{EE}$ = 0 V, See Figure 16 through Figure 19, Figure 26, Figure 47, Figure 49, and Figure 50	150	200	300	ns
t_{sk-p}	Pulse Skew $\lvert t_{PHL} – t_{PLH}\rvert$			1.7	10	ns
t_{sk-pp}	Part-to-part skew(1)				45	ns
t_{sk2-pp}	Part-to-part skew(2)		–50		50	ns
t_r	Output signal rise time			55		ns
t_f	Output signal fall time			10		ns
$t_{DESAT\ (90\%)}$	DESAT sense to 90% VOUT delay	R_G = 10 Ω, C_G = 10 nF, $V_{CC2} – V_{EE-P}$ = 30 V, $V_E – V_{EE-P}$ = 0 V, See Figure 20 through Figure 25, Figure 48 and Figure 51		300	550	ns
$t_{DESAT\ (10\%)}$	DESAT sense to 10% VOUT delay			1.8	2.3	μs
$t_{DESAT\ (\overline{FAULT})}$	DESAT sense to $\overline{\text{FAULT}}$ low output delay			290	550	ns
$t_{DESAT\ (LOW)}$	DESAT sense to DESAT low propagation delay			180		ns
$t_{\overline{RESET}\ (\overline{FAULT})}$	$\overline{\text{RESET}}$ to high-level $\overline{\text{FAULT}}$ signal delay		3	8.2	13	μs
$t_{UVLO\ (ON)}$	UVLO to V_{OUT} high delay	1ms ramp from 0 V to 30 V		4		μs
$t_{UVLO\ (OFF)}$	UVLO to V_{OUT} low delay	1ms ramp from 30 V to 0 V		6		μs
t_{FS}	Failsafe output delay time from input power loss			2.8		μs

(1) t_{sk-pp} is the maximum difference in same edge propagation delay times (either V_{IN+} to V_{OUT} or $V_{IN–}$ to V_{OUT}) between two devices operating at the same supply voltage, same temperature, and having identical packages and test circuits.

$$\text{i.e. max}\left\{\begin{array}{l}\left[t_{PHL\text{-}max}\left(V_{CC1},V_{CC2},T_A\right) - t_{PHL\text{-}min}\left(V_{CC1},V_{CC2},T_A\right)\right],\\ \left[t_{PLH\text{-}max}\left(V_{CC1},V_{CC2},T_A\right) - t_{PLH\text{-}min}\left(V_{CC1},V_{CC2},T_A\right)\right]\end{array}\right\}$$

(2) t_{sk2-pp} is the propagation delay difference in high-to-low to low-to-high transition (any of the combinations V_{IN+} to V_{OUT} or $V_{IN–}$ to V_{OUT}) between two devices operating at the same supply voltage, same temperature, and having identical packages and test circuits.

i.e.
$$\min = t_{PHL\text{-}min}\left(V_{CC1},V_{CC2},T_A\right) - t_{PLH\text{-}max}\left(V_{CC1},V_{CC2},T_A\right)$$
$$\max = t_{PHL\text{-}max}\left(V_{CC1},V_{CC2},T_A\right) - t_{PLH\text{-}min}\left(V_{CC1},V_{CC2},T_A\right)$$

TYPICAL CHARACTERISTICS

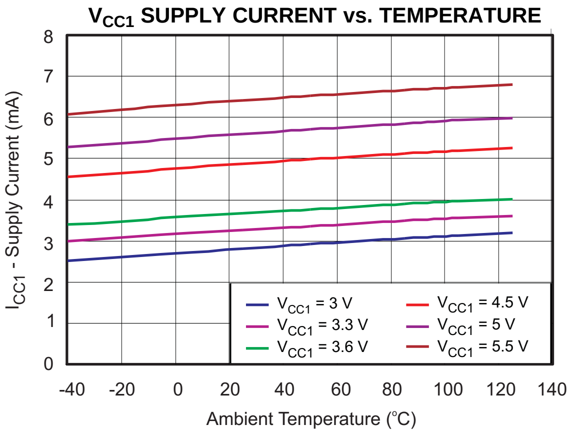


Figure 1.

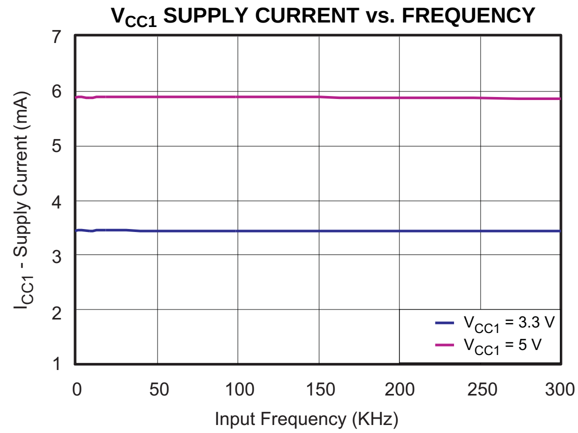


Figure 2.

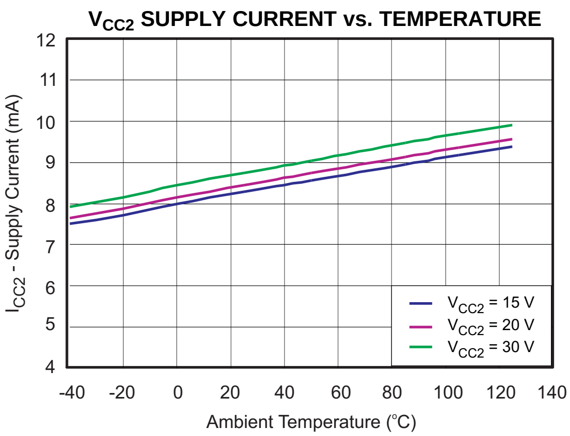


Figure 3.

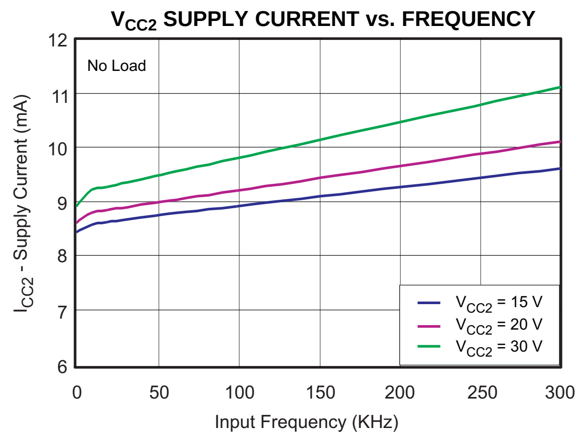


Figure 4.

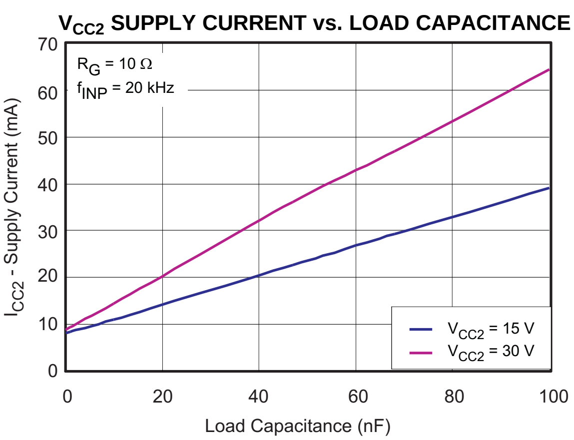


Figure 5.

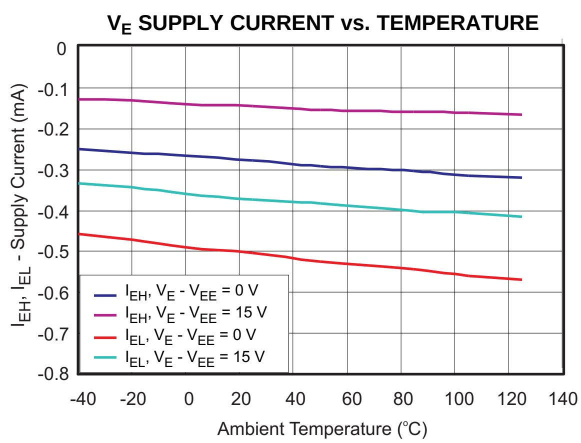


Figure 6.

TYPICAL CHARACTERISTICS (continued)

OUTPUT DRIVE CURRENT vs. TEMPERATURE

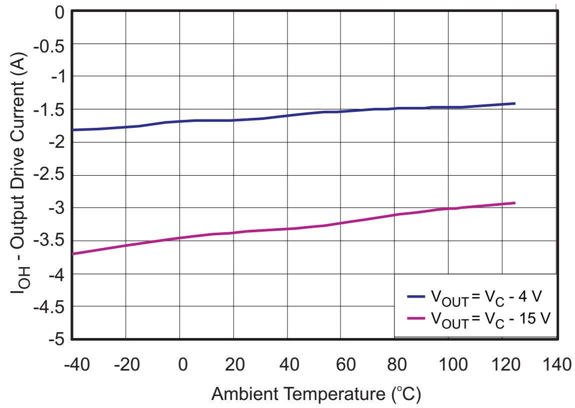


Figure 7.

OUTPUT SINK CURRENT vs. TEMPERATURE

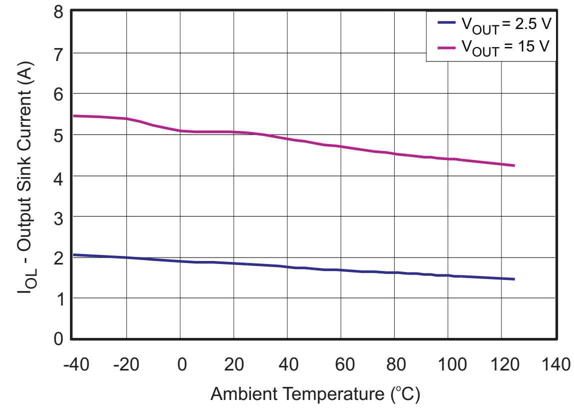


Figure 8.

OUTPUT SINK CURRENT DURING A FAULT CONDITION vs. OUTPUT VOLTAGE

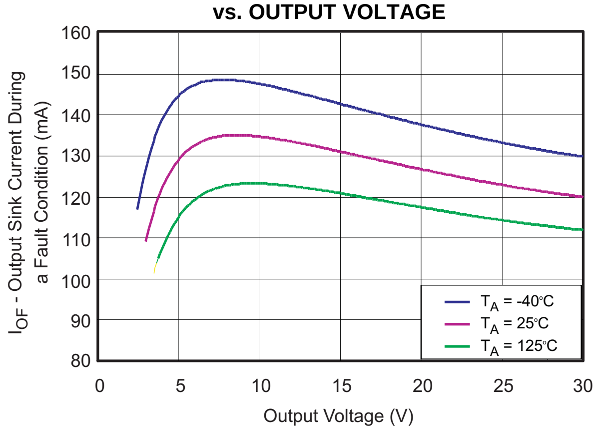


Figure 9.

HIGH OUTPUT VOLTAGE DROP vs. TEMPERATURE

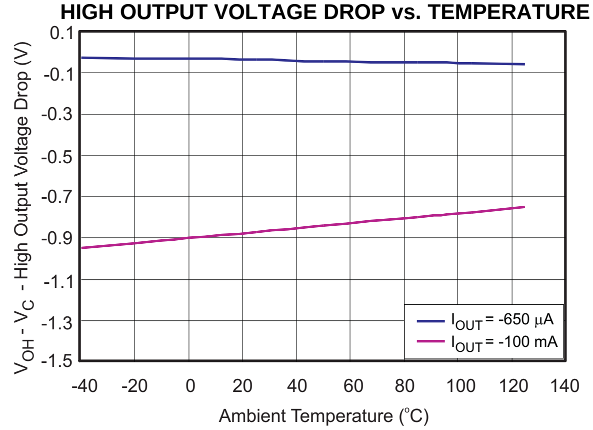


Figure 10.

HIGH OUTPUT VOLTAGE vs. OUTPUT DRIVE CURRENT

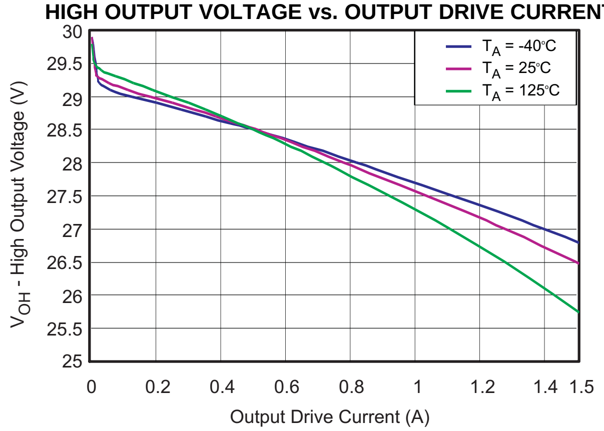


Figure 11.

LOW OUTPUT VOLTAGE vs. TEMPERATURE

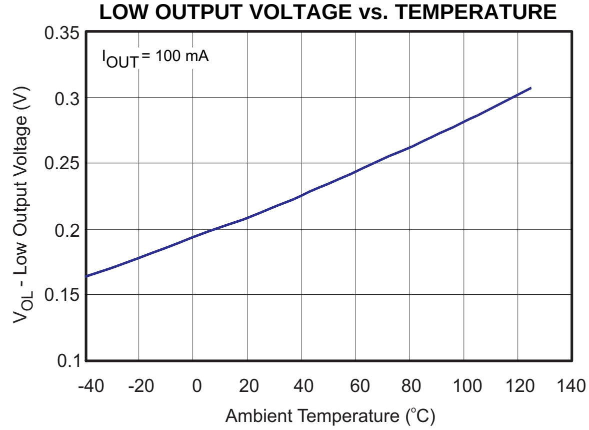


Figure 12.

TYPICAL CHARACTERISTICS (continued)

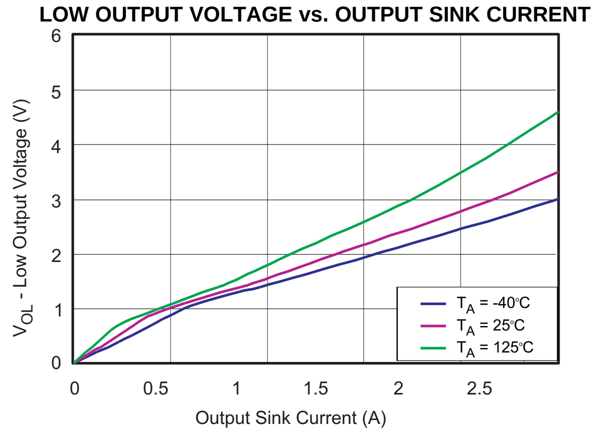


Figure 13.

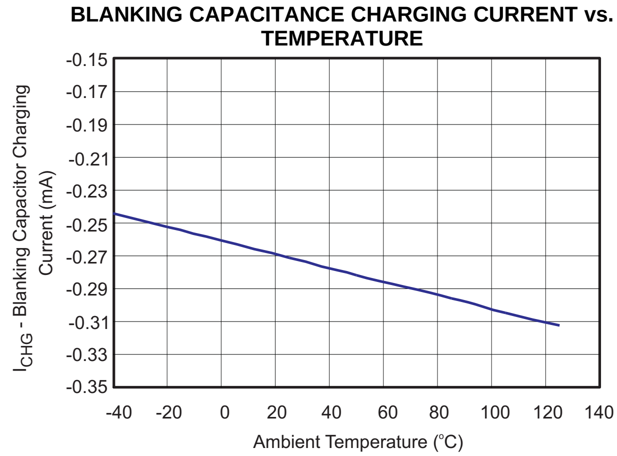


Figure 14.

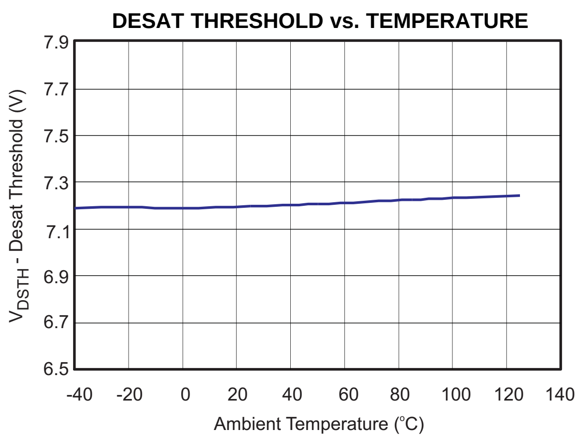


Figure 15.

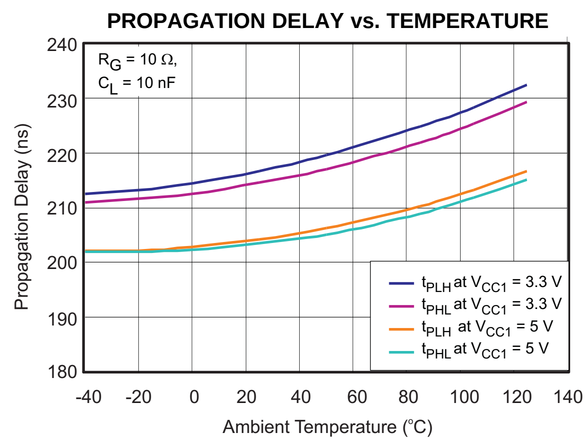


Figure 16.

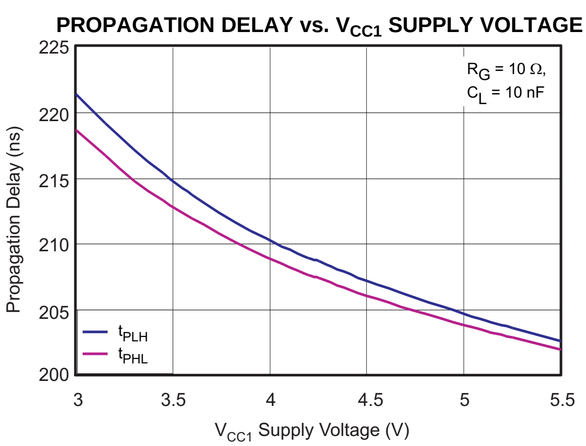


Figure 17.

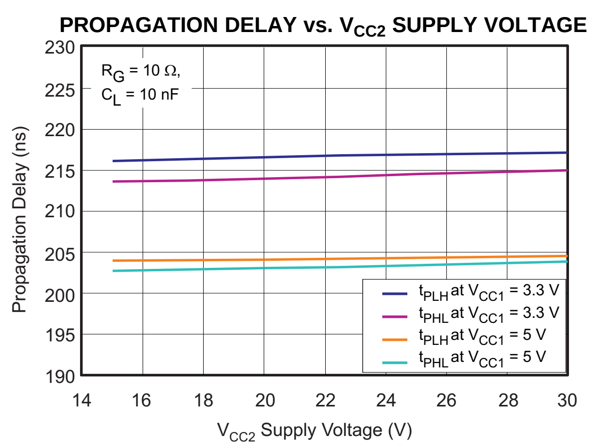


Figure 18.

TYPICAL CHARACTERISTICS (continued)

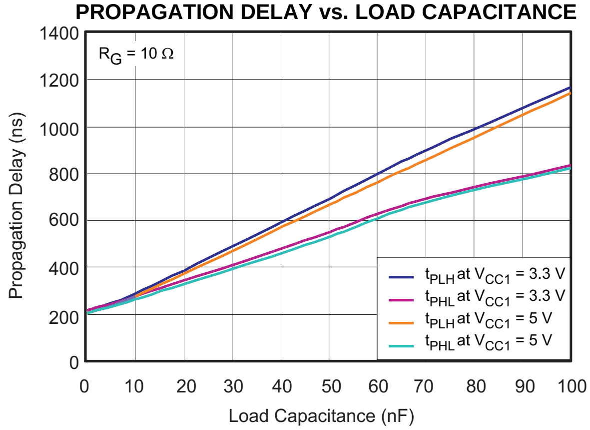


Figure 19.

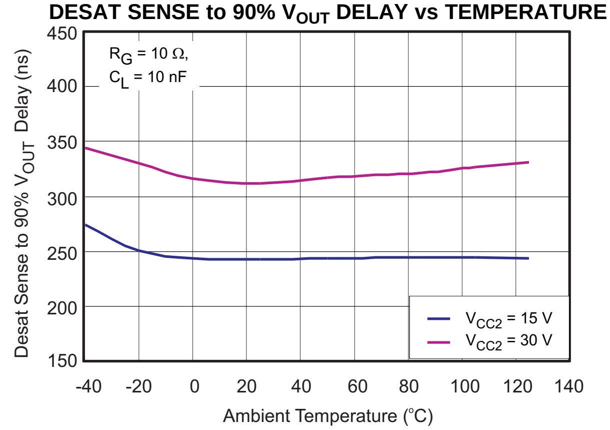


Figure 20.

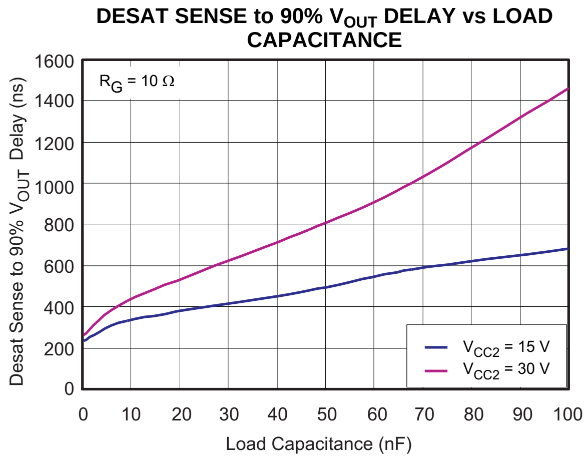


Figure 21.

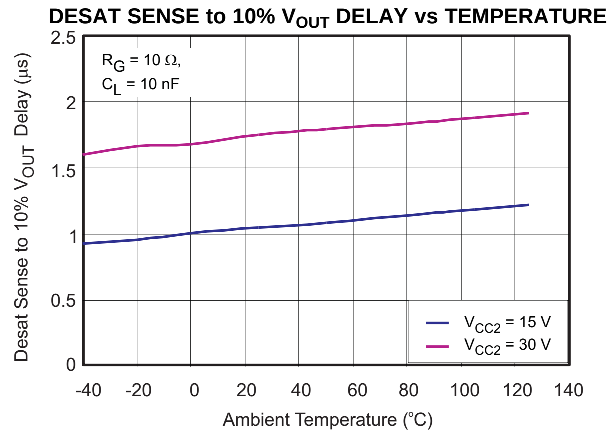


Figure 22.

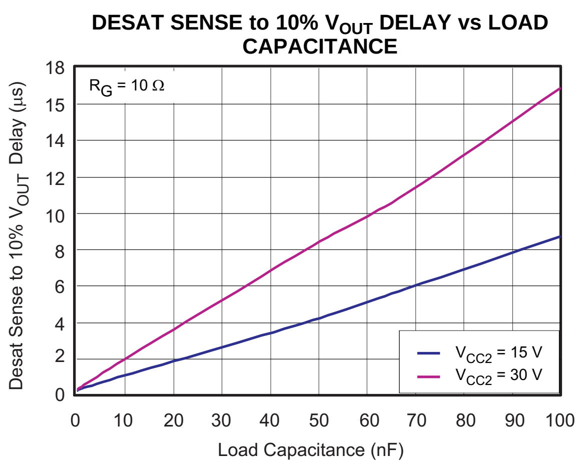


Figure 23.

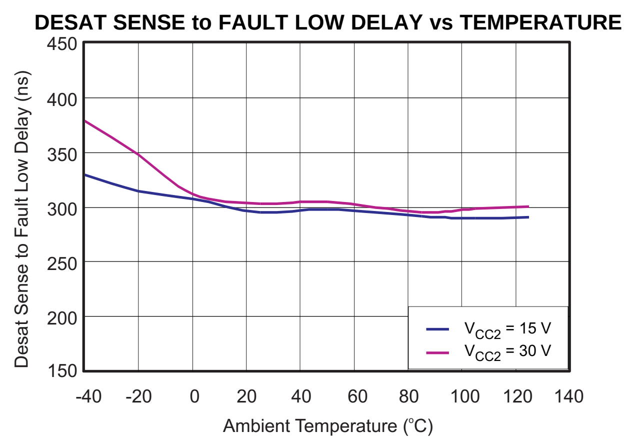


Figure 24.

TYPICAL CHARACTERISTICS (continued)

RESET to FAULT DELAY vs TEMPERATURE

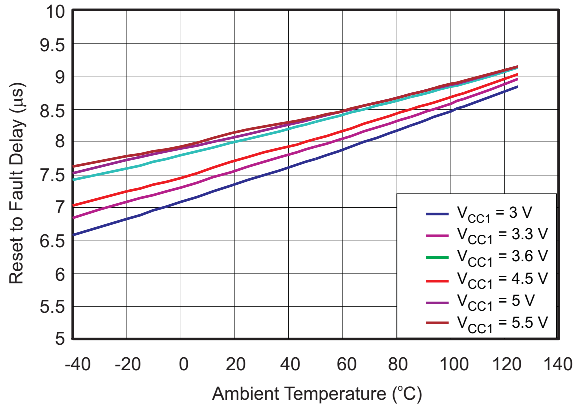


Figure 25.

OUTPUT WAVEFORM

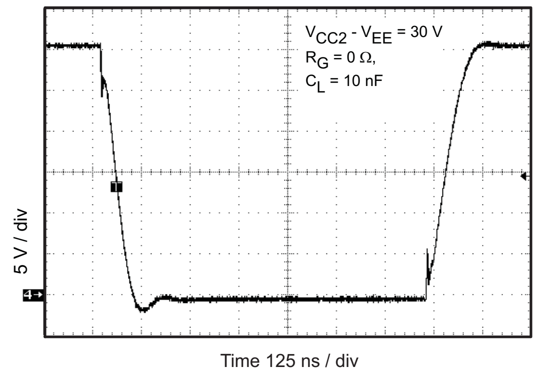


Figure 26.

V_C SUPPLY CURRENT vs. TEMPERATURE

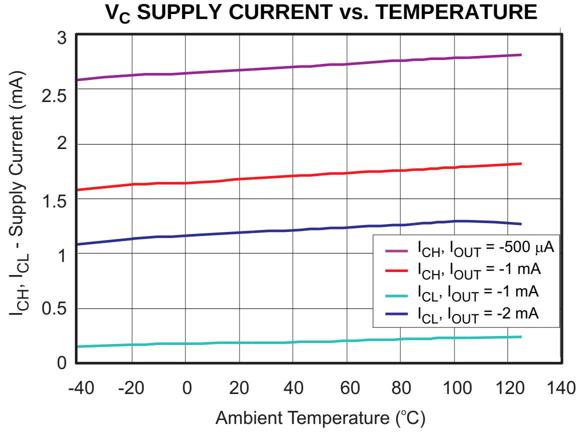


Figure 27.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUITS

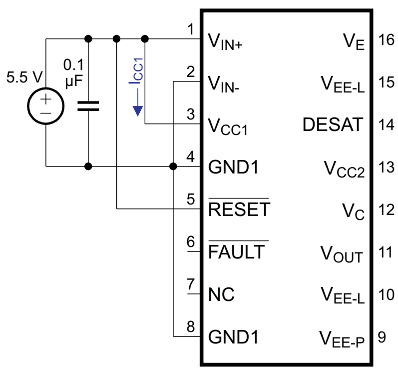


Figure 28. I_{CC1H} Test Circuit

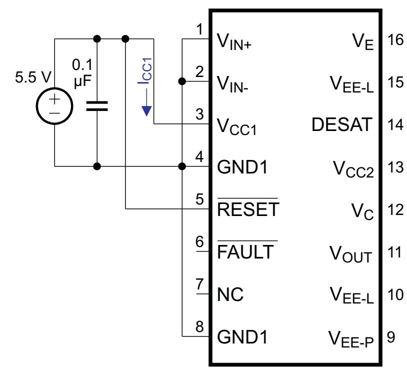


Figure 29. I_{CC1L} Test Circuit

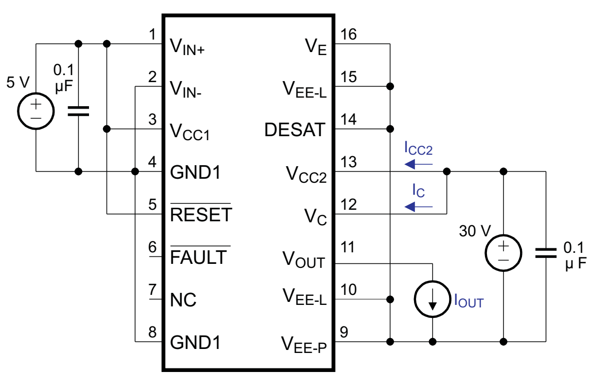


Figure 30. I_{CC2H}, I_{CH} Test Circuit

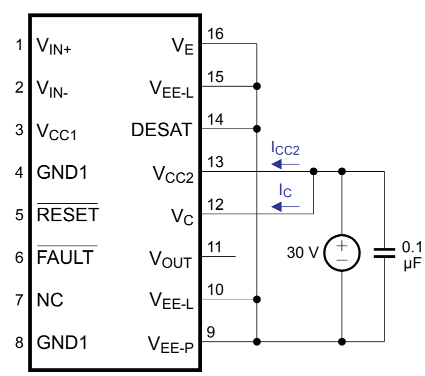


Figure 31. I_{CC2L}, I_{CL} Test Circuit

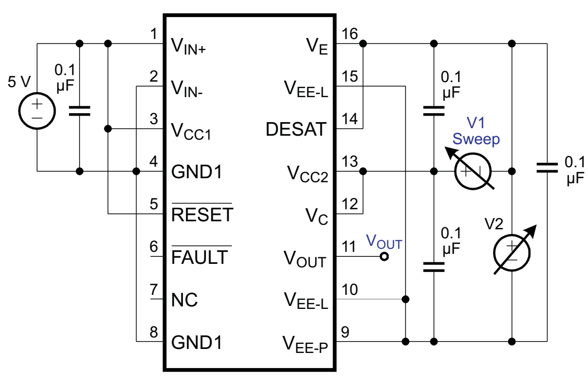


Figure 32. $V_{IT(UVLO)}$ Test Circuit

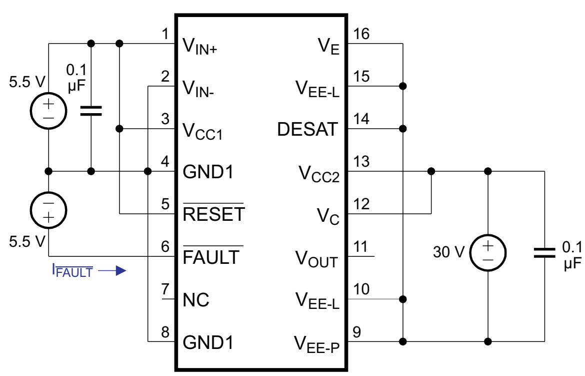


Figure 33. I_{FH} Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

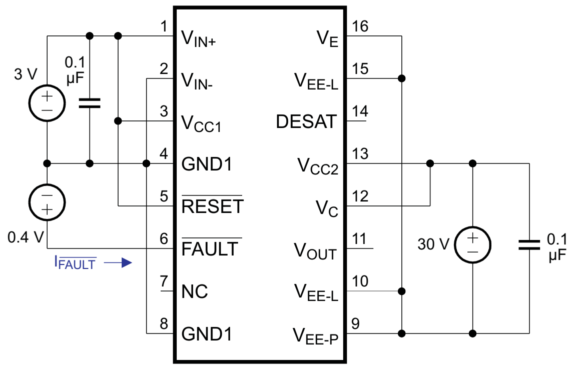


Figure 34. I_{FL} Test Circuit

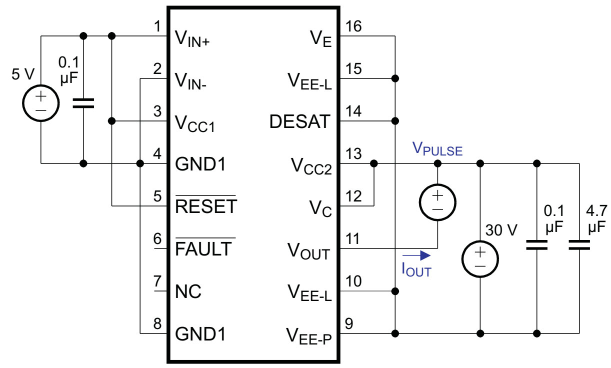


Figure 35. I_{OH} Test Circuit

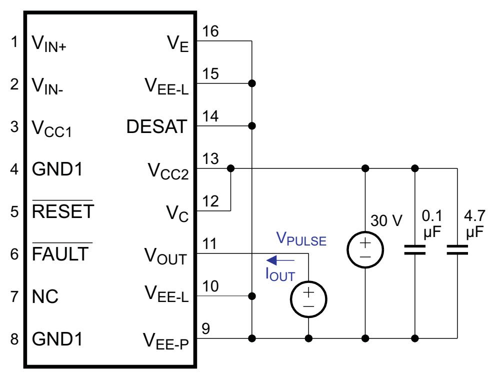


Figure 36. I_{OL} Test Circuit

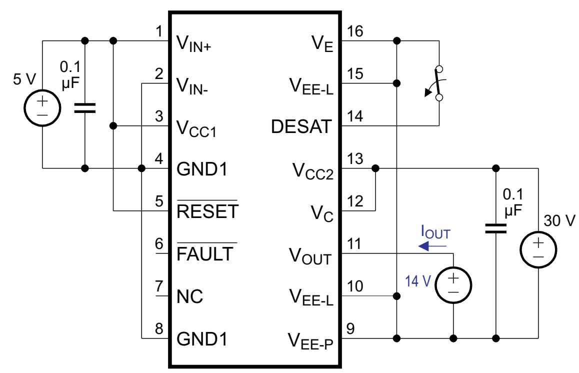


Figure 37. I_{OF} Test Circuit

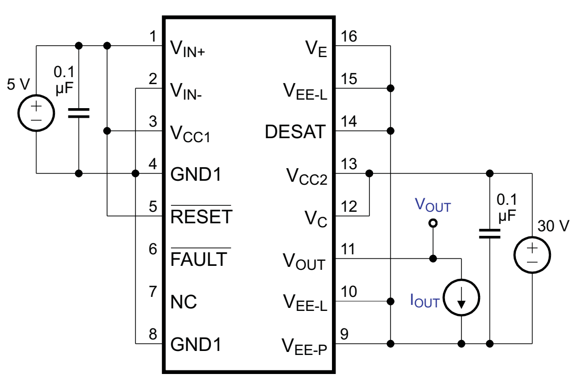


Figure 38. V_{OH} Test Circuit

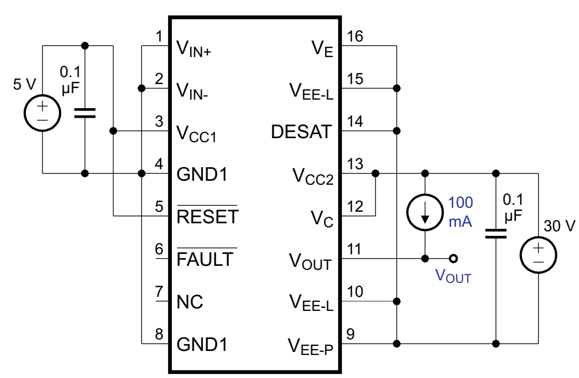


Figure 39. V_{OL} Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

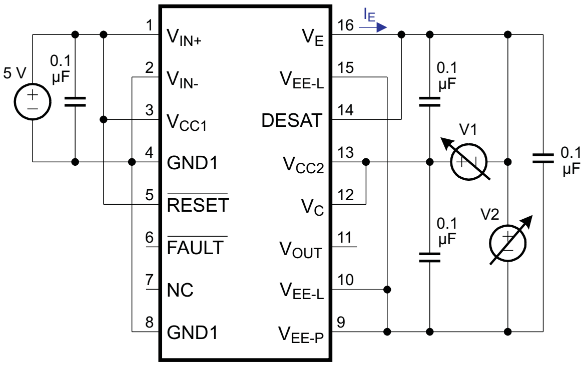


Figure 40. I_{EH} Test Circuit

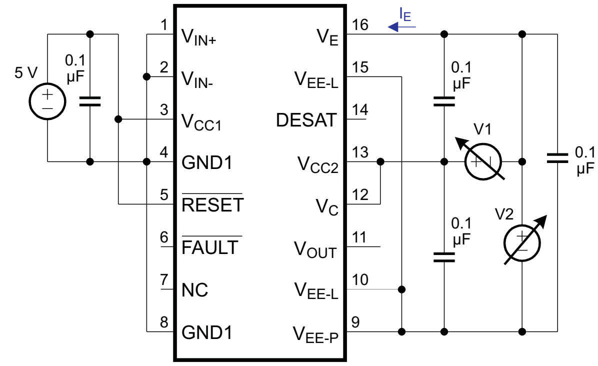


Figure 41. I_{EL} Test Circuit

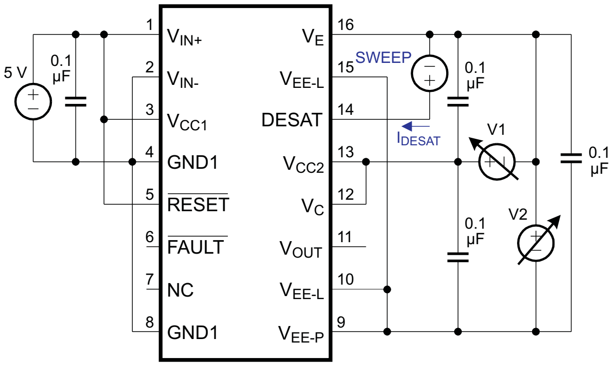


Figure 42. I_{CHG}, I_{DSCHG}, V_{DSTH} Test Circuit

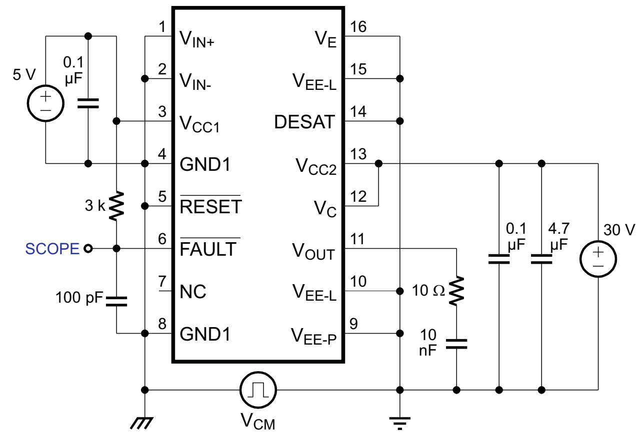


Figure 43. CMTI V_{FH} Test Circuit

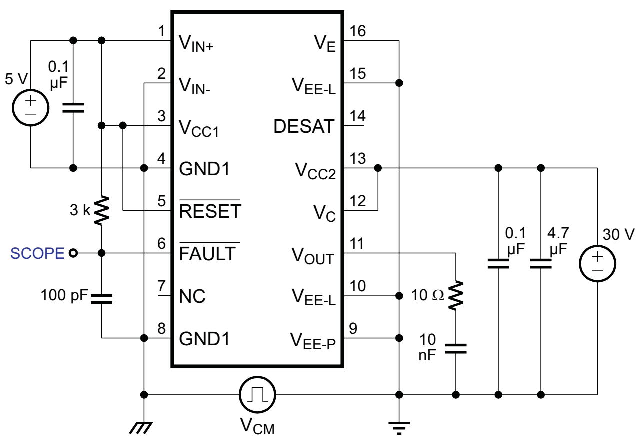


Figure 44. CMTI V_{FL} Test Circuit

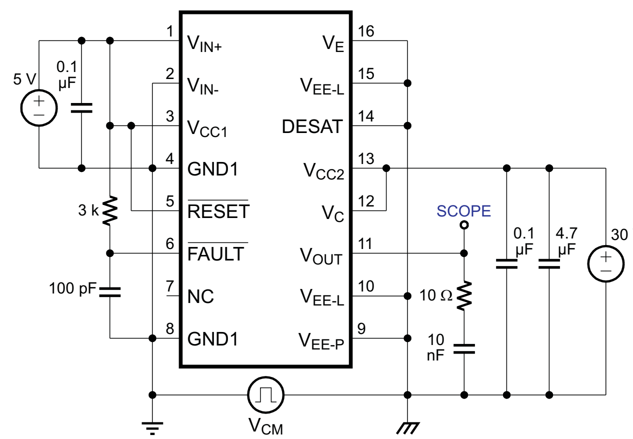


Figure 45. CMTI V_{OH} Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

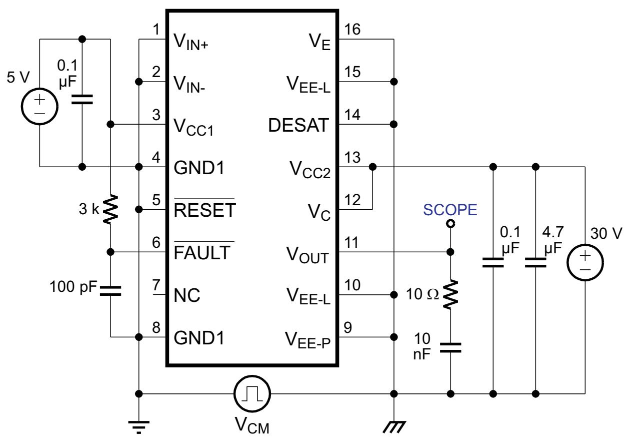


Figure 46. CMTI V_{OL} Test Circuit

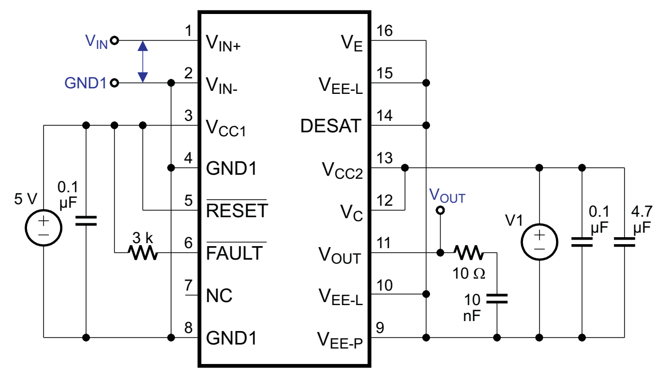


Figure 47. t_{PLH}, t_{PHL}, t_r, t_f Test Circuit

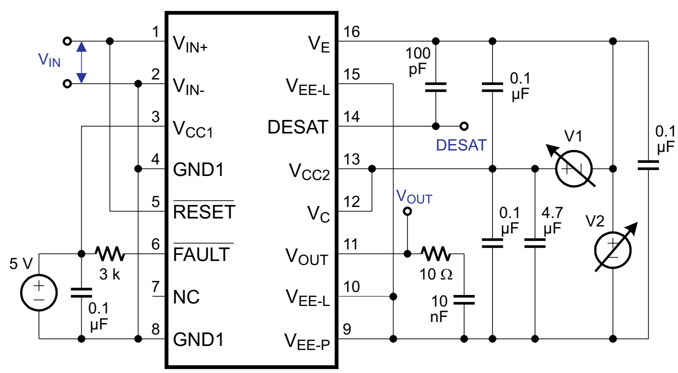


Figure 48. t_{DESAT}, $t_{\overline{RESET}}$ Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

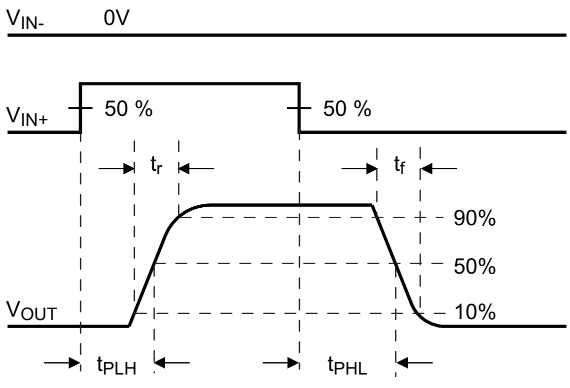


Figure 49. V_{OUT} Propagation Delay, Non-inverting Configuration

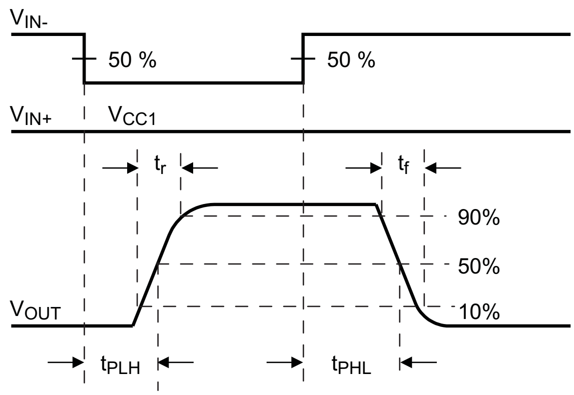


Figure 50. V_{OUT} Propagation Delay, Inverting Configuration

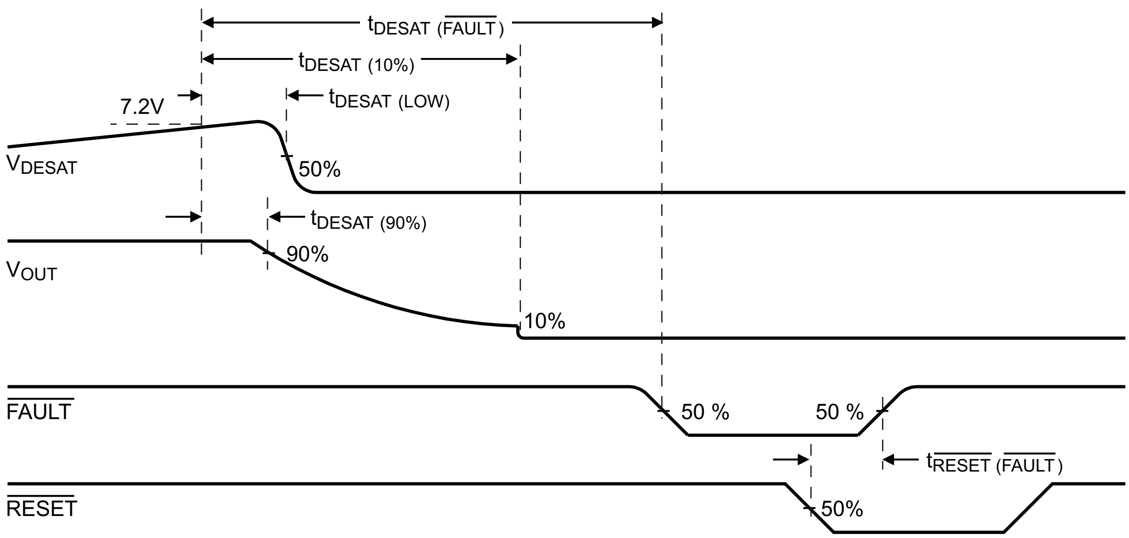


Figure 51. DESAT, V_{OUT}, $\overline{FAULT}$, $\overline{RESET}$ Delays

PARAMETER MEASUREMENT INFORMATION (continued)

PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$L_{(I01)}$	Minimum air gap (clearance[1])	Shortest terminal to terminal distance through air	8.3			mm
$L_{(I02)}$	Minimum external tracking (creepage[1])	Shortest terminal to terminal distance across the package surface	8.1			mm
	Minimum internal gap (internal clearance)	Distance through the insulation	0.012			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	400			V
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V[2]		$>10^{12}$		Ω
C_{IO}	Barrier capacitance input-to-output	V_{IO} = 0.4 sin (2πft), f = 1 MHz[2]		1.25		pF
C_I	Input capacitance to ground	$V_I = V_{CC}/2$ + 0.4 sin (2π ft), f = 2 MHz, V_{CC} = 5V		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the isolation glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase their specification.
(2) All pins on each side of the barrier tied together creating a two-terminal device

INSULATION CHARACTERISTICS FOR DW-16 PACKAGE

Over recommended operating conditions (unless noted otherwise)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage per DIN EN 60747-5-2		1200/848	V_{PEAK}/V_{RMS}
V_{PR}	Input to output test voltage per DIN EN 60747-5-2	After Input/Output safety test subgroup 2/3, $V_{PR} = 1.2 \times V_{IORM}$, t = 10 sec, Partial discharge < 5 pC	1440/1018	
		Method a, After environmental tests subgroup 1, $V_{PR} = 1.6 \times V_{IORM}$, t = 10 sec (qualification) Partial discharge < 5pC	1920/1358	
		Method b1, 100% Production test, $V_{PR} = 1.875 \times V_{IORM}$, t = 1 sec Partial discharge < 5pC	2250/1591	
V_{IOTM}	Transient overvoltage per DIN EN 60747-5-2	$V_{TEST} = V_{IOTM}$, t = 60 sec (qualification), t = 1 sec (100% production)	6000/4243	
V_{ISO}	Isolation voltage per UL 1577	$V_{TEST} = V_{ISO}$, t = 60 sec (qualification)	6000/4243	
		$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 sec (100% production)	7200/5092	
R_S	Insulation resistance	V_{IO} = 500 V at T_S = 150°C	$> 10^9$	Ω
	Pollution degree		2	

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to DIN EN 60747-5-2 and EN 61010-1	Approved under CSA Component Acceptance Notice 5A	Recognized under 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 6000 V_{PK} Maximum Working Voltage, 1200 V_{PK}	Basic and Reinforced Insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed)	Single Protection, 4243 V_{RMS} [1]
File Number: pending	File Number: pending	File Number: E181974

(1) Production tested ≥ 5092 V_{RMS} for 1 second in accordance with UL 1577.

IEC 60664-1 RATING TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation Classification	Rated Mains Voltage ≤ 300 V_{RMS}	I-IV
	Rated Mains Voltage ≤ 600 V_{RMS}	I-III
	Rated Mains Voltage ≤ 848 V_{RMS}	I-II

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety Limiting Current	θ_{JA} = 76°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			530	mA
		θ_{JA} = 76°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			347	
		θ_{JA} = 76°C/W, V_I = 30 V, T_J = 170°C, T_A = 25°C			64	
T_S	Case Temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

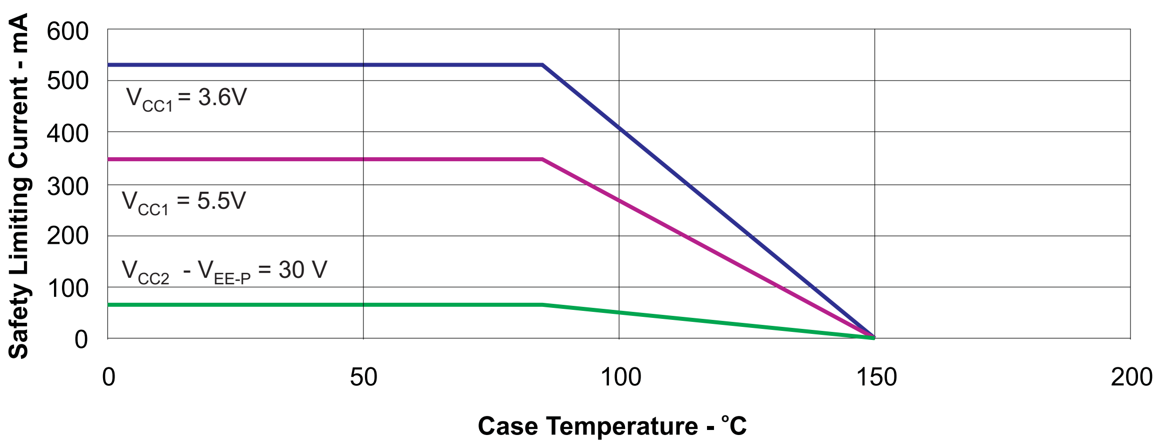


Figure 52. DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5.2

THERMAL INFORMATION

THERMAL METRIC[(1)]		ISO5500 DW (16) PIN	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	76	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34	
θ_{JB}	Junction-to-board thermal resistance	36	
ψ_{JT}	Junction-to-top characterization parameter	8	
ψ_{JB}	Junction-to-board characterization parameter	35	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	
T_{SHDN+}	Thermal Shutdown	185	°C
T_{SHDN-}		173	°C
$T_{SHDN-HYS}$	Thermal Shutdown Hysteresis	12	°C
P_D	Power Dissipation See Equation 2 through Equation 6	592	mW

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：SPRA953）。

BEHAVIORAL MODEL

Figure 53 and Figure 54 show the detailed behavioral model of the ISO5500 for a non-inverting input configuration and its corresponding timing diagram for normal operation, fault condition, and Reset.

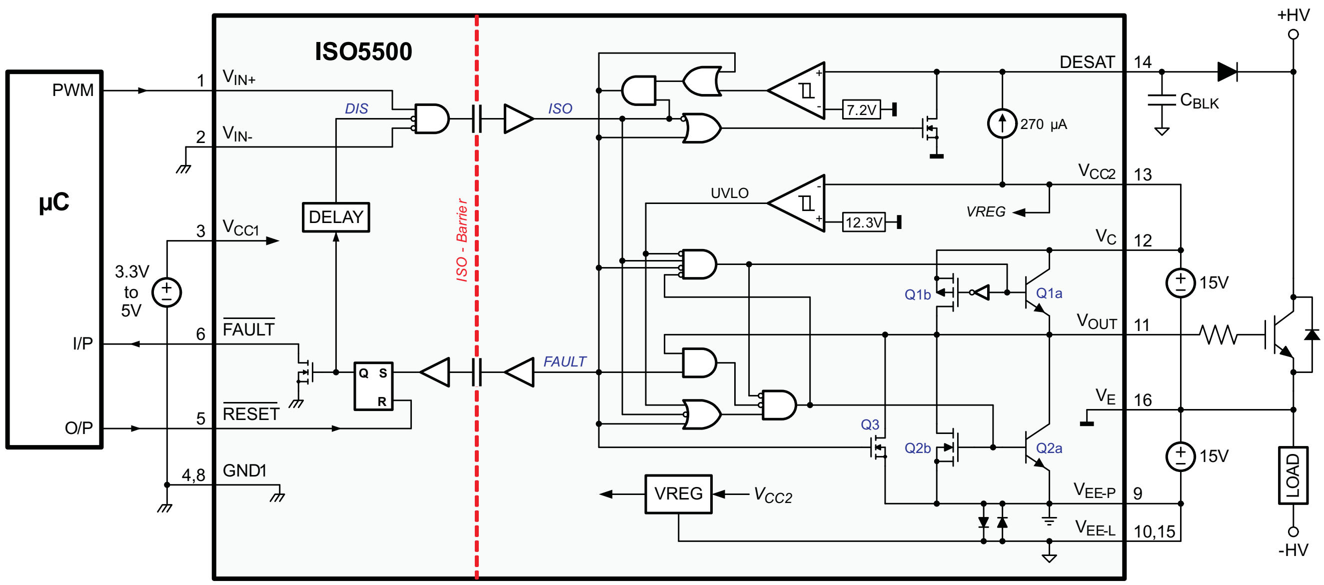


Figure 53. ISO5500 Behavioral Model

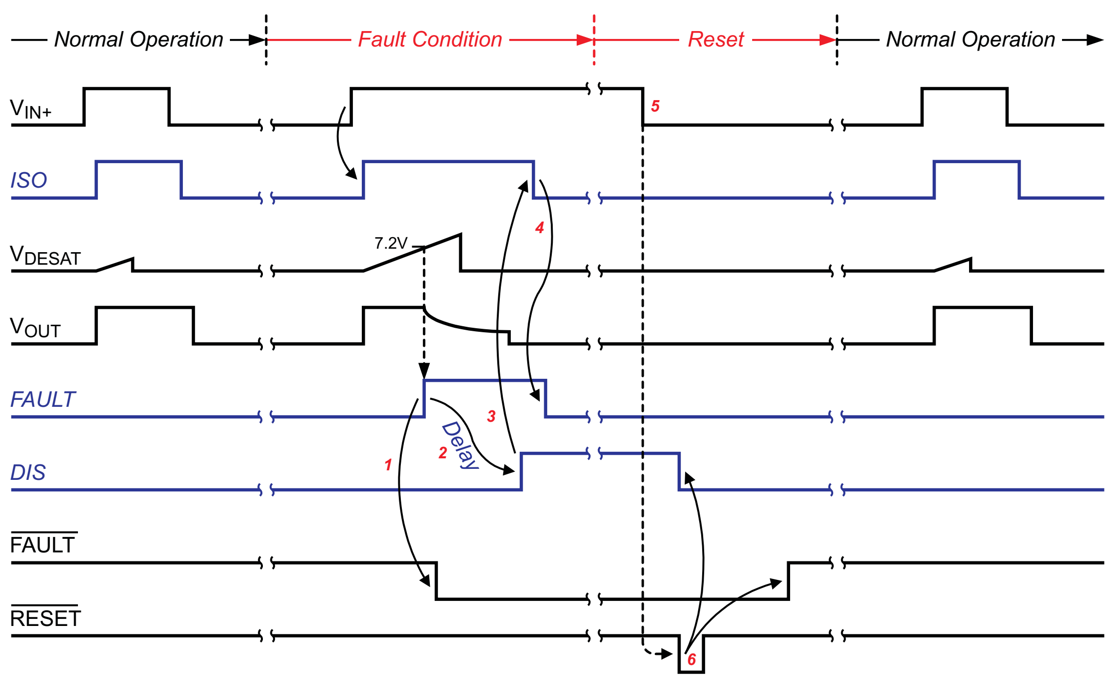


Figure 54. Complete Timing Diagram

DEVICE INFORMATION

POWER SUPPLIES

V_{CC1} and GND1 are the power supply input and output for the input side of the ISO5500. The supply voltage at V_{CC1} can range from 3 V up to 5.5 V with respect to GND1, thus supporting the direct interface to state-of-the-art 3.3 V low-power controllers as well as legacy 5 V controllers.

V_{CC2}, V_{EE-P} and V_{EE-L} are the power supply input and supply returns for the output side of the ISO5500. V_{EE-P} is the supply return for the output driver and V_{EE-L} is the return for the logic circuitry. With V_{EE-P} as the main reference potential, V_{EE-L} should always be directly connected to V_{EE-P}. The supply voltage at V_{CC2} can range from 15 V up to 30 V with respect to V_{EE-P}.

A third voltage input, V_E, serves as reference voltage input for the internal UVLO and DESAT comparators. V_E also represents the common return path for the gate voltage of the external power device. The ISO5500 is designed for driving MOSFETs and IGBTs. Because MOSFETs do not require a negative gate-voltage, the voltage potential at V_E with respect to V_{EE-P} can range from 0 V for MOSFETs and up to 15 V for IGBTs.

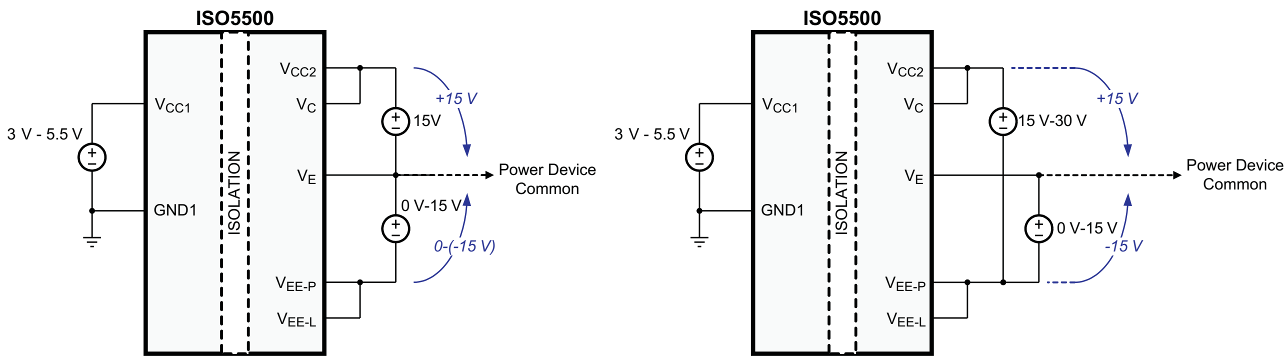


Figure 55. Power Supply Configurations

The output supply configuration on the left uses symmetrical ±15 V supplies for V_{CC2} and V_{EE-P} with respect to V_E. This configuration is mostly applied when deriving the output supply from the input supply via an isolated DC-DC converter with symmetrical voltage outputs. The configuration on the right, having both supplies referenced to V_{EE-P}, is found in applications where the device output supply is derived from the high-voltage IGBT supplies.

CONTROL SIGNAL INPUTS

The two digital, TTL control inputs, V_{IN+} and V_{IN-}, allow for inverting and non-inverting control of the gate driver output. In the non-inverting configuration V_{IN+} receives the control input signal and V_{IN-} is connected to GND1. In the inverting configuration V_{IN-} is the control input while V_{IN+} is connected to V_{CC1}.

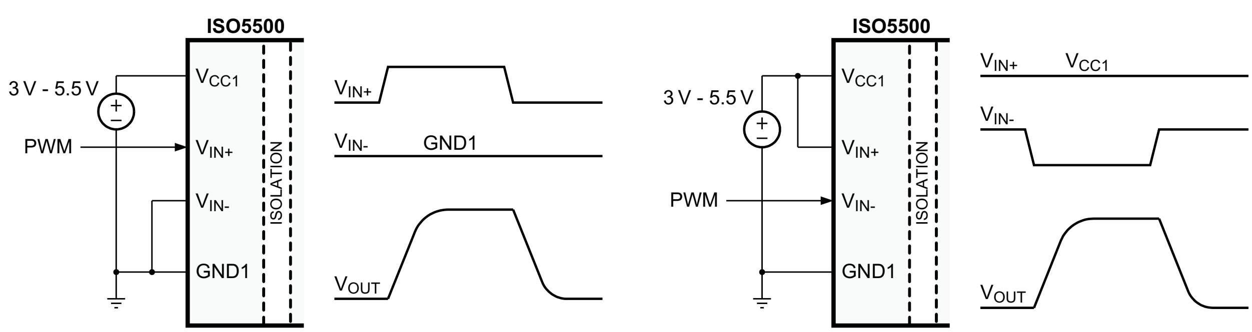


Figure 56. Non-inverting (left) and Inverting (right) Input Configurations

OUTPUT STAGE

The output stage provides the actual IGBT gate drive by switching the output voltage pin, V_{OUT}, between the most positive potential, typically V_{CC2}, and the most negative potential, V_{EE-P}.

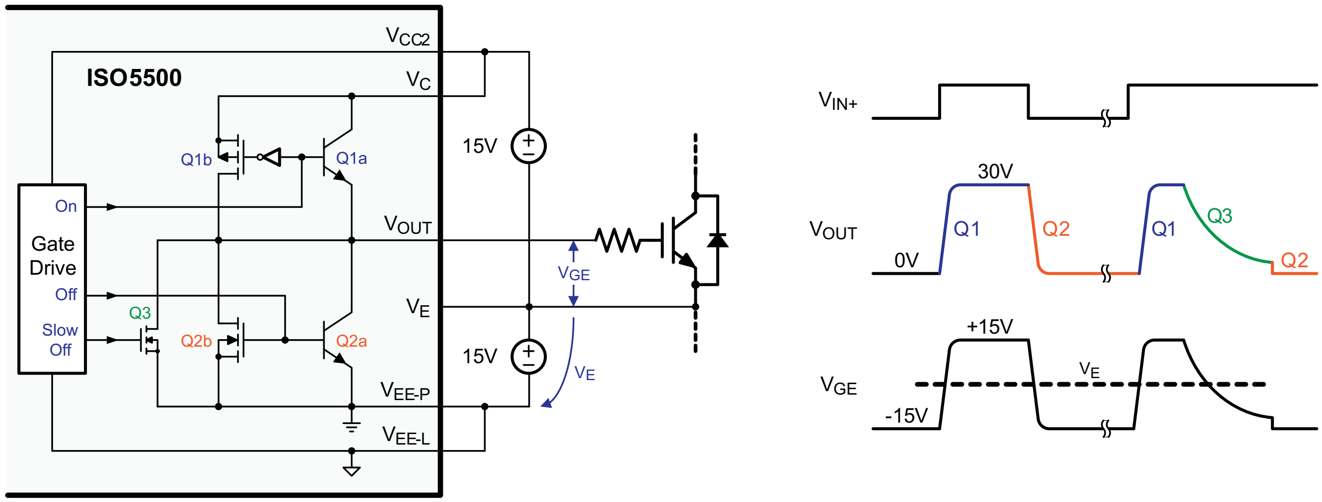


Figure 57. Output Stage Design and Timing

This stage consists of an upper transistor pair (Q1a and Q1b) turning the IGBT on, and a lower transistor pair (Q2a and Q2b) turning the IGBT off. Each transistor pair possesses a bipolar transistor for high current drive and a MOSFET for close-to-rail switching capability.

An additional, weak MOSFET (Q3) is used to softly turn-off the IGBT in the event of a short circuit fault to prevent large di/dt voltage transients which potentially could damage the output circuitry.

The output control signals, On, Off, and Slow-Off are provided by the gate-drive and fault-logic circuit which also includes a break-before-make function to prevent both transistor pairs from conducting at the same time.

By introducing the reference potential for the IGBT emitter, V_E, the final IGBT gate voltage, V_{GE}, assumes positive and negative values with respect to V_E.

A positive V_{GE} of typically 15 V is required to switch the IGBT well into saturation while assuring the survival of short circuit currents of up to 5–10 times the rated collector current over a time span of up to 10 μs.

Negative values of V_E, ranging from a required minimum of –5 V up to a recommended –15 V, are necessary to keep the IGBT turned off and to prevent it from unintentional conducting due to noise transients, particularly during short circuit faults. As previously mentioned, MOSFETs do not require a negative gate-voltage and thus allow the V_E-pin to be directly connected to V_{EE-P}.

The timing diagram in Figure 57 shows that during normal operation V_{OUT} follows the switching sequence of V_{IN+} (here shown for the non-inverting input configuration), and only the Q1 and Q2 transistor pairs applying V_{CC2} and V_{EE-P} potential to the V_{OUT}-pin respectively.

In the event of a short circuit fault, however, while the IGBT is actively driven, the Q1 pair is turned off and Q3 turns on to slowly reduce V_{OUT} in a controlled manner down to a level of approximately 2 V above V_{EE-P}. At this voltage level, the strong Q2 pair then conducts holding V_{OUT} at V_{EE-P} potential.

UNDER VOLTAGE LOCKOUT (UVLO)

The Under Voltage Lockout feature prevents the application of insufficient gate voltage (V_{GE-ON}) to the power device by forcing V_{OUT} low ($V_{OUT} = V_{EE-P}$) during power-up and whenever else $V_{CC2} – V_E$ drops below 12.3 V.

IGBTs and MOSFETs typically require gate voltages of V_{GE} = 15 V to achieve their rated, low saturation voltage, V_{CES}. At gate voltages below 13 V typically, their V_{CE-ON} increases drastically, especially at higher collector currents. At even lower voltages, i.e. V_{GE} < 10 V, an IGBT starts operating in the linear region and quickly overheats. Figure 58 shows the principle operation of the UVLO feature.

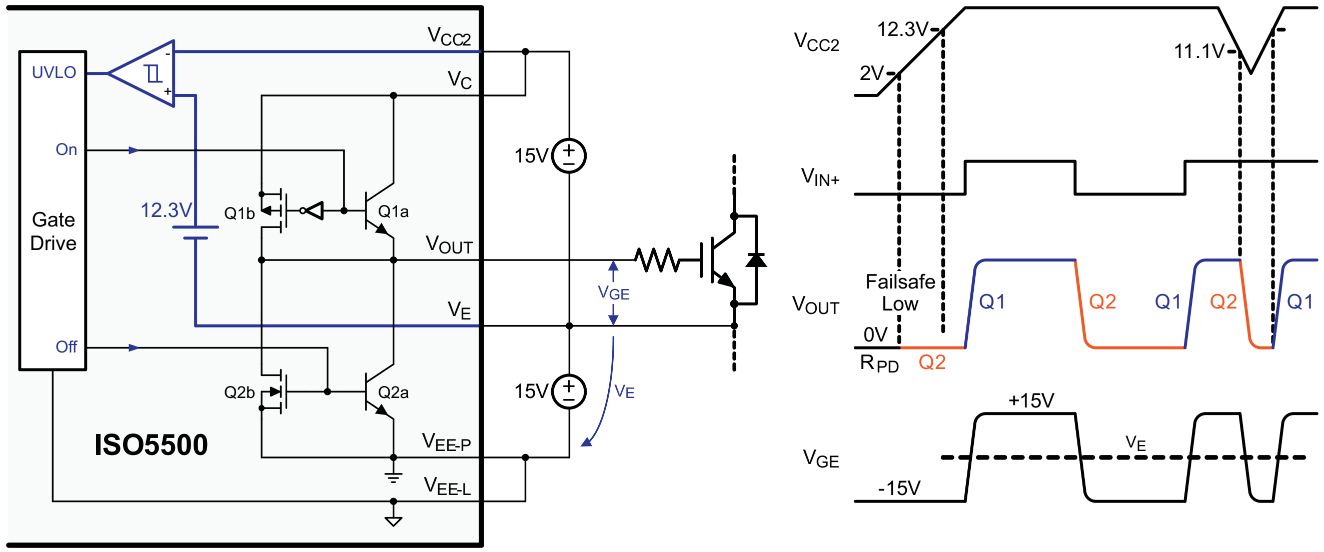


Figure 58. Under Voltage Lockout (UVLO) Function

Because V_{CC2} with respect to V_E represents the gate-on voltage, $V_{GE\text{-}ON} = V_{CC2} – V_E$, the UVLO comparator compares V_{CC2} to a 12.3 V reference voltage that is also referenced to V_E via the connection of the ISO5500 V_E-pin to the emitter potential of the power device.

The comparator hysteresis is 1.2 V typical and the typical values for the positive and negative going input threshold voltages are V_{TH+} = 12.3 V and $V_{TH–}$ = 11.1 V.

The timing diagram shows that at V_{CC2} levels below 2 V V_{OUT} is 0 V. Because none of the internal circuitry operates at such low supply levels, an internal 100 kΩ pull-down resistor is used to pull V_{OUT} down to $V_{EE\text{-}P}$ potential. This initial weak clamping, known as failsafe-low output, strengthens with rising V_{CC2}. Above 2 V the Q2-pair starts conducting gradually until V_{CC2} reaches 12.3 V at which point the logic states of the control inputs V_{IN+} and $V_{IN–}$ begin to determine the state of V_{OUT}.

Another UVLO event takes place should V_{CC2} drop slightly below 11 V while the IGBT is actively driven. At that moment the UVLO comparator output causes the gate-drive logic to turn off Q1 and turn on Q2. Now V_{OUT} is clamped hard to $V_{EE\text{-}P}$. This condition remains until V_{CC2} returns to above 12.3 V and normal operation commences.

NOTE

An Under Voltage Lockout does not indicate a Fault condition.

DESATURATION FAULT DETECTION (DESAT)

The DESAT fault detection prevents IGBT destruction due to excessive collector currents during a short circuit fault. Short circuits caused by user misconnect, bad wiring, or overload conditions induced by the load can cause a rapid increase in IGBT current, leading to excessive power dissipation and heating. IGBTs become damaged when the current load approaches the saturation current of the device and the collector-emitter voltage, V_{CE}, rises above the saturation voltage level, $V_{CE\text{-}sat}$. The drastically increased power dissipation overheats and destroys the IGBT.

To prevent damage to IGBT applications, the implemented fault detection slowly reduces the overcurrent in a controlled manner during the fault condition.

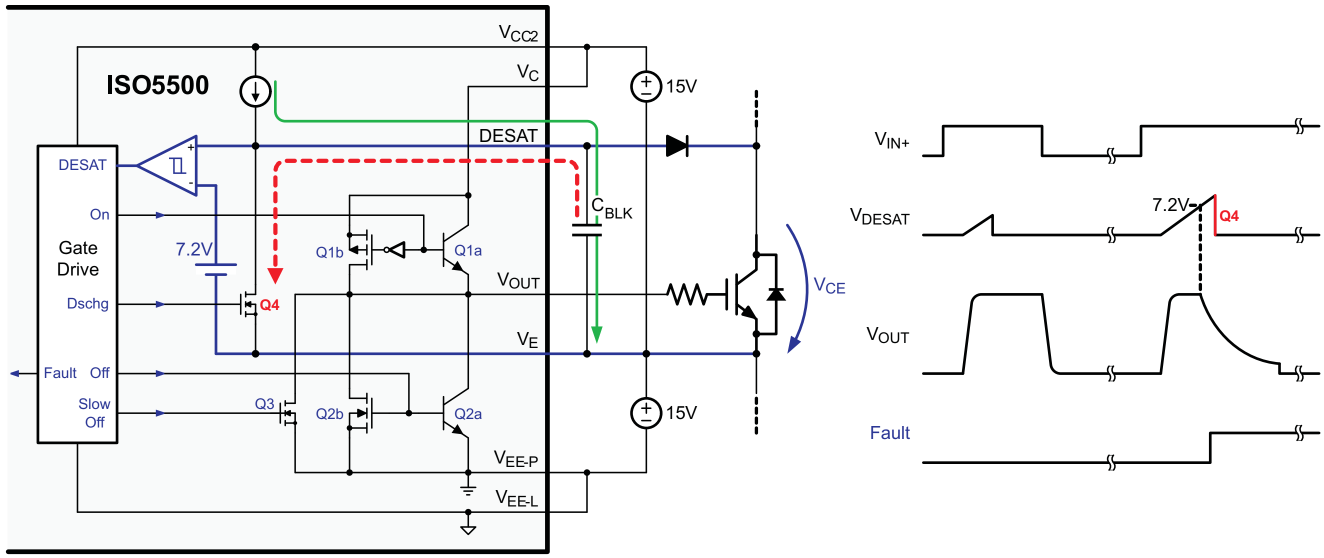


Figure 59. DESAT Fault Detection and Protection

The DESAT fault detection involves a comparator that monitors the IGBT's V_{CE} and compares it to an internal 7.2 V reference. If V_{CE} exceeds this reference voltage, the comparator causes the gate-drive and fault-logic to initiate a fault shutdown sequence. This sequence starts with the immediate generation of a fault signal, which is transmitted across the isolation barrier towards the Fault indicator circuit at the input side of the ISO5500.

At the same time the fault logic turns off the power-pair Q1 and turns on the small discharge MOSFETs, Q3 and Q4. Q3 slowly discharges the IGBT gate voltage which causes the high short-circuit current through the IGBT to gradually decrease, thereby preventing large di/dt induced voltage transients. Q4 discharges the blanking capacitor. Once V_{OUT} is sufficiently close to $V_{EE\text{-}P}$ potential (at approximately 2 V), the large Q2-pair turns on in addition to Q3 to clamp the IGBT gate to $V_{EE\text{-}P}$.

NOTE

The DESAT detection circuit is only active when the IGBT is turned on. When the IGBT is turned off, and its V_{CE} is at maximum, the fault detection is simply disabled to prevent false triggering of fault signals.

DESAT BLANKING TIME

The DESAT fault detection must remain disabled for a short time period following the turn-on of the IGBT to allow its collector voltage to drop below the 7.2 V DESAT threshold. This time period, called the DESAT blanking time, t_{BLK}, is controlled by an internal charge current of I_{CHG} = 270 μA, the 7.2 V DESAT threshold, V_{DSTH}, and an external blanking capacitor, C_{BLK}.

The nominal blanking time with a recommended capacitor value of C_{BLK} = 100 pF is calculated with:

$$t_{BLK} = \frac{C_{BLK} \times V_{DSTH}}{I_{CHG}} = \frac{100\ \text{pF} \times 7.2\ \text{V}}{270\ \mu\text{A}} = 2.7\ \mu\text{s} \tag{1}$$

The capacitor value can be scaled slightly to adjust the blanking time. However, because the blanking capacitor and the DESAT diode capacitance build a voltage divider that attenuates large voltage transients at DESAT, C_{BLK} values smaller than 100 pF are not recommended. The nominal blanking time also represents the ISO5500 maximum response time to a DESAT fault condition.

If a short circuit condition exists prior to the turn-on of the IGBT, (*causing the IGBT switching into a short*) the soft shutdown sequence begins after approximately 3 μs. However, if a short circuit condition occurs while the IGBT is already on, the response time is significantly shorter due to the parasitic parallel capacitance of the DESAT diode. The recommended value of 100 pF however, provides sufficient blanking and fault response times for most applications.

The timing diagram in Figure 59 shows the DESAT function for both, normal operation and a short-circuit fault condition. The use of V_{IN+} as control input implies non-inverting input configuration.

During normal operation V_{DESAT} will display a small sawtooth waveform every time V_{IN+} goes high. The ramp of the sawtooth is caused by the internal current source charging the blanking capacitor. Once the IGBT collector has sufficiently dropped below the capacitor voltage, the DESAT diode conducts and discharges C_{BLK} through the IGBT.

In the event of a short circuit fault; however, high IGBT collector voltage prevents the diode from conducting and the voltage at the blanking capacitor continues to rise until it reaches the DESAT threshold. When the output of the DESAT comparator goes high, the gate-drive and fault-logic circuit initiates the soft shutdown sequence and also produces a Fault signal that is fed back to the input side of the ISO5500.

$\overline{\text{FAULT}}$ ALARM

The Fault alarm unit consists of three circuit elements, a RS flip-flop to store the fault signal received from the gate-drive and fault-logic, an open-drain MOSFET output signaling the fault condition to the micro controller, and a delay circuit blocking the control inputs after the soft shutdown sequence of the IGBT has been completed.

Figure 60 shows the ISO5500 in a non-inverting input configuration. Because the $\overline{\text{FAULT}}$-pin is an open-drain output, it requires a pull-up resistor, R_{PU}, in the order of 3.3 kΩ to 10 kΩ. The internal signals DIS, ISO, and FAULT represent the input-disable signal, the isolator output signal, and the fault feedback signal respectively.

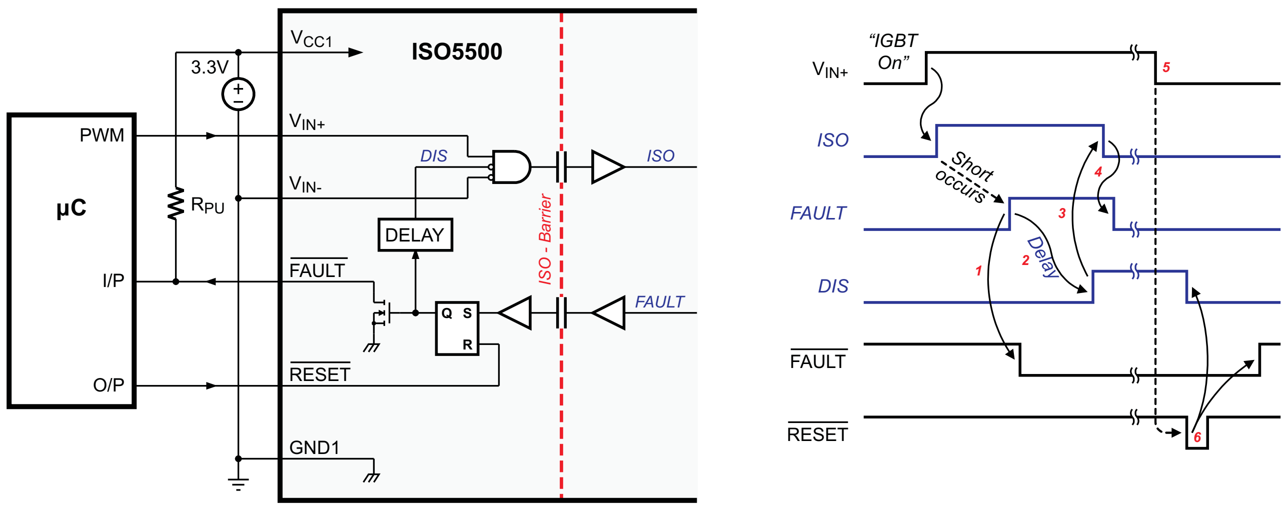


Figure 60. Fault Alarm Circuitry and Timing Sequence

The timing diagram shows that the micro controller initiates an IGBT-on command by taking V_{IN+} high. After propagating across the isolation barrier ISO goes high, activating the output stage.

1. Upon a short circuit condition the gate-drive and fault-logic feeds back a fault signal (*FAULT = high*) which sets the RS-FF driving the $\overline{\text{FAULT}}$ output active-low.
2. After a delay of approximately 3 µs, the time required to shutdown the IGBT, *DIS* becomes high and blocks the control inputs
3. This in turn drives *ISO* low
4. which, after propagating through the output fault-logic, drives *FAULT* low.

   At this time both flip-flop inputs are low and the fault signal is stored.
5. Once the failure cause has been removed the micro controller must set the control inputs into an "Output-low" state before applying the Reset pulse.
6. Taking the $\overline{\text{RESET}}$-input low resets the flip-flop, which removes the fault signal from the controller by pulling $\overline{\text{FAULT}}$ high and releases the control inputs by driving *DIS* low

APPLICATION INFORMATION

TYPICAL APPLICATION

Figure 61 shows the typical application of a three-phase inverter using six ISO5500 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed of AC motors and for high power applications such as High-Voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of three single-phase inverter switches each comprising two ISO5500 devices that are connected to one of the three load terminals. The operation of the three switches is coordinated so that one switch operates at each 60 degree point of the fundamental output waveform, thus creating a six-step line-to-line output waveform. In this type of applications carrier-based PWM techniques are applied to retain waveform envelope and cancel harmonics.

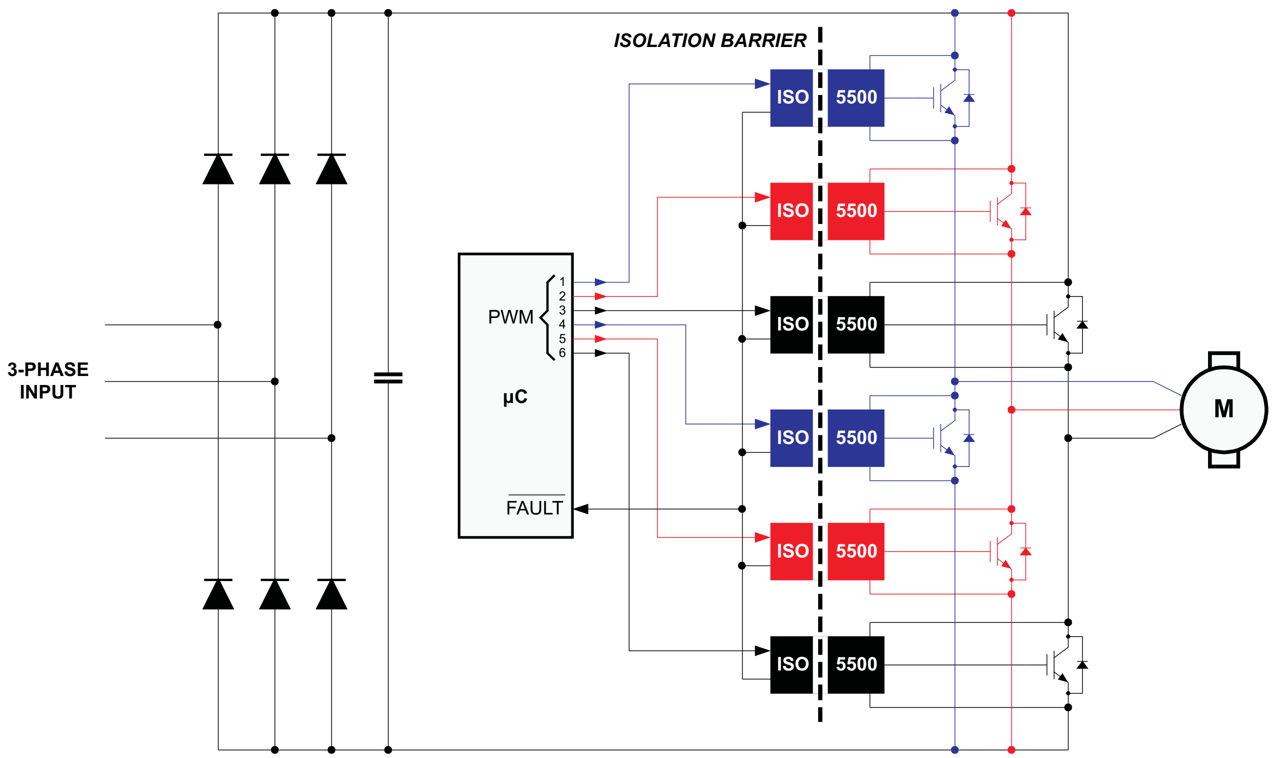


Figure 61. Typical Motor Drive Application

RECOMMENDED ISO5500 APPLICATION CIRCUIT

The ISO5500 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open drain fault output suitable for wired-OR applications. The recommended application circuit in Figure 62 illustrates a typical gate drive implementation using the ISO5500.

The four 0.1 µF supply bypass capacitors provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, low current (20 mA) power supplies for V_{CC2} and V_{EE-P} suffice. The 100 pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode and its 100 Ω series resistor are important external protection components for the fault detection circuitry. The 10 Ω gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain fault output has a passive 3.3 kΩ pull-up resistor and a 330pF filtering capacitor. In this application, the IGBT gate driver will shut down when a fault is detected and will not resume switching until the micro-controller applies a reset signal.

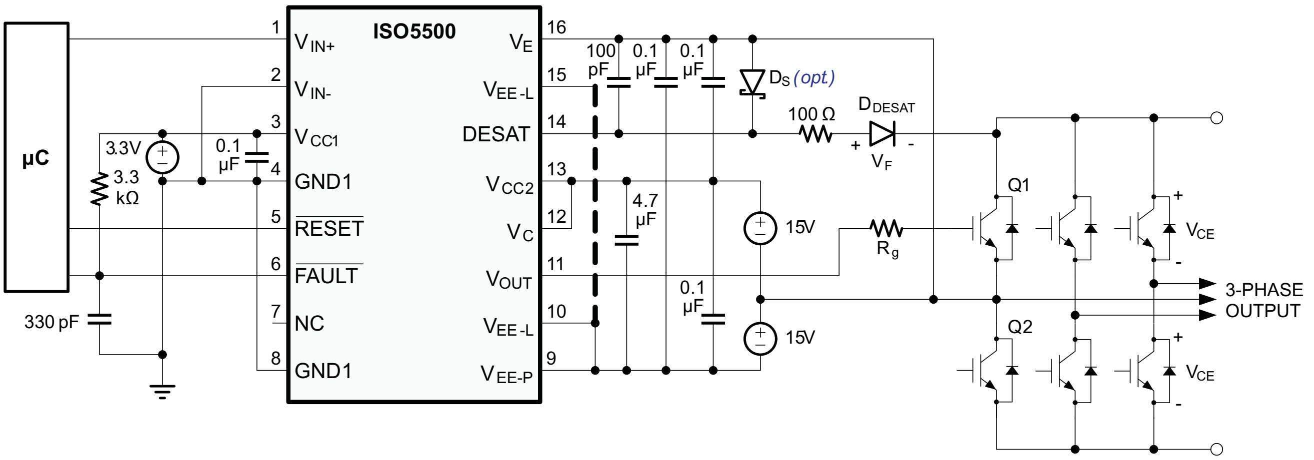


Figure 62. Recommended Application Circuit

$\overline{\text{FAULT}}$ PIN CIRCUITRY

The $\overline{\text{FAULT}}$ pin is an open-drain output requiring a 3.3 kΩ pull-up resistor to provide logic high when $\overline{\text{FAULT}}$ is inactive.

Because fast common mode transients can alter the $\overline{\text{FAULT}}$-pin voltage during high state, a 330 pF capacitor connected between $\overline{\text{FAULT}}$ and GND1 is recommended to provide sufficient noise margin at the specified CMTI of 50 kV/µs. The added capacitance does not increase the $\overline{\text{FAULT}}$ response time during a fault condition.

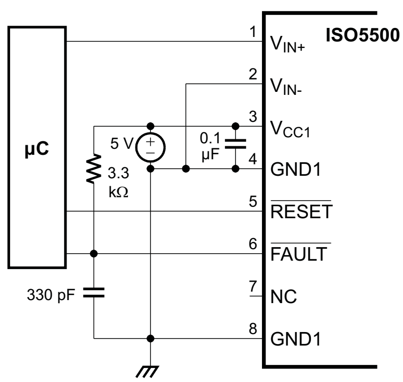


Figure 63. $\overline{\text{FAULT}}$ Pin Circuitry for High CMTI

DRIVING THE CONTROL INPUTS

The amount of common-mode transient immunity (CMTI) is primarily determined by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5500. For maximum CMTI performance, the digital control inputs, V_{IN+} and V_{IN-}, must be actively driven by standard CMOS or TTL, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5500 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pull-up resistors, must be avoided.

LOCAL SHUTDOWN AND RESET

In applications with local shutdown and reset, the $\overline{\text{FAULT}}$ output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

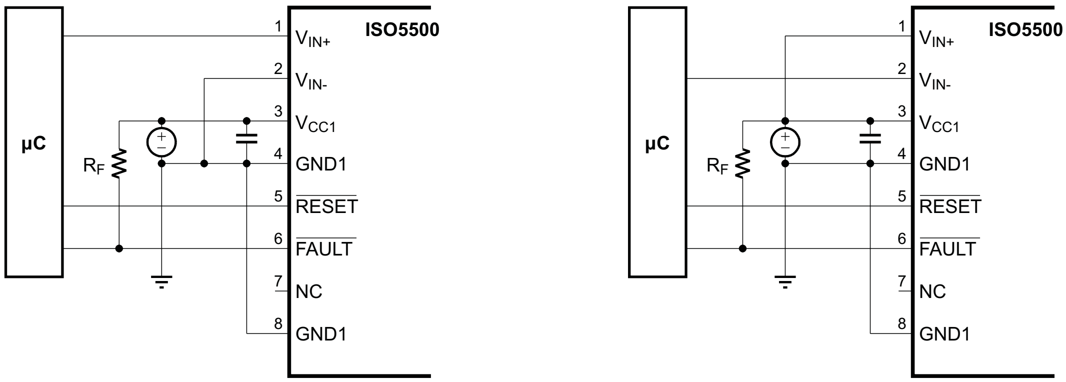


Figure 64. Local Shutdown and Reset for Non-inverting (left) and Inverting Input Configuration (right)

GLOBAL-SHUTDOWN AND RESET

When configured for inverting operation, the ISO5500 can be configured to shutdown automatically in the event of a fault condition by tying the $\overline{\text{FAULT}}$ output to V_{IN+}. For high reliability drives, the open drain $\overline{\text{FAULT}}$ outputs of multiple ISO5500 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low $\overline{\text{FAULT}}$ output disables all six gate drivers simultaneously; thereby, providing protection against further catastrophic failures.

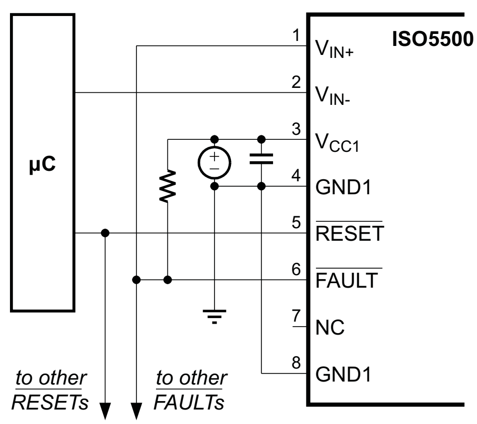


Figure 65. Global Shutdown with Inverting Input Configuration

AUTO-RESET

Connecting $\overline{\text{RESET}}$ to the active control input (V_{IN+} for non-inverting, or V_{IN-} for inverting operation) configures the ISO5500 for automatic reset capability. In this case, the gate control signal at V_{IN} is also applied to the $\overline{\text{RESET}}$ input to reset the fault latch every switching cycle. During normal IGBT operation, asserting $\overline{\text{RESET}}$ low has no effect on the output. For a fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the 'gate low' state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before V_{IN+} goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next 'on' cycle. When the ISO5500 is configured for Auto Reset, the specified minimum $\overline{\text{FAULT}}$ signal pulse width is 3 µs.

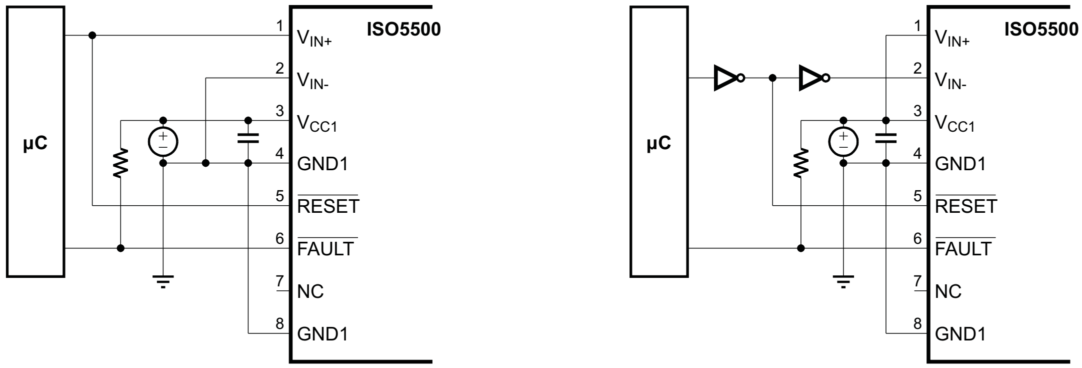


Figure 66. Auto Reset for Non-inverting and Inverting Input Configuration

RESETTING FOLLOWING A FAULT CONDITION

To resume normal switching operation following a fault condition ($\overline{\text{FAULT}}$ output low), the gate control signal must be driven into a 'gate low' state before asserting $\overline{\text{RESET}}$ low. This can be accomplished with a micro-controller, or an additional logic gate that synchronizes the $\overline{\text{RESET}}$ signal with the appropriate input signal.

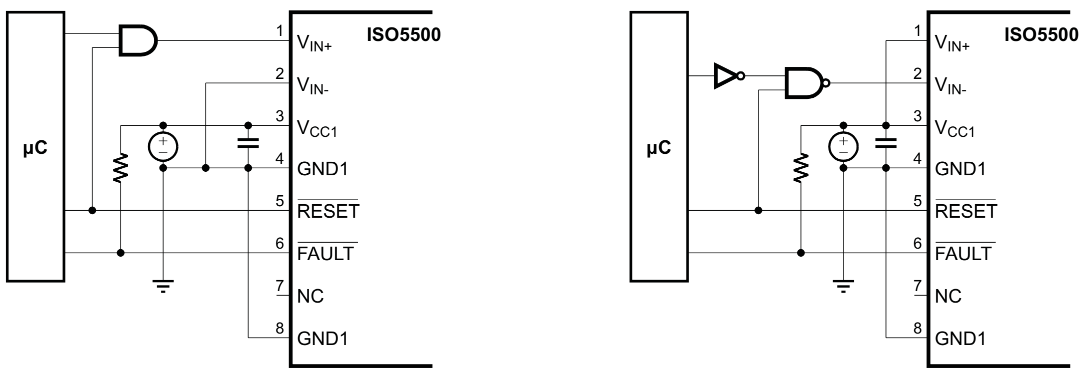


Figure 67. Auto Reset with Prior Gate-low Assertion for Non-inverting and Inverting Input Configuration

DESAT PIN PROTECTION

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100 Ω to 1 kΩ resistor is connected in series with the DESAT diode. The added resistance neither alters the DESAT threshold nor the DESAT blanking time.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to V_E potential at low voltage levels.

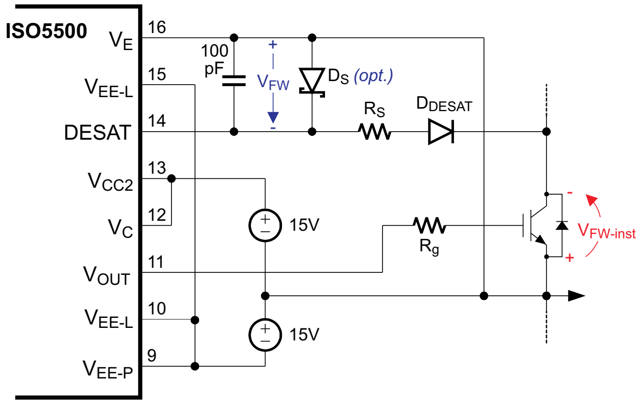


Figure 68. DESAT Pin Protection with Series Resistor and Optional Schottky Diode

DESAT DIODE AND DESAT THRESHOLD

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage, V_{CESAT}, (when the IGBT is "on") and to block high voltages (when the IGBT is "off"). During the short transition time when the IGBT is switching, there is commonly a high dV_{CE}/dt voltage ramp rate across the IGBT. This results in a charging current $I_{CHARGE} = C_{D\text{-}DESAT} \times d_{VCE}/dt$, charging the blanking capacitor.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of $1 + C_{BLANK} / C_{D\text{-}DESAT}$.

Table 1 lists a number of fast-recovery diodes suitable for the use as DESAT diodes.

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{DESAT}$, the V_{CE} level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series: $V_{CE\text{-}FAULT(TH)} = 7.2\text{ V} - n \times VF$ (where n is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.

Table 1. Recommended DESAT Diodes

PART NUMBER	MANUFACTURER	t_{rr} (ns)	$V_{RRM\text{-}max}$ (V)	PACKAGE
STTH112	STM	75	1200	SMA, SMB, DO-41
MUR100E	Motorola	75	1000	59-04 (axial leaded)
MURS160T3	Motorola	75	600	Case 403A (SMD)
UF4007	General Semi.	75	1000	DO-204AL (axial leaded)
BYM26E	Philips	75	1000	SOD64 (axial leaded)
BYV26E	Philips	75	1000	SOD57 (axial leaded)
BYV99	Philips	75	600	SOD87 (axial leaded)

DETERMINING THE MAXIMUM AVAILABLE, DYNAMIC OUTPUT POWER, $P_{OD\text{-}max}$

The ISO5500 total power consumption of P_D = 592 mW consists of the total input power, P_{ID}, the total output power, P_{OD}, and the output power under load, P_{OL}:

$P_D = P_{ID} + P_{OD} + P_{OL}$ (2)

With: $P_{ID} = V_{CC1\text{-}max} \times I_{CC1\text{-}max} = 5.5\text{ V} \times 8.5\text{ mA} = 47\text{ mW}$, (3)

and: $P_{OD} = (V_{CC2} - V_{EE\text{-}P}) \times I_{CC2\text{-}q} = 30\text{ V} \times 14\text{ mA} = 420\text{ mW}$, (4)

then: $P_{OL} = P_D - P_{ID} - P_{OD} = 592\text{ mW} - 47\text{ mW} - 420\text{ mW} = 125\text{ mW}$. (5)

In comparison to P_{OL}, the actual dynamic output power under worst case condition, $P_{OL\text{-}WC}$, depends on a variety of parameters:

$$P_{OL\text{-}WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE\text{-}P}) \times \left(\frac{r_{on\text{-}max}}{r_{on\text{-}max} + R_G} + \frac{r_{off\text{-}max}}{r_{off\text{-}max} + R_G} \right) \quad (6)$$

Where

- f_{INP} = signal frequency at the control input $V_{IN(\pm)}$
- Q_G = power device gate charge
- V_{CC2} = positive output supply with respect to V_E
- $V_{EE\text{-}P}$ = negative output supply with respect to V_E
- $r_{on\text{-}max}$ = worst case output resistance in the on-state: 4Ω
- $r_{off\text{-}max}$ = worst case output resistance in the off-state: 2.5Ω
- R_G = gate resistor

Once RG is determined, Equation 6 is to be used to verify whether $P_{OL\text{-}WC} < P_{OL}$. Figure 69 shows a simplified output stage model for calculating $P_{OL\text{-}WC}$.

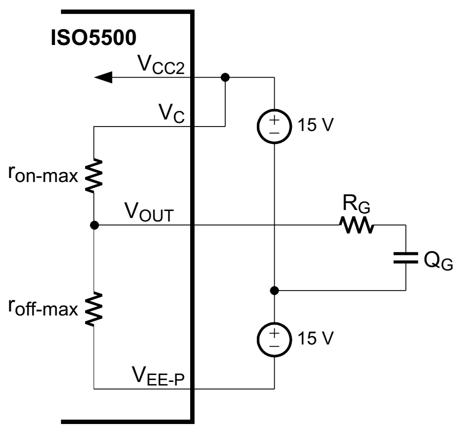


Figure 69. Simplified Output Model for Calculating $P_{OL\text{-}WC}$

DETERMINING GATE RESISTOR, R_G

The value of the gate resistor determines the peak charge and discharge currents, $I_{ON\text{-}PK}$ and $I_{OFF\text{-}PK}$. Due to the transient nature of these currents, their peak values only occur during the on-to-off and off-to-on transitions of the gate voltage. In order to calculate R_G for the maximum peak current, r_{on} and r_{off} must be assumed zero. The resulting charge and discharge models are shown in Figure 70.

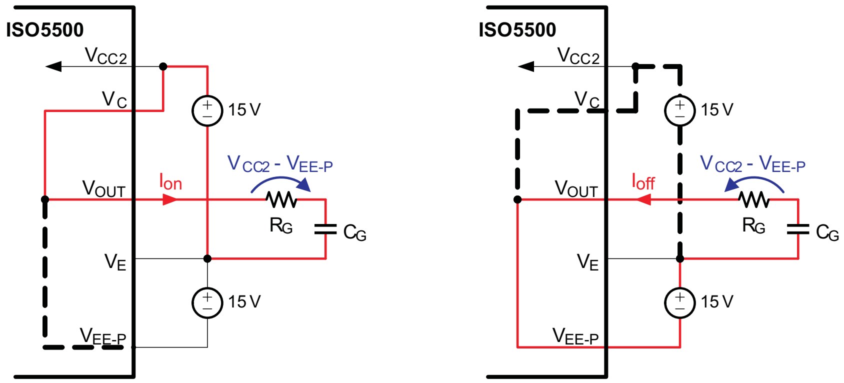


Figure 70. Simplified Gate Charge and Discharge Model

Off-to-On Transition

In the off-state, the upper plate of the gate capacitance, C_G, assumes a steady-state potential of $–V_{EE\text{-}P}$ with respect to V_E. When turning on the power device, V_{CC2} is applied to V_{OUT} and the voltage drop across R_G results in a peak charge current of $I_{ON\text{-}PK} = (V_{CC2} – V_{EE\text{-}P})/R_G$. Solving for R_G then provides the necessary resistor value for a desired on-current via:

$$R_G = \frac{V_{CC2} - V_{EE\text{-}P}}{I_{ON\text{-}PK}} \tag{7}$$

On-to-Off Transition

When turning the power device off, the current and voltage relations are reversed but the equation for calculating R_G remains the same.

Once R_G has been calculated, it is necessary to check whether the resulting, worst-case power consumption, $P_{OD\text{-}WC}$, (derived in Equation 6) is below the calculated maximum, P_{OL} = 125 mW (calculated in Equation 5).

Example

The example below considers an IGBT drive with the following parameters:

$I_{ON\text{-}PK}$ = 2 A, Q_G = 650 nC, f_{INP} = 20 kHz, V_{CC2} = 15V, $V_{EE\text{-}P}$ = –5 V

Applying Equation 7, the value of the gate resistor is calculated with

$$R_G = \frac{15V - (-5V)}{2A} = 10\ \Omega \tag{8}$$

Then, calculating the worst-case output power consumption as a function of R_G, using Equation 6 yields

$$P_{OL\text{-}WC} = 0.5 \times 20\ \text{kHz} \times 650\ \text{nC} \times \big(15\ \text{V} - (-5\text{V})\big) \times \left(\frac{4\ \Omega}{4\ \Omega + 10\Omega} + \frac{2.5\ \Omega}{2.5\ \Omega + 10\ \Omega}\right) = 63\ \text{mW} \tag{9}$$

Because $P_{OL\text{-}WC}$ = 63 mW is well below the calculated maximum of P_{OL} = 125 mW, the resistor value of R_G = 10Ω is fully suitable for this application.

DETERMINING COLLECTOR RESISTOR, R_C

Despite equal charge and discharge currents, many power devices possess longer turn-off propagation and fall times than turn-on propagation and rise times. In order to compensate for the difference in switching times, it might be necessary to significantly reduce the charge current, I_{ON-PK}, versus the discharge current, I_{OFF-PK}.

Reducing I_{ON-PK} is accomplished by inserting an external resistor, R_C, between the V_C- pin and the V_{CC2}- pin of the ISO5500.

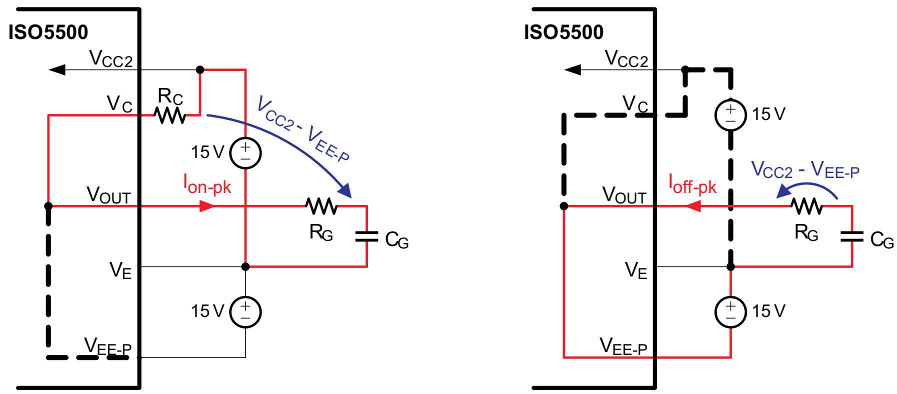


Figure 71. Reducing I_{ON-PK} by Inserting Resistor R_C

Figure 71 (right) shows that during the on-transition, the (V_{CC2} – V_{EE-P}) voltage drop occurs across the series resistance of R_C + R_G, thus reducing the peak charge current to: $I_{ON-PK} = (V_{CC2} – V_{EE-P}) /(R_C + R_G)$. Solving for R_C provides:

$$R_C = \frac{V_{CC2} - V_{EE-P}}{I_{ON-PK}} - R_G \tag{10}$$

To stay below the maximum output power consumption, R_G must be calculated first via:

$$R_G = \left| \frac{V_{CC2} - V_{EE-P}}{I_{OFF-PK}} \right| \tag{11}$$

and the necessary comparison of P_{OL-WC} versus P_{OL} must be completed.

Once R_G is determined, calculate R_C for a desired on-current using Equation 10.

Another method is to insert Equation 11 into Equation 10 and arriving at:

$$R_C = R_G \times \left(\frac{I_{OFF-PK}}{I_{ON-PK}} - 1 \right) \tag{12}$$

Example

Reducing the peak charge current from the previous example to I_{ON-PK} = 1.5 A, requires a R_C value of:

$$R_C = 10\ \Omega \times \left(\frac{2\ A}{1.5\ A} - 1 \right) = 3.33\ \Omega \tag{13}$$

HIGHER OUTPUT CURRENT USING AN EXTERNAL CURRENT BUFFER

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 72) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.

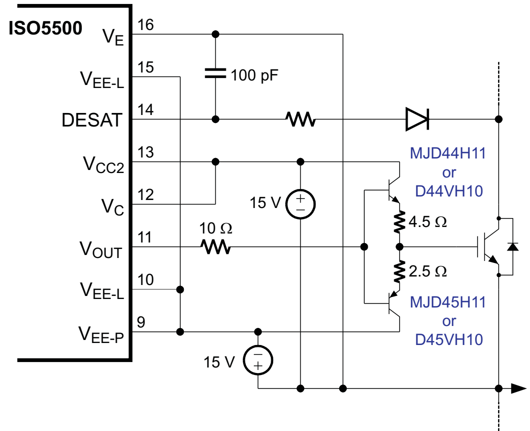


Figure 72. Current Buffer for Increased Drive Current

REVISION HISTORY

Changes from Original (September 2011) to Revision A	Page
• 将器件状态从：产品预览改为：生产	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ISO5500DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ISO5500DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

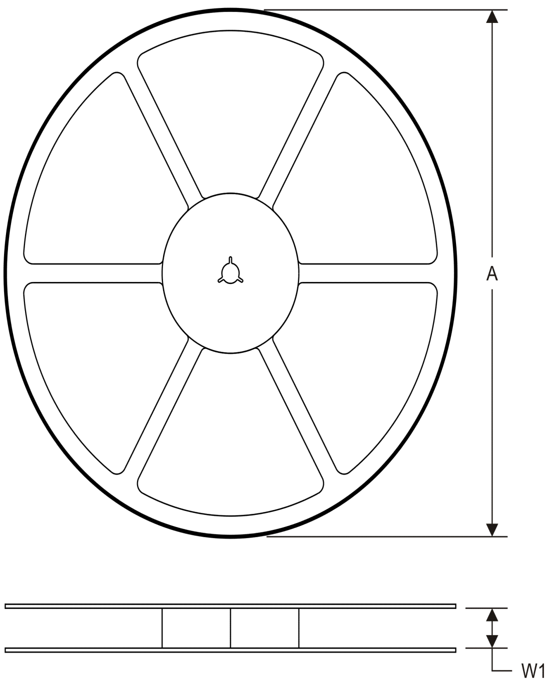
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

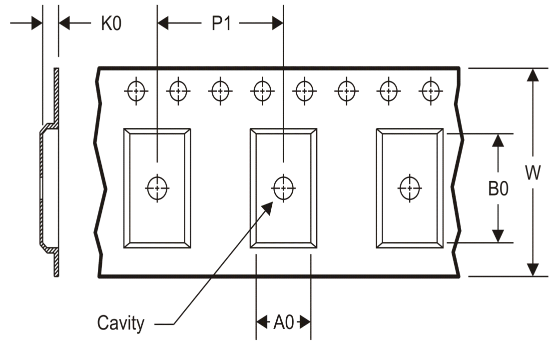
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



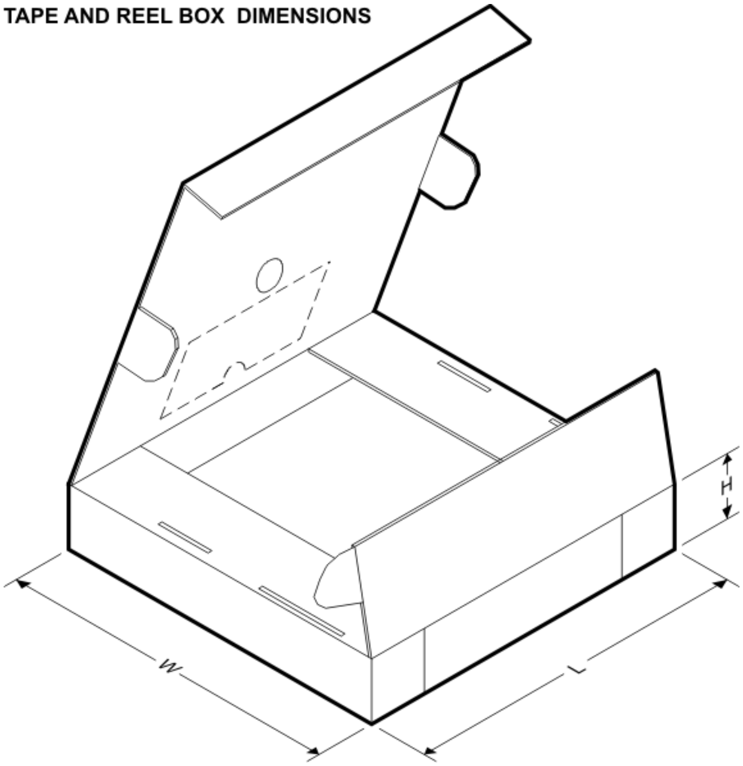
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO5500DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

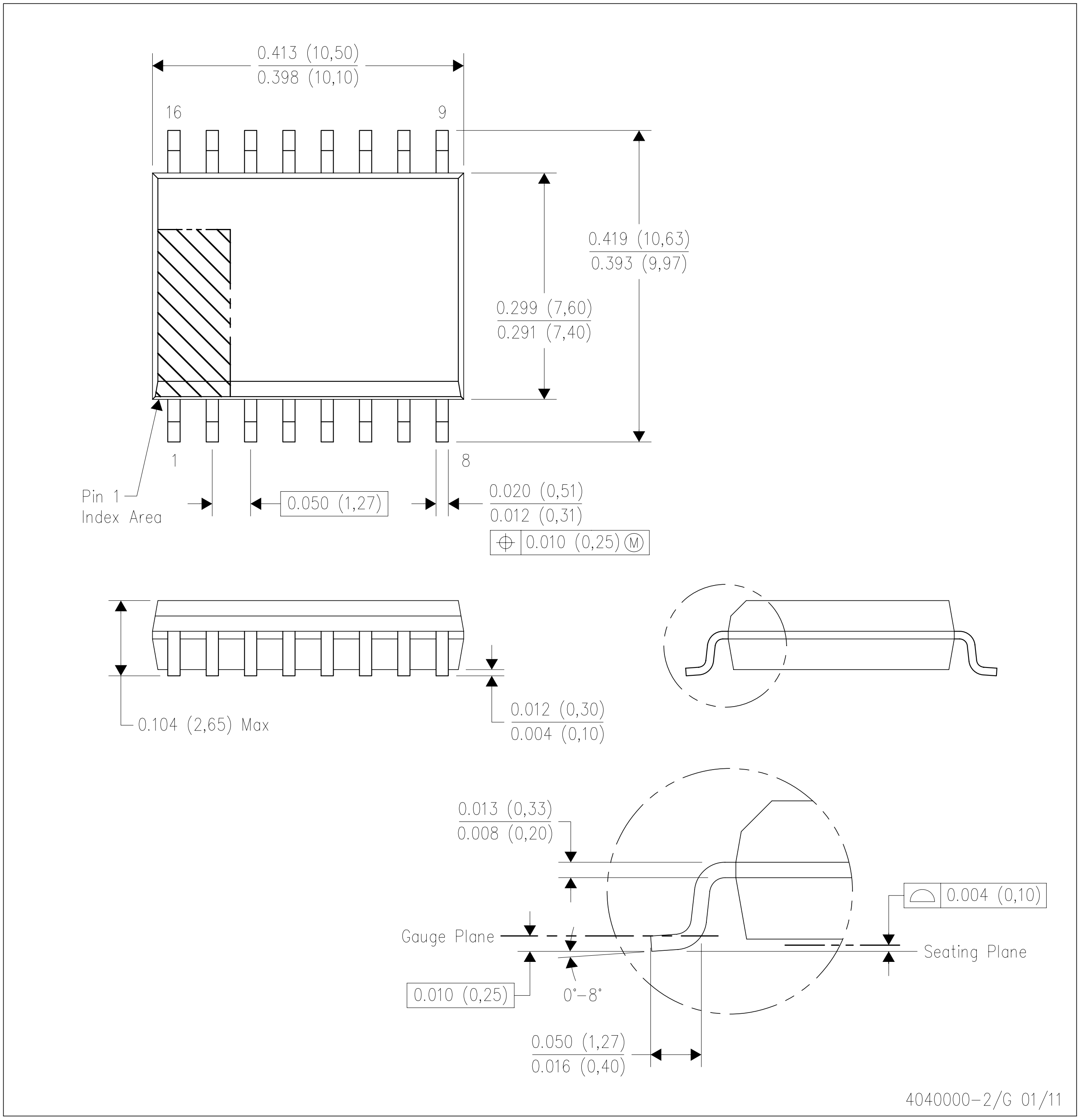
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

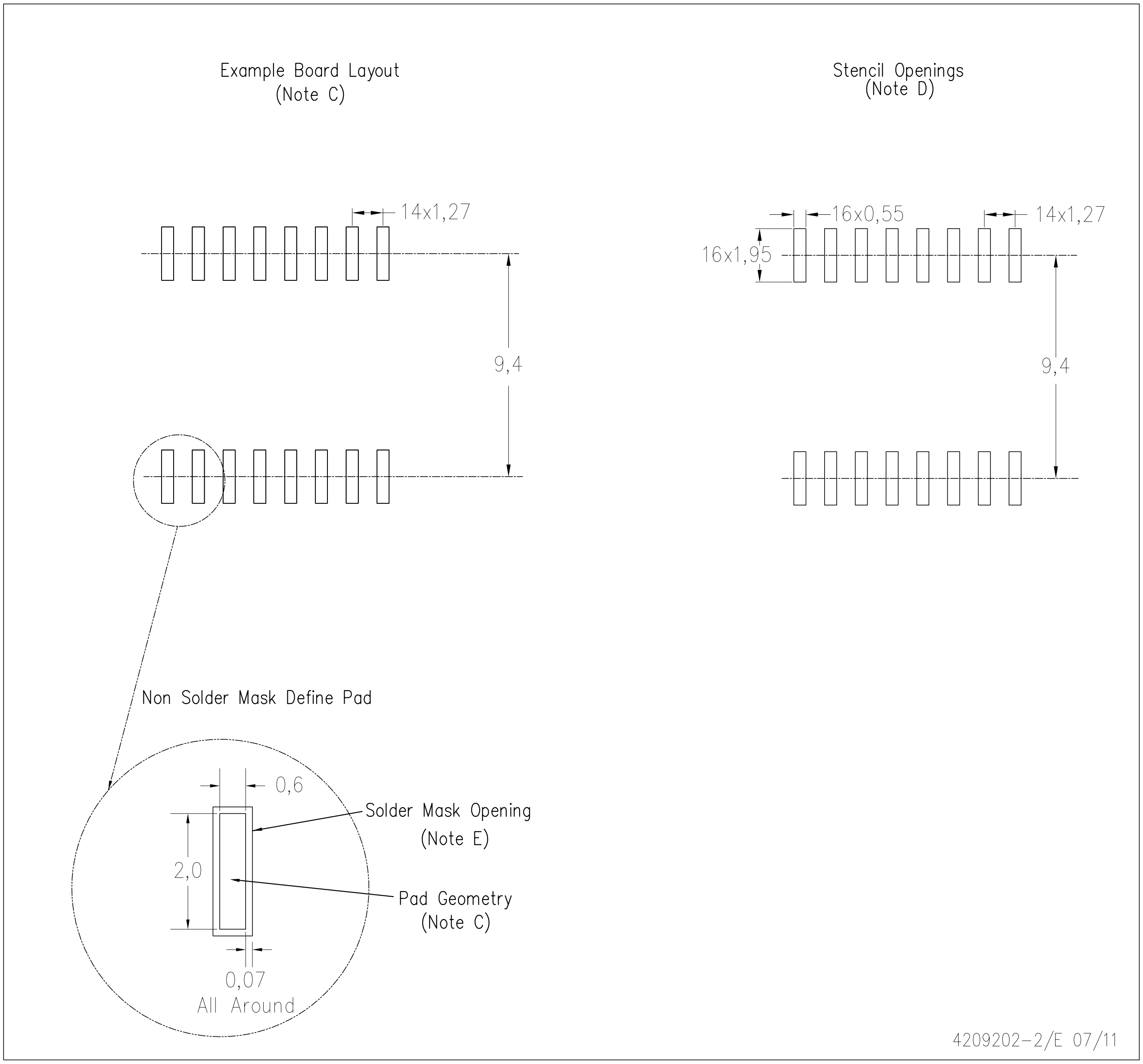
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO5500DWR	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明

德州仪器(TI) 及其下属子公司有权在不事先通知的情况下, 随时对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权随时中止提供任何产品和服务。客户在下订单前应获取最新的相关信息 , 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的硬件产品的性能符合TI 标准保修的适用规范。仅在TI 保证的范围内 , 且TI 认为有必要时才会使用测试或其它质量控制技术。除非政府做出了硬性规定 , 否则没有必要对每种产品的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何TI 专利权、版权、屏蔽作品权或其它与使用了TI 产品或服务的组合设备、机器、流程相关的TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是TI 的专利权或其它知识产权方面的许可。

对于TI 的产品手册或数据表，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。在复制信息的过程中对内容的篡改属于非法的、欺诈性商业行为。TI 对此类篡改过的文件不承担任何责任。

在转售TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关TI 产品或服务的明示或暗示授权，且这是非法的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

TI 产品未获得用于关键的安全应用中的授权，例如生命支持应用（在该类应用中一旦TI 产品故障将预计造成重大的人员伤亡），除非各方官员已经达成了专门管控此类使用的协议。购买者的购买行为即表示，他们具备有关其应用安全以及规章衍生所需的所有专业技术和知识，并且认可和同意，尽管任何应用相关信息或支持仍可能由TI 提供，但他们将独力负责满足在关键安全应用中使用其产 品及TI 产品所需的所有法律、法规和安全相关要求。此外，购买者必须全额赔偿因在此类关键安全应用中使用TI 产品而对TI 及其 代表造成的损失。

TI 产品并非设计或专门用于军事/航空应用，以及环境方面的产品，除非TI 特别注明该产品属于"军用"或"增强型塑料"产品。只 有TI 指定的军用产品才满足军用规格。购买者认可并同意，对TI 未指定军用的产品进行军事方面的应用，风险由购买者单独承担，并且独力负责在此类相关使用中满足所有法律和法规要求。

TI 产品并非设计或专门用于汽车应用以及环境方面的产品，除非TI 特别注明该产品符合ISO/TS 16949 要求。购买者认可并同意，如果他们在汽车应用中使用任何未被指定的产品，TI 对未能满足应用所需要求不承担任何责任。

可访问以下URL 地址以获取有关其它TI 产品和应用解决方案的信息：

产品		应用	
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP 机动性处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity		
	德州仪器在线技术支持社区	www.deyisupport.com	

邮寄地址： 上海市浦东新区世纪大道 1568 号，中建大厦 32 楼 邮政编码： 200122