



Design Example Report

Title	Wide Input, High Efficiency ($\geq 90\%$), High Differential Surge (>2.5 kV) High Power Factor (>0.9), Class C, 30 W LED Driver Using LinkSwitch™-PH LNK419EG
Specification	90 VAC – 308 VAC Input; 30 V, 1 A Output
Application	LED Driver
Author	Applications Engineering Department
Document Number	DER-286
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Revision	1.0

Summary and Features

- Highly energy efficient
 - >89% at 115 VAC and >90% 230 VAC input
- No high-voltage aluminum electrolytic capacitors used in the primary side
- Easily meets IEC61000-3-2 Class C harmonics at 230 VAC input
- Low THD
 - <15% at 115 VAC input
 - <20% at 230 VAC input
- Low cost, low component count and small printed circuit board footprint solution
 - Frequency jitter for smaller, lower cost EMI filter components
- Complies with IEC61000-4-5 >2.5 kV, 1.2 μ s / 50 μ s differential surge
- Complies with EN55015 B conducted EMI

PATENT INFORMATION

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document describes an isolated, power factor corrected, very high efficiency LED driver designed to drive an LED string of 30 V at a current of 1 A (both nominal) from an input voltage range of 90 VAC to 308 VAC.

The LED driver uses a LNK419EG device from the LinkSwitch-PH family of ICs. This integrated controller and 725 V MOSFET dramatically reduces the complexity and component count of the solution.

The key design goals were to achieve the highest possible efficiency, to pass >2.5 kV, 1.2 μ s / 50 μ s differential surge, and meet IEC 61000-3-2 Class C harmonics.

This document contains the LED driver specification, schematic, bill of material, transformer documentation, and typical performance characteristics.



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2 Populated Circuit Board

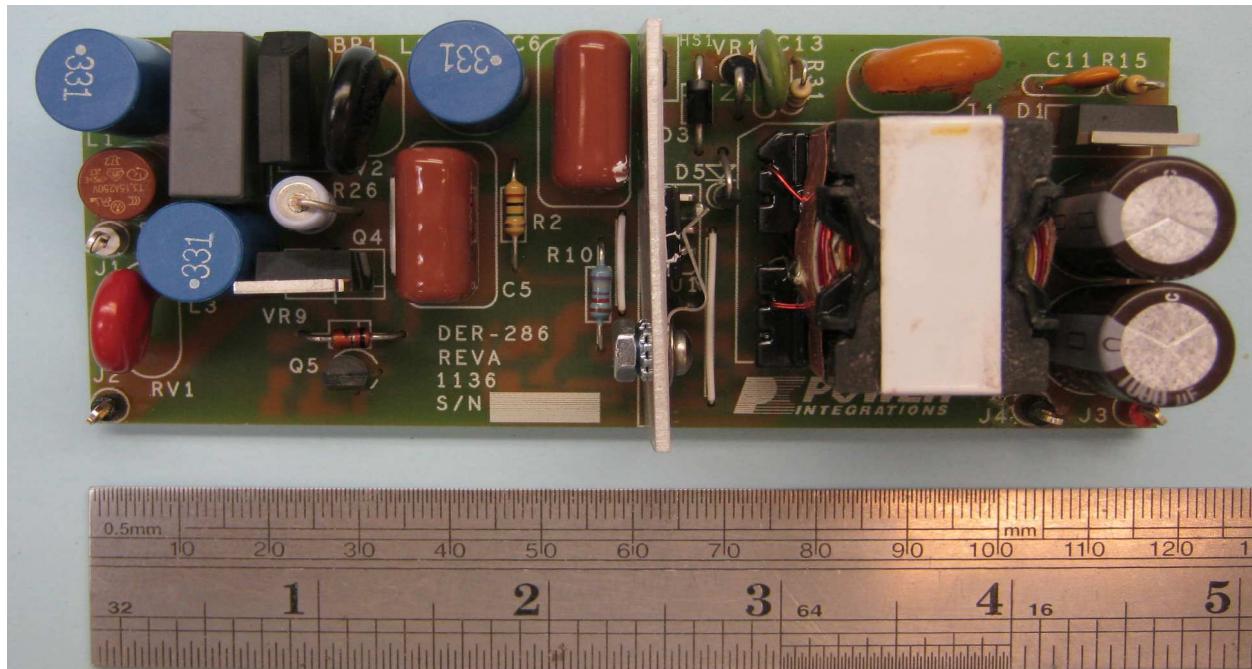


Figure 1 – Populated Circuit Board Photograph (Top View).

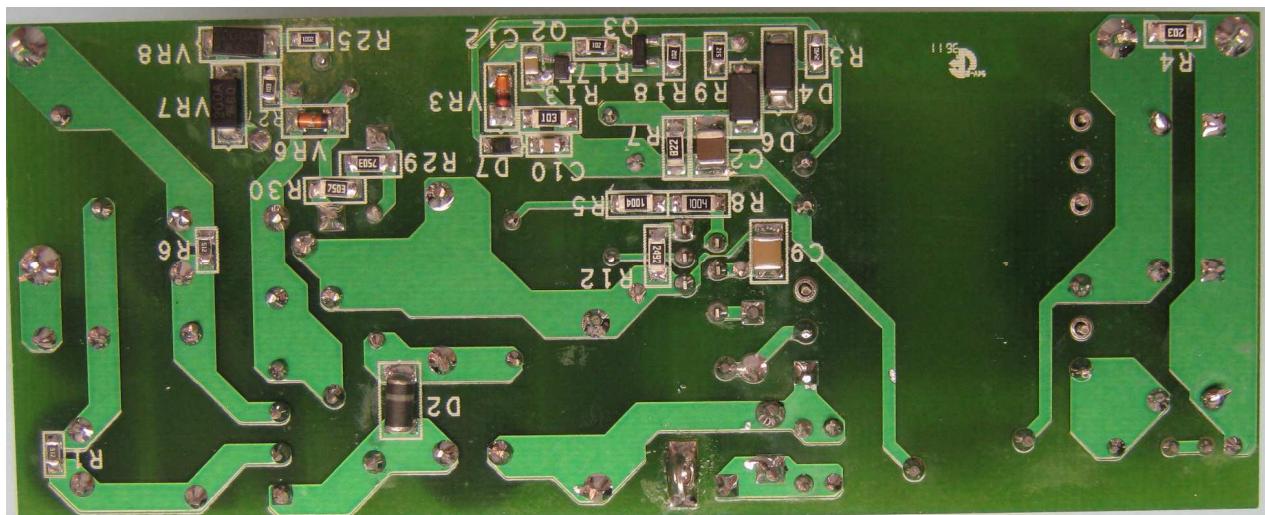


Figure 2 – Populated Circuit Board Photograph (Bottom View).

3 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage Frequency	V_{IN} f_{LINE}	90 47	115/230 50/60	308 64	VAC Hz	2 Wire – no P.E.
Output						
Output Voltage Output Current	V_{OUT} I_{OUT}	27	30 1	33	V A	
Total Output Power						
Continuous Output Power	P_{OUT}		30		W	
Efficiency						
Full Load	$\eta_{(115)}$ $\eta_{(230)}$	89 90			% %	Measured at P_{OUT} , 25 °C, 115 VAC Measured at P_{OUT} , 25 °C, 230 VAC
Environmental						
Conducted EMI 1.2 μ s / 50 μ s and 200 A Ring Wave (100 kHz) Differential Mode (L1-L2)			Meets CISPR 15B / EN55015B			
		2.5			kV	IEC 61000-4-5,
Power Factor		0.9				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 115 / 230 VAC
Harmonic Currents			EN 61000-3-2 Class C			
Ambient Temperature	T_{AMB}		40		°C	Free convection, sea level



4 Schematic

Two versions of the design are shown below. They differ in how the 2.5 kV surge withstand is achieved. To avoid the need for electrolytic capacitors on the primary side, the first design uses a switched series impedance to limit the maximum DC bus voltage. This is the circuit block within the dotted box in Figure 3. For differential surge levels of 500 V or less this block may be omitted.

The second schematic uses a capacitor to limit the DC bus voltage. Due to the value required (10 μ F or 4.7 μ F) an electrolytic type was selected for cost reasons. The capacitor is diode isolated from the DC bus such that it does not impact the PF or harmonic performance. As the capacitor is not part of the power train, end of life of this component will not affect lamp operation and will not therefore reduce system life.

4.1 Schematic (No Primary Side Aluminum Capacitor)

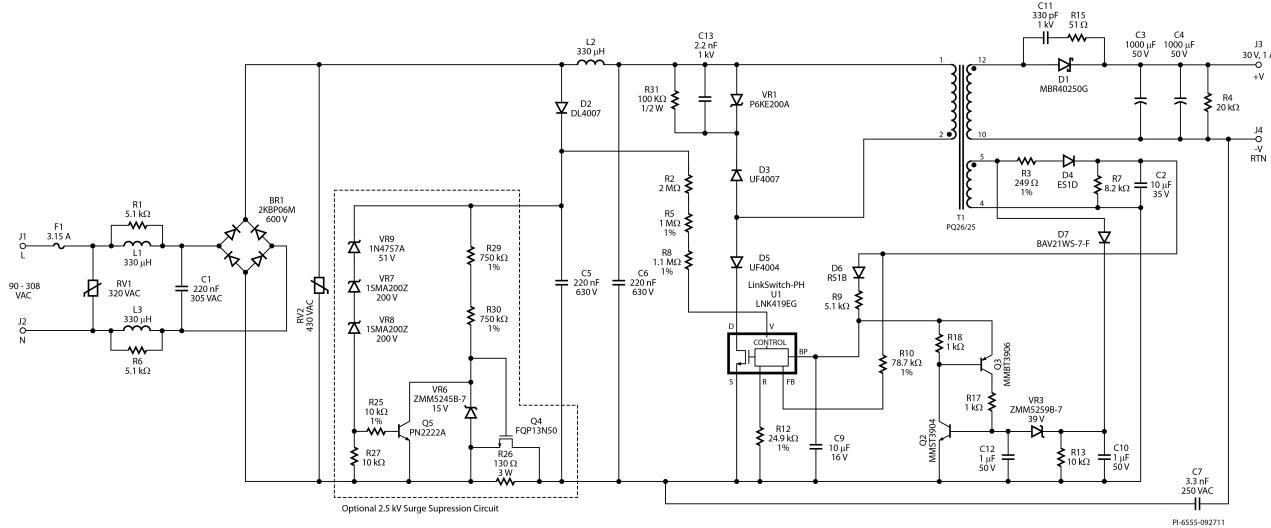


Figure 3 – Schematic (No Aluminum Input Capacitor).



4.2 Schematic (With Primary Side Aluminum Capacitor)

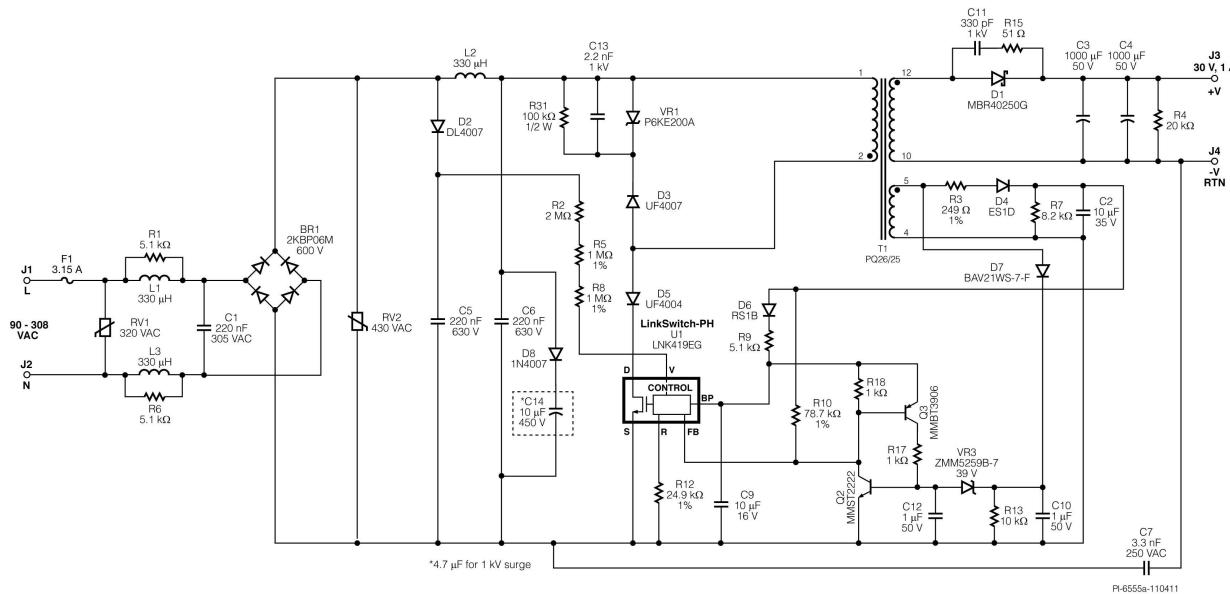


Figure 4 – Schematic (with 10 μ F Aluminum Capacitor).



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5 PCB Layout

5.1 No Primary Side Aluminum Capacitor (Figure 3)

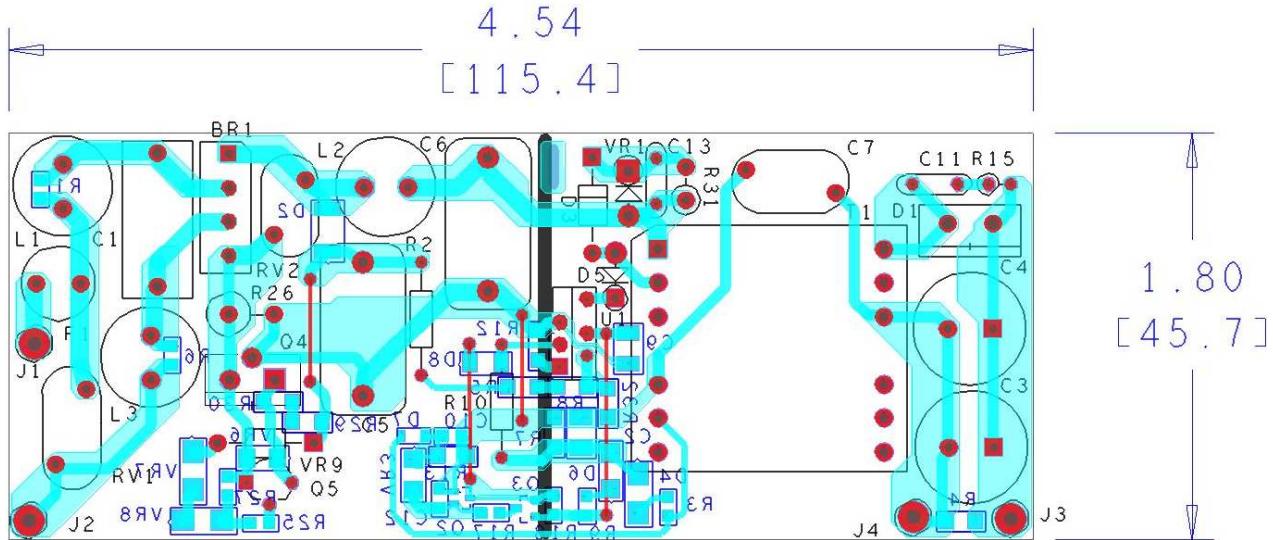


Figure 5 – Layout (4.54" x 1.80").

The same layout was used for the schematic shown in Figure 4. Here the additional components (within highlighted box in Figure 3) were removed. Resistor R26 was replaced with a jumper and D8 and C14 soldered across C6.



6 Description

The LinkSwitch-PH device is a controller and integrated 725 V MOSFET designed for LED driver applications. The LinkSwitch-PH is configured for use in a continuous conduction mode flyback topology and provides a primary side regulated constant current output while maintaining high power factor from the AC input.

6.1 Input Filtering

Fuse F1 provides protection following catastrophic component failures and BR1 rectifies the AC line voltage. Inductor L1-L3, C1, R1, and R6 form the EMI filter and together with C7 (Y1 safety) capacitor allow the design to meet EN55015B conducted EMI limits. Capacitor C6 provides a low impedance path for the primary switching current, a low value of capacitance is necessary to maintain a power factor of greater than 0.9.

6.2 LinkSwitch-PH Primary

Diode D2 and high-voltage film capacitor C5 detects the peak of the AC line voltage. This voltage is converted to a current into the VOLTAGE MONITOR (V) pin via R2, R5 and R8. This current is also used by the device to set the input over/undervoltage protection thresholds. The V pin current and the FEEDBACK (FB) pin current are used internally to control the average output LED current. Non-dimming designs require 24.9 k Ω resistor on the REFERENCE (R) pin (R12) and 4 M Ω on the V pin (R2+R5+R8).

Diode D3, VR1, R31, and C13 clamp the drain voltage to below the BV_{DSS} rating (725 V) of the internal power MOSFET in U1. Diode D5 is necessary to prevent reverse current from flowing through the LinkSwitch-PH device (the result of the minimal input capacitance).

6.3 Bias Supply and Output Overvoltage Sensing

Diode D4, C2, R7, and R3 form the primary bias supply. This supplies the IC operating current into the BYPASS (BP) pin through D6 and R9 during normal operation. Resistor R3 provides filtering to improve output regulation while R7 acts as a minimum load.

Capacitor C9 is the supply decoupling for the LinkSwitch-PH. During start-up, C9 is charged to ~6 V from an internal high-voltage current source tied to the device DRAIN (D) pin. Once charged the energy stored in C9 is used to run the device until the output and bias winding voltage rise and current is supplied via R9.

A disconnected load / overvoltage shutdown function is provided by D7, C10, R13, VR3, C12, R17, R18, Q2, and Q3. A second bias winding output voltage is used to eliminate the delay introduced by the larger value of C2 compared to C10. Should the output LED load be disconnected, the output voltage and therefore the bias winding voltage across C10 will rise. Once this exceeds the voltage rating of VR3 plus the V_{BE} of Q2, Q2 is biased on and turns-on Q3 (which keeps pulling down the BP pin voltage.)



6.4 Output Feedback

A current proportional to the output voltage from the primary bias winding is fed into the FB pin through R10. This information together with the line input voltage and the drain current are used to maintain a constant output current.

6.5 Output Rectification and Filtering

Diode D1 rectifies the secondary winding while capacitors C3 and C4 filter the output. A 40 A, 250 V Schottky diode was selected for high efficiency. Filter C11 and R15 reduce the reverse voltage spikes across D1. Resistor R4 provides a minimum load to ensure the LED current falls when the AC is removed and LEDs extinguish.

6.6 High Surge Protection Circuit without Aluminum Capacitor (Figure 3)

MOVs RV1 and RV2 clamp the voltage rise across C6 when differential surge events are present at the AC input. Even with RV1 and RV2 present, the limited capacitance ($C_5 + C_6$) after the bridge, allows the DC voltage to exceed the voltage rating of U1. To further limit the voltage R26 is connected in series with the output of the bridge rectifier during surge events. Thus a significant proportion of the voltage (set by the clamping level of RV1 and RV2) now appear across the series resistor, reducing the voltage across C6 and U1.

To prevent excessive dissipation the resistor is shorted by Q4 during normal operation. Zener diodes V57, 8 and 9 set a 450 V threshold. Above this Q5 turns on, pulling the gate of Q4 low and connecting R26 in circuit. Below this level the gate of Q4 is clamped to 15 V by VR6 with R29 and R30 providing a turn on charge. A 13 A, 500 V FET was selected for low R_{DS} . A low current, higher R_{DS} FET can be used for high input voltage only application.

6.7 High Surge Protection Circuit with Aluminum Capacitor (Figure 4)

In applications where a primary side electrolytic capacitor is acceptable, 2.5 kV surge withstand can be met using a clamp formed by D8 and C14. The diode isolates the capacitor from the DC bus so that high PF is maintained but allows the capacitor to charge if the DC bus voltage rises. The relatively large capacitance value integrates the surge energy limiting the maximum voltage. Typically, the leakage current is sufficient to discharge the capacitor but a high value parallel resistor may also be added.

7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	600 V, 2 A, Bridge Rectifier, Glass Passivated	2KBP06M-E4/51	Vishay
2	1	C1	220 nF, 305 VAC, Film, X2	R463I322000M2M	Kemet
3	1	C2	10 μ F, 35 V, Ceramic, X5R, 1210	GMK325BJ106KN-T	Taiyo Yuden
4	2	C3 C4	1000 μ F, 50 V, Electrolytic, Gen. Purpose, (12.5 x 25)	EKMG500ELL102MK25S	Nippon Chemi-Con
6	2	C5 C6	220 nF, 630 V, Film	ECQ-E6224KF	Panasonic
8	1	C7	3.3 nF, Ceramic, Y1	440LD33-R	Vishay
9	1	C9	10 μ F, 16 V, Ceramic, X5R, 1210	C1210C106K4PACTU	Kemet
10	1	C10	1 μ F, 50 V, Ceramic, X7R, 0805	08055D105KAT2A	AVX
11	1	C11	330 pF, 1 kV, Disc Ceramic	562R5GAT33	Vishay
12	1	C12	1 μ F, 50 V, Ceramic, X7R, 0805	08055D105KAT2A	AVX
13	1	C13	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC Components
14	1	D1	250 V, 40 A, Schottky, TO-220AC	MBR40250G	ON Semi
15	1	D2	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
16	1	D3	1000 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4007-E3	Vishay
17	1	D4	200 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1D	Vishay
18	1	D5	400 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4004-E3	Vishay
19	1	D6	100 V, 1 A, Fast Recovery, 150 ns, SMA	RS1B-13-F	Diodes, Inc
20	1	D7	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes Inc.
21	1	F1	3.15 A, 250 V, Slow, TR5	37213150411	Wickman
22	3	L1 L2 L3	330 μ H, 0.87 A, Radial	TSL1112RA-331KR82-PF	TDK
23	1	Q2	NPN, Medium Power BJT, 40 V, 0.2 A, SOT-323	MMST2222AT146	ROHM
24	1	Q3	PNP, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3906LT1G	On Semi
25	1	Q4	500 V, 12.5 A, 430 m Ω N-Channel, TO-220-3-1	2SK2842	Toshiba
26	1	Q5	NPN, Small Signal BJT, 40 V, 0.6 A, TO-92	PN2222AG	On Semi
27	1	R1	5.1 k Ω 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
28	1	R2	2.0 M Ω 5%, 1/4 W, Carbon Film	CFR-25JB-2M0	Yageo
29	1	R3	249 Ω 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2490V	Panasonic
30	1	R4	20 k Ω 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
31	1	R5	1.00 M Ω 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1004V	Panasonic
32	1	R6	5.1 k Ω 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
33	1	R7	8.2 k Ω 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ822V	Panasonic
34	1	R8	1.10 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1104V	Panasonic
35	1	R9	5.1 k Ω 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
36	1	R10	78.7 k Ω 1%, 1/4 W, Metal Film	MFR-25FBF-78K7	Yageo
37	1	R12	24.9 k Ω 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2492V	Panasonic
38	1	R13	10 k Ω 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
39	1	R15	51 Ω 5%, 1/4 W, Carbon Film	CFR-25JB-51R	Yageo
40	2	R17 R18	1 k Ω 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
41	1	R25	10 k Ω 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
42	1	R26	130 Ω 5%, 3 W, Metal Oxide	ERG-3SJ131	Panasonic
43	1	R27	10 k Ω 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
44	2	R29 R30	750 k Ω 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7503V	Panasonic
45	1	R31	100 k Ω 5%, 1/4 W, Carbon Film	CFR-25JB-100K	Yageo
46	1	RV1	320 V, 48 J, 10 mm, RADIAL	V320LA10P	Littlefuse
47	1	RV2	430 V, 100 J, 14 mm, RADIAL	ERZ-V14D431	Panasonic
48	1	T1	Bobbin, PQ26/25, Vertical, 12 pins	PQ26X25	Pin Shine



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49	1	U1	LinkSwitch-PH, eSIP	LNK419EG	Power Integrations
50	1	VR1	200 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE200ARLG	On Semi
51	1	VR3	39 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5259B-7	Diodes, Inc.
52	1	VR6	15 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5245B-7	Diodes, Inc.
53	2	VR7 VR8	200 V, 5%, 1.25 W, DO-214AC	1SMA200Z	Taiwan Semi
54	1	VR9	51 V, 5%, 1 W, DO-41	1N4757A	Micro Semi

8 Transformer Specification

8.1 Electrical Diagram

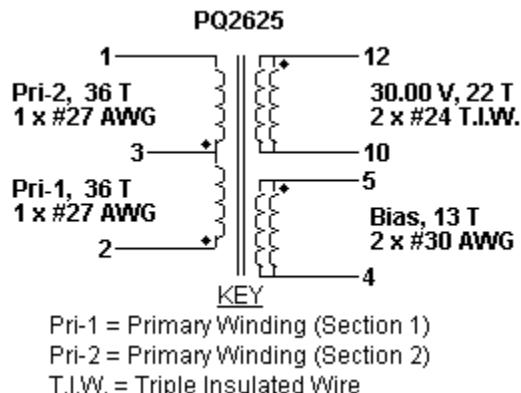


Figure 6 – Transformer Electrical Diagram.

8.2 Electrical Test Specifications

Parameter	Condition	Spec
Electrical Strength	60 Hz 1 second, from pins 1, 2, 3, 4, 5 to pins 10, 12.	3000 VAC
Nominal Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between pin 1 to pin 2, with all other windings open.	2072 μ H
Tolerance	Tolerance of primary inductance.	$\pm 10\%$
Maximum Primary Leakage	Measured between pin 1 to pin 2, with all other windings shorted.	51.8 μ H

8.3 Material

Item	Description
[1]	Core: PQ2625, PC95 or Equivalent, gapped for A_{LG} of 398 nH/t ²
[2]	Bobbin: Generic, 5 primary + 3 secondary
[3]	Barrier Tape: Polyester film [1 mil (25 µm) base thickness], 13.60 mm wide
[4]	Copper Tape: 2 mil thick
[5]	Varnish
[6]	Magnet Wire: #27 AWG, Solderable Double Coated
[7]	Triple Insulated Wire: 24 AWG
[8]	Magnet Wire: #30 AWG, Solderable Double Coated

8.4 Mechanical Diagram

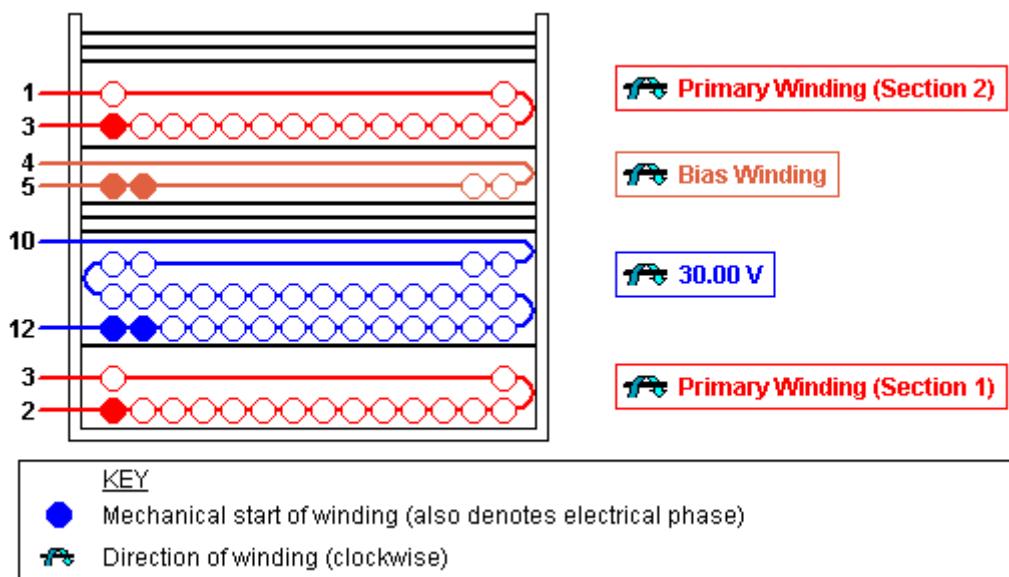


Figure 7 – Transformer Mechanical Diagram.

8.5 Winding Instructions

Primary Winding (Section 1)	Start on pin(s) 2 and wind 36 turns (x1 filar) of item [6] in 2 layer(s) from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 3. Add 1 layer of tape, item [3], for insulation.
Secondary Winding	Start on pin(s) 12 and wind 22 turns (x2 filar) of item [7]. Spread the winding evenly across entire bobbin. Wind in same rotational direction as primary winding. Finish this winding on pin(s) 10. Add 3 layers of tape, item [3], for insulation.
Bias Winding	Start on pin(s) 5 and wind 13 turns (x2 filar) of item [8]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 4. Add 1 layer of tape, item [3], for insulation.
Primary Winding (Section 2)	Start on pin(s) 3 and wind 36 turns (x1 filar) of item [6] in 2 layer(s) from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1. Add 3 layers of tape, item [3], for insulation.
Core Assembly	Assemble and secure core halves. Item [1].
Flux-Band	Construct a flux band by wrapping a single shorted turn of item [4] around the outside of windings and core halves with tight tension. Make an electrical connection to pin(s) 1 using wire. Add 3 layers of tape, item [3], for insulation.
Varnish	Dip varnish uniformly in item [5]. Do not vacuum impregnate.



9 Transformer Design Spreadsheet

ACDC_LinkSwitch-PH_032511; Rev.1.3; Copyright Power Integrations 2011		INPUT	INFO	OUTPUT	UNIT	LinkSwitch-PH_032511: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES						
Dimming required	NO		NO		Select 'YES' option if dimming is required. Otherwise select 'NO'.	
VACMIN	190		190	V	Minimum AC Input Voltage	
VACMAX	265		265	V	Maximum AC input voltage	
fL			50	Hz	AC Mains Frequency	
VO	30.00			V	Typical output voltage of LED string at full load	
VO_MAX			33.00	V	Maximum expected LED string Voltage.	
VO_MIN			27.00	V	Minimum expected LED string Voltage.	
V_OVP			35.00	V	Over-voltage protection setpoint	
IO	1.00			A	Typical full load LED current	
PO			30.0	W	Output Power	
n	0.90		0.9		Estimated efficiency of operation	
VB	17		17	V	Bias Voltage	
ENTER LinkSwitch-PH VARIABLES						
LinkSwitch-PH	LNK419			Universal	115 Doubled/230V	
Chosen Device		LNK419	Power Out	18W	8W	
Current Limit Mode	RED		RED		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode	
ILIMITMIN			2.35	A	Minimum current limit	
ILIMITMAX			2.73	A	Maximum current limit	
fS			66000	Hz	Switching Frequency	
fSmin			62000	Hz	Minimum Switching Frequency	
fSmax			70000	Hz	Maximum Switching Frequency	
IV			80.3	uA	V pin current	
RV			3.909	M-ohms	Upper V pin resistor	
RV2			1.402	M-ohms	Lower V pin resistor	
IFB	180.00		180.0	uA	FB pin current (85 uA < IFB < 210 uA)	
RFB1			77.8	k-ohms	FB pin resistor	
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage	
VD	0.50			V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)	
VDB	0.70			V	Bias Winding Diode Forward Voltage Drop	
Key Design Parameters						
KP	0.60		0.6		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)	
LP			2072	uH	Primary Inductance	
VOR	100.00		100	V	Reflected Output Voltage.	
Expected IO (average)			1.01	A	Expected Average Output Current	
KP_VACMAX			0.63		Expected ripple current ratio at VACMAX	
TON_MIN			3.19	us	Minimum on time at maximum AC input voltage	
PCLAMP			0.35	W	Estimated dissipation in primary clamp	
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES						
Core Type	PQ2625		PQ2625			
Bobbin		#N/A		P/N:	#N/A	
AE	1.2000		1.2	cm^2	Core Effective Cross Sectional Area	
LE	5.4300		5.43	cm	Core Effective Path Length	
AL	4200.0		4200	nH/T^2	Ungapped Core Effective Inductance	
BW	13.6		13.6	mm	Bobbin Physical Winding Width	
M	0.0		0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)	
L	2.00		2		Number of Primary Layers	
NS	22		22		Number of Secondary Turns	
DC INPUT VOLTAGE PARAMETERS						
VMIN			269	V	Peak input voltage at VACMIN	
VMAX			375	V	Peak input voltage at VACMAX	



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CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX		0.28			Minimum duty cycle at peak of VACMIN
IAVG		0.21	A		Average Primary Current
IP		1.22	A		Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS		0.39	A		Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP		2072	uH		Primary Inductance
NP		72			Primary Winding Number of Turns
NB		13			Bias Winding Number of Turns
ALG		398	nH/T^2		Gapped Core Effective Inductance
BM		2931	Gauss		Maximum Flux Density at PO, VMIN (BM<3100)
BP		3419	Gauss		Peak Flux Density (BP<3700)
BAC		879	Gauss		AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1512			Relative Permeability of Ungapped Core
LG		0.34	mm		Gap Length (Lg > 0.1 mm)
BWE		27.2	mm		Effective Bobbin Width
OD		0.38	mm		Maximum Primary Wire Diameter including insulation
INS		0.06	mm		Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.32	mm		Bare conductor diameter
AWG		29	AWG		Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		128	Cmils		Bare conductor effective area in circular mils
CMA		332	Cmils/Amp		Primary Winding Current Capacity (200 < CMA < 600)
LP_TOL		10			Tolerance of primary inductance
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP		4.01	A		Peak Secondary Current
ISRMS		1.87	A		Secondary RMS Current
IRIPPLE		1.58	A		Output Capacitor RMS Ripple Current
CMS		374	Cmils		Secondary Bare Conductor minimum circular mils
AWGS		24	AWG		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.51	mm		Secondary Minimum Bare Conductor Diameter
ODS		0.62	mm		Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS					
VDRAIN		581	V		Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS		149	V		Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB		86	V		Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1		3.91	M-ohms		Upper V Pin Resistor Value
RV2		1.40	M-ohms		Lower V Pin Resistor Value
VAC1		115.0	V		Test Input Voltage Condition1
VAC2		230.0	V		Test Input Voltage Condition2
IO_VAC1		1.00	A		Measured Output Current at VAC1
IO_VAC2		1.00	A		Measured Output Current at VAC2
RV1 (new)		3.91	M-ohms		New RV1
RV2 (new)		1.40	M-ohms		New RV2
V_OV		318.3	V		Typical AC input voltage at which OV shutdown will be triggered
V_UV		70.8	V		Typical AC input voltage beyond which power

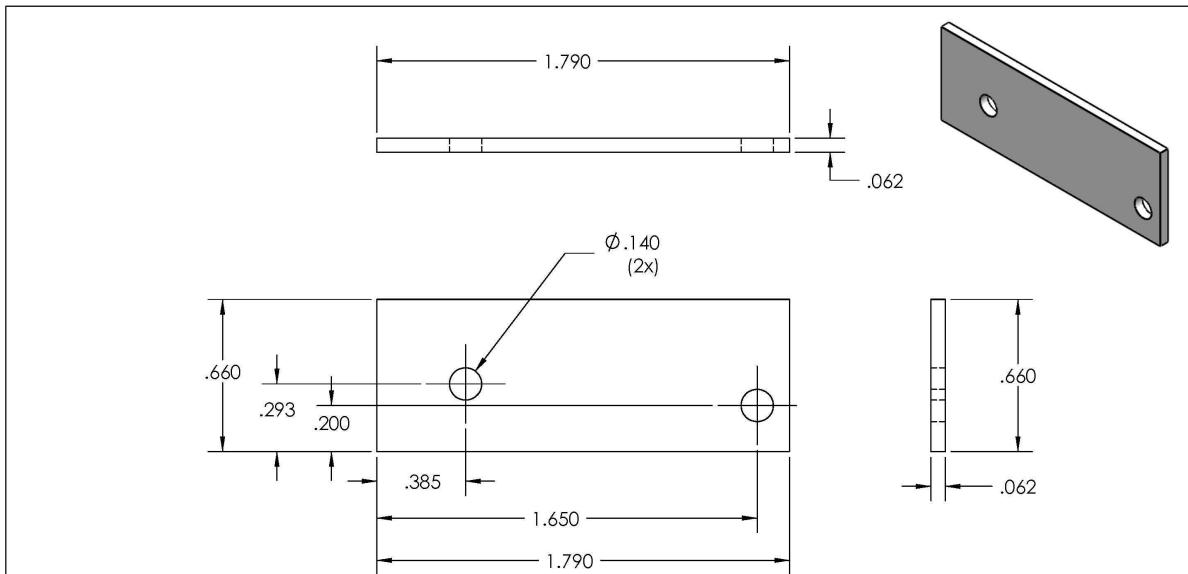


					supply can startup
FB pin resistor Fine Tuning					
RFB1			78	k-ohms	Upper FB Pin Resistor Value
RFB2			1E+012	k-ohms	Lower FB Pin Resistor Value
VB1			15.3	V	Test Bias Voltage Condition1
VB2			18.7	V	Test Bias Voltage Condition2
IO1			1.00	A	Measured Output Current at Vb1
IO2			1.00	A	Measured Output Current at Vb2
RFB1 (new)			77.8	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2

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10 Heat Sink Assembly

10.1 Heat Sink Drawing



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Reports\DER-286\Heatsink\PDF



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REMOVE ALL BURRS	UNLESS OTHERWISE SPECIFIED:	NAME	DATE	Power Integrations
BREAK SHARP EDGES	DIMENSIONS ARE IN INCHES	DRAWN BY:	JNG 090711	TITLE:
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS	TOLERANCES: ANGULAR: MACH $\pm 0^{\circ}30'$ XX ± 0.1 XXX ± 0.01 XXXX ± 0.005	CHECKED BY:		HEATSINK, DWG, eSIP WITH BRKT, DER286, PI CUSTOM
	ASME Y14.5	ENG APPR.		
NEXT ASSY	MATERIAL	MFG APPR.		
USED ON	FINISH	Q.A.		
APPLICATION	DO NOT SCALE DRAWING	COMMENTS:		
			SIZE	DWG. NO.
			A	61-00077-00
				REV
				01
		SCALE: 2:1	WEIGHT:	SHEET 1 OF 1

5 4 3 2 1



10.2 Heat Sink Fabrication Drawing

1 FOR COMPLETED ASSEMBLY
SEE 61-00077-02

FABRICATOR TO INSTALL ITEM 2 AS SHOWN.

ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00077-00	HEATSINK, CUSTOM, AL, 3003, 0.062" THK	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	1

F:\Apps_Files\Public\Design Example Reports \DER-286\Heatsink\PDF

® REMOVE ALL BURRS		UNLESS OTHERWISE SPECIFIED:	DRAWN BY: JNG 090711 CHECKED BY: ENG APPR. MFG APPR. QA.	TITLE: HEATSINK,FAB,eSIP WITH BRKT, DER286, PI CUST	Power Integrations		
BREAK SHARP EDGES		DIMENSIONS ARE IN INCHES					
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS		TOLERANCES: ANGULAR: MACH \pm 0°30' XX \pm 0.1 XXX \pm 0.01 XXXX \pm 0.005					
		ASME Y14.5					
NEXT ASSY		MATERIAL					
USED ON		FINISH					
APPLICATION		DO NOT SCALE DRAWING	SIZE	DWG. NO.	REV		
			A	61-00077-01	01		
			SCALE: 2:1	WEIGHT:	SHEET 1 OF 1		

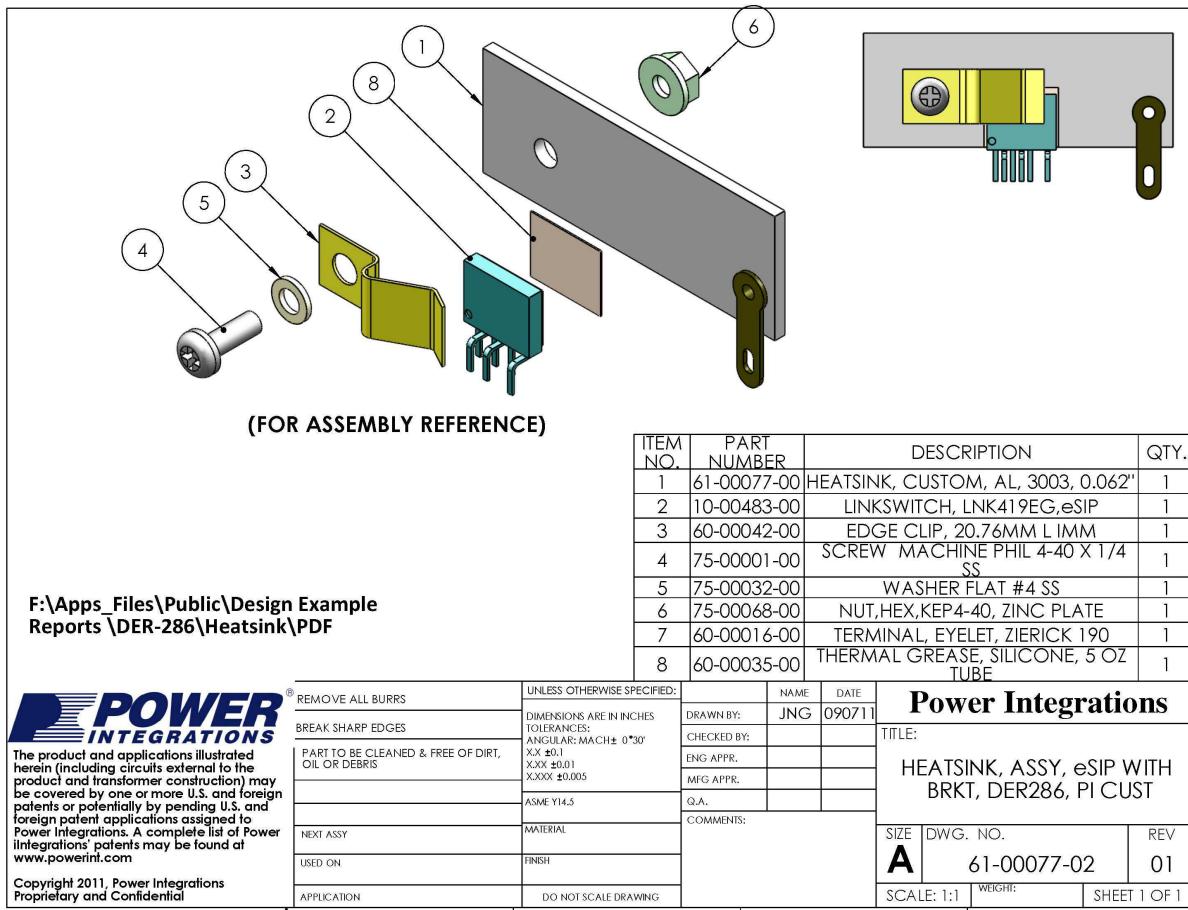
5 1 4 1 3 1 2 1 1

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10.3 eSIP and Heat Sink Assembly Drawing



11 Performance Data

All measurements performed at room temperature.

11.1 Efficiency vs. Line and Output (LED String) Voltage

11.1.1 30 V LED String

Input		Input Measurement					Load Measurement			Calculation		
VAC (VRMS)	Freq (Hz)	V _{IN} (VRMS)	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
85	60	84.92	434.19	36.584	0.992	12.33	30.0300	1064.400	32.068	31.96	87.66	4.52
90	60	89.88	409.19	36.477	0.992	12.74	30.0300	1067.200	32.152	32.05	88.14	4.33
100	60	99.92	367.28	36.361	0.991	13.49	30.0340	1073.200	32.337	32.23	88.93	4.02
115	60	114.94	319.57	36.331	0.989	14.49	30.0420	1082.100	32.611	32.51	89.76	3.72
135	60	134.93	272.82	36.313	0.986	15.73	30.0470	1090.000	32.854	32.75	90.47	3.46
180	50	179.97	205.67	36.294	0.981	17.15	30.0460	1097.300	33.105	32.97	91.21	3.19
200	50	199.92	184.47	36.000	0.976	17.84	30.0290	1090.800	32.886	32.76	91.35	3.11
220	50	219.91	166.91	35.630	0.971	18.38	30.0090	1080.600	32.555	32.43	91.37	3.08
230	50	229.94	159.26	35.430	0.967	18.63	29.9960	1074.700	32.362	32.24	91.34	3.07
265	50	264.94	137.02	34.527	0.951	19.9	29.9520	1048.100	31.508	31.39	91.26	3.02
308	60	306.30	119.84	32.937	0.897	21.06	29.8150	1000.300	29.901	29.82	90.78	3.04

11.1.2 27 V LED String

Input		Input Measurement					Load Measurement			Calculation		
VAC (VRMS)	Freq (Hz)	V _{IN} (VRMS)	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
85	60	84.95	378.98	31.909	0.991	13.28	27.0180	1032.100	27.992	27.89	87.72	3.92
90	60	89.91	358.66	31.942	0.991	13.73	27.0230	1038.000	28.158	28.05	88.15	3.78
100	60	99.94	323.79	32.015	0.989	14.48	27.0330	1048.200	28.444	28.34	88.85	3.57
115	60	114.96	283.35	32.161	0.987	15.49	27.0450	1061.300	28.810	28.70	89.58	3.35
135	60	134.95	243.25	32.309	0.984	16.69	27.0560	1073.200	29.142	29.04	90.20	3.17
180	50	179.98	184.30	32.421	0.977	18.05	27.0580	1083.000	29.444	29.30	90.82	2.98
200	50	199.93	165.72	32.220	0.972	18.68	27.0440	1077.700	29.283	29.15	90.88	2.94
220	50	219.91	150.26	31.920	0.966	19.11	27.0280	1068.200	29.003	28.87	90.86	2.92
230	50	229.95	143.36	31.711	0.962	19.33	27.0160	1062.200	28.826	28.70	90.90	2.89
265	50	264.95	124.08	30.990	0.943	20.43	26.9770	1036.900	28.094	27.97	90.66	2.90
308	60	306.33	109.75	29.569	0.880	21.09	26.7770	991.600	26.634	26.55	90.07	2.94



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11.1.3 33 V LED String

Input		Input Measurement					Load Measurement			Calculation		
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{dc})	I _{OUT} (mA _{dc})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
85	60	84.92	503.32	42.440	0.993	11.54	33.1160	1115.500	37.050	36.94	87.30	5.39
33V	60	89.88	472.27	42.134	0.993	11.93	33.1090	1115.500	37.039	36.93	87.91	5.10
100	60	99.92	420.48	41.670	0.992	12.7	33.1040	1114.600	37.001	36.90	88.80	4.67
115	60	114.94	363.38	41.367	0.991	13.57	33.1060	1118.200	37.124	37.02	89.74	4.24
135	60	134.93	308.80	41.176	0.988	14.58	33.1100	1123.100	37.286	37.19	90.55	3.89
180	50	179.97	231.11	40.893	0.983	16.49	33.1030	1125.400	37.388	37.25	91.43	3.51
200	50	199.92	206.69	40.470	0.980	17.26	33.0820	1116.800	37.074	36.95	91.61	3.40
220	50	219.91	186.64	40.010	0.975	17.88	33.0600	1105.800	36.681	36.56	91.68	3.33
230	50	229.94	177.71	39.720	0.972	18.12	33.0420	1098.500	36.419	36.30	91.69	3.30
265	50	264.94	152.09	38.620	0.958	19.42	32.9840	1068.900	35.368	35.26	91.58	3.25
308	60	306.26	132.08	36.948	0.913	20.75	33.0170	1019.700	33.740	33.67	91.32	3.21



11.2 Regulation

11.2.1 Low Line Regulation

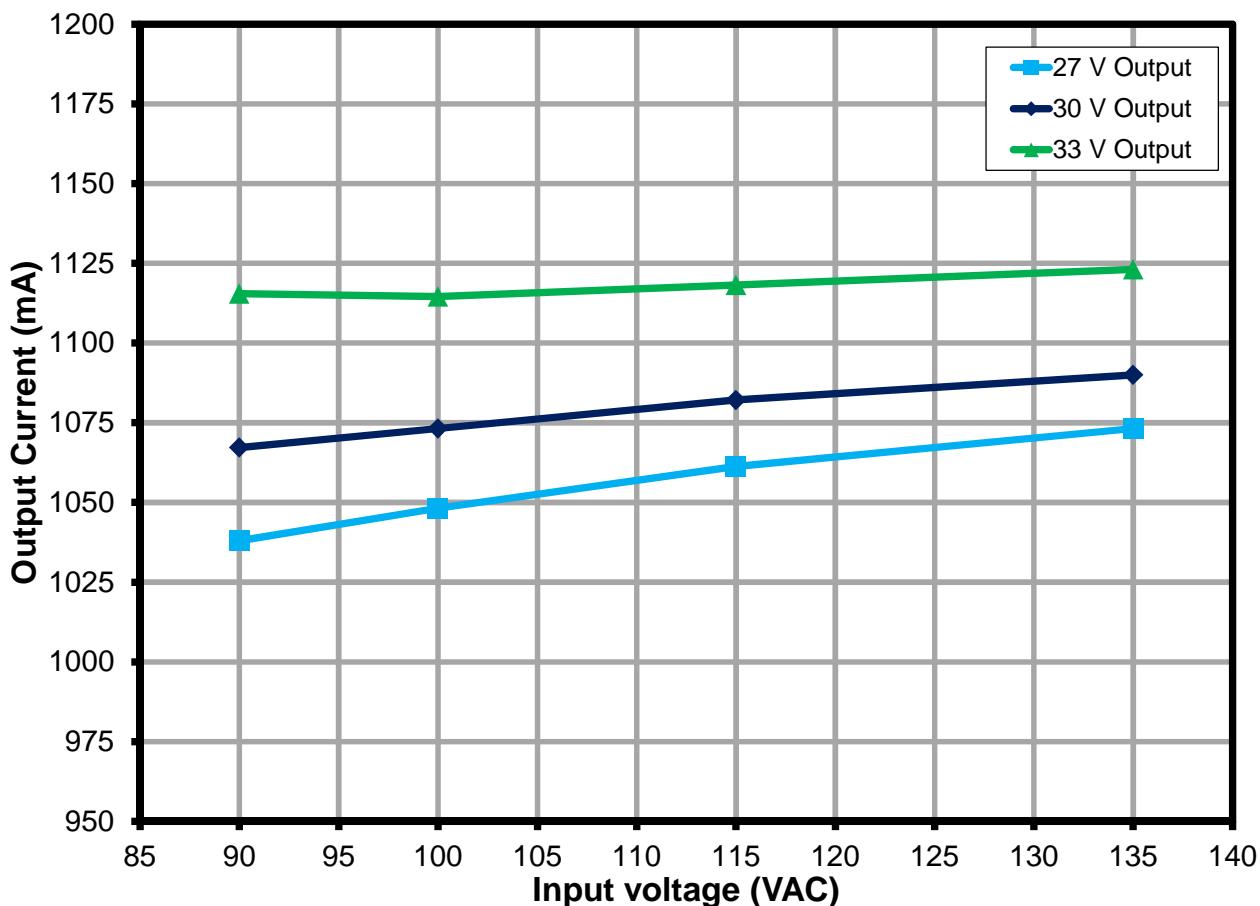


Figure 8 – Low-Line Regulation, Room Temperature, Full Load.



11.2.2 High Line Regulation

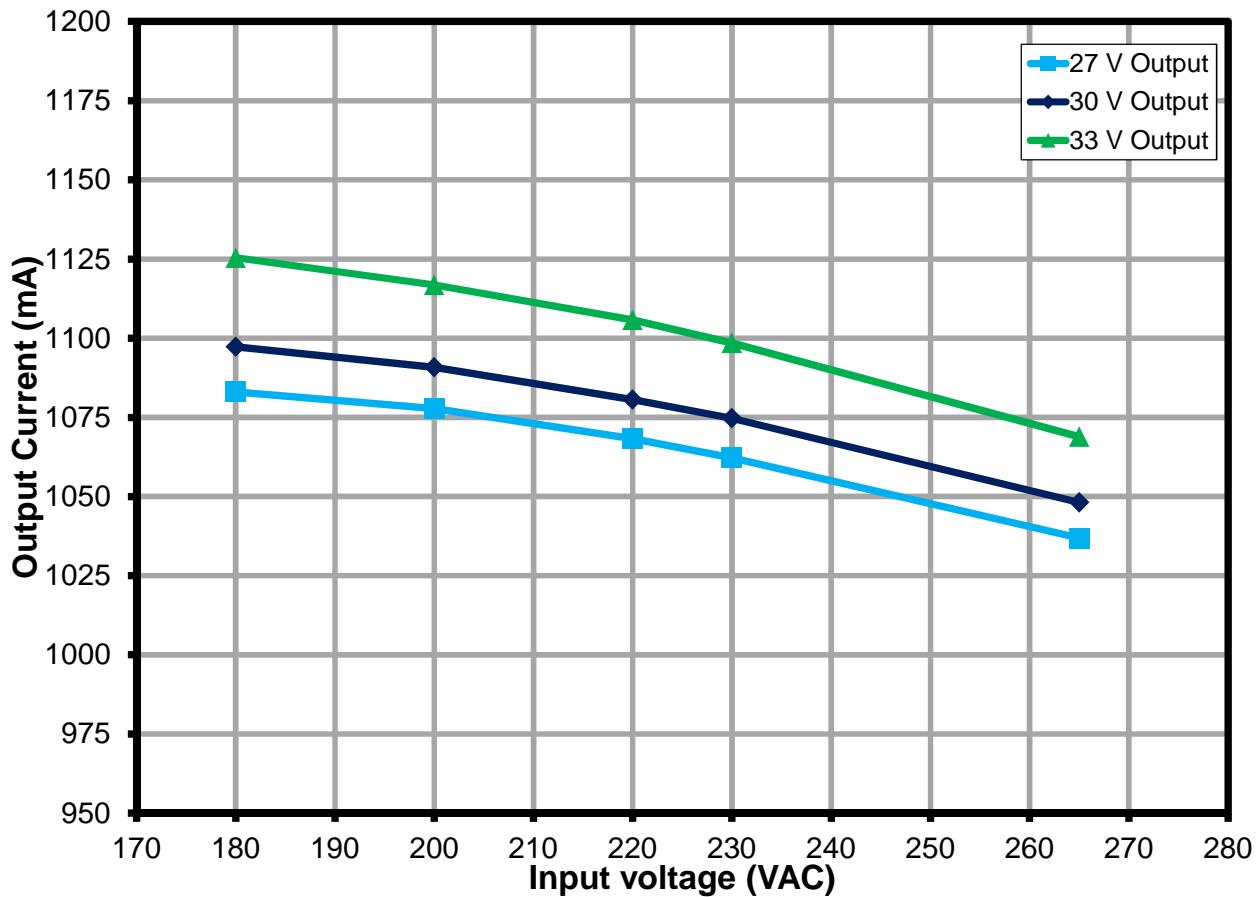


Figure 9 – High-Line Regulation, Room Temperature, Full Load.



12 Thermal Performance

Images captured after running for 30 minutes at room temperature (25 °C), full load (30 V, 500 mA). Hottest component is U1, providing system thermal protection via internal hysteretic thermal shutdown.

12.1 $V_{IN} = 115$ VAC

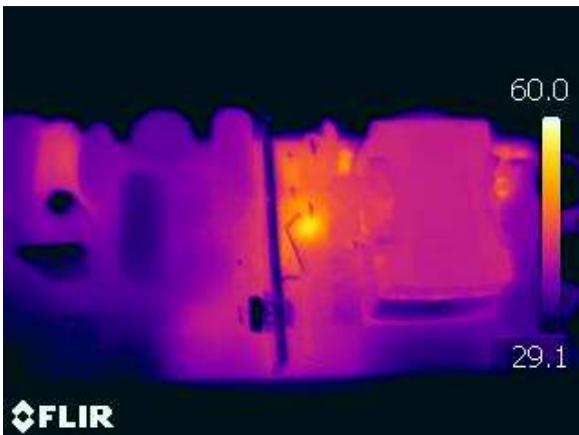


Figure 10 – Top Side.

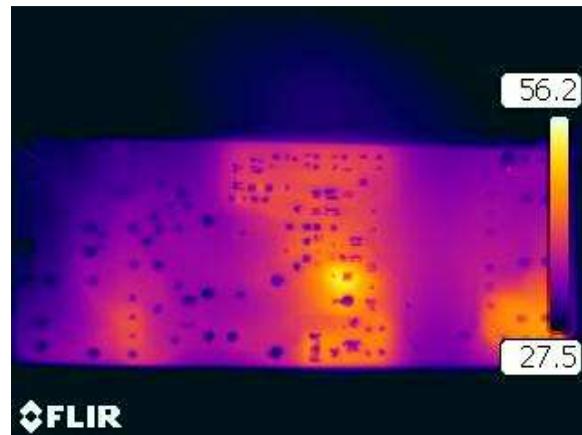


Figure 11 – Bottom Side.

12.2 $V_{IN} = 230$ VAC

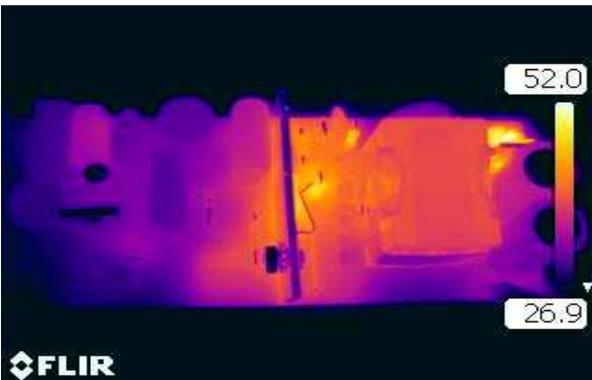


Figure 12 – Top Side.

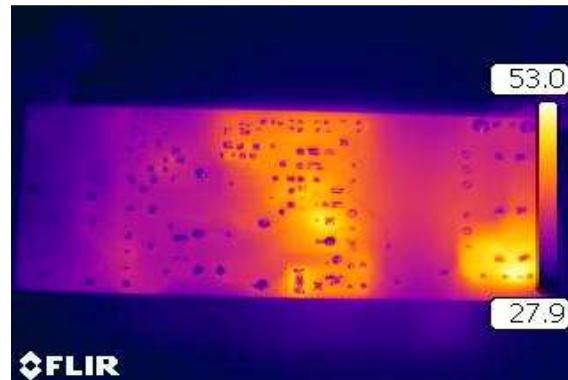


Figure 13 – Bottom Side.



13 Harmonic Data

The design passes Class C requirement.

13.1 115 VAC Input

V	Frequency	I (mA)	P	PF	%THD
115	60.00	319.57	36.3310	0.9891	14.49
nth Order	mA Content	% Content	Limit <25 W	Limit >25 W	Remarks
1	316.09				
2	0.58	0.18%		2.00%	
3	40.60	12.84%	247.0508	29.67%	Pass
5	14.54	4.60%	138.0578	10.00%	Pass
7	8.77	2.77%	72.6620	7.00%	Pass
9	4.49	1.42%	36.3310	5.00%	Pass
11	4.43	1.40%	25.4317	3.00%	Pass
13	2.16	0.68%	21.5191	3.00%	Pass
15	2.49	0.79%	18.6499	3.00%	Pass
17	1.78	0.56%	16.4558	3.00%	Pass
19	1.94	0.61%	14.7236	3.00%	Pass
21	1.52	0.48%	13.3214	3.00%	Pass
23	1.45	0.46%	12.1630	3.00%	Pass
25	1.59	0.50%	11.1899	3.00%	Pass
27	1.41	0.45%	10.3611	3.00%	Pass
29	1.27	0.40%	9.6465	3.00%	Pass
31	1.03	0.33%	9.0242	3.00%	Pass
33	1.05	0.33%	8.4772	3.00%	Pass
35	1.02	0.32%	7.9928	3.00%	Pass
37	0.79	0.25%	7.5608	3.00%	Pass
39	0.90	0.28%	7.1730	3.00%	Pass

Figure 14 – 115 VAC Harmonic, Room Temperature, Full Load.



13.2 230 VAC Input

V	Frequency	I (mA)	P	PF	%THD
230	50.00	159.26	35.4300	0.9674	18.63
nth Order	mA Content	% Content	Limit <25 W	Limit >25 W	Remarks
1	156.40				
2	0.05	0.03%		2.00%	
3	25.42	16.25%	120.4620	29.02%	Pass
5	10.90	6.97%	67.3170	10.00%	Pass
7	6.76	4.32%	35.4300	7.00%	Pass
9	3.44	2.20%	17.7150	5.00%	Pass
11	3.19	2.04%	12.4005	3.00%	Pass
13	1.68	1.07%	10.4927	3.00%	Pass
15	1.95	1.25%	9.0937	3.00%	Pass
17	1.21	0.77%	8.0239	3.00%	Pass
19	1.28	0.82%	7.1792	3.00%	Pass
21	1.06	0.68%	6.4955	3.00%	Pass
23	0.87	0.56%	5.9307	3.00%	Pass
25	0.95	0.61%	5.4562	3.00%	Pass
27	0.66	0.42%	5.0521	3.00%	Pass
29	0.82	0.52%	4.7036	3.00%	Pass
31	0.57	0.36%	4.4002	3.00%	Pass
33	0.62	0.40%	4.1335	3.00%	Pass
35	0.63	0.40%	3.8973	3.00%	Pass
37	0.52	0.33%	3.6866	3.00%	Pass
39	0.57	0.36%	3.4976	3.00%	Pass

Figure 15 – 230 VAC Harmonic, Room Temperature, Full Load.

V _{IN} = 115 VAC		
THD (%)	Limit (%)	Margin (%)
14.5	33	18.5
V _{IN} = 230 VAC		
THD (%)	Limit (%)	Margin (%)
18.6	33	14.4

Figure 16 – Total Harmonic Distortion (%).

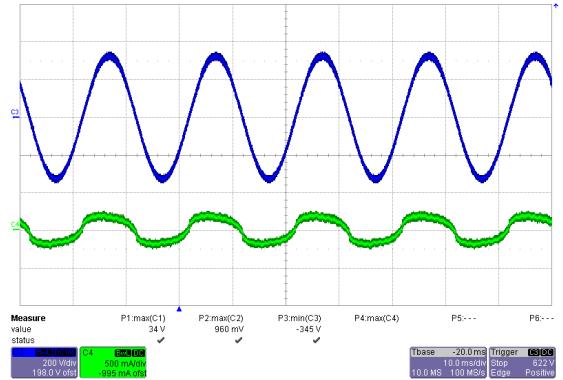
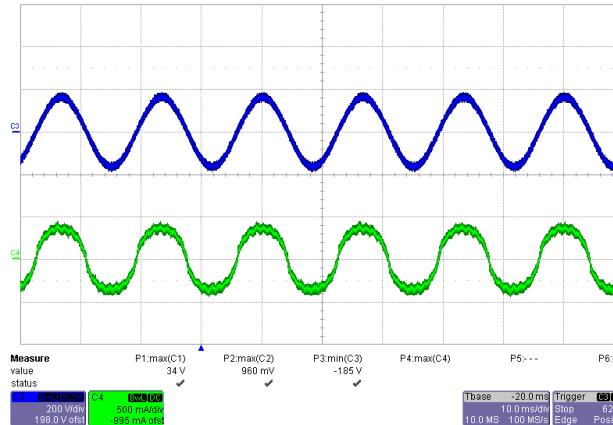


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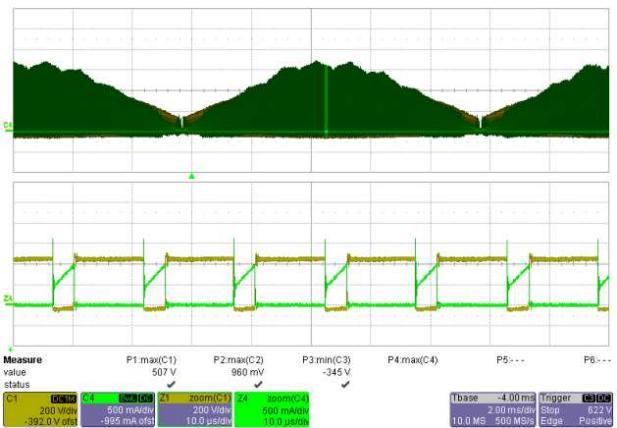
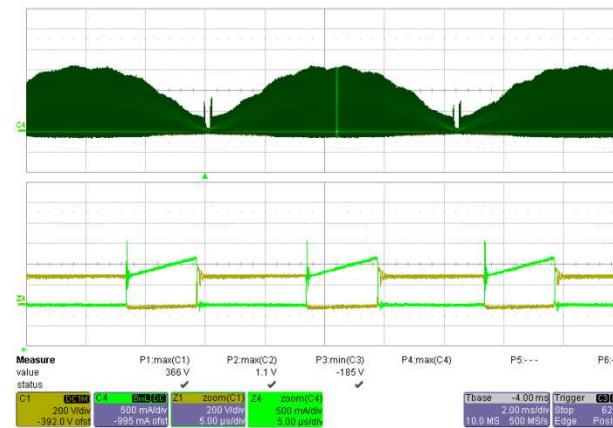
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14 Waveforms

14.1 Input Line Voltage and Current



14.2 Drain Voltage and Current



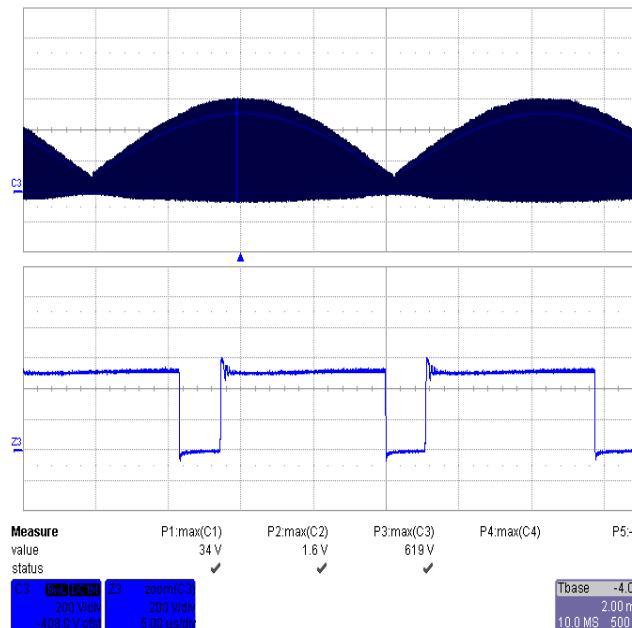


Figure 21 – 308 VAC, Full Load.
 V_{DRAIN} , 200 V / div, 2 ms / 5 μ s div.

14.3 Output Voltage and Ripple Current

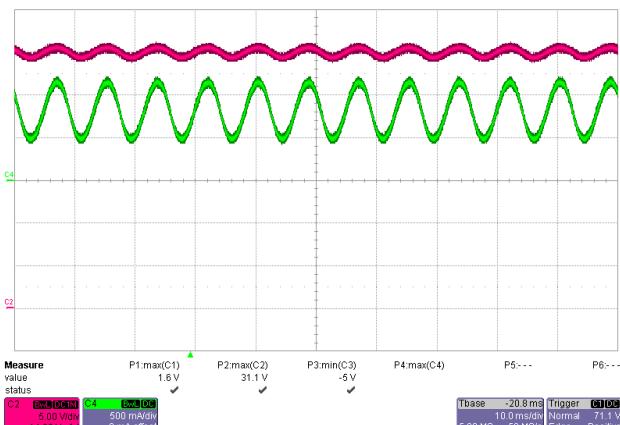


Figure 22 – 115 VAC, Full Load.
 Upper: V_{OUT} , 5 V / div.
 Lower: I_{OUT} , 0.5 A, 5 ms / div.

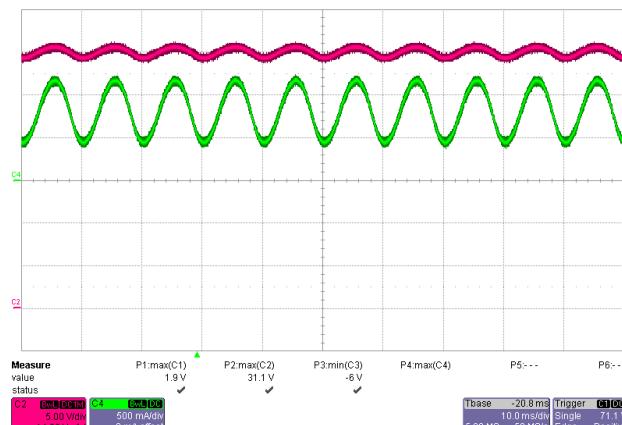


Figure 23 – 230 VAC, Full Load.
 Upper: V_{OUT} , 5 V / div.
 Lower: I_{OUT} , 0.5 A, 5 ms / div.



14.4 Output Rectifier Voltage and Current

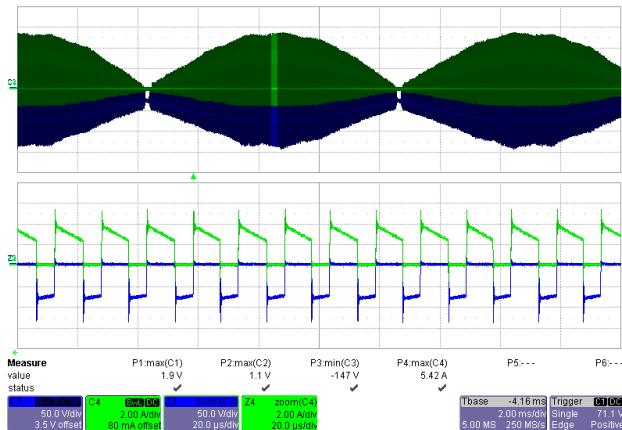


Figure 24 – 115 VAC, Full Load.

Upper: I_{RIPPLE} , 2 A / div.

Lower: V_{DIODE} , 50 V, 2 ms / 20 μs / div.

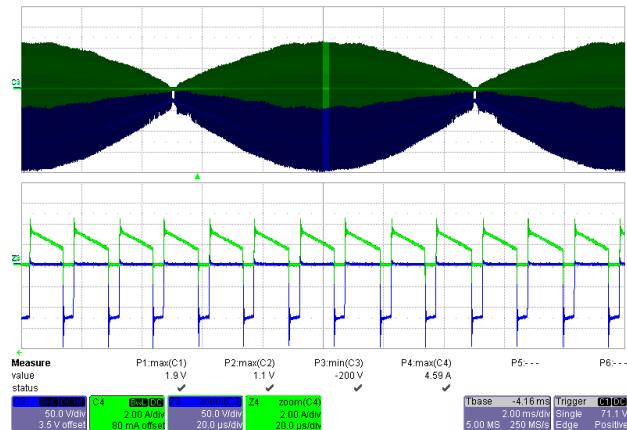


Figure 25 – 230 VAC, Full Load.

Upper: I_{RIPPLE} , 2 A / div.

Lower: V_{DIODE} , 50 V, 2 ms / 20 μs / div.

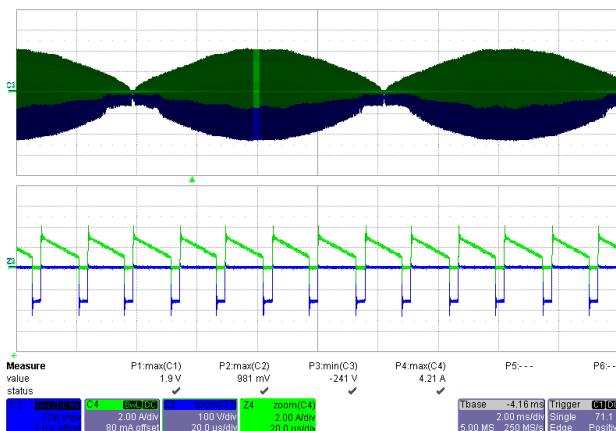


Figure 26 – 308 VAC, Full Load.

Upper: I_{RIPPLE} , 2 A / div.

Lower: V_{DIODE} , 100 V, 2 ms / 20 μs / div.



14.5 Input and Output Voltages Start-up Profile

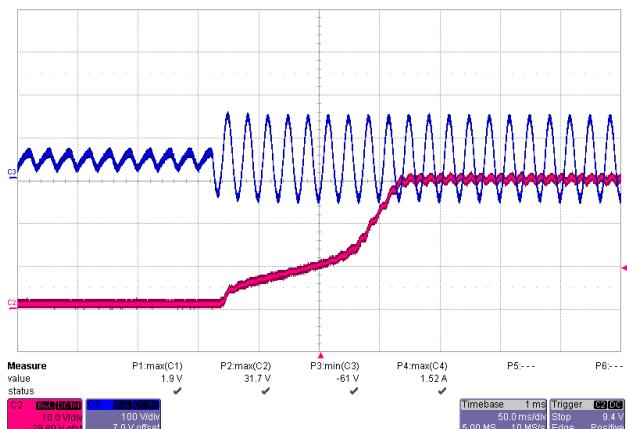


Figure 27 – 115 VAC, Full Load.

Upper: V_{IN} , 100 V / div.

Lower: V_{OUT} , 10 V, 50 ms / div.

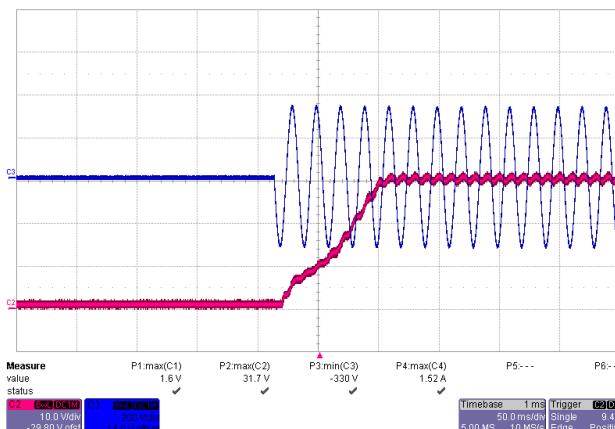


Figure 28 – 230 VAC, Full Load.

Upper: V_{IN} , 200 V / div.

Lower: V_{OUT} , 10 V, 50 ms / div.



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14.6 Output Current and Drain Voltage with Shorted Output

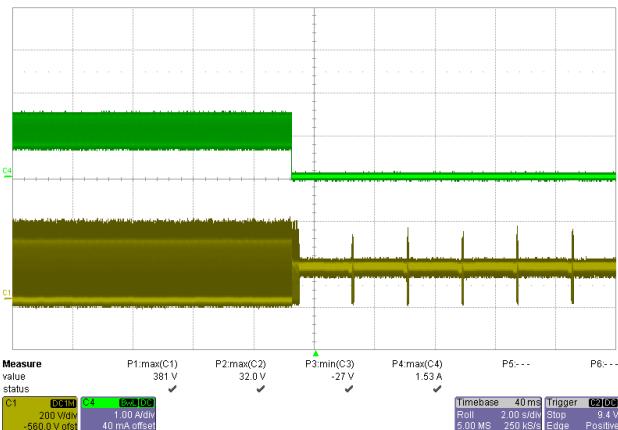


Figure 29 – 115 VAC, Full Load.

Upper: I_{OUT} , 1 A / div.
Lower: V_{DRAIN} , 200 V, 2 s / div.

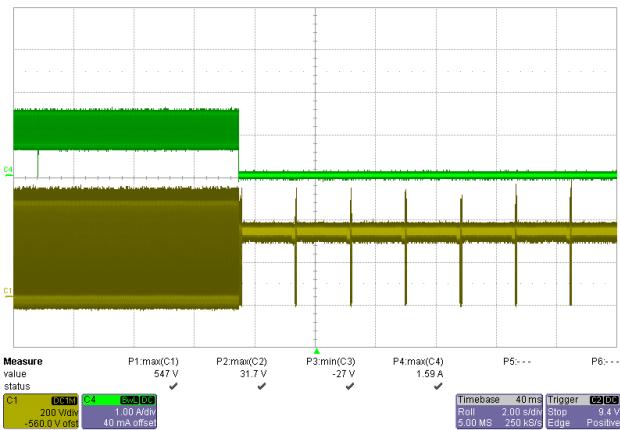


Figure 30 – 230 VAC, Full Load.

Upper: I_{OUT} , 1 A / div.
Lower: V_{DRAIN} , 200 V, 2 s / div.

14.7 Open Load Output Voltage

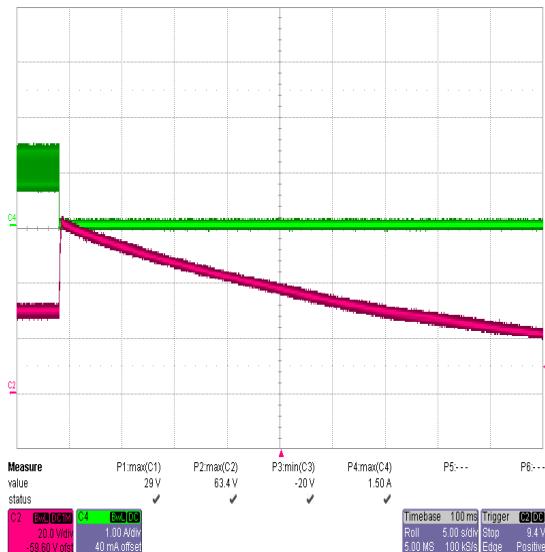


Figure 31 – 115 VAC, Full Load.

Upper: I_{OUT} , 1 A / div.
Lower: V_{OUT} , 20 V, 5 s / div.

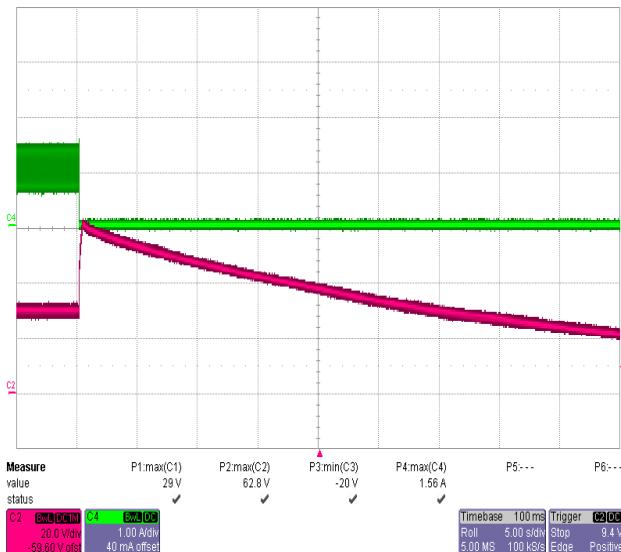


Figure 32 – 230 VAC, Full Load.

Upper: I_{OUT} , 1 A / div.
Lower: V_{OUT} , 20 V, 5 s / div.



15 Line Surge

1.2 μ s/ 50 μ s Surge

15.1 2.5 kV 2 Ω Differential Surge (No Primary Side Aluminum Capacitor)

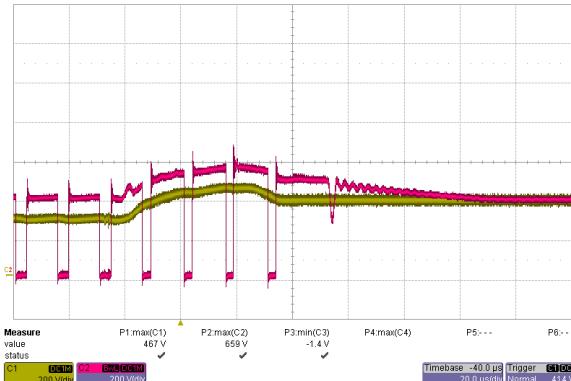


Figure 33 – 230 VAC, Full Load. (90°).

Yellow: V_{BUS} , 200 V / div.
Red: V_{DRAIN} , 200 V / 20 μ s div.

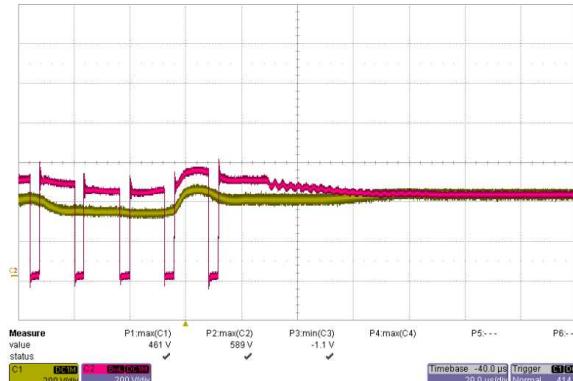


Figure 34 – 230 VAC, Full Load. (0°).

Yellow: V_{BUS} , 200 V / div.
Red: V_{DRAIN} , 200 V / 20 μ s div.

15.2 2.5 kV 2 Ω Differential Surge (With 10 μ F)

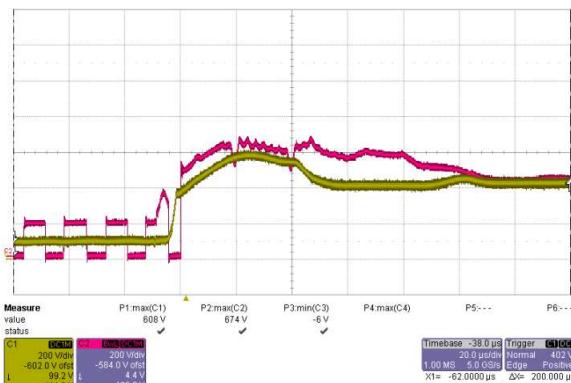


Figure 35 – 230 VAC, Full Load. (90°).

Yellow: V_{BUS} , 200 V / div.
Red: V_{DRAIN} , 200 V / 20 μ s div.

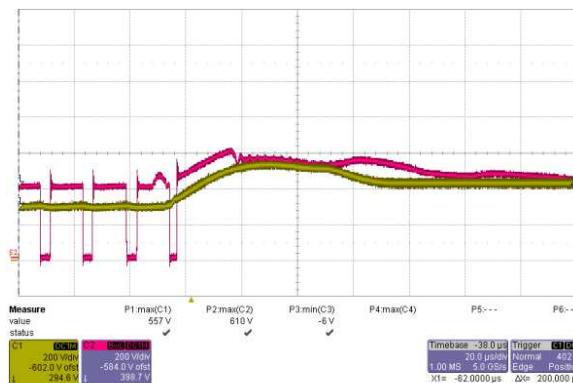


Figure 36 – 230 VAC, Full Load. (0°).

Yellow: V_{BUS} , 200 V / div.
Red: V_{DRAIN} , 200 V / 20 μ s div.



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16 Conductive EMI

Note: Refer to table for margin to standard – blue line is Quasi peak measurement and red line is average measurement

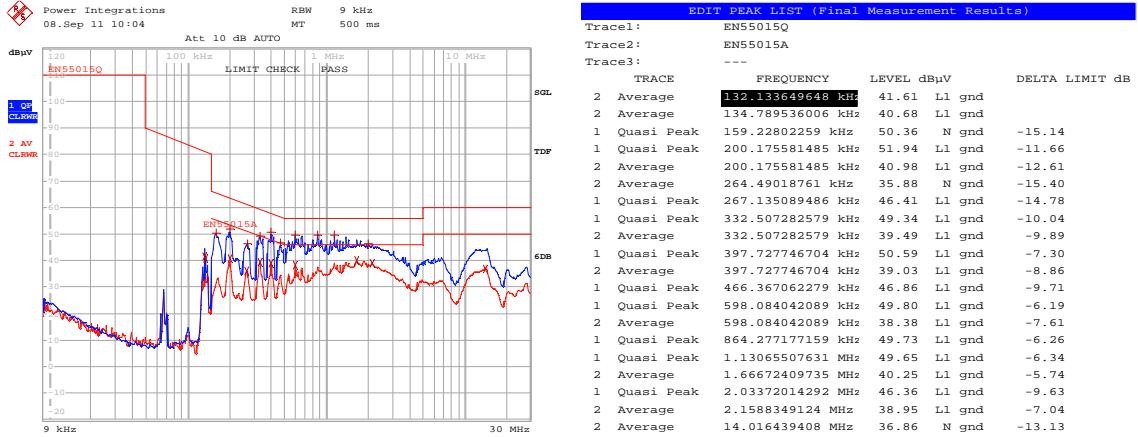


Figure 37 – Conducted EMI, Maximum Steady-State Load, 230 VAC, Neutral, 60 Hz, and EN55015 B Limits.

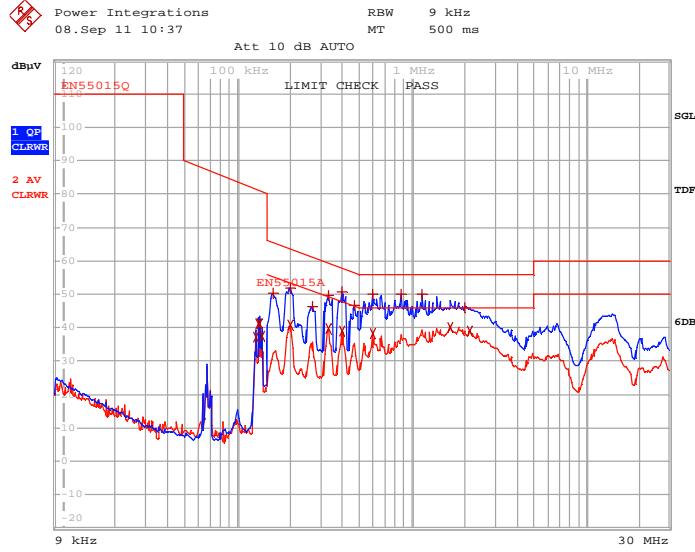


Figure 38 – Conducted EMI, Maximum Steady-State Load, 230 VAC, Line, 60 Hz, and EN55015 B Limits.



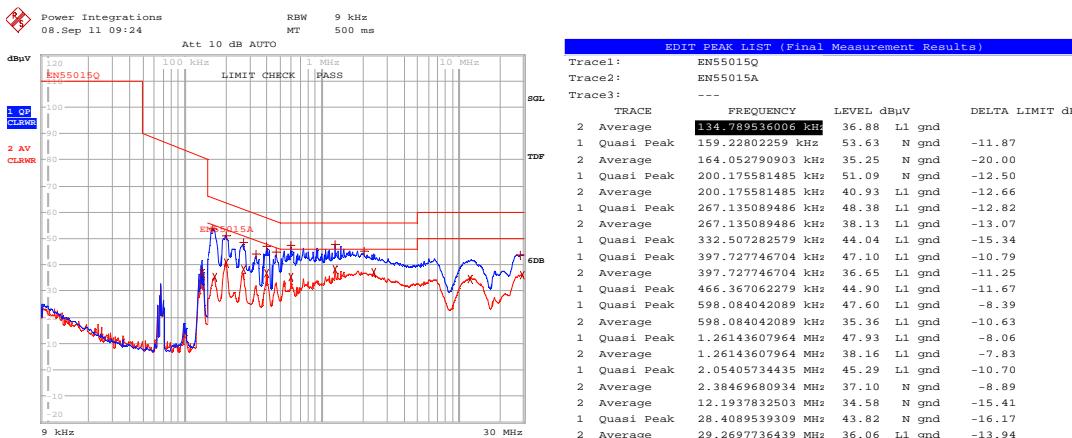


Figure 39 – Conducted EMI, Maximum Steady-State Load, 115 VAC, Neutral, 60 Hz, and EN55015 B Limits.

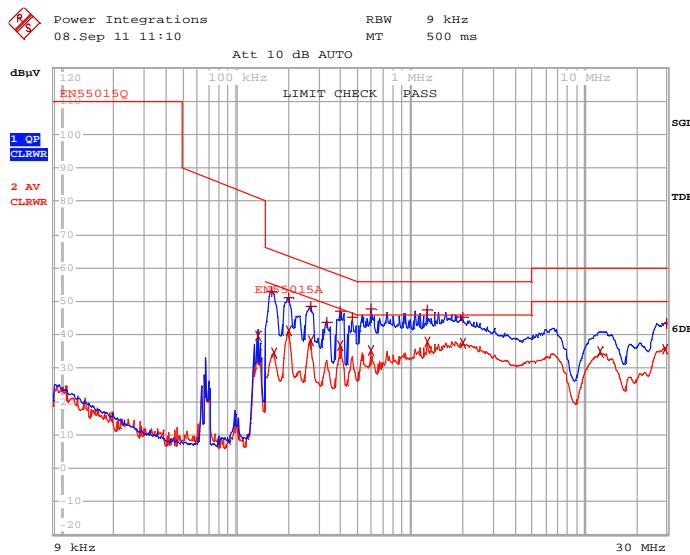


Figure 40 – Conducted EMI, Maximum Steady-State Load, 115 VAC, Line, 60 Hz, and EN55015 B Limits.



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17 Revision History

Date	Author	Revision	Description and Changes	Reviewed
07-Nov-11	DK	1.0	Initial Release	Apps & Mktg

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