

LED Driver Controller with Power Factor Correction

FEATURES

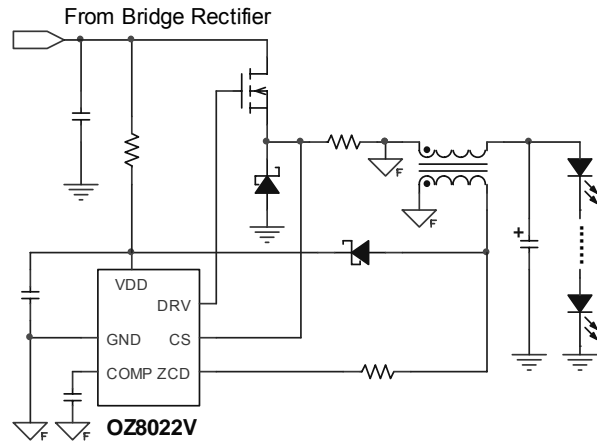
- Quasi-resonant converter controller for high brightness LEDs
- Supports high power factor for LED lighting applications
- Low start-up current and operating current to maximize conversion efficiency
- Voltage-mode control to simplify circuit design
- Under-voltage lockout with hysteresis
- Minimum off-time control for light-load operation maximizing efficiency
- Provides complete protection functions
 - Maximum gate drive output clamp
 - Over-voltage protection for IC bias voltage
 - Cycle-by-cycle current limit at current sense
 - LED short circuit protection
 - Output over-voltage protection
 - Internal over-temperature protection

feature to maximize the operating efficiency. Cycle-by-cycle current limiting at the CS pin ensures a safe operation during short-circuit at the output. The driver output voltage is clamped to protect the external power MOSFET. The IC provides over-voltage and over-temperature protection features.

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ8022V	-40°C to +105°C Note 3, Page 4	SOT23-6 Lead-Free

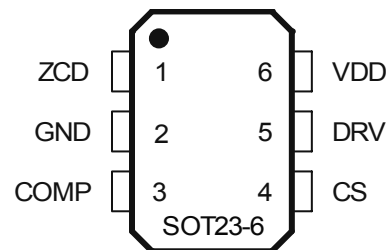
TYPICAL OPERATING CIRCUIT



APPLICATION

- LED driver

PIN DIAGRAM



GENERAL DESCRIPTION

OZ8022V is a controller for Buck converter utilizing quasi-resonant conversion technology. OZ8022V can be used for driving high-brightness LEDs with Power Factor Correction in off-line applications. The controller is implemented with a compensated voltage mode control to regulate the average LED current. The operation of the Buck converter is between the continuous mode and the discontinuous mode of the inductor current. During light-load condition, it provides a minimum off-time

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PIN DESCRIPTION

Name	I/O ¹	Pin No.	Description
ZCD	I	1	Input from auxiliary winding for zero-current detection and output over-voltage sense.
GND	Power	2	Power ground.
COMP	O	3	Output of the error amplifier. A compensation network is placed between COMP and GND to provide stable frequency response.
CS	I	4	Current sense pin. A resistor is connected to sense the MOSFET current.
DRV	O	5	Output to drive the external power MOSFET.
VDD	Power	6	Power Supply.

Note¹: I=Input, O=Output

BLOCK DIAGRAM

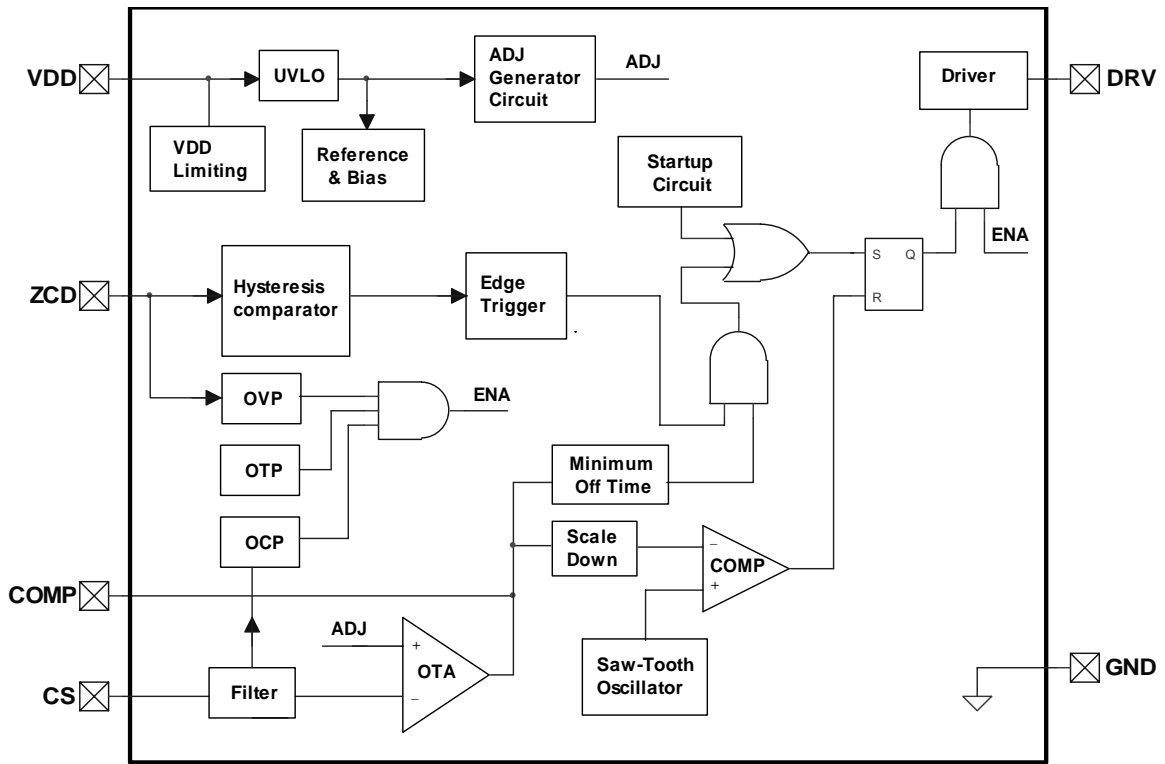


Figure 1: Block Diagram

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ABSOLUTE MAXIMUM RATINGS²

Parameter	
Supply Voltage	-0.3V to 35.0V
VDD Maximum Supply Current Limit for OVP Condition	20.0mA
Input Voltage to CS Pin	-0.3V to 7.0V
Output Voltage at the COMP pin	-0.3V to 7.0V
Maximum Current at ZCD Pin	10mA (Source) 10mA (Sink)
Maximum Operating Junction Temperature ³	150°C
Storage Temperature Range	-55°C to 150°C

Note: Operation beyond the above ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter		
VDD Supply Voltage	17.0V ~ 25.0V	
Operating Temperature ³	-40°C to +105°C	
Operating Junction Temperature ³	125°C	
Thermal Impedance ^{3,4}	θ_{J-C}	θ_{J-A}
SOT23-6	15°C/W	113°C/W

Note²: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the IC. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The “Electrical Characteristics” table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability

Note³: Not to exceed the maximum junction temperature of the IC, which relates to the operating power of the IC and the thermal resistance of the IC/package as above.

- Using OZ8022V in an application circuit with an ambient temperature near 105°C, the recommended power dissipation of the SOT23-6 package is less than 175 mW.
- It is recommended that the customer contact their local O2Micro Field Application Engineer (FAE), if the application is significantly different from the Reference Application Circuit illustrated in Figure 4, Page 10.

Note⁴: Still air, low effective thermal conductivity board per JESD51-3.

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ELECTRICAL CHARACTERISTICS⁵

All specifications below are at ambient 25°C; VDD=18.0V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Supply Voltage (VDD Pin)						
I _{ST}	Startup Current	Before IC turns on VDD=10V		6	12	µA
I _{SS}	Operating Current	@ 70kHz	0.5	1.7	3.0	mA
V _{DDON}	Turn-on Threshold Voltage		14.5	15.5	16.5	V
V _{DDOFF}	Turn-off Threshold Voltage		8.5	9.5	10.5	V
V _{DDHY}	UVLO Hysteresis		4.0	6.0	8.0	V
V _{DDCLAMP}	VDD Clamp Voltage	30mA sink current	29.0	32.0	35.0	V
V _{DDOVP}	VDD Threshold with DRV Turn-Off		26.0	29.0	32.0	V
Internal OTA						
V _{OTAP}	Reference for Non-Inverting Input (ADJ)	(**)	208	232	256	mV
OCP	Over Current Protection Threshold	CS Pin	0.8	0.9	1.0	V
	Over Current Protection Release Threshold		200	235	270	mV
Zero Current Detector (ZCD Pin)						
V _{ZCDU}	Upper Clamp Voltage	ZCD Pin	2.7	3.0	3.2	V
V _{ZCDL}	Lower Clamp Voltage	ZCD Pin	0.2	0.3	0.4	V
V _{ZCDSE}	ZCD Voltage with 2.5mA Source Current	I _{ZCDSE} =2.5mA	0.1	0.2	0.3	V
V _{ZCDSK}	ZCD Voltage with 2.5mA Sink Current	I _{ZCDSK} =2.5mA	2.7	3.0	3.3	V
I _{OVP}	Over Voltage Protection Threshold at ZCD Pin	ZCD Pin	270	300	330	µA
Start-up Circuit						
t _{ST}	Start-up Period		30	51	73	µs
Current Sense (CS Pin)						
T _{LEB}	Leading-Edge Blanking Time	CS Pin	250	400	550	ns
GATE Drive Output (DRV Pin)						
T _R	Rise Time	C _L =1nF	20	60	100	ns
T _F	Fall Time	C _L =1nF	20	60	100	ns
V _{GCLAMP}	Gate Clamp Voltage		15.5	17.5	19.5	V

Note⁵: Use of this product outside the limits of the test conditions may experience in a variation of parameters from the published parameters. If additional information is needed, please consult with your O2Micro Field Application Engineer (FAE).

(**) +3.5% of equivalent ADJ (230mV – 246mV) is guaranteed when application circuit is implemented as shown in Figure 5.

PARAMETERS GUARANTEED BY DESIGN⁶

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Zero Current Detector (ZCD Pin)						
V _{PET}	Threshold for Positive Going Edge		1.4	1.5	1.6	V
V _{NET}	Threshold for Negative Going Edge		0.9	1.0	1.1	V
T _{BLANK}	Blanking Time after DRV Signal High-to Low Transition	V _{COMP} ≥ 1V	3.0	4.0	5.0	μs
		V _{COMP} = 0V	30	40	50	
T _{B_OVP}	Blanking Time for OVP Detection	ZCD Pin	1.2	1.6	2.0	μs
Current Sense (CS Pin)						
V _{CL}	Current Limit Threshold		1.0	1.1	1.2	V
GATE Drive Output (DRV Pin)						
V _{OL}	Output Low Level				1.0	V
V _{OH}	Output High Level		6.0			V
Over-Temperature Protection						
OTP	Over Temperature Lockout		130	140	150	°C
	Over Temperature Resume		100	110	120	°C

Note⁶: Parameters Not Tested

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FUNCTIONAL DESCRIPTION

OZ8022V is a controller for Buck converter applications utilizing quasi-resonant conversion technique. It is optimized for high brightness LED driver applications with Power Factor Correction. It operates near the Discontinuous-Mode and Continuous-Mode operation of the inductor. It provides a high conversion efficiency and lower EMI for the AC/DC converter application. Refer to Figure 1, Page 3, and Figure 4, Page 10 for the following discussions. All parameters mentioned below are typical values.

Startup Current and Under Voltage Lockout

Applying the AC power to the rectifier will provide the initial the operation the controller. It takes a typical of 6uA to start the IC. To minimize power losses, a large start-up resistor can be connected between rectified line voltage and VDD pin. During start-up, a capacitor C3 is charged up to 15.5V by resistors R1, R2 and R3. The turn-on and turn-off thresholds of OZ8022V are designed to be 15.5V and 9.5V respectively. The hysteresis is implemented to prevent abnormal shutdown due to line voltage transient drop during the period.

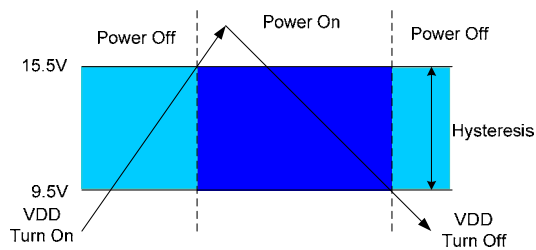


Figure 2: VDD Power Supply Hysteresis

Before normal operation of the converter, the internal startup circuit generates drive pulses to initiate the operation of the quasi-resonant converter. The pluses turn on switch Q1. The time when compensated signal intersects with the saw-tooth signal will turn off the switch. This provides current flowing through the transformer (inductor) T1, inducing current sense signal and a zero-current-detect signal. These are described below.

Zero Current Detector

During normal operation, the turn-on and turn-off of Q1 introduces a switching waveform seen at the auxiliary winding of T1. ZCD pin receives a positive-swing voltage signal when Q1 turns off.

Internal to the ZCD pin is designed to provide clamping thresholds between 0.3V and 3.0V. When the positive-swing signal goes beyond 1.5V, the ZCD circuit is ready to control the next turn-on of the switch Q1 after a blank-off time. The blank-off time is provided to avoid any noises and/or any resonance of parasitic effect during the switching. After the blank-off time, when ZCD detects a voltage falls to 1.0V, the controller initiates the next cycle turn-on of the switch Q1. Current flows through the sense resistor R4 and transformer (inductor) T1. The current is detected through CS pin and being processed to compare with an internal reference ADJ to yield a compensation signal. The compensation signal is then further compared with an internal saw-tooth waveform generated by Saw-Tooth Oscillator. Once the compensated signal intersects with the saw-tooth signal, the switch Q1 will be turned off. Energy stored in the transformer (inductor) is now being delivered to the load through via the free-wheeling diode D1. It continues until the current flow decreases to near zero, the winding voltage swings the polarity, the ZCD signal is then again to turn on switch Q1 for the next cycle.

The operation repeats. The ON time of the switch is controlled and kept a constant value corresponding to an input line voltage. A high power factor is then provided with a low rate-of-change control loop.

Parasitic effect or noises may be more significant during high-input voltage conditions in practices. The ZCD pin which dictates the turn-on of the switch Q1 is designed to blank off any possible noises during operation. When input voltage goes higher, current sense pin CS rises, the COMP, compensated signal will decrease. The controller is built-in with compensated blank-off time followed the voltage signal at COMP. This is illustrated in Figure 3. Under the condition, the application circuit is operated with an equivalent "minimum off time" of the switch Q1. The stated quasi-resonant mode is no longer the operating mode. Power factor is slightly affected.

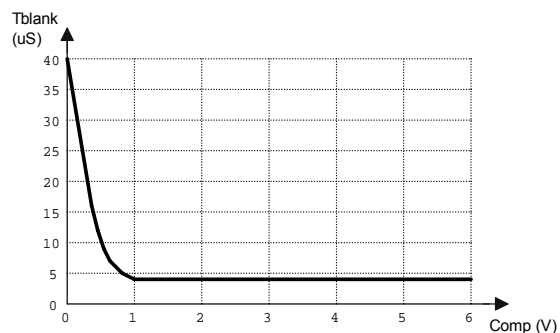


Figure 3: COMP Voltage vs. Blanking Time

Gate Driver

A totem-pole drive output at DRV delivers the gate-drive signals to the external power MOSFET. A proprietary soft-clamp circuit is designed to protect the external power MOSFET from being over stressed.

Internal Filter at Current Sense

When MOSFET Q1 is switched on, a current spike may occur at pin CS due to any parasitics in the application circuit. The controller provides a built-in filter to ignore the first 400ns period at CS signal to avoid the MOSFET being turned off inadvertently. Select resistor R4 at pin CS for LED current setting. It is to compare with the internal reference ADJ as 232mV. The LED typical current can be calculated by the equation:

$$I_{LED} = \frac{V_{ADJ}}{R_{Sense}} = \frac{232(mV)}{R_4(ohm)} \quad (1)$$

Open LED Protection (OVP)

When the LED load is opened, the control loop intends to regulate the rated current flowing through LEDs. Under this condition, the output voltage rises. The voltage at the auxiliary winding of the transformer increases. The voltage at VDD is therefore increases. Internal to the IC, the VDD pin is designed to clamp at 32V while is capable of sinking 30mA. Meanwhile, the voltage at the auxiliary winding supply a current through resistor R7 to ZCD pin. If the current received at pin ZCD exceeds 300uA for longer than 1.6μs during the off-time of the MOSFET Q1, OZ8022V will shut off the control (switching) operation. To resume, the voltage at VDD needs to drop to a threshold of 9.5V (UVLO) and then increases to the turn-on threshold voltage of 15.5V.

Designing a circuit to prevent the output voltage at LED from being excessive, designer can select parameters based on the following equation

$$V_{OUT_OVP} = \frac{N_P}{N_{AUX}} \times (300\mu A \times R_{ZCD} + 3.0V) \quad (2)$$

where N_P is the number of turns of the primary winding connected to LED output. N_{AUX} is the number of turns of the auxiliary winding. R_{ZCD} (R7) represents the resistor connected between pin ZCD and auxiliary winding.

VDD Over Voltage Protection and Clamp Function

OZ8022V provides VDD over voltage protection function. When the VDD voltage exceeds 29V, the controller will turn off the power MOSFET. To resume operation, the voltage at VDD needs to drop to 9.5V (UVLO) and then increases to the turn-on threshold of 15.5V. If abnormal condition happens, after VDD voltage reaches 32V, VDD voltage will be clamped at 32V.

Short LED Protection

CS pin in the controller provides a current sense as well as over current protection. Switch Q1 will be turned off when CS pin reaches an average of 0.9V as a threshold for over-current protection. When a number of LEDs in a string are shorted, or the output terminal for the LEDs is shorted to ground, current flowing through the inductor rises sharply. When the current sense pin CS reaches 1.1V threshold, the controller turns off the output driver. It will not be turned on again until the next cycle starts. The cycle-by-cycle current-limit function prevents external components from being damaged under the fault conditions. As the short-circuit condition continues, the output voltage will drop. The reflected voltage at VDD will also decrease. Once the voltage at VDD drops below a threshold of 9.5V, the IC will cease operation. Once OZ8022V is shut off, the rectified line voltage will charge the VDD capacitor via the start-up resistor following the start-up mode described above.

Thermal Protection

Thermal protection occurs when the IC experiences a high junction temperature. The MOSFET drive is turned off once the junction temperature exceeds approximately 140°C. It resumes normal operation when the junction temperature drops to or below approximately 110°C.

LED current accuracy

The application circuit in Figure 4 is recommended to operate at the output voltage range between 10V to 40V and 85Vac-265Vac line input. The LED current is the average of the inductor current. The current at CS pin is a saw-tooth waveform modulated with the line frequency signal, it is not a DC value and the gain of the internal OTA is not uniformed within the line-frequency period. The equivalent ADJ voltage range is between 208mV and 256mV defined in the electrical characteristic.

The LED typical current is set by the equation (1), and the LED current will experience a $\pm 10\%$ tolerance.

When the current-sense signal is filtered through a low-pass filter R9 and C5, as shown in Figure 5 of an Application Circuit, the gain of the internal OTA is uniformed during the operation. The equivalent ADJ voltage range is between 230mV and 246mV as stated in the Electrical Characteristic. Since the low-pass filter may not react fast to LED short-circuit condition, the protection is implemented by circuitry R10, C6 and Q2. When LED short circuit occurs, the MOSFET Q2 is turned on to pull COMP pin to GND to prevent any damages under the short-circuit condition.

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TYPICAL APPLICATION SCHEMATIC

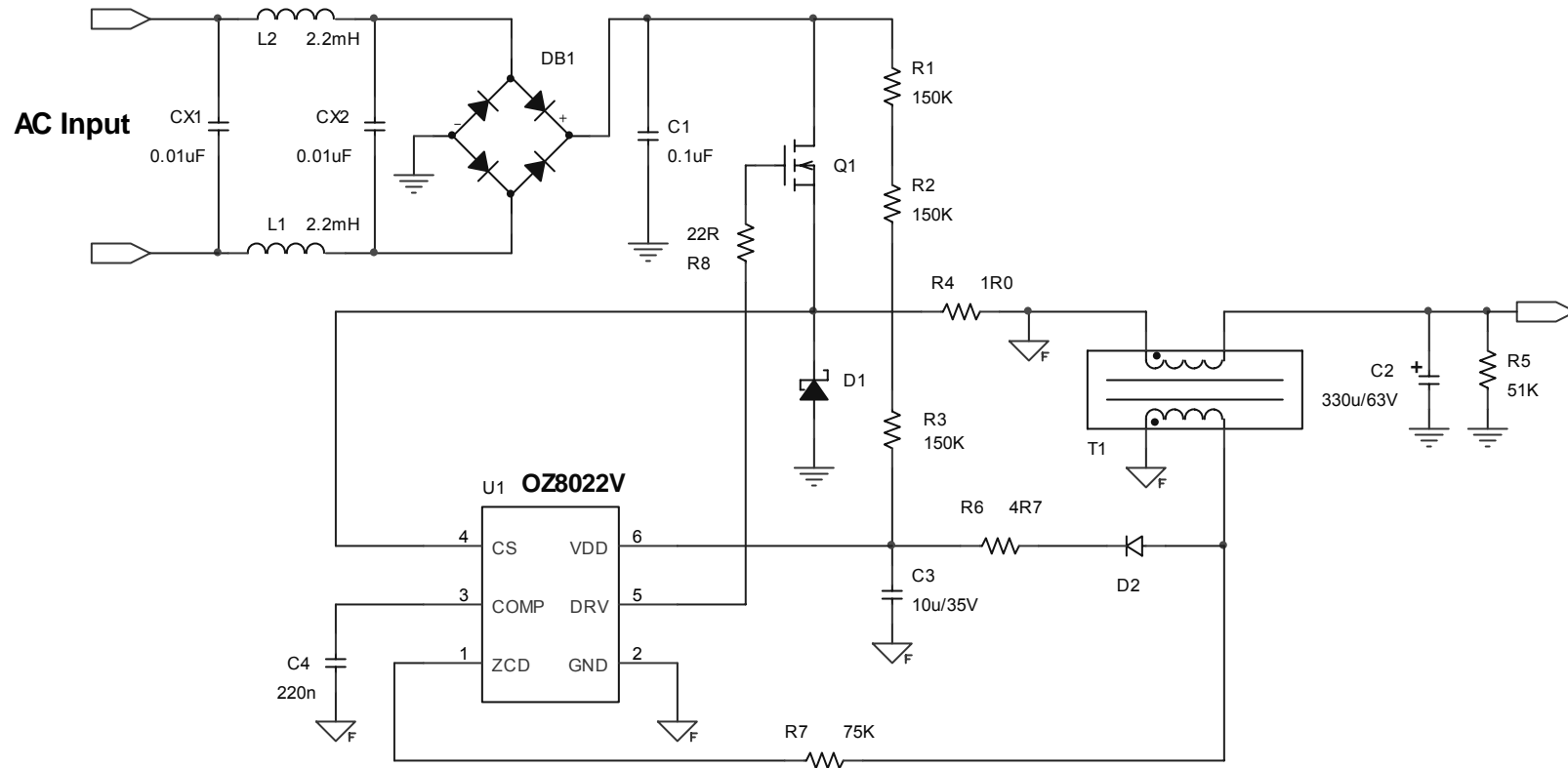


Figure 4: Typical Application Circuit

Note 1: If input voltage range is from 85VAC to 265VAC with Figure 4 schematic, recommended LED voltage should be between 10V to 40V.

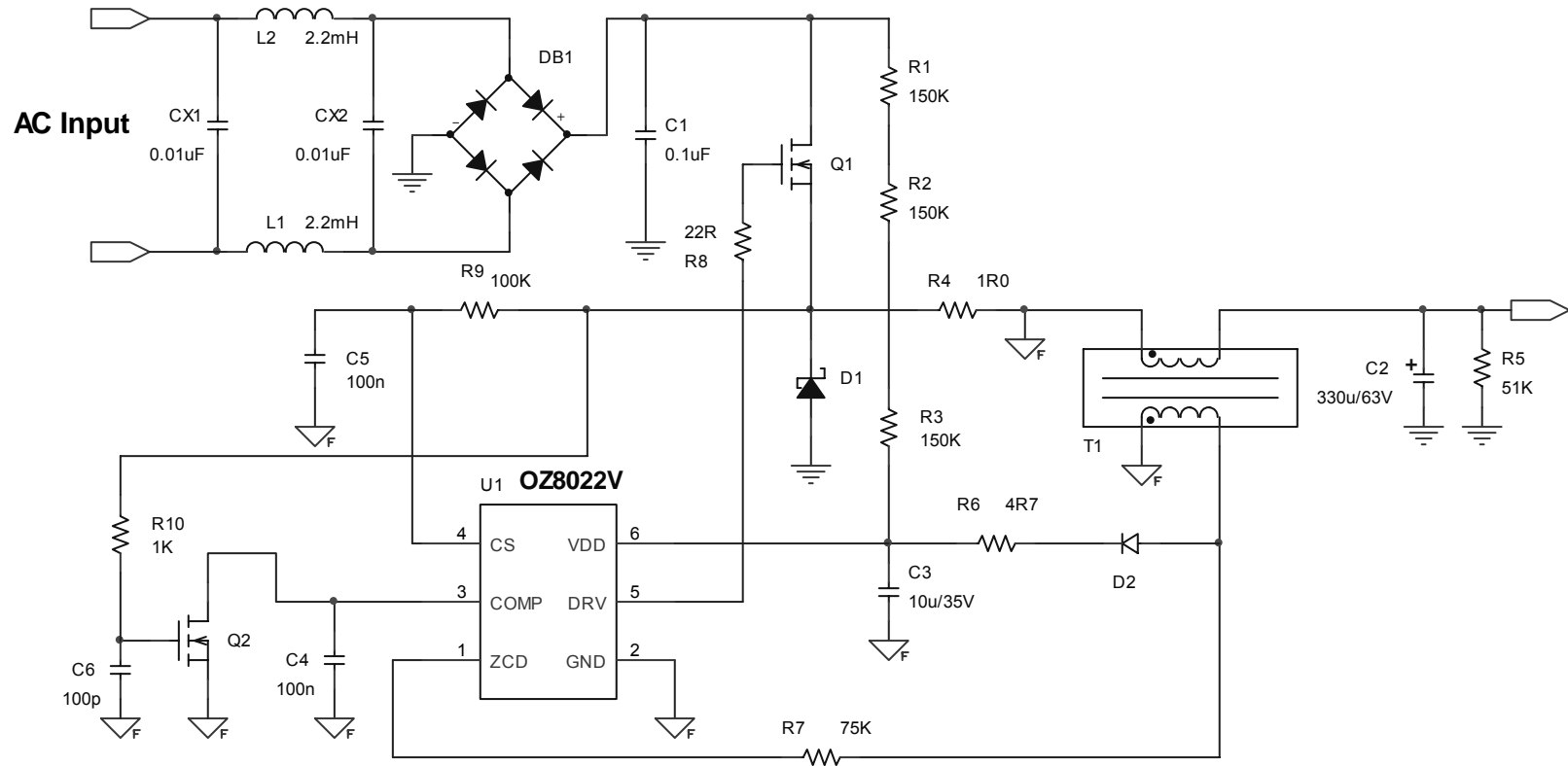
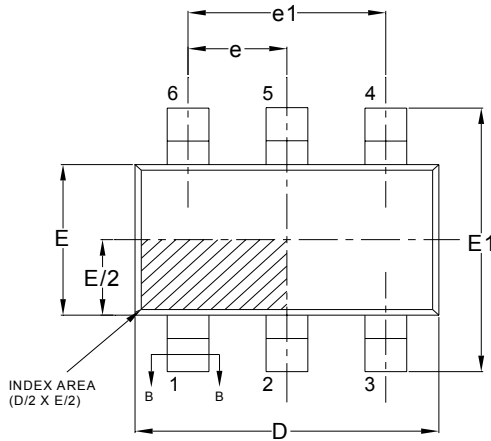


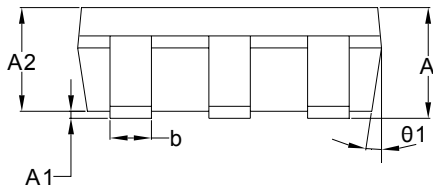
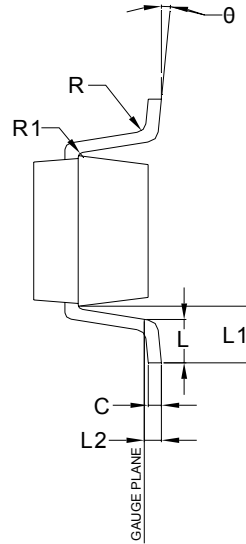
Figure 5: Typical Application Circuit

PACKAGE INFORMATION: SOT23-6: OZ8022V

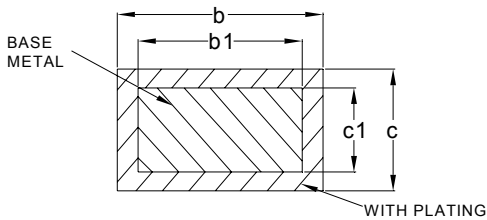
6L SOT23 Package Outline Drawing



TOP VIEW



SIDE VIEW



SECTION B-B

NOTES:

1. REFER TO JEDEC OUTLINE MO-178
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER END. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE

Symbol	Millimeters (unit : mm)		
	MIN.	NOM.	MAX.
A	-	-	1.45
A1	-	-	0.15
A2	0.90	1.15	1.30
b	0.30	-	0.50
b1	0.30	0.40	0.45
c	0.08	-	0.22
c1	0.08	0.13	0.20
D	2.90 BSC		
E	1.60 BSC		
E1	2.80 BSC		
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
L1	0.60 BSC		
L2	0.25 BSC		
theta	0°	4°	8°
theta1	5°	10°	15°
R	0.10	-	-
R1	0.10	-	0.25

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