Desaturation Fault Detection
Optocoupler Gate Drive Product with Feature: ACPL-332J, ACPL-331J and HCPL-316J

Application Note 5324

1. Introduction

Desaturation fault detection circuit provides protection for power semiconductor switches (IGBT or MOSFETs) against short-circuit current events which may lead to destruction of these power switches. This desaturation of the inverters can also occur due to an insufficient gate drive signal from the inverter gate driver misperformance or driver supply voltage issues. Other failure modes that can potentially cause excessive currents and excessive power dissipations in the inverters can be due to phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, over load conditions induced by the load, and component failures in the gate drive circuitry. The drastically increased power dissipation very quickly overheats the power inverter and destroys it. To prevent catastrophic damage to the drive, desaturation fault detection and protection must be implemented to reduce or turn-off the overcurrents during the fault condition. This application note covers the design of desaturation fault detection feature provided by Avago Intelligent Gate Driver.

How does desaturation fault detection feature work in Avago driver?

i. Fault Detection

The IGBT collector-emitter voltage, VCESAT, is monitored by the DESAT pin of the Gate Drive Optocoupler (Pin 14 of Figure 1). When there is short circuit in an application and a very high current flow through the IGBT, it will go into desaturation mode; hence its VCESAT voltage will rise up. A fault is detected by the optocoupler gate driver (while the IGBT is ON) once this VCESAT voltage goes above the internal desaturation fault detection threshold voltage which is typically 7.0V. This fault detection triggers two events:

a. Vout of the optocoupler gate driver is slowly brought low in order to "softly" turn-off the IGBT and prevent large di/dt induced voltage spikes and

b. Also activated is an internal feedback channel which brings the Fault output low for the purpose of notifying the micro-controller of the fault condition. At this point, the microcontroller must take the appropriate action to shutdown or reset the motor drive.

by the DESAT feature, a weak pull-down device in the output drive stage will turn on to 'softly' turn off the IGBT and prevents large di/dt induced voltages. This device slowly discharges the IGBT gate to prevent fast changes in collector current that could cause damaging voltage spikes due to stray inductances. During the slow turn off, the large output pull-down device remains off until the output voltage falls below \( V_{EE} + 2 \) Volts, at which time the large pull down device clamps the IGBT gate to \( V_{EE} \) (Refer to Figure 1).

ii. Soft turn-off

This feature exists in Avago gate optocoupler, (e.g. ACPL-332J, ACPL-331J and HCPL-316J). When fault is detected by the DESAT feature, a weak pull-down device in the output drive stage will turn on to 'softly' turn off the IGBT and prevents large di/dt induced voltages. This device slowly discharges the IGBT gate to prevent fast changes in collector current that could cause damaging voltage spikes due to stray inductances. During the slow turn off, the large output pull-down device remains off until the output voltage falls below \( V_{EE} + 2 \) Volts, at which time the large pull down device clamps the IGBT gate to \( V_{EE} \) (Refer to Figure 1).

iii. Off State and Reset

During the IGBT off state, the driver fault detection circuitry is disabled to prevent false ‘fault’ signals. The fault output, Pin 3 of Figure 1 is pulled down and output Pin 11 goes low for the duration of the fault. In ACPL-332J and ACPL-331J, the fault is reset at the next positive input signal to the driver after a fixed mute time. For HCPL-316J, it has to be reset externally through a Reset pin (Pin 5 of Figure 2). For both case, it will only be cleared when DESAT detection has gone to low (Short-circuit is cleared).

iv. Under Voltage Lock-Out protection (UVLO) with hysteresis

The Output of the optocoupler gate driver and the FAULT status are controlled by a combination of \( V_{IN} \), UVLO, and the detected IGBT Desat condition. During power up, the UVLO feature prevents the application of insufficient gate voltage to the IGBT, by forcing the output of the optocoupler gate driver low. Once the power supply of the optocoupler gate driver are above the positive UVLO threshold levels the DESAT detection feature is the primary source of the IGBT protection. The output of the optocoupler is safely brought low once the power supply of the optocoupler falls below the negative UVLO threshold level. A hysteresis in the Positive UVLO and negative UVLO threshold levels provides an appropriate noise margin for the UVLO detection and output shutdown feature.

Figure 1. Desaturation Detection Circuit for ACPL-332J and ACPL-331J.

Figure 2. Desaturation Detection Circuit for HCPL-316J
2. Basic DESAT detector circuit component selection

For typical application, the three external components required to build the DESAT circuit are the DESAT diode, $D_{DESAT}$, DESAT resistor, $R_{DESAT}$ and blank capacitor, $C_{BLANK}$.

**Blanking Time**

The DESAT fault detection circuitry should remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. The time period, called the DESAT blanking time ensures that there is no nuisance tripping during IGBT turn-on. This time also represents the time it takes for the driver to a fault condition. The blanking time is controlled by internal DESAT charge current, $I_{CHG}$ of 250µA (typ), the DESAT voltage threshold, $V_{DESAT}$ and the external blank capacitor, $C_{BLANK}$.

During operation, blank capacitor is discharged when driver output is low (IGBT off). That is, the DESAT detection features becomes active only when the output of the gate driver optocoupler is in the high state driving the IGBT in saturation. When the IGBT is turned on, the DESAT capacitor starts charging and protection becomes effective only if the DESAT threshold is exceeded after the blanking time.

**Blanking Time Capacitor Sizing**

Blanking time is determined using formula (1):

$$t_{BLANK} = \frac{C_{BLANK} \cdot V_{DESAT}}{I_{CHG}} \quad \text{(1)}$$

The recommended value is 100pF which gives a blank time of 2.6µs (Condition: $I_{CHG} = 250 \mu A$ and $V_{DESAT} = 6.5V$; Page 9 of HCPL-316J datasheet AV01-0579EN).

**HV Blocking Diode and DESAT Threshold**

The DESAT diode function is to conduct forward current, allowing sensing of IGBT’s $V_{CESAT}$. In high power application, DESAT pin may be pulled low due to reverse recovery spikes of the freewheeling diode. This reverse recovery spike tend to forward bias the substrate diode of HCPL-316J, which may respond by generating “false” detection signal. In order to minimize this charging current and avoid false DESAT triggering, it is best to use very fast reverse recovery time diodes with very small reverse parasitic capacitance. Listed in the table below are fast-recovery diodes that are suitable for use as a DESAT diode, $D_{DESAT}$.

The DESAT detection threshold voltage of 7V (typical) can be reduce by placing a string of DESAT diodes in series or place a low voltage zener diode in series.

For the string of DESAT diode method,

$$V_{DESAT \text{ (New Threshold )}} = 7.0 - n \cdot V_z \quad \text{(2)}$$

For the DESAT diode with Zener Diode method,

$$V_{DESAT \text{ (New Threshold )}} = 7.0 - V_F - V_z \quad \text{(3)}$$

where $n$ is the number of DESAT diodes, $V_z$ is the zener voltage value and $V_F$ is the forward voltage of DESAT diode. This allow the designer to choose the appropriate threshold voltage.

**DESAT Resistor**

The anti-parallel diode of the IGBT can have a large instantaneous forward voltage transient which exceeds the nominal forward voltage of the diode. This may result in large negative voltage spike on the DESAT pin which will draw a substantial amount of current out of the driver. To limit the current level drawn from the gate driver, a DESAT resistor can be added (100Ω recommended) in series with the DESAT diode. The added resistor will not appreciably alter the DESAT threshold or the blanking time.

**FAULT Output Pin**

The FAULT pin (Pin 3 of ACPL-332J/331J and Pin 6 of HCPL-316J) is an open collector output and requires a pull-up resistor, $R_F$ (2.1kΩ for ACPL-332J and 331J, 3.3 kΩ for HCPL-316J) to provide a high level signal. In order to prevent the FAULT pin from being “triggered” by high CMR noise, a filter capacitor, $C_F$ is included between FAULT pin and ground (Figure 1).

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Trr (ns)</th>
<th>VRRM (Volts)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ERA34-10</td>
<td>Fuji Semiconductor</td>
<td>15</td>
<td>1000</td>
<td>Axial Leaded</td>
</tr>
<tr>
<td>MUR1100E</td>
<td>Motorola</td>
<td>75</td>
<td>1000</td>
<td>59-04 (Axial leaded)</td>
</tr>
<tr>
<td>UF4007</td>
<td>General Semi.</td>
<td>75</td>
<td>1000</td>
<td>DO-204AL (Axial leaded)</td>
</tr>
<tr>
<td>BYM26E</td>
<td>Philips</td>
<td>75</td>
<td>1000</td>
<td>SOD64 (axial leaded)</td>
</tr>
<tr>
<td>BYV26E</td>
<td>Philips</td>
<td>75</td>
<td>1000</td>
<td>SOD57 (axial leaded)</td>
</tr>
<tr>
<td>BYV99</td>
<td>Philips</td>
<td>75</td>
<td>600</td>
<td>SOD87 (surface mount)</td>
</tr>
<tr>
<td>MURS160T3</td>
<td>Motorola</td>
<td>75</td>
<td>600</td>
<td>Case 403A (Surface Mt)</td>
</tr>
</tbody>
</table>
### 3. Advanced desaturation detection topic

**Internal Charging Current Source Wide Variation, I\textsubscript{CHG}**

The “blanking capacitor charge current” parameter in the data sheet (page 9 of HCPL-316J datasheet), its values are listed as:

<table>
<thead>
<tr>
<th>Blanking Capacitor Charging Current, I\textsubscript{CHG}</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>130</td>
<td>250</td>
<td>330</td>
<td>μA</td>
</tr>
</tbody>
</table>

Based on 7V desaturation voltage threshold and the above charging current, we will get three different blanking time; minimum, typical and maximum value.

\[
I_{CHG} = C \cdot \frac{\Delta V}{\Delta t} \quad (3)
\]

Using the above formula, the \(I_{CHG}, C_{BLANK} = 100\text{pF} \) (Figure 1) and \(\Delta V=7\text{V}\), we will have the following blanking time,

\[
\Delta t (\text{max}) = \frac{100 \text{ pF} \cdot 7 \text{V}}{130 \text{ A}} = 5.38 \mu\text{A}
\]

\[
\Delta t (\text{typ}) = \frac{100 \text{ pF} \cdot 7 \text{V}}{250 \text{ A}} = 2.8 \mu\text{A}
\]

\[
\Delta t (\text{min}) = \frac{100 \text{ pF} \cdot 7 \text{V}}{330 \text{ A}} = 2.12 \mu\text{A}
\]

For some application, this variation may not be a problem. However, to minimize the above variation, several externalblanking circuits are suggested in this Application Note. These are shown in figures 3, 4 and 5.

### Prevent False Fault Detection Due to Negative Voltage Spikes during Power Semiconductor Switching Operation

One of the situations that may cause the driver to generate a false fault signal is if the substrate diode of the driver is forward biased. This can happen if the reverse recovery spikes coming from the IGBT free wheeling diodes bring the DESAT pin below ground. Hence the DESAT pin voltage will be ‘brought’ above the threshold voltage. This negative going voltage spikes is typically generated by inductive loads or reverse recovery spikes of the IGBT/MOSFETs free-wheeling diodes.

In order to prevent false fault signal, it is highly recommended to connect a zener diode and schottky diode across DESAT pin and VE pin (e.g. for HCPL-316J, between pin 14 and 16). This circuit solution is shown in Figure 3. The schottky diode will prevent the substrate diode of the gate driver optocoupler from being forward biased while the zener diode (Value around 7.5 to 8V) is used to prevent any positive high transient voltage to affect the DESAT pin.

Other Methods of Tweaking DESAT detection Blanking time

Besides the recommended circuit to adjust blanking time in Figure 1 and 2, two other methods are introduced in this application note. The first method shown in Figure 3 and 4 uses additional capacitors, resistor and a FET. The second simpler method shown in Figure 5 requires only one additional resistor plus scaling of the blanking capacitor, C\textsubscript{BLANK}. The figures show how this can be connected using HCPL-316J. This circuitry is applicable with other similar drivers like ACPL-332J.

In Figure 3 and 4, the blanking time is controller by Q1 with time constant adjusted by capacitor value of 680pF and resistor 1kohm. Designers may choose to adjust this value according to their desired blanking time. The 4*RC time constant with 680pF and 1 kΩ provide for a blanking time of 2.7 µs.

Figure 5 shows another concept for an external blanking circuit. This method uses one additional external resistor RB connected from the output to the DESAT pin. This allows an additional blanking capacitor charging current component from the output of the gate driver optocoupler through RB and adds to the internal current source of the gate drive optocoupler. This higher blanking capacitor charging current allows a designer greater flexibility in choosing both an appropriate value of the blanking capacitor and an appropriate current through a choice of the external resistor RB. By adjusting the capacitance of the blanking capacitor and the additional current through RB a designer can set a specific precise blanking time, and an example calculation of the blanking time is shown below:

\[
V_C(t) = V_i - V_f \left(1 - e^{-\frac{t}{RC}}\right)
\]

**Conditions are**

\[
\begin{align*}
V_{EE} & = 9\text{V} \\
V_{CC2} & = 17\text{V} \\
R_B & = 1000\text{kohm} \\
C_{BLANK} & = 4700\text{pF} \\
\end{align*}
\]

At \(t = 0\),

\[
V_C(0) = V_i = -9\text{V}
\]

At \(t = \infty\),

\[
V_C(\infty) = V_i + V_f = -9 + 26 = 17\text{V}
\]
Hence,

\[ V_C(t) = V_i + V_f (1 - e^{-t/\tau}) \]

\[ V_C(t) = -9 + 26 (1 - e^{-t/\tau}) \]

where \( t = t_{\text{blank}} \) and \( V_c(t_{\text{blank}}) = 7 \text{V} \) (base of HCPL-316J threshold voltage)

\[ 7 = -9 + 26 (1 - e^{-t_{\text{blank}}/\tau}) \]

\[ e^{-t_{\text{blank}}/\tau} = 1 - \frac{16}{26} = 0.3846 \]

\[ -\frac{t_{\text{blank}}}{\tau} = \ln(0.3846) \]

With \( R_B = 1000 \), \( C_{\text{BLANK}} = 4700 \text{pF} \)

\[ t_{\text{BLANK}} = 4.5 \mu\text{s} \]

Figure 3. External blanking circuit with 2.5\( \mu \text{s} \) nominal blanking delay using HCPL-316J
Figure 4. External blanking circuit with external buffer for high current drive using HCPL-316J

Figure 5. Second Method of External Blanking Circuit using HCPL-316J

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