80V Half Bridge Gate Driver

General Description

The RT9622 is an 80V gate driver designed to drive both the high side and low side N-MOSFET in a half-bridge configuration or a synchronous Buck. The high side driver is capable of working with rail voltage up to 80V. The input of the driver is compatible with standard TTL logic level. The internal level shifter design enables the RT9622 to operate at high speed while providing clean transitions under high dv/dt noise circumstances. The RT9622 is available in a small SOP-8 package.

Ordering Information

RT9622 □□

Package Type
S : SOP-8

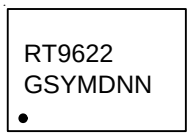
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT9622GS : Product Number
YMDNN : Date Code

Features

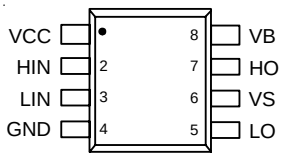
- **High Voltage Driver Up to 80V**
- **500mA Driving Current**
- **Output in Phase with Input**
- **Independent Control for High/Low Side Gates**
- **TTL Compatible Input Controls**
- **VCC and VB Operate from 10V to 20V**
- **Small SOP-8 Package**
- **RoHS Compliant and Halogen Free**

Applications

- E-Bike Drivers
- Half-Bridge and Full-Bridge Converters
- Push-Pull Converters
- Synchronous Buck Converters

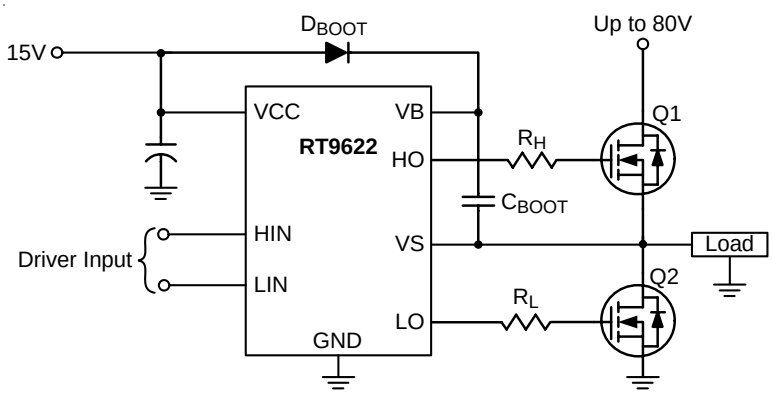
Pin Configurations

(TOP VIEW)



SOP-8

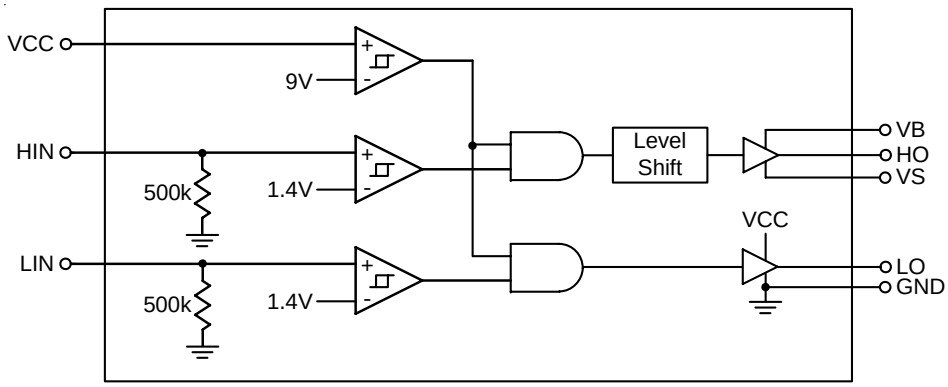
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCC	Power Supply Input. Connect a low ESR capacitor from this pin to GND for good bypass.
2	HIN	Logic Input for High Side Gate Driver. It is pulled low by an internal 500kΩ resistor if it is not connected.
3	LIN	Logic Input for Low Side Gate Driver. It is pulled low by an internal 500kΩ resistor if it is not connected.
4	GND	Ground.
5	LO	Output of Low Side Gate Driver.
6	VS	Switch Node.
7	HO	Output of High Side Gate Driver.
8	VB	Bootstrap for High Side Gate Driver. Connect a 1μF capacitor between the VB and VS pins.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 25V
- Bootstrap Voltage, VB ---------- V_{CC} to 95V
- Switch Voltage, VS ---------- (V_B – 10V) to (V_B + 0.3V)
- High Side Output, HO ---------- (V_S – 0.3V) to (V_B + 0.3V)
- Low Side Output, LO ---------- –0.3V to (V_{CC} + 0.3V)
- Inputs HIN, LIN ---------- –0.3V to 10V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.625W
- Package Thermal Resistance (Note 2)
  SOP-8, θ_{JA} ---------- 160°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode), Except HO & LO Pin ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage VCC, VBS ---------- 10V to 20V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 15V, V_{BS} = V_B – V_S = 15V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Voltage							
Supply Current		I_{VCC_H}	V_{LIN} High	--	1.8	--	mA
		I_{VCC_L}	V_{LIN} Low	--	1.8	--	
		I_{VB_H}	V_{HIN} High	--	0.2	--	
		I_{VB_L}	V_{HIN} Low	--	0.5	--	
VCC Under Voltage Lock Out Threshold		V_{UVLO_VCC}		--	8.7	--	V
VCC UVLO Hysteresis		ΔV_{UVLO_VCC}		--	0.5	--	V
VBS Under Voltage Lock Out Threshold		V_{UVLO_BS}		--	7.1	--	V
VBS UVLO Hysteresis		ΔV_{UVLO_BS}		--	0.4	--	V
Inputs and Outputs							
HIN, LIN Input Threshold Voltage	Logic-High	V_{IH}		2.8	--	--	V
	Logic-Low	V_{IL}		--	--	1.2	
HO Output Voltage	High-Level	V_{HO_H}	I_{HO} = –10mA	--	V_{VB} – 0.2	--	V
	Low-Level	V_{HO_L}	I_{HO} = 10mA	--	V_{VS} + 0.2	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current	I_{HIN}, I_{LIN}	V_{HIN}, V_{LIN} = 5V	--	50	--	μA
HO Propagation Delay	t_{ON_HO}	Low to High	--	70	--	ns
	t_{OFF_HO}	High to Low	--	95	--	
LO Propagation Delay	t_{ON_LO}	Low to High	--	90	--	ns
	t_{OFF_LO}	High to Low	--	55	--	
Turn-On Rising Time (LO to HO)	t_r	C_{LOAD} = 1nF	--	17	--	ns
Turn-Off Falling Time (HO to LO)	t_f	C_{LOAD} = 1nF	--	15	--	ns

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

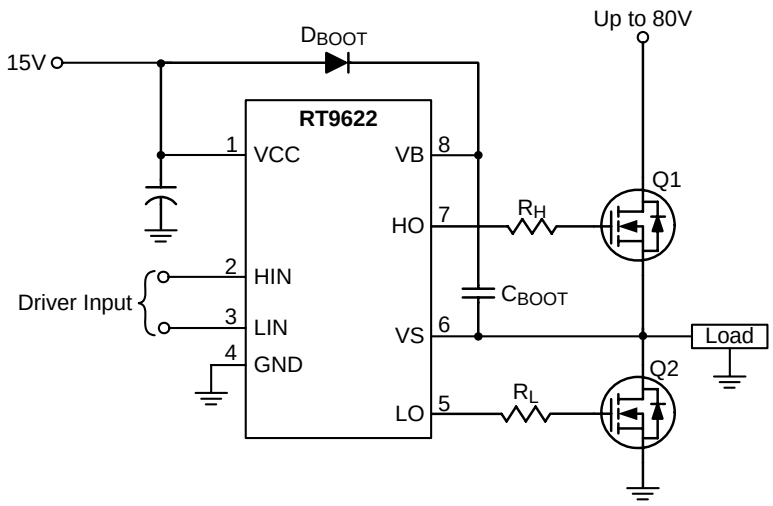
Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

To be continued

Typical Application Circuit



Timing Diagram

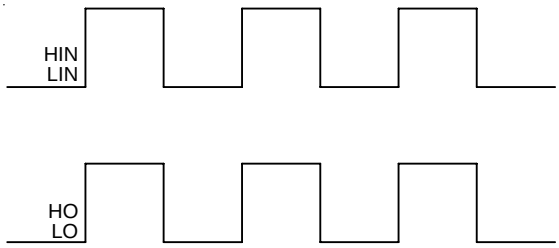


Figure 1. Input/Output Timing Diagram

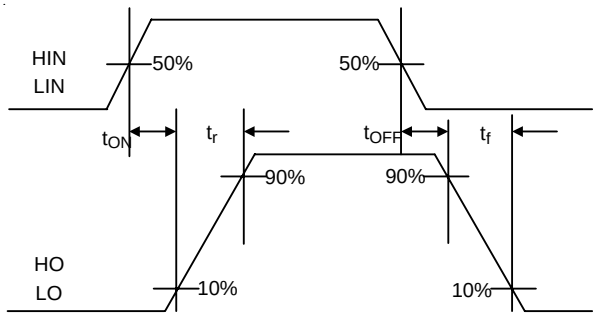


Figure 2. Switch Time Waveform Definitions

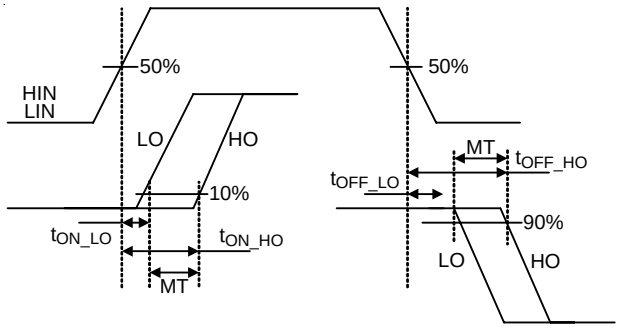
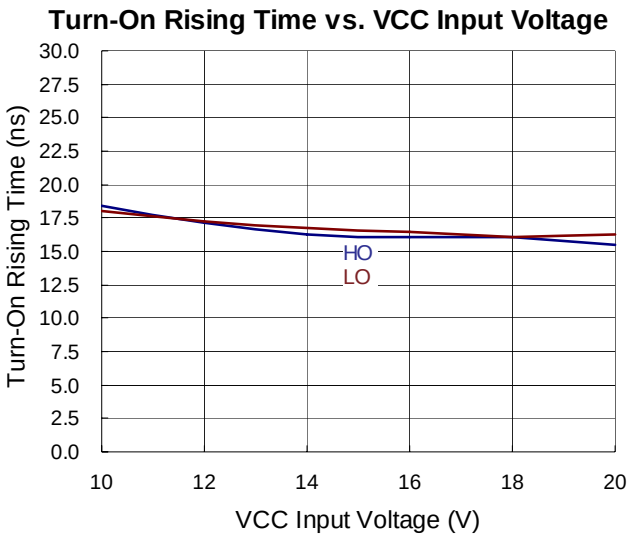
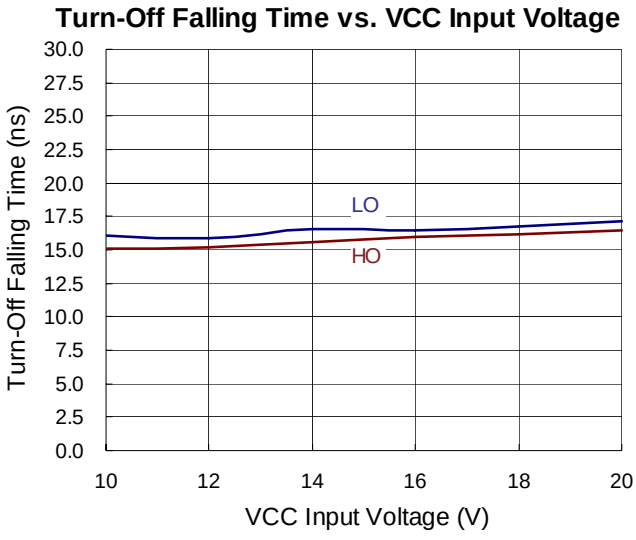
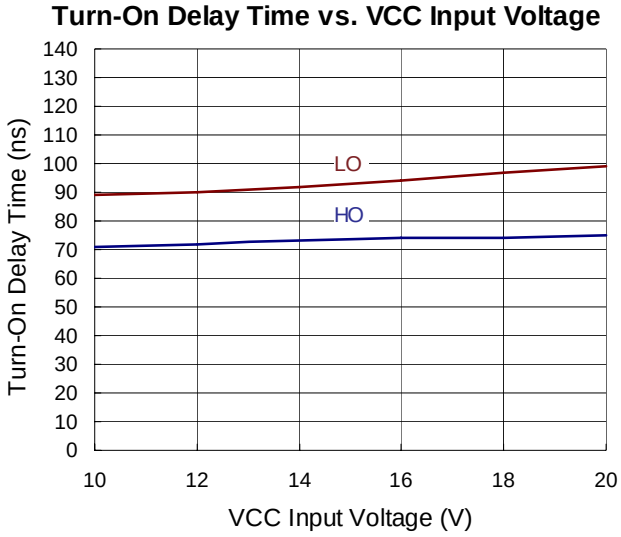


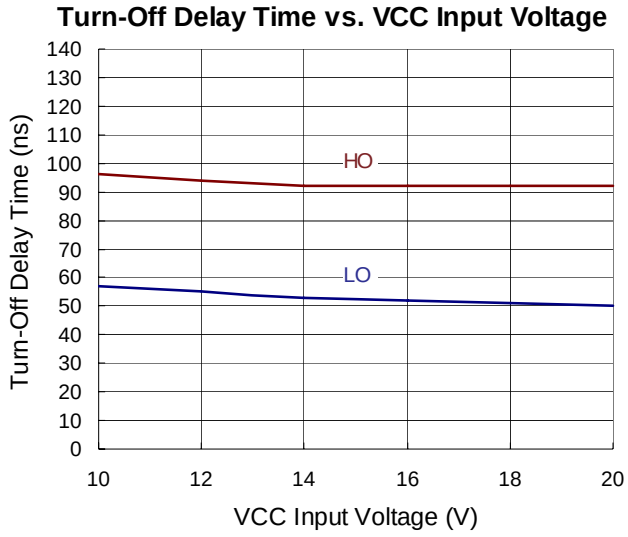
Figure 3. Delay Matching Waveform Definitions

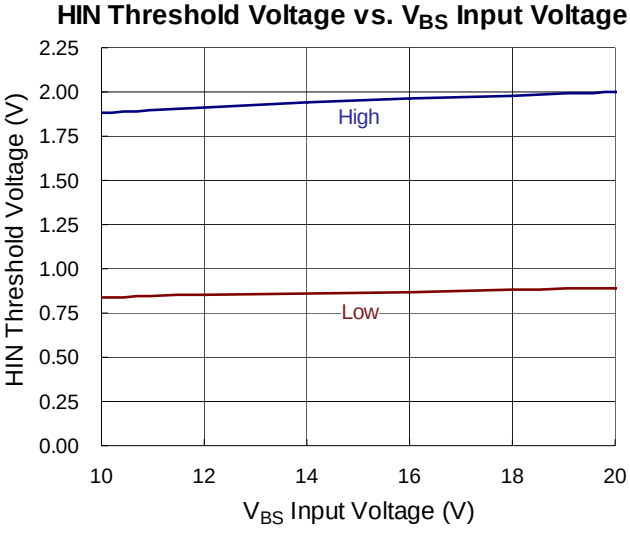
Typical Operating Characteristics

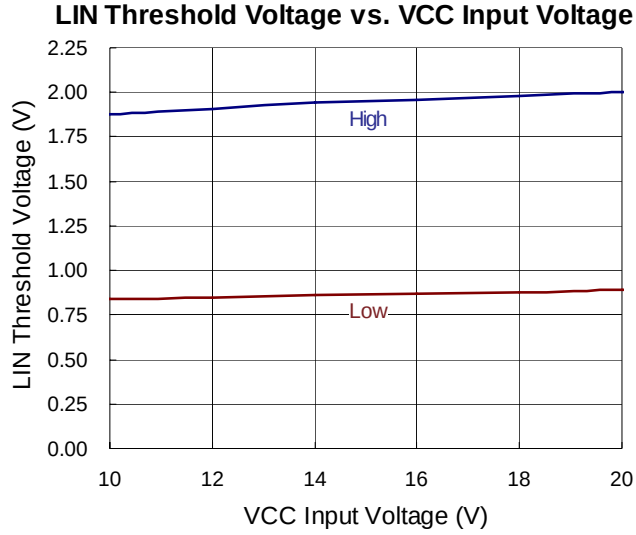




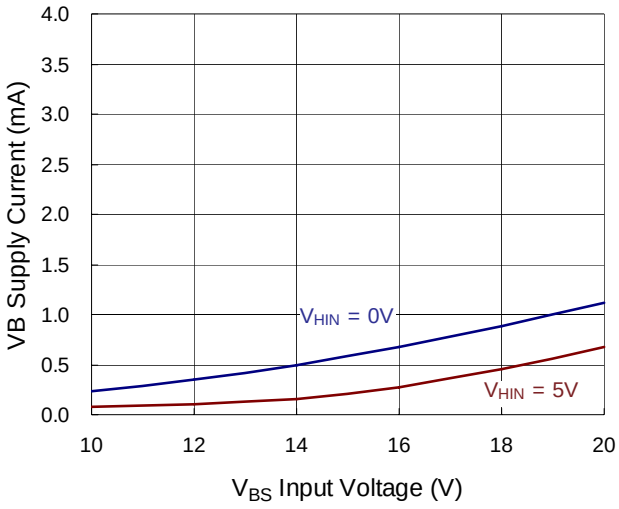




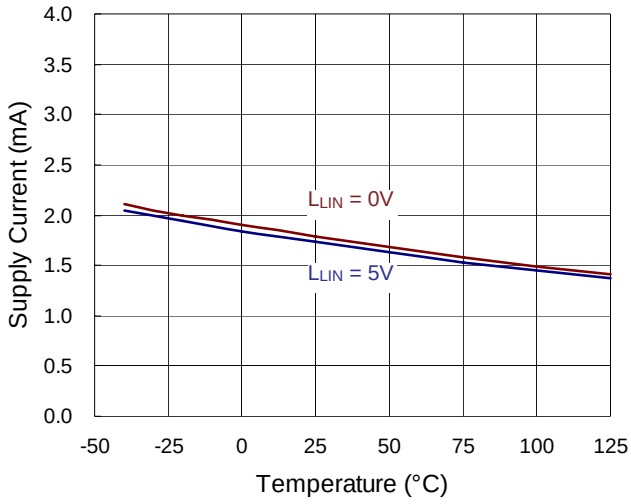




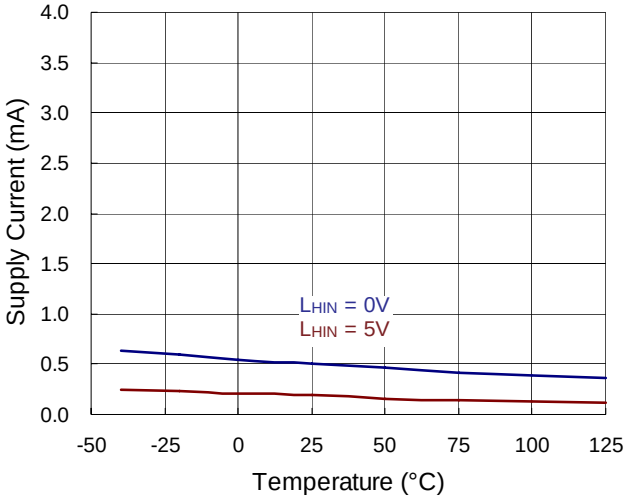
VB Supply Current vs. V_{BS} Input Voltage



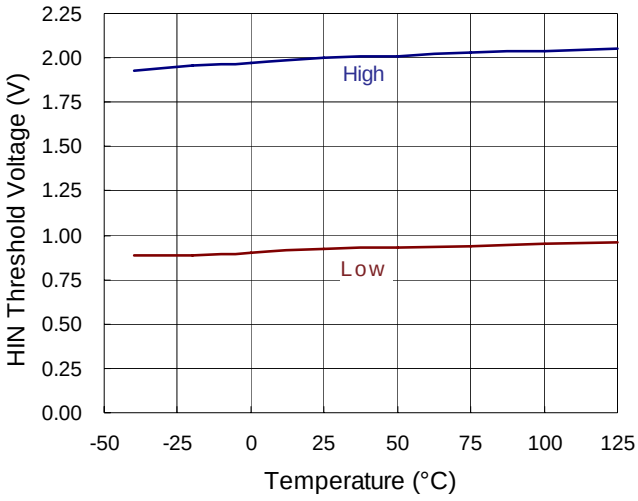
VCC Supply Current vs. Temperature



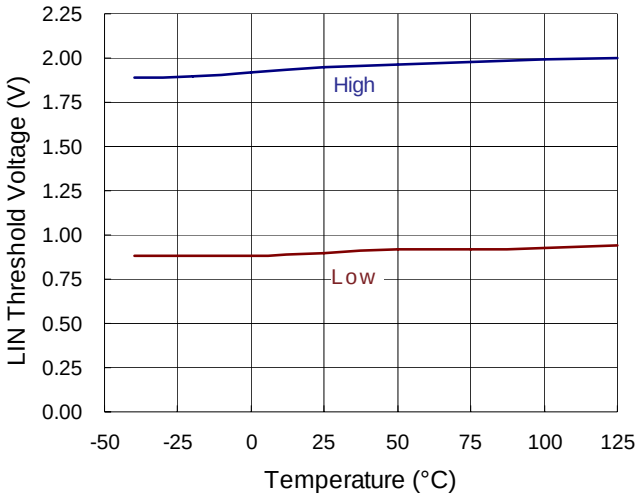
VB Supply Current vs. Temperature



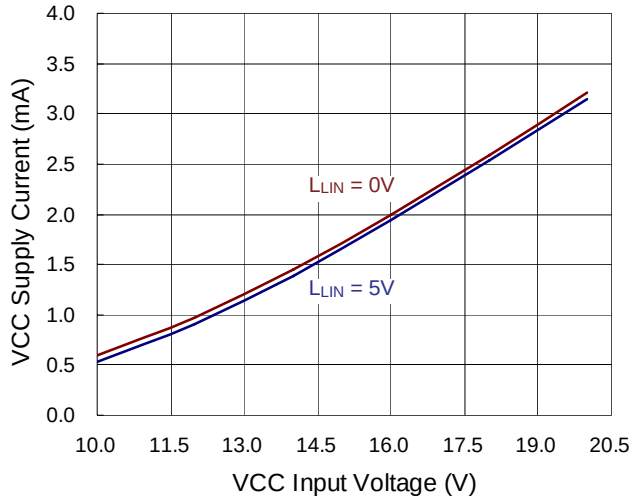
HIN Threshold Voltage vs. Temperature



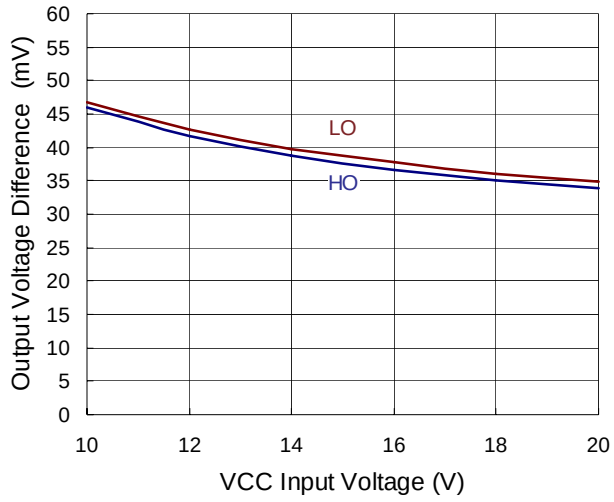
LIN Threshold Voltage vs. Temperature



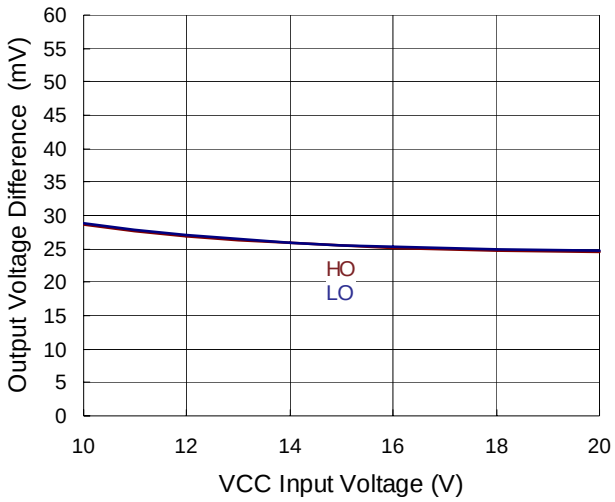
VCC Supply Current vs. VCC Input Voltage



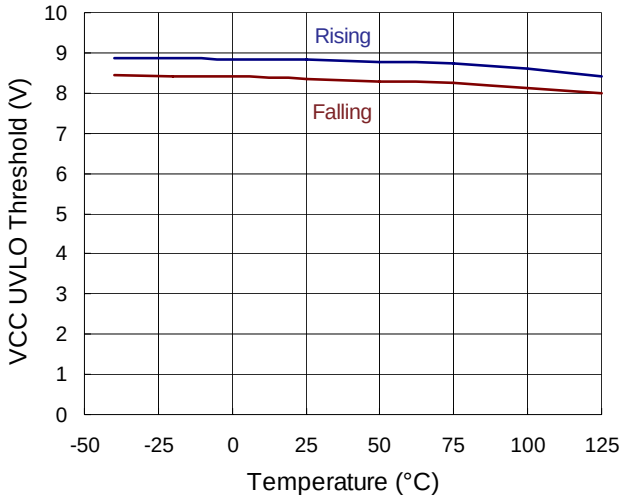
Output Voltage Difference vs. VCC Input Voltage



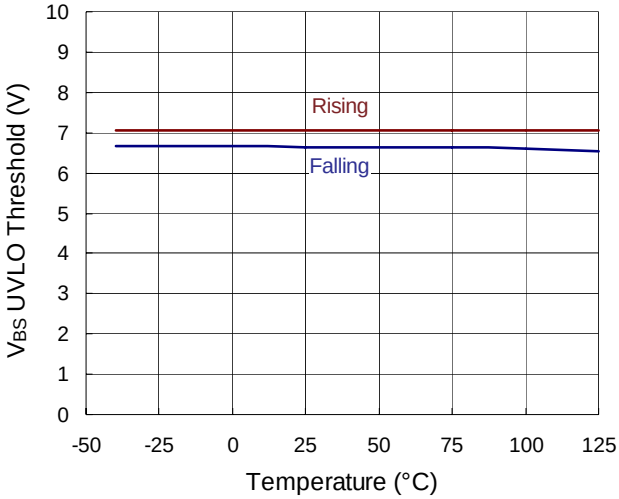
Output Voltage Difference vs. VCC Input Voltage



VCC UVLO Threshold vs. Temperature



V_{BS} UVLO Threshold vs. Temperature



Application Information

The RT9622 are designed to drive up to six MOSFET or IGBT power devices. The output that drives the gate of the external power switch is defined as HO for the high side power switch and LO for the low side power switch.

Switching and Timing Relationships

The relationship between the input and output signals of the RT9622 are illustrated in Figure 2. The definitions of several timing parameters (t_{ON}, t_{OFF}, tr, and tf) associated with this device are showed in this figure.

Dead Time and Shoot-Through Prevention

In Figure 4, the RT9622 receives the input command to turn on both the high side and low side switches at the same time; as a result, the shoot-through protection of the RT9622 has prevented this condition and both the high side and low side outputs are held at off state.

The RT9622 features integrated dead time protection circuitry. The dead time is designed to be fixed (DT). A minimum dead time will be automatically inserted whenever the external dead time is shorter than DT.

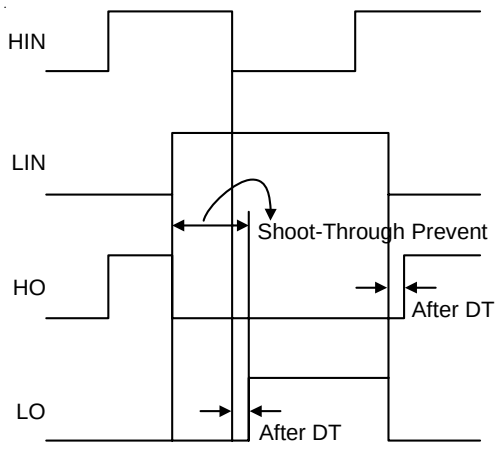


Figure 4. Shoot-Through Prevention

Under Voltage Lockout Protection

The UVLO protection ensures that the RT9622 drives the external power devices only when the gate supply voltage is sufficient to fully turn on the power devices. Without this feature, when the gate of the external power switch is driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this will result in a very high conduction loss within the power device and lead to power device failure.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 package, the thermal resistance, θ_{JA}, is 160°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (160°C/W) = 0.625W for SOP-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

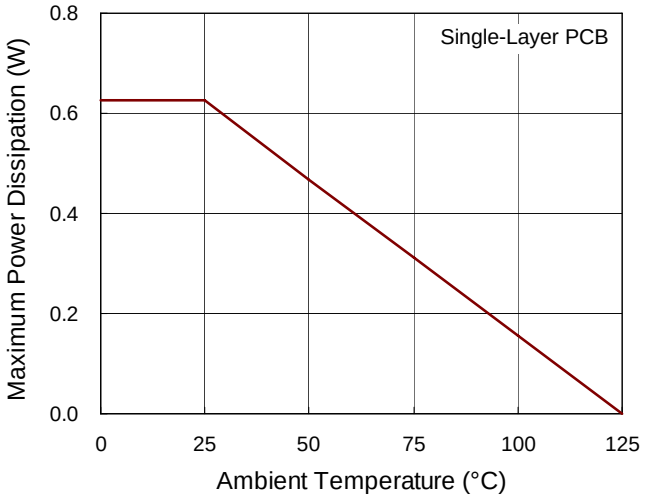


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Consideration

For best performance of the RT9622, the following layout guidelines must be strictly followed.

- VS node is with high frequency voltage swing and should be kept at small area. Keep the trace between high side MOSFET source, low side MOSFET drain and VS pin as short as possible.
- The trace from HO, LO to power MOSFET should be short to reduce the noise.
- Put the bypass capacitor C_{IN} as close as possible to the VCC pin.
- The bootstrap capacitor (C_{BOOT}) should be placed as close to the IC as possible.

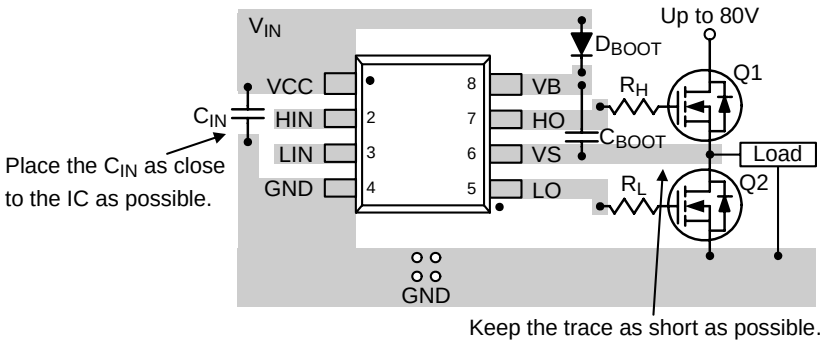
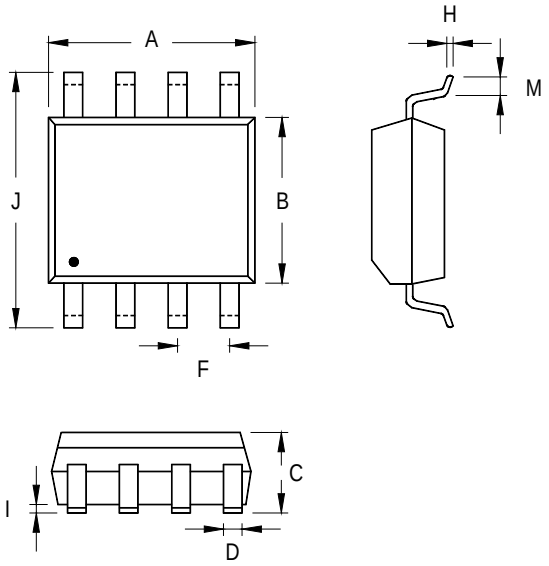


Figure 6. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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Datasheet Revision History

Version	Data	Page No.	Item	Description
P00	2010/4/6			First Edition
P01	2011/7/19		Ordering Information	Modify
P02	2012/4/24		General Description Features Applications Simplified Application Circuit Functional Pin Description Absolute Maximum Ratings Recommended Operating Conditions Electrical Characteristics Typical Operating Characteristics Application Information	Modify & New Format (some item) Add Simplified Application Circuit & Application Information