Switch Dimmable LED Driver

Features

- Four level switch dimming
- Very accurate current regulator
- Output over-current / short circuit protection
- IC over-temperature protection
- Available in 8L-SOIC and 16L-SOIC packages

Applications

- Switch dimmable LED bulbs and fixtures

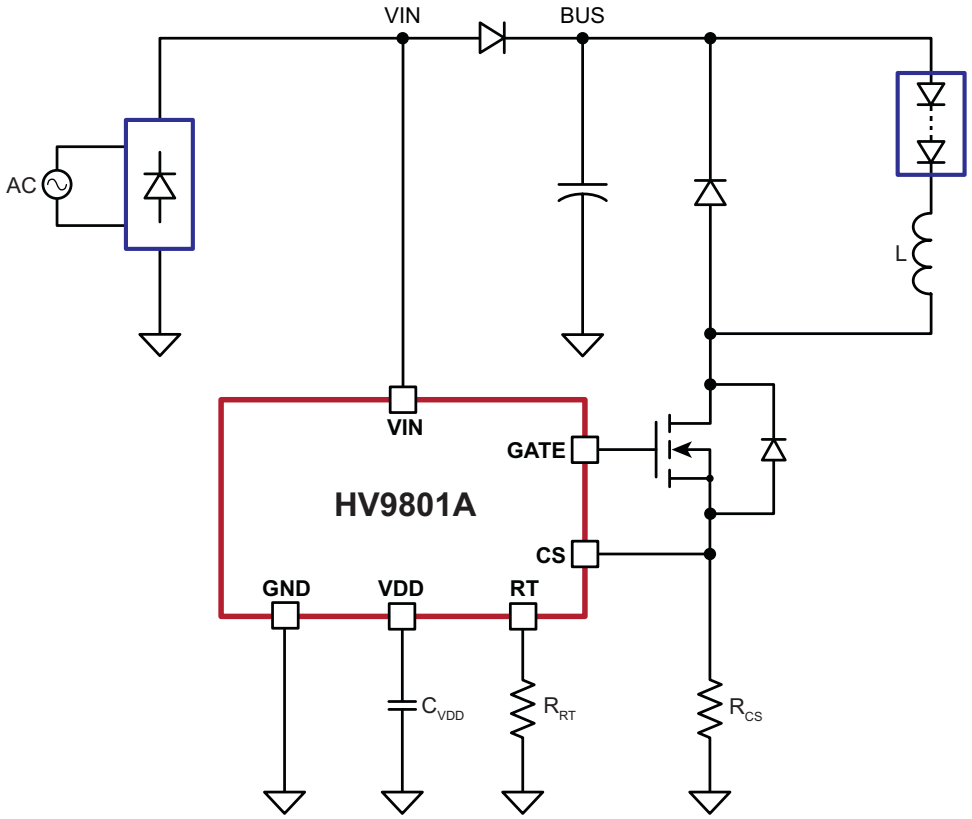
General Description

The HV9801A LED driver is ideally suited for switch dimmable applications using LED bulbs and fixtures.

Through switch dimming, the lamp can be adjusted to four discrete brightness levels by rapid cycling of the light switch. The brightness levels are traversed in up and down manner. Brightness resumes at the highest level when power is removed for more than a second.

The device can be powered directly from rectified AC through an internal VDD regulator rated at 450V.

Typical Application Circuit

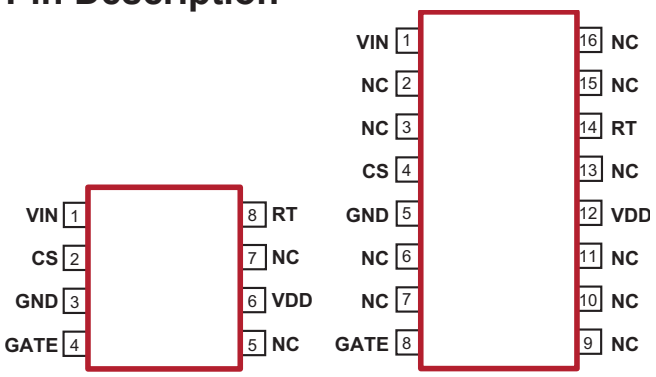


Ordering Information

Device	Package Options	
	8-Lead SOIC *4.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*	16-Lead SOIC *9.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*
HV9801A	HV9801ALG-G	HV9801ANG-G

-G indicates package is RoHS compliant ('Green')

Pin Description



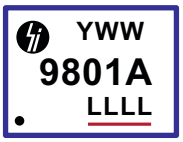
8-Lead SOIC (LG) **16-Lead SOIC (NG)**

Absolute Maximum Ratings

Parameter	Value
V_{VIN}	470V
V_{VDD}	12V
V_{CS}, V_{LD}, V_{PWMD}, V_{GATE}	-0.3V to (V_{VDD} +0.3V)
Junction temperature range	-40°C to +150°C
Storage temperature range	-65°C to +150°C
Continuous power dissipation *(T_A = +25°C)* 8-Lead SOIC 16-Lead SOIC	 650mW 1000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Product Marking

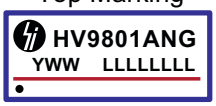


Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

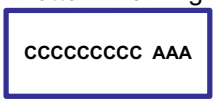
Package may or may not include the following marks: Si or

8-Lead SOIC (LG)

Top Marking



Bottom Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

16-Lead SOIC (NG)

Electrical Characteristics *(Specifications are at T_A = 25°C, V_{VIN} = 15V unless otherwise noted)*

Sym	Description		Min	Typ	Max	Unit	Conditions
Input							
V_{VIN}	Input voltage	T	15	-	450	V	---
I_{VIN}	Input current	-	-	1	2	mA	---
$I_{VIN,OT}$	Supply current, OTP shutdown	G	-	-	500	µA	---
VDD Regulator							
V_{UVLO}	Undervoltage lockout threshold	T	6.45	6.70	7.10	V	V_{VIN} rising
ΔV_{UVLO}	Undervoltage lockout hysteresis	-	-	500	-	mV	V_{VIN} falling
I_{UVLO}	Maximum input current, limited by UVLO	G	3.5	-	-	mA	T_A = 25°C
			1.5	-	-	mA	T_A = 125°C

Notes:

G Not production tested; guaranteed by design or characterization.

T Specifications apply over the full operating ambient temperature range of -40°C < T_A < +125°C.

Electrical Characteristics *(Specifications are at T_A = 25°C, V_{VIN} = 15V unless otherwise noted)*

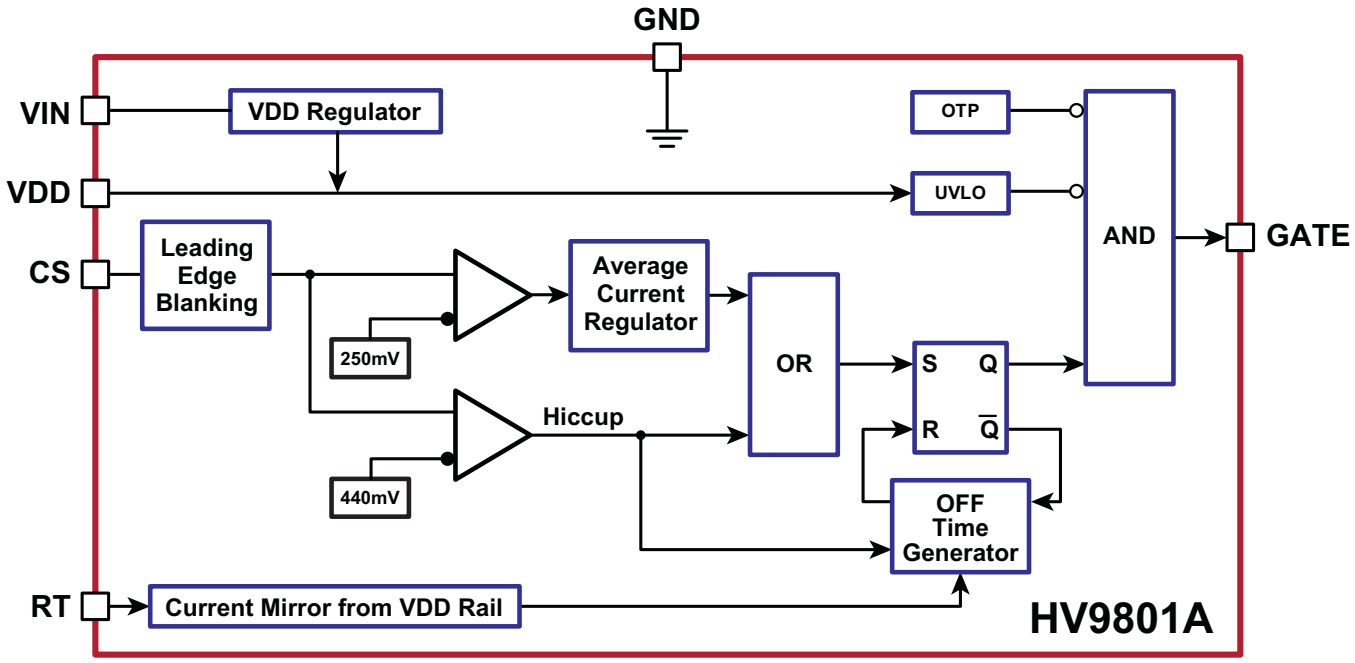
Sym	Description		Min	Typ	Max	Unit	Conditions
VDD Regulator *(cont.)*							
V_{VDD}	Output voltage	-	7.25	7.50	7.75	V	C_{GATE} = 500pF; R_{RT} = 226kΩ
ΔV_{LINE}	Line regulation	-	-	-	1	V	V_{IN} = 15 to 450V; C_{GATE} = 500pF; R_{RT} = 226kΩ
$\Delta V_{DD(UV)}$	V_{DD} Voltage margin	T	500	-	-	mV	$\Delta V_{DD(UV)} = V_{DD}$ - UVLO
ΔV_{LOAD}	Load regulation	-	-	-	100	mV	I_{VDD} = 0 to 1mA; C_{GATE} = 500pF; R_{RT} = 226kΩ
Switch Dimming							
I_{VDDX}	Supply current after power loss	T	-	-	700	µA	---
V_{UVLO}	Undervoltage lockout during VIN power loss	-	-	3.5	-	V	---
T_{PL1}	Power loss, qualification-time	-	-	7	-	ms	V_{VIN} falling below V_{UVLO}
T_{PL2}	Power loss, time to reset	G	-	1	-	s	
F_{PWM}	PWM dimming frequency	-	-	1.2	-	kHz	---
LED Current Regulator							
V_{CST}	Current sense threshold	T	236	250	256	mV	---
T_{LEB}	Leading edge blanking time	T	110	-	260	ns	---
T_{ONX}	Minimum on-time	-	-	-	760	ns	$V_{CS} = V_{CST}$ + 30mV
D_{MAX}	Maximum duty cycle maintaining regulation	-	80	-	-	%	LED current falls beyond this duty cycle
Short Circuit Protection							
V_{CSH}	Hiccup threshold	-	-	440	-	mV	---
T_{DLY}	V_{CS} high to GATE low delay	-	-	-	180	ns	$V_{CS} = V_{CST}$ + 30mV
T_{SCH}	Hiccup time	-	-	750	-	µs	---
T_{ONX}	Minimum on-time	-	-	-	430	ns	$C_S = V_{DD}$
T_{OFF} Timer							
T_{OFF}	Off-time	-	32	40	48	µs	R_{RT} = 1MΩ
		-	8.0	10	12		R_{RT} = 226kΩ
GATE Driver							
I_{SRC}	Sourcing current	-	165	-	-	mA	V_{GATE} = 0V
I_{SINK}	Sinking current	-	165	-	-	mA	$V_{GATE} = V_{DD}$
t_{RISE}	Rise time	-	-	30	50	ns	C_{GATE} = 500pF
t_{FALL}	Fall time	-	-	30	50	ns	C_{GATE} = 500pF
Over-temperature Protection							
T_{TRIP}	Trip temperature	G	-	140	-	°C	---

Notes:

G Not production tested; guaranteed by design or characterization.

T Specifications apply over the full operating ambient temperature range of -40°C < T_A < +125°C.

Functional Block Diagram



Application Information

Current Control

Continuous Conduction Mode

The HV9801A is designed for control of a buck converter operating in continuous conduction mode.

CCM operation is characterized by converter operation with non-zero inductor current throughout the switching cycle. Such operation can be achieved by selection of the inductance.

LED Current

The HV9801A regulates the LED current with an accuracy far superior to that of competing peak current mode controllers.

Average LED current is set by the current sense resistor R_{CS} and the current regulator reference voltage :

$$V = (I) \bullet (R)$$

$$250mV = (I_{LED}) \bullet (R_{RCS})$$

For example, a 2Ω resistor correponds to a 125mA (average) LED current.

Current Control Performance

The control method of the HV9801A virtually eliminates the regulation errors associated with peak current mode controllers, such as errors caused by: inductor tolerance; propagation delay of the current sense comparator; tolerance in the oscillator frequency or off-timer; and changes in line and load voltage.

Fig. 1 compares the load regulation of the HV9801A and that of a device with peak current control. The difference in load regulation between the HV9801A and the HV9910B, a peak current regulator, is clearly visible.

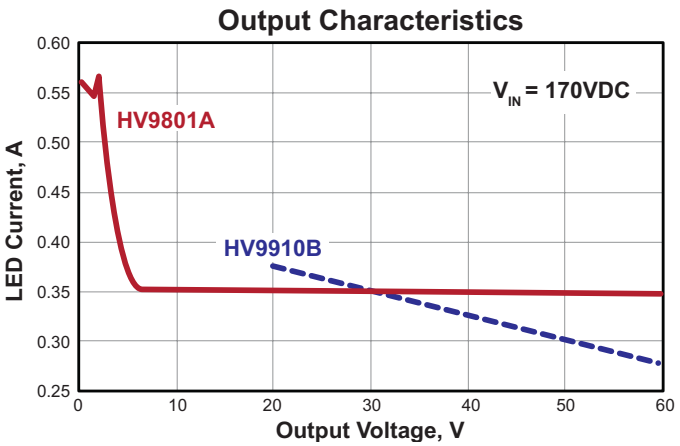


Fig.1. Typical output characteristic of the HV9801A LED driver.

Duty Cycle, Off-time, On-time, Inductor

Duty cycle

The duty cycle (D) is related to the load voltage (V_{LED}) and input voltage (V_{BUS}) by the simple relation:

$$V_{OUT} = (D) \bullet (VI_N)$$

$$V_{LED} = (D) \bullet (V_{BUS})$$

Off-time

The HV9801A employs constant off-time control. Operation with constant off-time suppresses subharmonic oscillation.

Switching period and switching frequency are related to on-time and off-time as follows:

$$T_{SW} = (T_{ON} + T_{OFF})$$

$$F_{SW} = 1 / T_{SW}$$

On-time is related to off-time and duty cycle as follows:

$$D = (T_{ON}) / (T_{ON} + T_{OFF})$$

With a given T_{OFF}, the HV9801A dynamically adjusts T_{ON} to regulate the LED current. Specifically, T_{ON} adapts to the duty cycle associated with given V_{BUS} and V_{LED}.

Switching period and switching frequency are related to on-time and off-time as follows:

$$T_{SW} = (T_{ON} + T_{OFF})$$

$$F_{SW} = 1 / T_{SW}$$

Off-time Programming

Off-time is programmed by the R_T resistor:

$$T_{OFF} = (A) \bullet (R_{RT}) + B$$

where A = 40ps / Ω and B = 300ns

For instance, a 200kΩ resistor corresponds to 8.3µs off-time.

An acceptable range for R_T is 30kΩ to 1MΩ, corresponding to an off-time range between 1.5µs and 40.3µs.

Inductor

The converter should operate in continuous conduction mode. As such, the inductor current should not fall to zero within a switching cycle, and inductor current ripple should be sized accordingly.

A common choice for peak-to-peak Inductor current ripple (PPR) is 30 to 40% of nominal LED current.

Inductance can be calculated from the current drop during off-time:

$$(L) \bullet (\Delta I) = (V) \bullet (\Delta T)$$

$$(L) \bullet (PPR) \bullet (I_{LED}) = (V_{LED}) \bullet (T_{OFF})$$

For instance, 30% PPR on 350mA average current equates to 105mA ripple, which together with 5µs off-time, and 30V LED string voltage corresponds to 143µH inductance.

A design with 30V LED voltage and with 150V bus voltage corresponds to 20% duty cycle; respectively, with a 120V bus voltage to 25% duty cycle. 20% duty cycle corresponds to 1.25µs on-time, 25% duty cycle corresponds to 1.67µs. Hence, the switching frequency is 167kHz at 150V bus voltage and 150kHz at 120V bus voltage.

Maximum Duty Cycle

Duty cycle should be limited to the specified maximum (80%). Accordingly, the LED string voltage and the bus voltage are limited to the same ratio. Operation at a larger duty cycle results in an LED current lower than programmed.

Minimum Duty Cycle

Duty cycle is limited on the low side by the minimum on-time specification (760ns). Operation at a smaller on-time causes the LED current to exceed the programmed value.

LED string voltage can not be made arbitrarily low. Minimum LED voltage can be determined from the following:

$$D_{MIN} = (T_{ONX}) / (T_{OFF} + T_{ONX})$$

$$V_{LED} = (D_{MIN}) \bullet (V_{BUS})$$

For instance, with 5µs off-time, the duty cycle should be kept above 13%. Such a duty cycle corresponds to an LED string voltage of 19.5V at 150V bus voltage.

A design requiring a lower LED string voltage requires change to a longer off-time.

Short Circuit Protection

A rise of the LED current sense signal above 440mV (176% of nominal) trips the short circuit comparator thereby causing the converter to switch to hiccup mode. In hiccup mode, off-time is lengthened to about 750µs to allow the inductor current to drop to a safe level.

Without the extended off-time the inductor current increases with every switching cycle, thereby causing over-current damage to the converter.

The extension of the off-time can be observed in Fig.2:

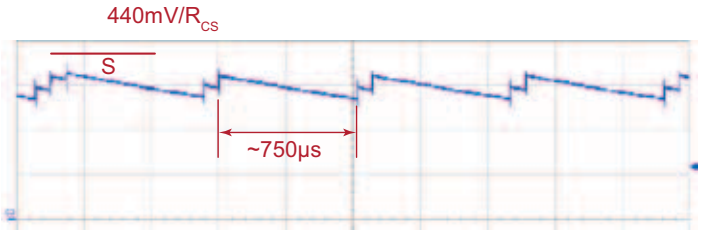


Fig.2. Short-circuit inductor current.

Leading Edge Blanking

The MOSFET drain current, and thereby the current sense signal, exhibits a spike at the start of a switching cycle which arises from the MOSFET gate charging current and the current required for discharge of the MOSFET drain node. These two currents typically exceed the inductor by quite a margin.

The current sense signal is blanked at the start of the switching cycle in order to avoid a premature trigger of the current sense and the short circuit protection comparators.

V_{DD} Regulator

The V_{DD} regulator generates a source of regulated voltage for operation of internal and external circuits from the power applied at the VIN pin. Alternatively, the V_{DD} voltage can be supplied from a source directly connected to the VDD pin. The V_{DD} regulator will turn off.

Switch Dimming

General

Lamp brightness can be adjusted to one of four discrete levels by rapidly cycling power with the light switch. The brightness levels are traversed in an up and down manner, the levels being 100%, 50%, 25% and 12.5%. Brightness resumes at the highest level when power is removed for more than a second.

Reduction of LED current is accomplished through PWM dimming with a PWM dimming frequency of about 1kHz. The PWM frequency is generated by an internal oscillator and the duty cycle by means of digital logic.

Turning the light switch off and on within one second adjusts LED current to the next higher or lower level, see the illustration below. The sequence starts at 100% and adjusts to a lower level with the following step. Upon reaching the highest or lowest level the direction of the sequence reverses. When power is removed for more than one second, the dimming sequence is terminated and brightness is reset to 100% upon turn-on of the light switch.

V_{DD} capacitor

The V_{DD} voltage should be maintained for at least one second and above the 3.5V level after loss of V_{IN} power to allow certain timing circuits to function.

The minimum required capacitance can be calculated from:

$$(C) \bullet (\Delta V) = (I) \bullet (\Delta T)$$

$$(C_{VDD}) \bullet (7.5 - 3.5V) = (I_{VDDX}) \bullet (1s)$$

With 700µA of I_{VDDX} the bypass capacitance should be 175µF.

Detection of Power Cycling

The presence of AC line power is detected at the VIN pin. To this end, loss of AC power should result in a rapidly falling voltage at the output of the bridge rectifier.

The V_{VIN} voltage drops due to the current draw from the V_{DD} regulator. In order to facilitate a quick fall of the voltage, a diode should be added to isolate the bus capacitor from the VIN pin as shown in the Typical Application Circuit.

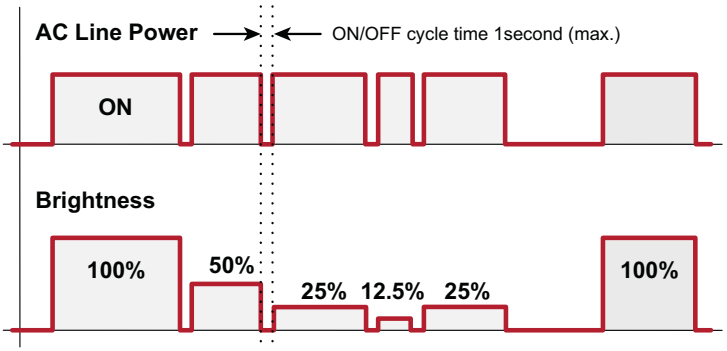


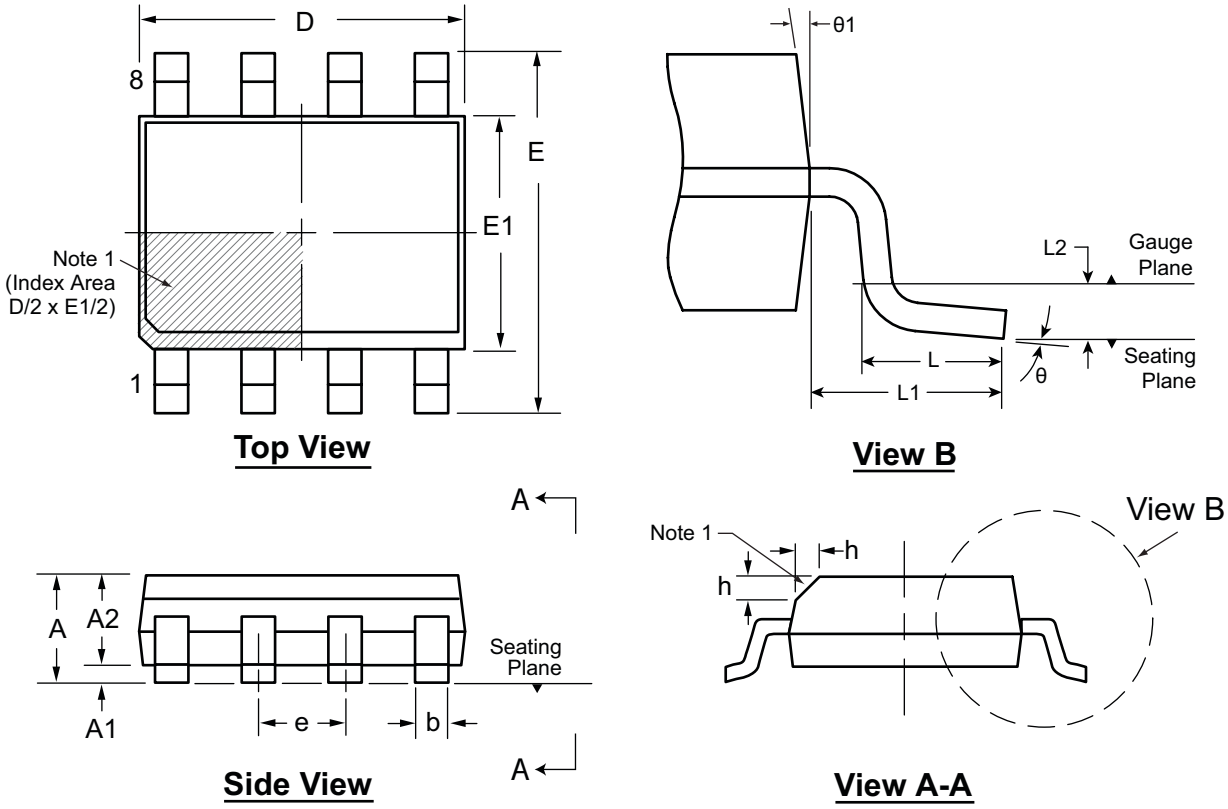
Fig.3. LED brightness and AC line power.

Pin Description

Pin #		Function	Description
8-Lead SOIC	16-Lead SOIC		
1	1	VIN	Connect to bridge rectifier output. Supplies power to the VDD regulator. Detects light switch power-off event through loss of bridge rectifier output voltage. Do not connect excessive capacitance before or after the bridge so as to allow V_{IN} to drop rapidly after loss of power.
2	4	CS	Current sense input.
3	5	GND	Ground.
4	8	GATE	Gate driver output.
6	12	VDD	VDD regulator output. Connect a high frequency bypass and a hold-up capacitor at VDD. Bypass capacitor to be 100nF minimum. See applications section for hold-up capacitance.
8	14	RT	Off-time programming input. Connect programming resistor to GND.
5, 7	2, 3, 6, 7, 9, 10, 11, 13, 15, 16	NC	No connection

8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

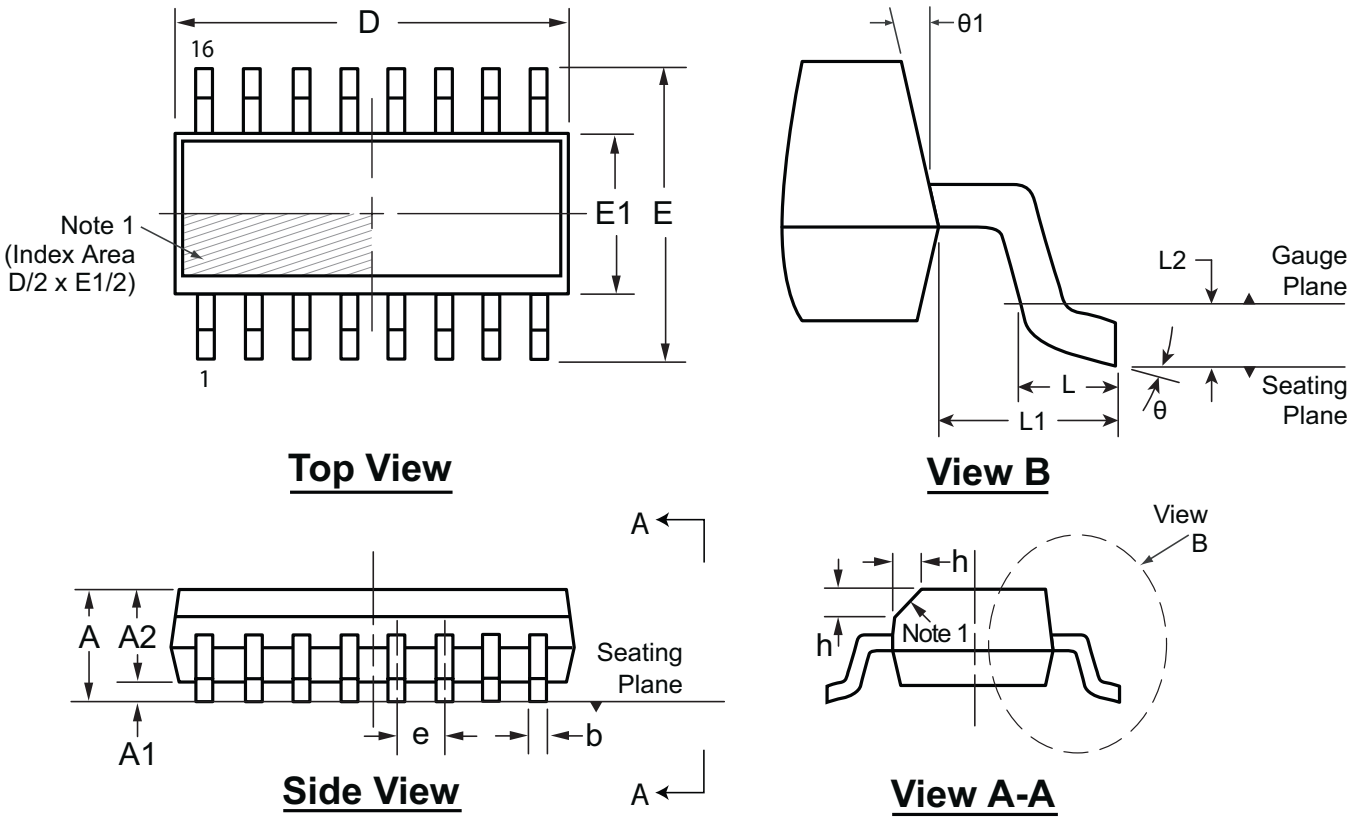
1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0^O	5^O
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8^O	15^O

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-8SOLGTG, Version I041309.*

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-16SONG, Version G041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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