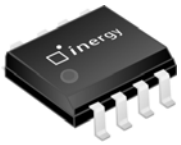


TRANSITION-MODE SINGLE STAGE PFC LED POWER SUPPLY

1. Description

The iP7302B operates on fly-back circuit after rectifier diode, so the waveform of input current follows that of input voltage. It is a peak current mode fly-back PFC controller, with valley turn-on /Quasi Resonant mode (QR), so very high efficiency is easily achieved.

FB pin is connected to positive input and pull up 50KΩ resistor to internal supply of 5V. The negative input is connected to output to form unity gain buffer. This is specially made to suit single stage LED power supply which requires PFC.

The structure of single stage LED power supply with PFC offers several advantages: high PF, no need of bulk electrolytic capacitor, output isolates from line input, reasonable size and cost. The disadvantage is that the output contains 120/100Hz ripple. But with iP7700, the average current may be controlled very well.

With gate drive output clamp at 18V, the iP7302B has a wide VDD operation range. The turn-on delay of soft-drive facilitates valley voltage switching, and the soft drive itself minimizes turn-on current spike. Thus higher efficiency could be achieved.

The iP7302B is packaged with small size SOP-8L, and it is easy to use with few external components. It is also equipped with under voltage lock out (UVLO) with very small start-up current.

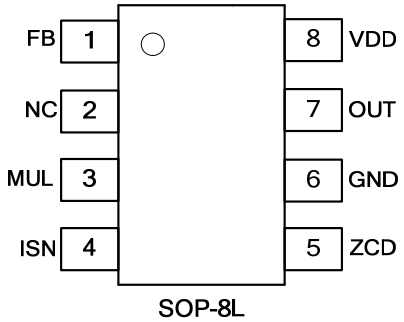
2. Features

- Wide VDD operation range with OVP latch at 22V
- Gate drive output voltage clamp at 18V
- UVLO with low standby current
- Soft drive for minimizing turn-on current spike
- Zero current with valley voltage switching
- Low operating current
- Over voltage protection
- Output short circuit protection
- Over load protection and feedback open protection
- Over temperature protection
- High/Low line compensation
- SOP-8L packaging with few external components needed
- High power factor with low THD

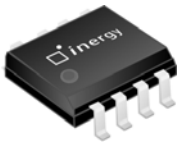
3. Applications

- LED lighting

4. Pin Assignments



SOP-8L



5. Marking Information

Product Name	Marking
iP7302B	iP7302B XXXXX X : Date Code

6. Ordering Code

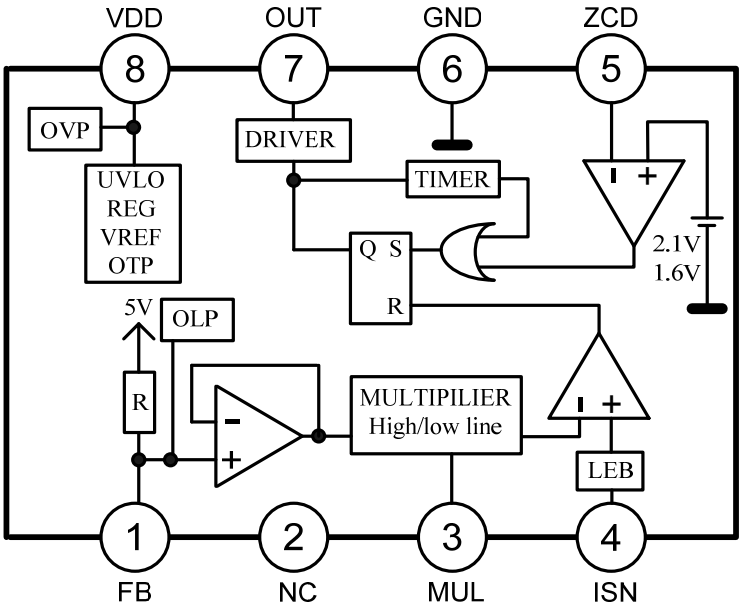
iP7302B □ └— Assembly Material	Assembly Material G: Halogen and Lead Free Device

Note: inergy defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight ; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

7. Pin Definitions

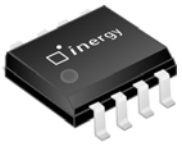
Pin	Name	Description
1	FB	Non inverting input of the buffer. A 50KΩ resistor is connected between this pin and internal 5V.
2	NC	No connected.
3	MUL	Input of the multiplier stage. A resistive divider is connected between the rectified mains and this pin, to provide the sinusoidal reference to the multiplier.
4	ISN	Input of the PWM comparator. The current flowing in the MOSFET is sensed by a resistor and the resulting voltage is applied to this pin.
5	ZCD	Flyback inductor’s demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET’s turn on.
6	GND	Ground.
7	OUT	Gate driver output.
8	VDD	Supply voltage of driver and control circuits.

8. Block Diagram



9. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	VDD	30	V
Maximum voltage on FB, ISN, MUL	V	- 0.3 ~ 7	V
Maximum voltage on ZCD	V	VDD + 0.3 ~ VDD - 50	V
Thermal resistance, Junction-to-Ambient	R_{thJA}	250	ºC/W
Junction temperature operating range	T_{OP}	- 40 ~125	ºC
Storage temperature	T_{STG}	- 60 ~150	ºC
ESD capability, HBM model	V	2.0	kV
ESD capability, MM model	V	200	V



10. Electrical Characteristics

(VDD = 15V, for typical values T_J = 25 ºC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE SECTION						
Operating Range	VDD	After turn-on	11	-	20	V
Turn-on Threshold	VDD on		12.5	14	15.5	V
Turn-off Threshold	VDD off		7.5	9	10.5	V
On/Off Hysteresis	Hys		4.15	5	5.85	V
Over Voltage	V_{OV}	Latch	20	22	24	V
SUPPLY CURRENT SECTION						
Start-up Current	IDD_{st}	before turn-on (VDD = 12V)	-	70	-	uA
Quiescent Current	Iq		-	1	-	mA
Operating Current	IDD_{op}	PWM loaded, f = 60kHz, C = 1nF	-	1.3	-	mA
Over Load Delay Time	T_{od}			160		mS
FEEDBACK SECTION						
Internal Pull Up Resistor	R_{FB}		-	50	-	kΩ
Open Circuit Voltage	V_{FB}		-	5.5	-	V
Overload On	V_{OL}		4.7	4.8	4.9	V
MULTIPLIER SECTION						
Input Bias Current	I_{MUL}		-	-	1	uA
Linear Operation Voltage	V_{MUL}		0 to 4	-	0 to 4.5	V
Gain	K	V_{MUL} = 1V V_{FB} = 3V	0.37	0.43	0.49	1/V
High/Low Line Threshold Volatage	V_g	Positive slop		4		V
High/Low Line Threshold Volatage Hysteresis	V_{gH}			0.4		V
ZERO CURRENT DETECTOR						
Input Bias Current	I_{ZCD}		-	-	1	uA
Zero Current Detect	V_{ZCD}	Negative slope	-	1.6	-	V
Zero Current Detect Hysteresis	V_H		-	0.5	-	V
Delay To Turn On	t_{ZCD}		-	350	-	ns
Input Capacitance	C_{par}	V_{ZCD} = 1.0V	-	10	-	pF
Maximum Off Time	t_{OFFMax}		75	150	300	us
Minimum Off Time	t_{OFFMin}		2	4	6	us
CURRENT SENSE COMPARATOR						
Input Bias Current	I_{CS}		-	-	1	uA
Delay To Turn Off	t_{delay}		-	300	450	ns
LEB	t_{LEB}		-	300	-	ns
Current Sense Limit	V_{limit}	V_{COMP} = Upper Clamp	1.7	1.85	2	V

OUTPUT SECTION						
Output Clamp	Vo_clamp		-	18	-	V
Dropout Voltage	V_{GD}	IGDsource = 200mA	-	3.3	-	V
		IGDsource = 20mA	-	1.4	-	V
		IGDsink = 150mA	-	1.8	-	V
		IGDsink = 20mA	-	0.2	-	V
PROTECTION SECTION						
Over Temperature on	T_{OT}		-	120	-	℃

11. Typical Characteristics

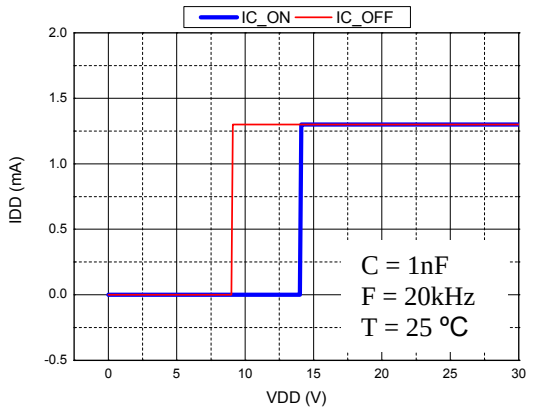


Figure 1. Supply Current vs. Supply Voltage

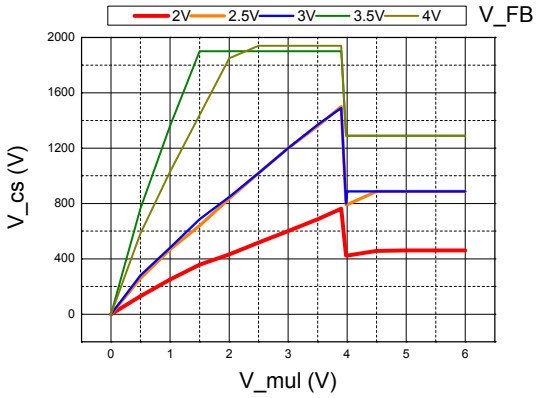


Figure 2. Multiplier Characteristics Family

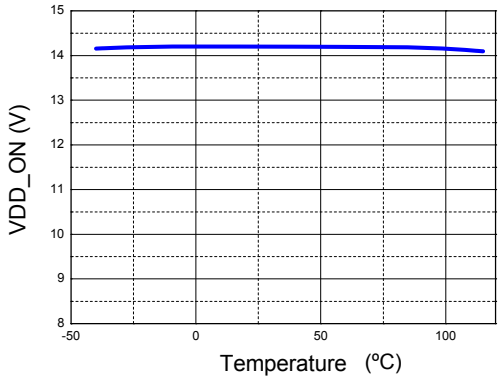


Figure 3. VDD_ON Voltage vs. Ambient Temperature

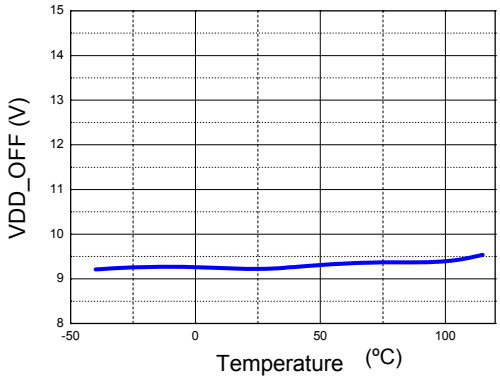
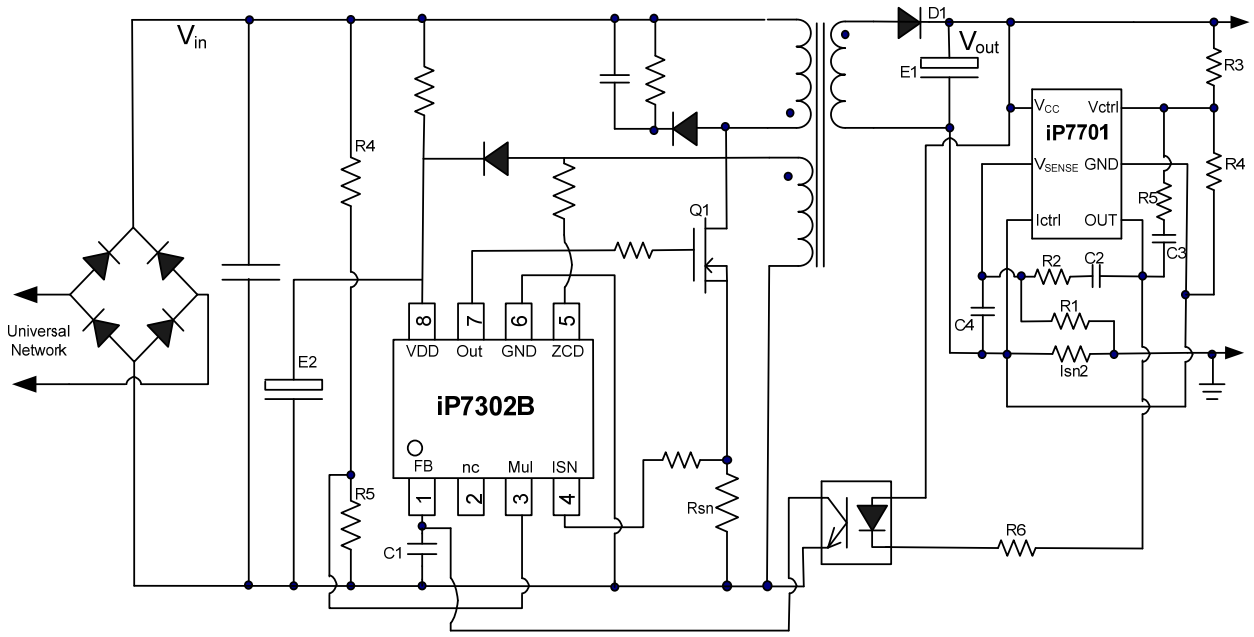


Figure 4. VDD_OFF Voltage vs. Ambient Temperature

12. Functional description and application circuit

12.1 Typical application circuit



12.2 Functional description

a. Power supply

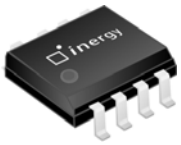
Power is supplied between VDD and GND pin. At VDD below UVLO off, IC is in Under Voltage Lock Out (UVLO) state, It does not operate and consumes very low current. As voltage increases above UVLO on, the IC starts to operate with 1mA power consumption. During this time IC power is provided by E2 capacitor, so voltage decreases, and before the voltage drops below UVLO off, auxiliary power should provides power for the IC continues to operate. However, if the voltage drops below UVLO off, it enters UVLO state.

b. PWM

During operation, if the iP7302B is off for more than t_{OFF}, an internal timer triggers the output on. It might happen at very beginning. The output drives the external MOSFET(Q1)on, so the current pass through primary winding of flyback transformer and Q1 increases with di/dt = Vin/L. The voltage across secondary winding of inductor is negative, and output diode is non-conducting.

The primary current is sensed through ISN pin by detecting voltage across a sense resistor. If it exceeds target values, output is turned off. As the current through transformer must be continuous, so it flows through flyback diode (D1) to output capacitor(E1). Voltage of E1 is always higher than zero, so the current is decreasing with di/dt = -Vout/L. The positive voltage across auxiliary winding of transformer is sensed by ZCD pin.

Re-turn on is initiated by two mechanisms: maximum off time and zero current detect(ZCD). As the current decreases to zero, the diode is off, and the drain voltage of Q1 is oscillating about Vin. As it swings through Vin, the auxiliary winding voltage swings through zero. When it swings down across 1.9V



ZCD trigger the output on. The process is repeated as PWM switching. Since iP7302B has soft drive function, its delay facilitate the valley voltage turn on to minimized turn on switching loss.

c. Current shaping

For QR mode, when Q1 is on, current always starts from zero, and Q1 is off when current reaches a target value that follow the input voltage. As Q1 is turn off, the current is diverted through D1 to output capacitor, and it is decreasing. The input current looks as triangle, and its peak follows input voltage. Therefore, if the current ripple at switching frequency is filtered (using C2), the average input current, which is half of its peak, would look as the input sinusoidal voltage. High power factor and low total Harmonics Distortion (THD) may be achieved.

d. Feedback output control

For LED power applications, current controls is the primary concerned, and voltage is controlled when output is open to prevent over voltage. The iP7700 serves for this purpose. It consists of two sets of voltage reference and error amplifier. First is 0.2 V, for current controls, and 2nd is 1.21V for voltage controls

Output current is sensed on the voltage difference between Rsn2. R1 is the input resistor of current controller. R2 and C2 is its PI (proportional integral) compensator.

Output voltage is sensed through R3, R4 voltage divider. Its effective resistance acts as input resistor of voltage controller. R5 and C3 is its PI (proportional integral) compensator.

The outputs of current and voltage controller are open drain, so they may be connected together as “OR” logic, which ever reaches will controls.

This output signal pulls current through R6 and photo-diode of photo-coupler, and proportional current passes through the transistor of photo-coupler, which would pull the FB pin down. The close loop would reach an (quasi) equilibrium, in which output current or voltage is near to the set point.

For LED application, the voltage’s set point is set possibly high, and current is set at the operation current of LED, so current is controlled. The respond of voltage control should be fast to avoid over voltage, however the time constant of current control should be properly adjusted for low input current distortion and high slew rate output current.

FB pin is internally pull up with 50K. This resistor, R6 and C1 constitute a filter, which should filter 100 or 120 Hz, twice the line frequency, so the voltage at FB pin is quasi DC, other wise the target current will be distorted.

e. Multiplication

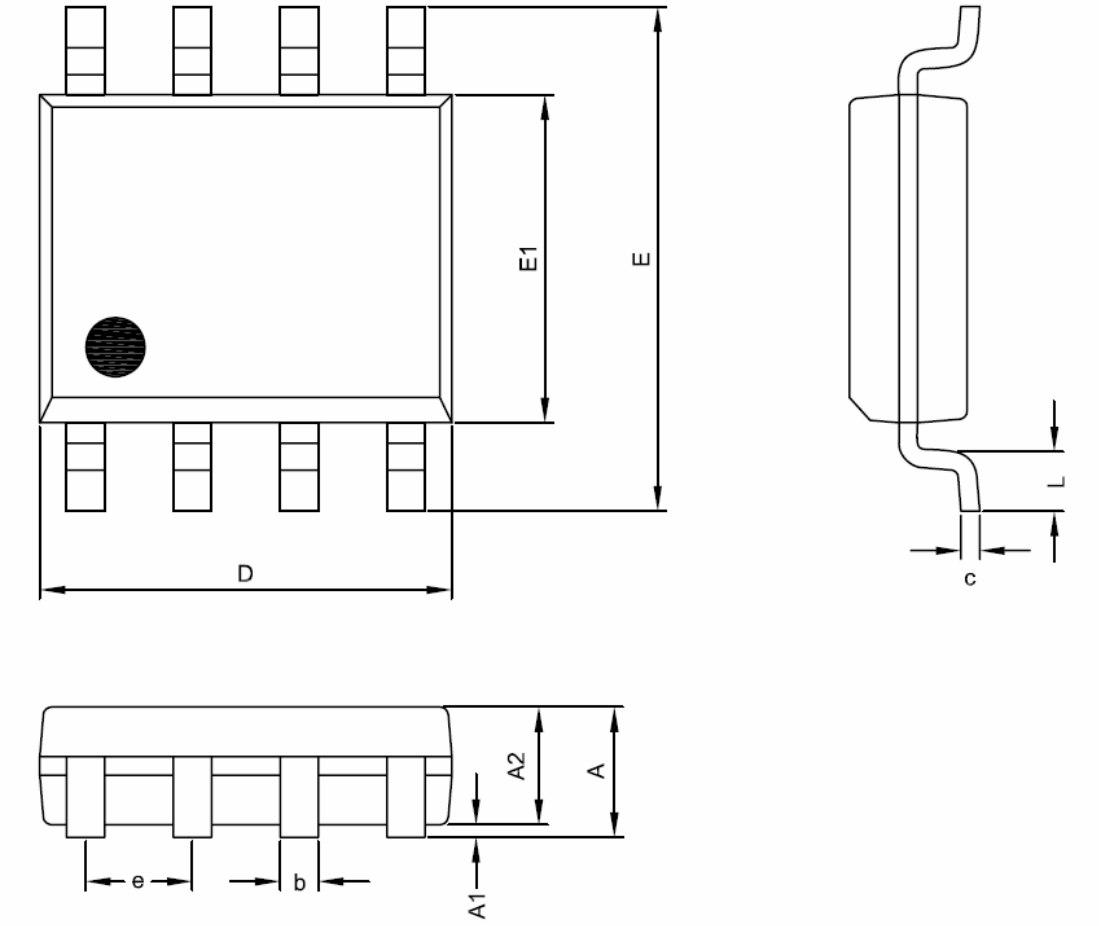
Mul pin is monitored with two 4.0/3.6V and 1.1V/0.9V hysteresis comparators. If Mul pin above 4.0 V is detected, “high-line” register is set and a 2-bit counter is reset (00). When high-line register is 1, This voltage reference is 3.6V and the ISN voltage reference with its limit are scaled by 0.7 (0 - 1.7 V → 0 - 1.2 V) . The 2-bit counter is incremented using output of 1.1V/0.7V comparator. High-line register is reset when this counter is overflow (11).

f. Protection

1. The internal 18V zener VDD clamp is removed. VDD pin is sensed, if it exceed 22V, Over voltage protect (OVP) is triggered, which consumes very low current, and it is reset when VDD voltage below 6V.
2. To avoid misfire or switching frequency too high, minimum off time of 4us is added. The output will not turn on even the ZCD turn on signal is detected, unless after 4us.
3. Over temperature protect is included, 120℃
4. UVLO on/off is 14/9V
5. If FB pin hits top more than 160ms, the output is off - Over Load Protect (OLP) and latched. It consumes about operation current. And OLP is reset at 2nd UVLO

13. Package Dimensions

SOP- 8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：

1. Jedec outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.