SSC9522S
Application Note Rev.0.3

The contents in this application note are preliminary, and are subject to changes without notice.

Taiwan Sanken Electric Co., Ltd.

http://www.sanken-ele.co.jp

Contents

1. General Descriptions

The SSC9522S is a controller IC (SMZ method) for half-bridge resonant type power supply, incorporating a floating drive circuit for High-side MOSFET drive.

※SMZ = Soft-switched Multi-resonant Zero Current switch

All switching periods work with soft switching operation.

The IC is in SOP18 package, and suitable for high performance power supply system with small size, high efficiency and low noise, because for various power supply specifications, more effective and easier design works are achievable with effective functions as the Automatic Dead Time Adjustment, the Uncontrollable Operation Detection and so on.

※Uncontrollable Operation Detection = there are two areas in resonant circuit impedance; capacitance area and inductance area. The Uncontrollable Operation occurs in capacitance area (the frequency is lower than the resonant frequency, f_O), the output voltage can not be controlled and the switching operation becomes hard switching.

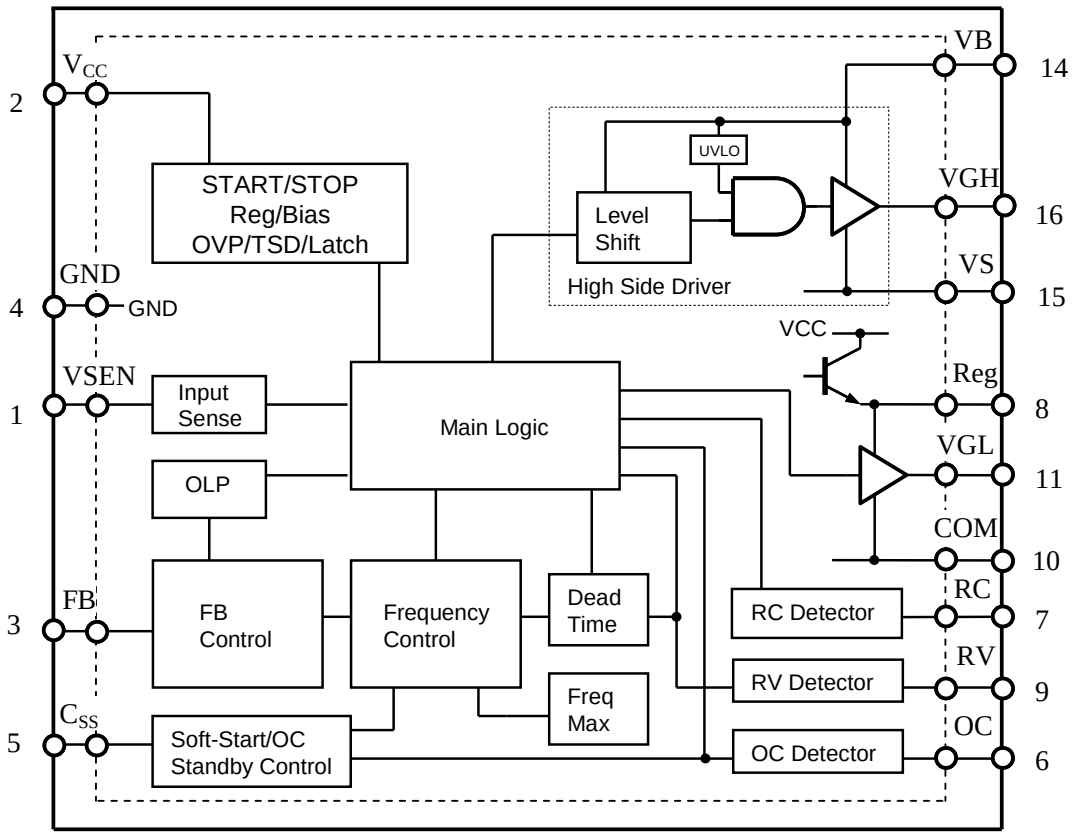
2. Features

Features and benefits include the followings:

- SOP18 package
- Built-in floating drive circuit for High-side MOSFET
- Soft Start Function, reducing of power MOSFET stress and preventing Uncontrollable Operation, at startup
- Uncontrollable Operation Detection Function on pulse-by-pulse basis, improving the ability of transformer output wattage because the frequency range is available up to the resonant frequency, f_O, and reducing power MOSFET stress
- Automatic Dead Time Adjustment Function, not being necessary to make the dead time adjustment for each power supply specification
- Protection Functions
  - Line Undervoltage Protection Function (Brown-In／Brown-Out Function) ---------- Prevention of excessive input current and overheat at low input voltage
  - External Latch Function ---------- Latch shutdown by external signal input
  - Overcurrent Protection Function (OCP) ---------- Three steps protection corresponding to overcurrent levels
  - Overvoltage Protection Function (OVP) ---------- Latch shutdown
  - Overload Protection Function (OLP) ---------- Latch shutdown
  - Thermal Shutdown Functions (TSD) ---------- Latch shutdown

3. Functional Block Diagram and Terminal List

Functional Block Diagram

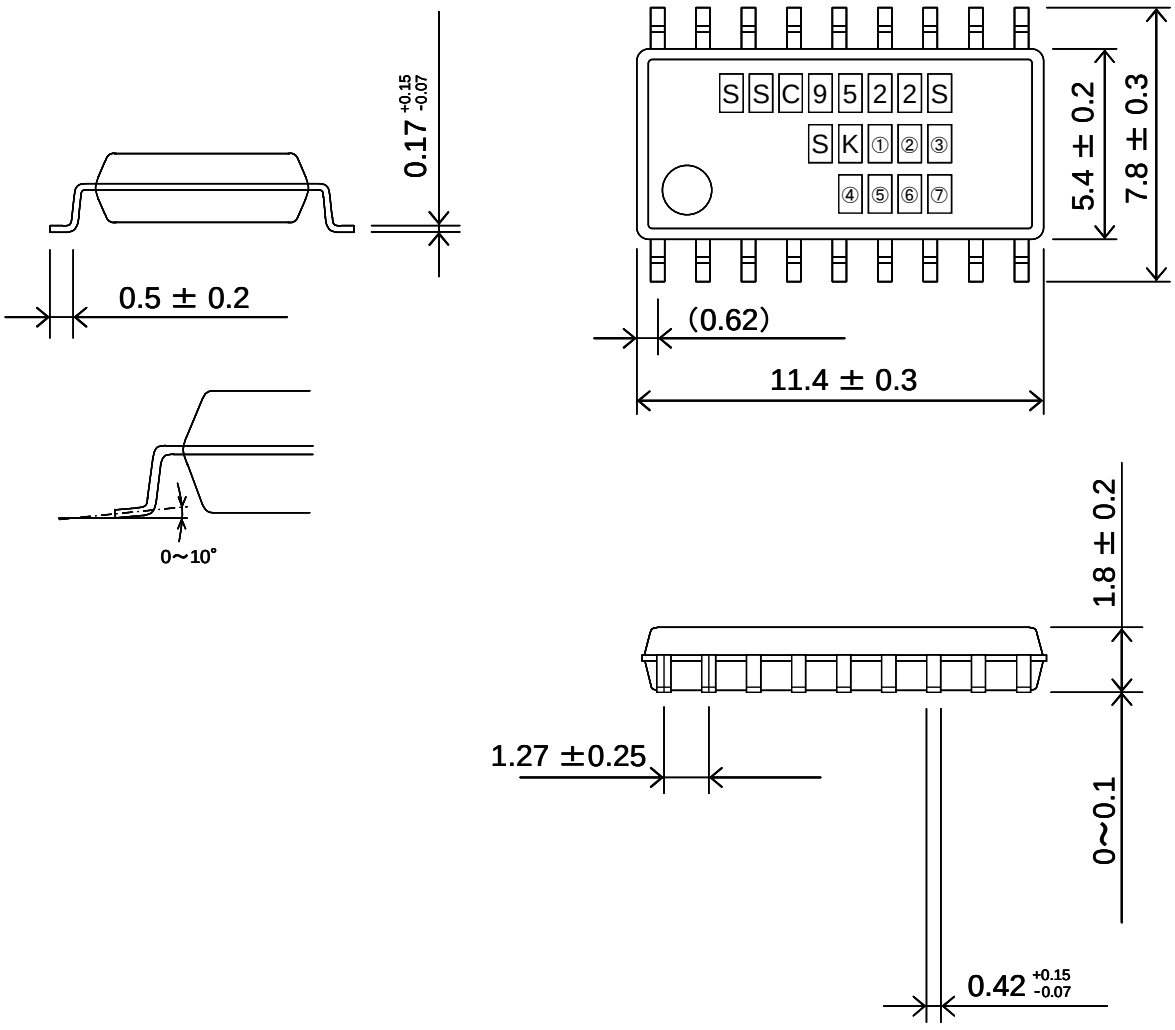


Terminal List Table

Terminal	Symbol	Functions
1	VSEN	AC line input voltage detection
2	V_{CC}	Power supply input for control circuit
3	FB	Constant voltage control signal input／Overload protection signal input
4	GND	Ground for control part
5	C_{SS}	Soft start capacitor connection
6	OC	Overcurrent protection signal input
7	RC	Resonant current signal input
8	Reg	Power supply output for gate drive
9	RV	Resonant voltage signal input
10	COM	Ground for power part
11	VGL	Low-side gate drive output
12, 13 17, 18	(NC)	(None)
14	VB	High-side gate drive voltage input
15	VS	High-side drive floating ground
16	VGH	High-side gate drive output

4. Package Information

The device is encapsulated in a standard 18 pin SOP package.



Dimensions in mm
Weight: Approx. 0.27g
Material of terminal: Cu
Treatment of terminal：solder plating

Upper tier：
Type symbol：SSC9522S
Middle, Lower tier：
『SK』＋『 Lot number ①—⑦ 』
・①：The last digit of year
・②：Month
1 to 9 for Jan. to Sep.
O for Oct.
N for Nov.
D for Dec.
・③：day
1st—10th ：1
11th—20th ：2
21st—31st ：3
・④～⑦：Sanken registration symbol

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Ta = 25°C, unless otherwise specified

Parameter	Terminal	Symbol	Ratings	Unit	Notes
VSEN terminal voltage	1−4	V_{SEN}	−0.3 toV_{REG}	V	
V_{CC} terminal voltage	2−4	V_{CC}	−0.3 to +35	V	
FB terminal voltage	3−4	V_{FB}	−0.3 to +10	V	
C_{SS} terminal voltage	5−4	V_{Css}	−0.3 to +12	V	
RC terminal voltage	7−4	V_{RC}	−6 to +6	V	
RV terminal current	9−4	I_{RV}	−2 to +2	mA	DC
			−100 to +100	mA	Pulse 40ns
OC terminal voltage	6−4	V_{OC}	−6 to +6	V	
VGL terminal voltage	11−4	V_{GL}	−0.3 to V_{REG}+0.3	V	
Reg terminal source current	8−4	I_{REG}	−20.0	mA	
Voltage between VB and VS terminal	14−15	V_B−V_S	−0.3 to +15.0	V	
VS terminal voltage	15−4	V_S	−1 to +600	V	
VGH terminal voltage	16−4	V_{GH}	V_S−0.3 to V_B+0.3	V	
Operating ambient temperature	—	T_{OP}	−20 to +85	℃	
Storage temperature	—	T_{stg}	−40 to +125	℃	
Junction temperature	—	T_j	+150	℃	

※Surge voltage withstand (Human body model) of No.14 to No.16 terminal is guaranteed 1000V.
Other terminals are guaranteed 2000V.

5.2 Electrical characteristics

V_{CC}=15V, Ta=25℃, unless otherwise specified.

Parameter	Terminal	Symbol	Ratings			Unit	Notes
			MIN	TYP	MAX		
Start／Circuit current							
Operation start voltage	2−4	$V_{CC(ON)}$	10.2	11.8	13.0	V	$V_{CC(OFF)}$ <$V_{CC(ON)}$
Operation stop voltage	2−4	$V_{CC(OFF)}$	8.8	9.8	10.9	V	
Circuit current in operation	2−4	$I_{CC(ON)}$	—	—	20.0	mA	
Circuit current in non-operation	2−4	$I_{CC(OFF)}$	—	—	1.2	mA	V_{CC}=9V
Circuit current in latch-operation	2−4	$I_{CC(L)}$	—	—	1.2	mA	V_{CC}=11V
OLP latch／External Latch							
FB terminal source current	3−4	I_{FB}	−30.5	−25.5	−20.5	μA	
FB terminal threshold voltage	3−4	V_{FB}	6.55	7.05	7.55	V	
C_{SS} terminal threshold voltage(1)	5−4	$V_{Css(1)}$	7.0	7.8	8.6	V	
Latch circuit release V_{CC} voltage	2−4	$V_{CC(La.Off)}$	6.7	8.2	9.5	V	$V_{CC(La.OFF)}$ <$V_{CC(OFF)}$
Oscillator							
Minimum frequency	11−10 16−15	$F_{(MIN)}$	26.2	28.3	31.2	kHz	
Maximum frequency	11−10 16−15	$F_{(MAX)}$	265	300	335	kHz	
Maximum dead-time	11−10 16−15	$t_{d(MAX)}$	1.90	2.45	3.00	μs	
Minimum dead-time	11−10 16−15	$t_{d(MIN)}$	0.25	0.50	0.75	μs	
Control							
Burst mode start FB terminal source current	3−4	$I_{CONT(1)}$	−2.9	−2.5	−2.1	mA	
Oscillation stop FB terminal source current	3−4	$I_{CONT(2)}$	−3.7	−3.1	−2.5	mA	
Soft start							
C_{SS} terminal charge current	5−4	$I_{Css(C)}$	−0.21	−0.18	−0.15	mA	
C_{SS} terminal reset current	5−4	$I_{Css(R)}$	1.0	1.8	2.4	mA	V_{CC}=9V
Overvoltage protection／Thermal protection							
OVP operating V_{CC} voltage	2−4	V_{OVP}	28.0	31.0	34.0	V	
Thermal shutdown operating temperature	—	$T_{j\,(TSD)}$	150	—	—	℃	
Detection of current resonant／Overcurrent protection							
Uncontrollability detection voltage	7−4	V_{RC}	±0.055	±0.155	±0.255	V	
RC terminal threshold voltage (Hi speed)	7−4	$V_{RC(S)}$	±2.15	±2.35	±2.55	V	
OC terminal threshold voltage(Low)	6-4	$V_{OC(L)}$	1.42	1.52	1.62	V	
OC terminal threshold voltage (High)	6-4	$V_{OC(H)}$	1.69	1.83	1.97	V	
OC terminal threshold voltage (Hi speed)	6-4	$V_{OC(S)}$	2.15	2.35	2.55	V	

Parameter	Terminal	Symbol		Ratings MIN	Ratings TYP	Ratings MAX	Unit	Notes
C_{SS} terminal sink current	5−4	I_{Css}	(L)	1.0	1.8	2.4	mA	
			(H)	12.0	20.0	28.0		
			(S)	11.0	18.3	25.0		
Detection of voltage resonant								
RV terminal voltage detect Resonance voltage(1)	9−4	$V_{RV(1)}$		3.8	4.9	5.4	V	
RV terminal voltage detect Resonance voltage(2)	9−4	$V_{RV(2)}$		1.20	1.77	2.30	V	
Stand by								
Burst oscillation frequency	5−4	f_{Css}		70	105	130	Hz	
ON／OFF								
C_{SS} terminal threshold voltage (2)	5−4	$V_{Css(2)}$		0.50	0.59	0.68	V	
Input voltage detect function								
VSEN terminal threshold voltage (ON)	1−4	$V_{SEN(ON)}$		1.32	1.42	1.52	V	
VSEN terminal threshold voltage (OFF)	1−4	$V_{SEN(OFF)}$		1.08	1.16	1.24	V	
Supply of driver circuit								
Reg terminal output voltage	8−4	V_{REG}		9.9	10.5	11.1	V	
High-side driver								
High-side drive operation start voltage	14−15	$V_{BUV(ON)}$		6.3	7.3	8.3	V	
High-side drive operation stop voltage	14−15	$V_{BUV(OFF)}$		5.5	6.4	7.2	V	
Drive circuit								
VGL,VGH terminal source current 1	11−10 16−15	$IGL_{SOURCE1}$ $IGH_{SOURCE1}$		—	515	—	mA	V_{Reg}=10.5V V_B=10.5V V_{GL}=0V V_{GH}=0V
VGL,VGH terminal sink current 1	11−10 16−15	IGL_{SINK1} IGH_{SINK1}		—	−685	—	mA	V_{Reg}=10.5V V_B=10.5V V_{GL}=10.5V V_{GH}=10.5V
VGL,VGH terminal source current 2	11−10 16−15	$IGL_{SOURCE2}$ $IGH_{SOURCE2}$		50	82	120	mA	V_{Reg}=12V V_B=12V V_{GL}=10.5V V_{GH}=10.5V
VGL,VGH terminal sink current 2	11−10 16−15	IGL_{SINK2} IGH_{SINK2}		−160	−113	−70	mA	V_{Reg}=12V V_B=12V V_{GL}=1.5V V_{GH}=1.5V

5.3 Thermal resistance

Parameter	Symbol	Ratings MIN	Ratings TYP	Ratings MAX	Unit	Notes
MIC junction to air	θ_{j-a}	—	—	95	℃/W	

6. Typical Application Circuit

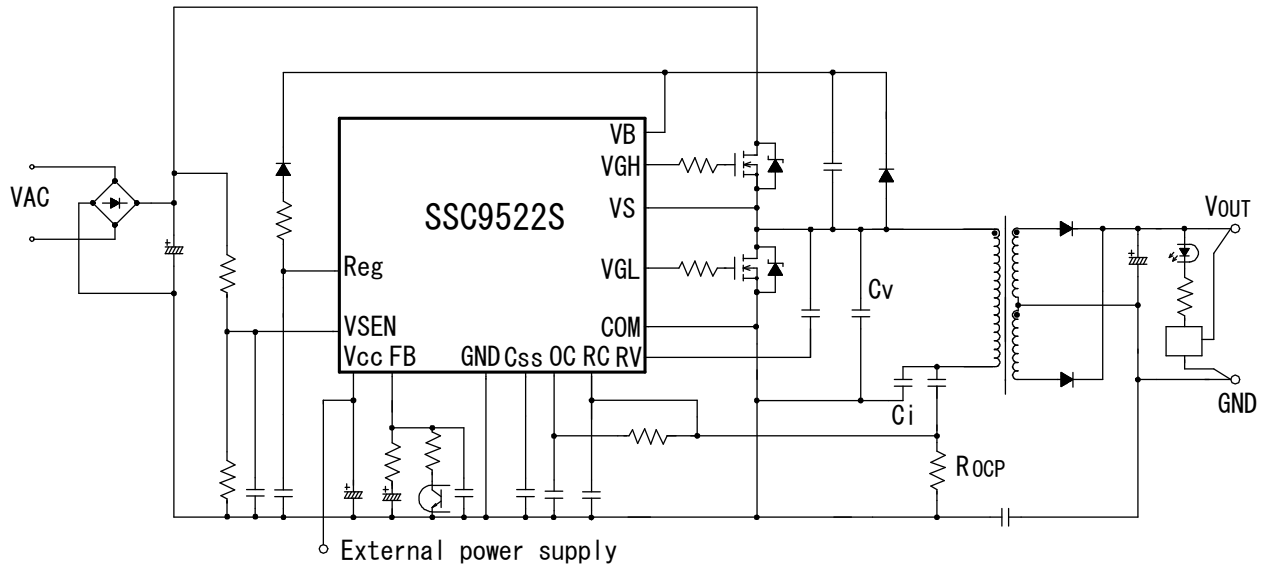


Figure 6 Typical application circuit example

7. Functional Descriptions

The polarity of current is shown as "+"for sink current and "−" for source current based on IC.

7.1 Resonant Circuit Operation

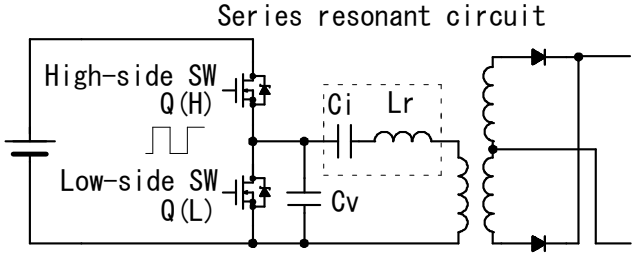


Figure 7-1 Principal of series resonant converter

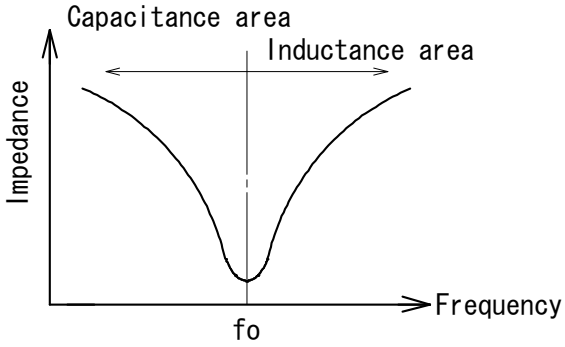


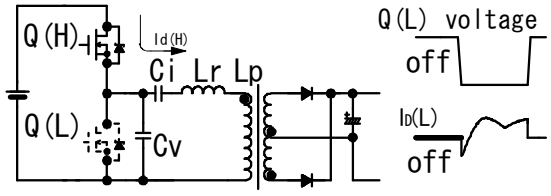
Figure 7-2 Resonant circuit impedance

Figure 7-1 depicts the principle of resonant converter. The Q(H) stands for High-side SW, the Q(L) stands for Low-side SW, the Ci stands for current resonant capacitor, and the C_V stands for voltage resonant capacitor.
When the frequency is changed, the impedance of resonant circuit is changed as shown in Figure 7-2.
Higher frequency area than the resonant frequency, f_O, is inductance area, lower frequency area is capacitance area.
Therefore, the resonant converter operates in inductance area due to soft-switching operation.

The thick waveform line of Figure 7-3 depicts Low-side SW current waveform of each timing in steady state.

①Period Operation

During Q(H) is ON, the energy is stored into series resonant circuit due to I_D(H) flowed through resonant circuit and transformer.



①Period

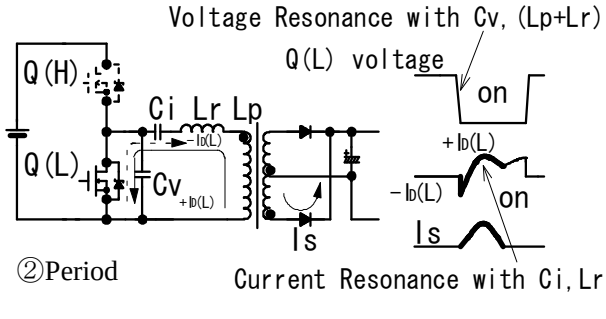
②Period Operation

When Q(H) turns off, $-I_D$(L) flows to Q(L) due to the energy stored series resonant circuit, C_V is discharged and Q(L) voltage goes down to the forward voltage of its body diode, V_F. Thus, when Q(L) turns on, ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) are achieved on Q(L).

The primary winding voltage of transformer adds Ci voltage, and the energy is transferred to the secondary circuit.

At the same time, Ci voltage goes down due to discharge.

When the primary winding voltage can not keep the secondary rectifier ON, the energy to the secondary circuit is stopped.



③Period Operation

I_D(L) keeps on flowing, and Ci keeps on discharging.

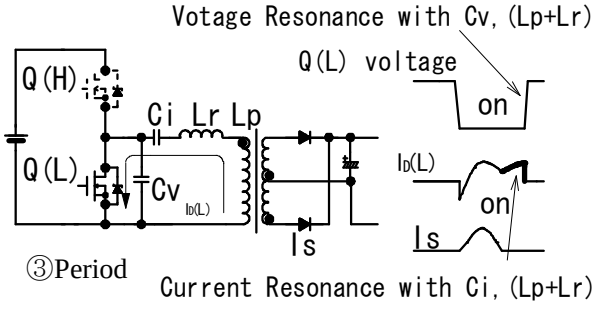


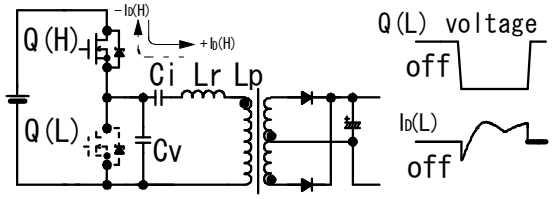
Figure 7-3-1 Resonant circuit operation

④Period Operation

When Q(L) turns off, $-I_D$(H) flows to Q(H) due to the energy stored series resonant circuit, C_V is charged and Q(L) goes up to the input voltage, Q(H) voltage is clamped with the forward voltage of its body diode, V_F. Thus, when Q(H) turns on, ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) are achieved on Q(H).

The primary winding voltage of transformer adds Ci voltage, and the energy is transferred to the secondary circuit.

At the same time, Ci voltage goes down due to discharge. When the primary winding voltage can not keep the secondary rectifier ON, the energy to the secondary circuit is stopped.



④Period

Figure 7-3-2 Resonant circuit operation

The above-mentioned operations are repeated, the energy to the secondary circuit is transferred with ZVS and ZCS operations.

7.2 Startup Operation

V_{CC} terminal voltage is provided with an external power supply as shown in Figure 7-4.

When V_{CC} terminal voltage reaches $V_{CC(ON)}$= 11.8V(TYP), the control circuit starts operation.

While the control circuit is in operation, if V_{CC} terminal voltage decreases to $V_{CC(OFF)}$= 9.8V(TYP), the control circuit stops operation by UVLO (Undervoltage lockout) circuit, and reverts to the state before startup.

Switching operation at startup starts when the following conditions are fulfilled.

- VSEN terminal voltage is $V_{SEN(ON)}$= 1.42V(TYP) and more.
- V_{CC} terminal voltage is $V_{CC(ON)}$= 11.8V(TYP) and more.
- C_{SS} terminal voltage is $V_{CSS(2)}$= 0.59V(TYP) and more.

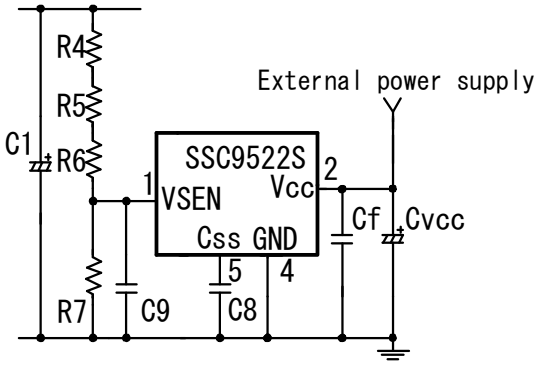


Figure 7-4 V_{CC} peripheral circuit

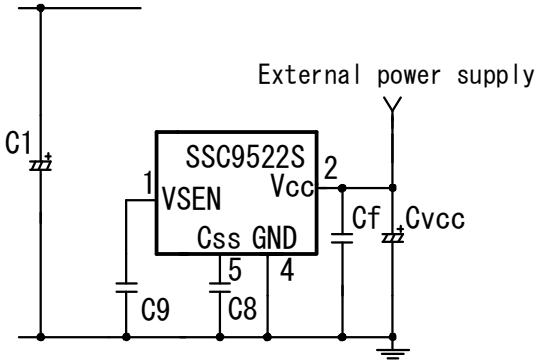


Figure 7-6 V_{CC} peripheral circuit without brown-in/brown-out function

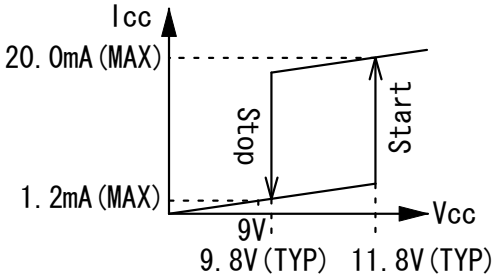


Figure 7-5 Relationship of V_{CC} and I_{CC} at Startup and Shutdown

After providing the input voltage, when the IC is turned on / off with V_{CC} terminal voltage provided from the external power supply, the startup time from $V_{CC(ON)}$= 11.8V(TYP) to the switching operation is shown below.

- In Figure 7-4, the approximate value, t_{ST1}, is as follows.

$$t_{st1} = C8 \times V_{CSS(2)} / I_{CSS(C)} \quad \text{----- (1)}$$

where $V_{CSS(2)}$= 0.59V(TYP)、$I_{CSS(C)}$= −0.18mA(TYP)

When C8 is 1μF, t_{ST1} is about 3.3ms.

- In Figure 7-6, VSEN terminal voltage is charged by the internal circuit after $V_{CC(ON)}$= 11.8V(TYP), the rising time, t_{ST2}, to $V_{SEN(ON)}$= 1.42V(TYP) is added to t_{ST1}.
  The approximate value, t_{ST2}, is as follows.
  The circuit without Brown-In / Brown-Out Functions refers to "7.8 Line Undervoltage Protection Function (Brown-In / Brown-Out Function)" section

$$t_{st2} = C9 \times 380k \quad \text{----- (2)}$$

When C8 is 1μF and C9 is 0.01μF, t_{ST1} is about 3.3ms and t_{ST2} is about 3.8ms. As a result, the total startup time is about 7.1ms.

7.3 Soft Start Function

The oscillation frequency varies with C_{SS} terminal voltage. The soft start operation is achieved by connecting the capacitor, C8, to C_{SS} terminal externally.
At startup, C8 is charged by $I_{CSS(C)}$= −0.18mA(TYP), and C_{SS} terminal voltage rises gradually.
Thus, the oscillation frequency decreases from Maximum frequency, $F_{(MAX)}$= 300kHz(TYP), and the output power of the SMPS increases.
By this soft start function at startup, both the reduction of stress on peripheral components and the prevention of uncontrollable operations are achieved.
When V_{CC} terminal voltage falls below $V_{CC(OFF)}$= 9.8V (TYP) or VSEN terminal voltage falls below $V_{SEN(OFF)}$= 1.16V(TYP) or External Latch Function or OVP latch or OLP latch or TSD latch works, C8 is discharged by $I_{CSS(R)}$= 1.8mA (TYP).

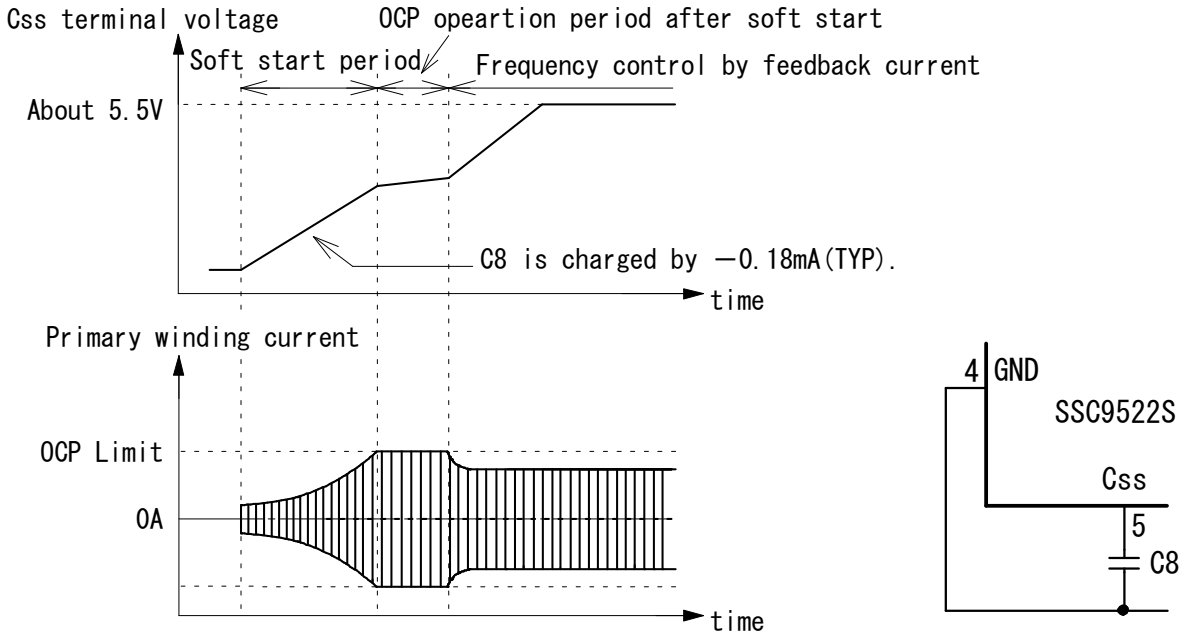


Figure 7-7 C_{SS} operation diagram

7.4 Constant Output Voltage Control

The constant output voltage is controlled by frequency control in the inductance area, by the feedback current sunk from FB terminal connected a photo-coupler.

At slight loads, the burst oscillation is achieved when the feedback current is $I_{CONT(1)}$= −2.5mA(TYP) and less. This mode reduces switching loss and restrains the output voltage of SMPS from increasing.

As the ability of the sink current from FB terminal is necessary to be sunk $I_{CONT(2)}$= −3.7mA(MIN) and less, the forward current of photo-coupler in the secondary circuit should be set in consideration of aging degradation of CTR (Current Transfer Ratio) and others.

In Figure 7-8, R2 value is recommended 560Ω.

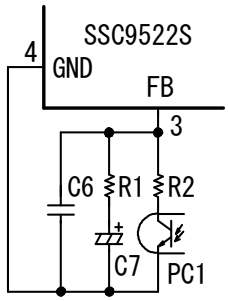


Figure 7-8 FB terminal peripheral circuit

7.5 Automatic Dead Time Adjustment Function

The Automatic Dead time Adjustment Function is incorporated, and thus, it is unnecessary to adjust the dead time for each SMPS specification.

By detecting dv/dt of Low-side MOSFET V_{DS} (Drain-to-Source voltage) waveform, the control circuit automatically controls ZVS (Zero Voltage Switching) operation on High-side / Low-side MOSFET.

A very simple peripheral circuit achieves this function, only by placing a high-voltage-type ceramic capacitor Crv (total capacitor value is about 5pF) between VS terminal and RV terminal, as shown in Figure 7-9.

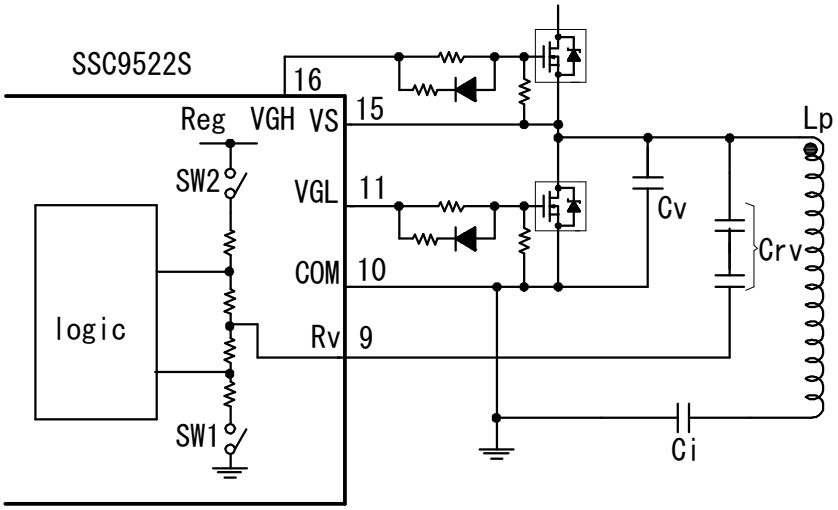


Figure 7-9 RV terminal peripheral circuit

RV terminal voltage is the divided voltage by resistors between internal reference voltage (Reg) and GND.

The differential current flown through Crv by the dv/dt of Low-side MOSFET V_{DS} waveform is provided to RV terminal. Thus, the dead time detection circuit detects dv/dt of Low-Side MOSFET.

Both the circuit current reduction and the differential circuit response improvement are achieved by turning on SW1 and SW2 together in the period needed the detection.

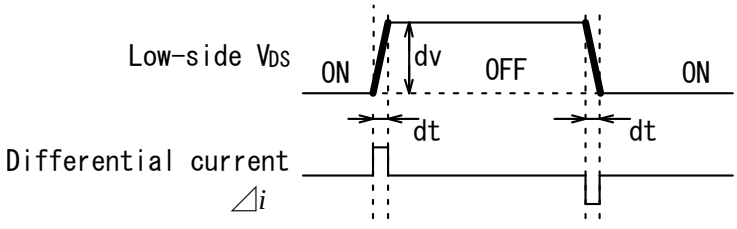


Figure 7-10 Differential current

The differential current Δi is as follows.

$$\Delta i = Crv \times (dv/dt) \qquad \text{-----(3)}$$

When the differential current Δi exceeds the current in the following equation, a smaller value of Crv is recommended.

$$\left| \Delta i \right| \leq \frac{100mA \times 40ns}{dt} \qquad \text{-----(4)}$$

When *dt* is 40ns or below, Δi is set to ±100mA.

Figure 7-11 shows the schematic operational waveforms of Automatic Dead Time Adjustment Function.

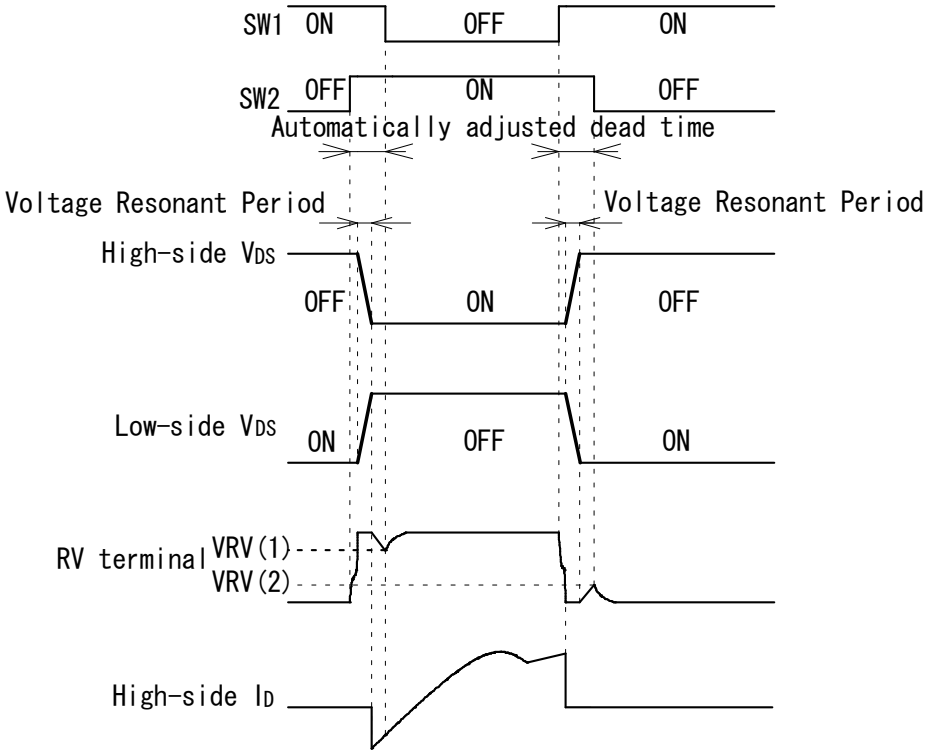


Figure 7-11 Operational waveform of Automatic Dead time Adjustment Function

- Voltage Resonant Period in Turning OFF Low-side MOSFET

  When Low-side MOSFET is turned off, SW2 is turned on while keeping SW1 turned on.
  At this time, the resonant current flows through C_V, Ci and L_P. Thus, C_V voltage rises from 0V.
  When this voltage reaches "Input voltage $+V_F$ of High-side MOSFET body diode", the resonant current flows through High-side MOSFET body diode, and the V_{DS} of Low-side MOSFET is clamped. This period is defined as Voltage Resonant Period.

  Because the differential current flown through Crv by the dv/dt of Low-side MOSFET V_{DS} waveform is provided to RV terminal, RV terminal voltage rises from the internally divided voltage by resistors, until clamped internally.
  When the Voltage Resonant Period ends and the differential current becomes zero, RV terminal voltage returns to the internally divided voltage.

  At this time, the control circuit detects the completion of Voltage Resonant Period, by detecting $V_{RV(1)}$= 4.9V (TYP). As a result, High-side MOSFET is turned on and SW1 is turned off. This period is automatically adjusted dead time.

- Voltage Resonant Period in Turning OFF High-side MOSFET

  When High-side MOSFET is turned off, SW1 is turned on while keeping SW2 turned on.
  At this time, the resonant current flows through C_V, Ci and L_P. Thus, C_V voltage falls from the input voltage.
  When this voltage falls below "$-V_F$ of Low- side MOSFET body diode", the resonant current flows through Low-side MOSFET body diode and the V_{DS} of High-side MOSFET is clamped. This period is defined as Voltage Resonant Period.

  Because the differential current flown through Crv by the dv/dt of Low-side MOSFET V_{DS} is provided to RV terminal, RV terminal voltage falls from the internally divided voltage by resistors, until clamped to internal GND level.
  When the Voltage Resonant Period ends and the differential current from RV terminal becomes zero, RV terminal voltage returns to the internally divided voltage.

  At this time, the control circuit detects the completion of Voltage Resonant Period by detecting $V_{RV(2)}$= 1.77V (TYP). As a result, Low-side MOSFET is turned on and SW2 is turned off. This period is automatically adjusted dead time.

When the dead time period becomes shorter than Voltage Resonant Period, switching losses are increased because power MOSFETs turn ON / OFF during Voltage Resonant Period, as shown in Figure 7-12.
It is usually necessary to adjust values of resonant circuit and evaluate voltage resonant operation over each condition of the SMPS specification because Voltage Resonant Period is variable on the condition of input voltage and output power of the SMPS.
However, the Automatic Dead Time Adjustment Function always makes ZVS (Zero Voltage Switching) for Voltage Resonant Period when RV terminal is provided the signals which reach $V_{RV(1)}$, $V_{RV(2)}$ threshold voltage.

Regarding ZCS (Zero Current Switching) of the IC, the minus current period of I_D (the period in which the current flows into power MOSFET body diode) should be more than 450ns as shown in Figure 7-13.

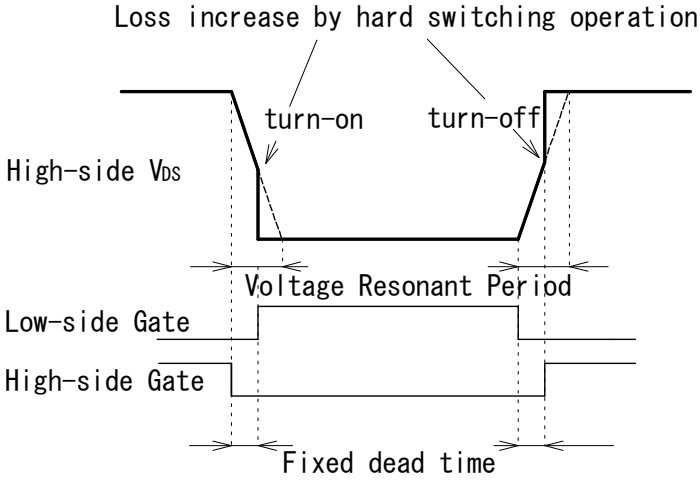


Figure 7-12 ZVS failure operation waveform

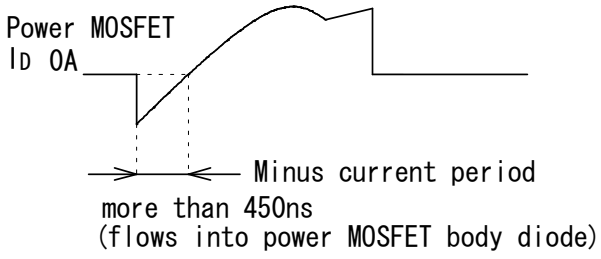


Figure 7-13 ZCS Check Point

7.6 Latch Function

The fault latch function stops switching operation with latch mode, when OVP and/or OLP and/or TSD protection functions are activated.

Releasing the latch is done by dropping the V_{CC} terminal voltage below $V_{CC(La.Off)}$= 8.2V(TYP).

7.7 External Latch Function

As the protection for abnormal operations, the latch circuit is activated when C_{SS} terminal voltage reaches $V_{CSS(1)}$= 7.8V(TYP) and more by an external circuit.
The current from the external circuit should be 100μA and more. Because the sink current flows into IC at C_{SS} terminal in OCP operation, if the current from the external circuit is lower than the sink current, C_{SS} terminal voltage could not rise
The external circuit should keep C_{SS} terminal voltage within Absolute Maximum Rating, 12V, for example, by clamping with a 10V zener diode (Figure 7-14) or other ways.

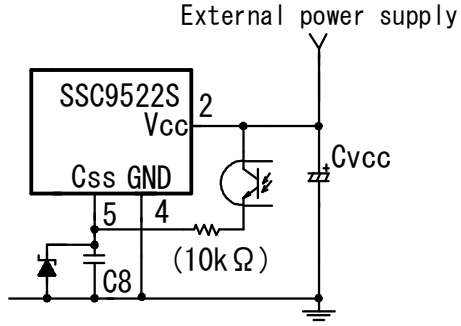


Figure 7-14 External latch example

7.8 Line Undervoltage Protection Function (Brown-In／Brown-Out Function)

VSEN terminal detects the input voltage and stops the oscillation at low input voltage (Brown-In / Brown-Out Function), this function prevents exceeding input current and overheat.

When this function is unnecessary, R4 to R7 are removed and C9 is recommended about 0.01μF to prevent malfunction caused by noise.

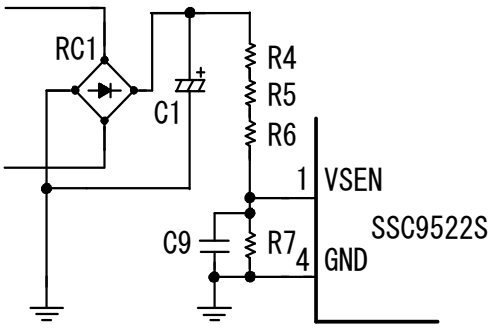


Figure 7-15 VSEN terminal peripheral circuit

The detecting voltage is set by R4 to R7 in Figure 7-15.

- When VSEN terminal voltage is $V_{SEN(ON)}$= 1.42V(TYP) and more, the control circuit starts operation.
- When VSEN terminal voltage is $V_{SEN(OFF)}$= 1.16V(TYP) and less, the control circuit stops oscillation.

The resistors, R4 to R7, and the operation voltages are as follows.

$$R4 + R5 + R6 \fallingdotseq \frac{E_{IN(ON)} - V_{SEN(ON)}}{V_{SEN(ON)}} \times R7 \ , \quad E_{IN(OFF)} \fallingdotseq \frac{V_{SEN(OFF)}}{V_{SEN(ON)}} \times E_{IN(ON)} \qquad \text{------(5)}$$

where $E_{IN(ON)}$ is the DC input voltage on which the control circuit starts operation, and $E_{IN(OFF)}$ is the DC input voltage on which the control circuit stops operation.

C9 capacitor reduces AC ripple and makes some delay time. The recommended value is about 0.1μF.
R4 to R6 applied high voltage are recommended anti-electromigration type of resistors, such as metal oxide film.
The values of R4 to R7 and C9 should be adjusted on actual operation.

7.9 Overvoltage Protection Function (OVP)

When the voltage of V_{OVP}= 28V(MIN) and more is applied between V_{CC} terminal and GND terminal, the control circuit stops oscillation in latch mode by internal OVP circuit operation,
The voltage applied to V_{CC} terminal should be below Absolute Maximum Rating, 35V.

7.10 Overload Protection Function (OLP)

When overload conditions (this state is limited by Overcurrent Protection (OCP)) continues during a certain time (delay time), the control circuit increases the switching frequency and limits the output power of the SMPS. Thus, this function reduces stresses of power MOSFETs, secondary diodes and so on.

In OCP operation, the output voltage falls down and the feedback current from secondary photo-coupler becomes zero. When the feedback current becomes zero, I_{FB}= −25.5μA(TYP) flows from FB terminal and charges C7 shown in Figure 7-16.
When FB terminal voltage reaches V_{FB}= 7.05V(TYP), the control circuit stops operation in latch mode.
This period is defined as Latch delay time, t_{DLY}, and the approximate value is as follows.

$$t_{DLY} \fallingdotseq \frac{\left(4.05V - R1 \times 25.5\mu A \right) \times C7}{25.5\mu A} \qquad \text{-----(6)}$$

When R1 is 47kΩ and C7 is 4.7μF, t_{DLY} is about 0.5sec.

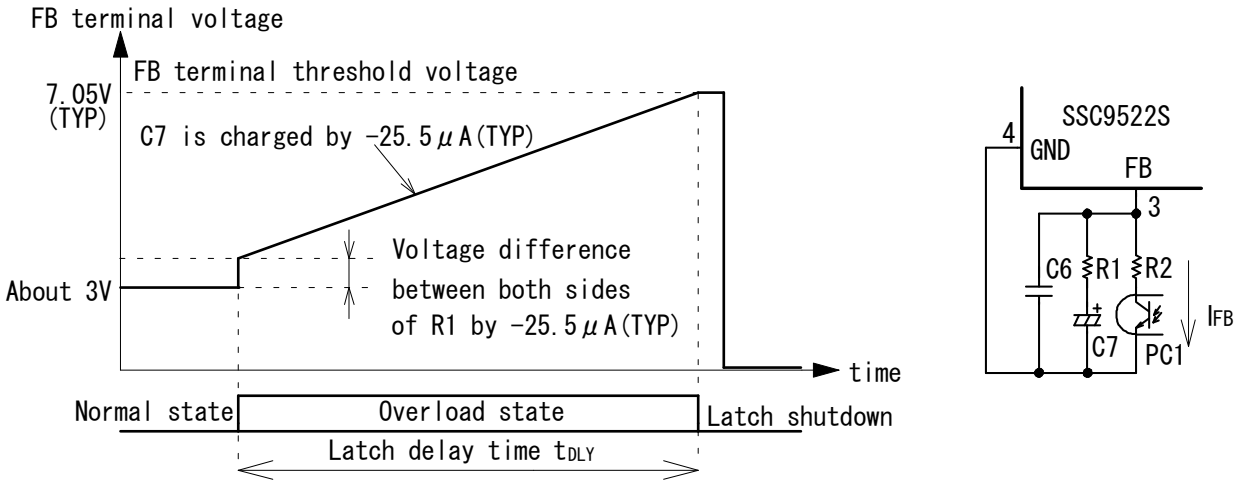


Figure 7-16 OLP operation

7.11 Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects the drain current, I_D, with pulse-by-pulse basis at OC terminal, and limits output power.

In Figure 7-17, by using a smaller capacitor for bypass capacitor C12 than the current resonant capacitor Ci, the detection current decreases. As a result, the power loss at the detecting resistor R_{OCP}, is reduced, and a smaller resistor is available.

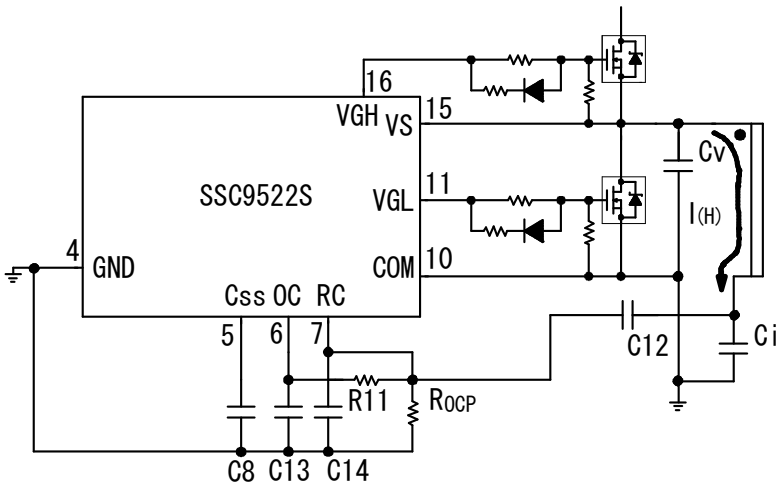


Figure 7-17 OC terminal peripheral circuit

For resonant power supplies, the values of R_{OCP}, R11, C12 and C13 should be adjusted on actual operation, because there is no convenient method to calculate the accurate resonant current value by input / output conditions and others.

The relationship among $V_{OC(L)}$, C12 and Ci is as follows.

$$R_{OCP} \fallingdotseq \frac{V_{OC(L)}}{I_{(H)} \times \frac{C12}{C12+Ci}} \qquad \text{----- (7)}$$

where $I_{(H)}$ is the drain current of High-side MOSFET as shown in Figure 7-17.

As R_{OCP} voltage is used for Uncontrollable Operation Detection as described in "7.12 Uncontrollable Operation Detection Function" section, R_{OCP} and C12 should be adjusted by both OCP detection and Uncontrollable Operation Detection.

The following values are recommended as target values.

C12 is adjusted so that R_{OCP} becomes about 100Ω, and generally it is about 1／100 of Ci.

R11 is about 470Ω and C13 is about 680pF for filter portion.

There are three steps protection corresponding to overcurrent levels as follows.

①OC Terminal Threshold Voltage (Low) : $V_{OC(L)}$

This protection works first. When OC terminal voltage exceeds $V_{OC(L)}$= 1.52V(TYP), C8 is discharged by $I_{CSS(L)}$= 1.8mA(TYP), and thus, the switching frequency increases, and the output power is limited.

When OC terminal voltage falls below $V_{OC(L)}$ in discharging C8, the discharge stops.

②OC Terminal Threshold Voltage (High) : $V_{OC(H)}$

This protection works second. When OC terminal voltage exceeds $V_{OC(H)}$= 1.83V(TYP), C8 is discharged by $I_{CSS(H)}$= 20mA(TYP), and thus, the switching frequency increases faster because $I_{CSS(H)}$ is about 11 times of $I_{CSS(L)}$, and the output power is limited.

When OC terminal voltage falls below $V_{OC(H)}$ in discharging C8, the above operation in ① is active.

③OC Terminal Threshold Voltage (Hi speed) : $V_{OC(S)}$

This protection works third. When OC terminal voltage exceeds $V_{OC(S)}$= 2.35V(TYP), power MOSFETs reverse ON / OFF, C8 is discharged by $I_{CSS(S)}$= 18.3mA(TYP), and thus, the Hi Speed OCP operation achieves so as to increase the switching frequency and to limit the output power.

This operation works to protect for exceeding overcurrent, such as the output shorted.

When OC terminal voltage falls below $V_{OC(S)}$ because of limiting the output power, the above operations in ① and ② are active.

7.12 Uncontrollable Operation Detection Function

The constant output voltage is controlled by frequency control, the switching frequency decreases when output power increases. When the switching frequency goes to capacitance area, the constant output voltage is uncontrollable, the hard switching makes loss increased, and power MOSFETs increase their stress.

This phenomenon is called Uncontrollable Operation.

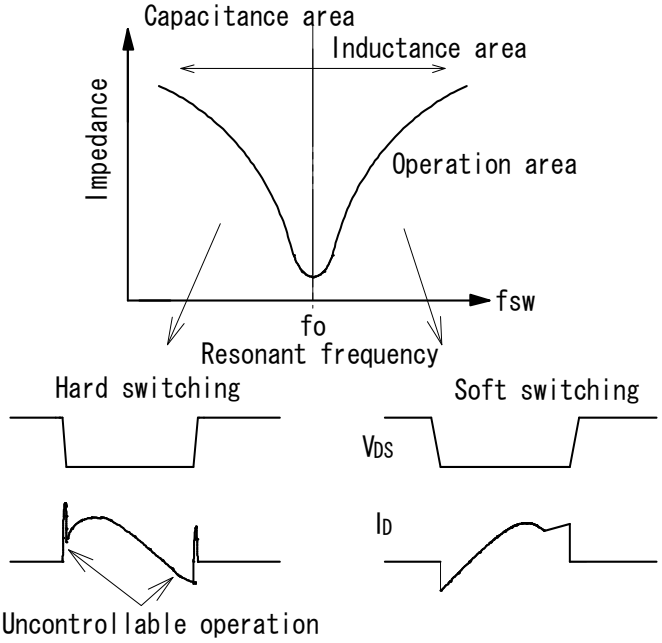


Figure 7-18 Uncontrollable operation

The Uncontrollable Operation Detection Function is incorporated in the IC. This function prevents the above-mentioned issues, and moreover, improves the ability of transformer because of enabling to operate in the resonant frequency, f_O (which makes the most of output power in series resonant circuit).

This function eliminates to adjust the minimum switching frequency to higher than the resonant frequency, f_O, for each power supply specification.

There are two Uncontrollable Operation Detection Functions.

- During High-side MOSFET turns on, when RC terminal voltage crosses V_{RC}= +0.155V(TYP) on the condition that RC terminal voltage changes from plus to minus, the control circuit detects Uncontrollable Operation (refer to RC Terminal Voltage in Capacitance Area waveform in Figure 7-19), and thus, High-side MOSFET turns off and Low-side MOSFET turns on.
- During Low-side MOSFET turns on, when RC terminal voltage crosses V_{RC}= −0.155V(TYP) on the condition that RC terminal voltage changes from minus to plus, the control circuit detects uncontrollable operation, and thus, Low-side MOSFET turns off and High-side MOSFET turns on.

By the above functions, the Uncontrollable Operation is detected with pulse-by-pulse basis.
By synchronizing the operational switching frequency with the Uncontrollable Operation frequency, it is available to prevent Uncontrollable Operation.

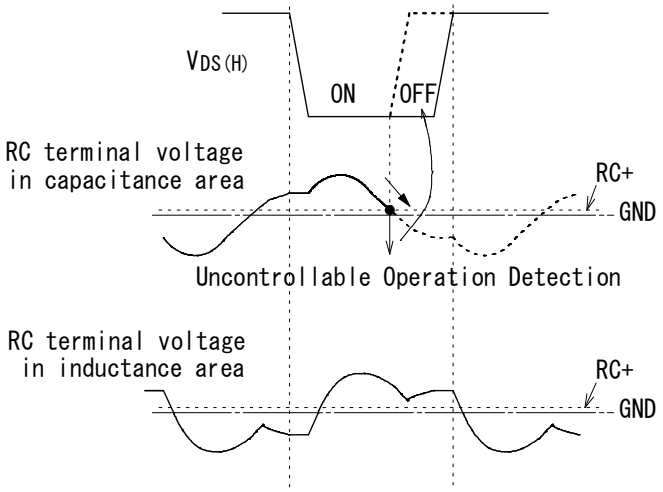


Figure 7-19 Uncontrollable Operation Detection on High-side MOSFET

For Uncontrollable Operation Detection, RC terminal should be connected to the input side of OC terminal filter circuit in order to improve the detection speed, as shown in Figure 7-20.
C14 is recommended about 100pF to prevent malfunctions caused by noise,
R_{OCP} and C12 should be adjusted as described in "7.11 Overcurrent Protection Function (OCP)" section.
In addition, R_{OCP} should be adjusted to reach V_{RC}= ±0.155V(TYP), on such conditions caused uncontrollable operation easily as SMPS is at startup, the input voltage is off, or the output is shorted.
RC terminal voltage should be within Absolute Maximum Rating, ±6V.

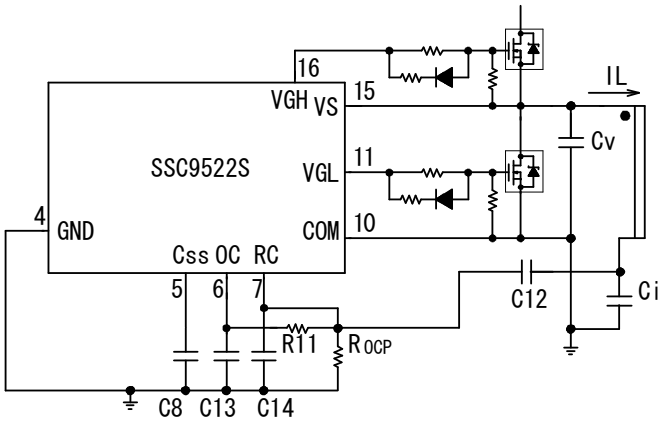


Figure 7-20 RC terminal peripheral circuit

RC terminal has $V_{RC(S)}$ threshold as well as $V_{OC(S)}$ of OC terminal functions.
When RC terminal voltage exceeds $V_{RC(S)}$ = ±2.35V(TYP), power MOSFETs reverse ON / OFF such as the Hi speed OCP operation.
Refer to "7.11 Overcurrent Protection Function (OCP) ③OC Terminal Threshold Voltage (Hi speed)" section for the Hi Speed OCP operation.

8. Design Notes

8.1 Boot strap peripheral circuit

Reg terminal is the output terminal of regulator voltage for bootstrap circuit, which drives High-side MOSFET. The bootstrap circuit is composed of D2, R9 and C11 between Reg terminal and VS terminal

The following function is incorporated, for the protection of abnormal operations caused by short circuit on C11. When the voltage between VB terminal and VS terminal falls below $V_{BUV(OFF)}$= 6.4V(TYP), the control circuit stops the High-side drive switching operation.

D2 is recommended an ultra fast speed diode with short recovery time and low leak current.

As for Sanken's diode lineup, AG01A (Vrm = 600V) of UFRD series is recommended.

C11 is recommended a film type or ceramic capacitor with low ESR and low leak current.

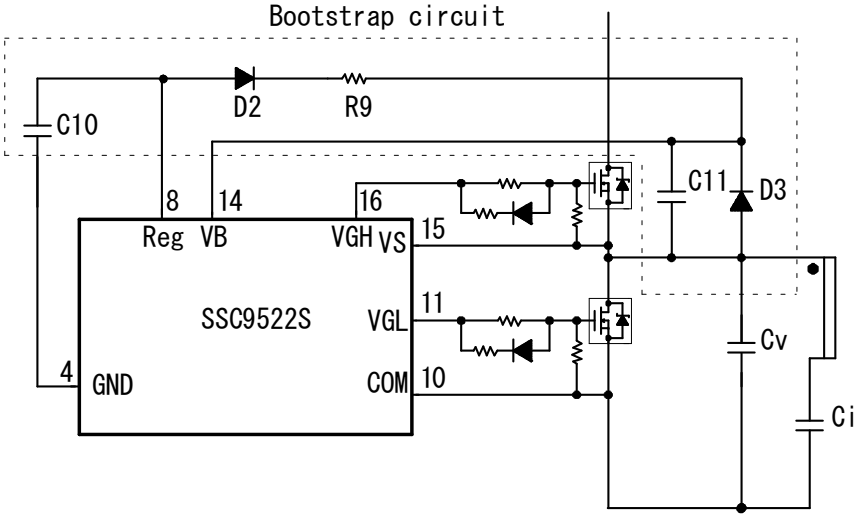


Figure 8-1 Bootstrap circuit

8.2 Gate terminal peripheral circuit

VGH terminal and VGL terminal are the gate drive terminals for external power MOSFETs.

The source peak current is −0.515A(TYP), and the sink peak current is 0.685A(TYP).

In Figure 8-2, R12, R13 and D4 should be adjusted considering power losses of power MOSFETs, gate waveforms (reduction of ringing caused by pattern layout, and others) and EMI noise.

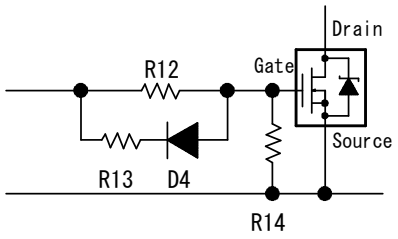


Figure 8-2 MOSFET Gate peripheral circuit

R14 prevents malfunctions caused by steep dv/dt at turning off power MOSFET. It is recommended to place a resistor in 10k to 100kΩ range close to Gate and Source of power MOSFET.

8.3 Peripheral Components

Take care to use properly rating and proper type of components.

- Input and output electrolytic capacitors : Apply proper margin to ripple current, voltage, and temperature rise. Use of high-ripple current and low impedance types, designed for switch mode power supplies, is recommended.
- Transformer : Apply proper design margin to temperature rise by core loss and copper loss.
- Current detecting resistor, R_{OCP} : Choose a low inductance and surge-proof type, because a high frequency switching current flows to R_{OCP} and some malfunction may be caused if a high inductance resistor is used.
- Current resonant capacitor, Ci : Apply a polypropylene film capacitor with low loss and high current capability.

8.4 Pattern layout and Component placement

PCB circuit trace design and component layout affect proper functioning during operation. Unless they are proper, malfunction, large noise and large power dissipation may occur.

Circuit loop traces flowing high frequency current, as shown in Figure 8-3, should be designed as wide, short and small as possible to reduce trace impedance.

In addition, earth ground traces affect radiation noise, and thus, it should be designed as wide and short as possible.

Switching mode power supplies consist of current traces with high frequency and high voltage, and thus, trace design and component layout should be done to comply with all safety guidelines.

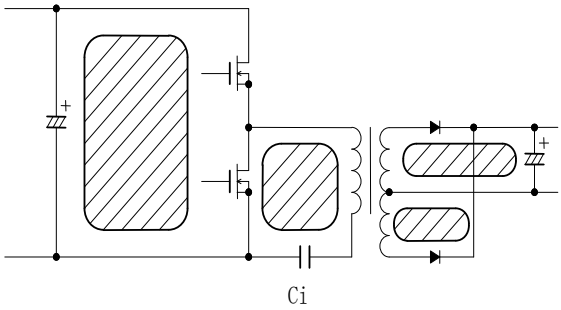


Figure 8-3 High frequency current loop

Furthermore, because an integrated power MOSFET is being used as the switching device, take account of the positive thermal coefficient of $R_{DS(ON)}$ for thermal design.

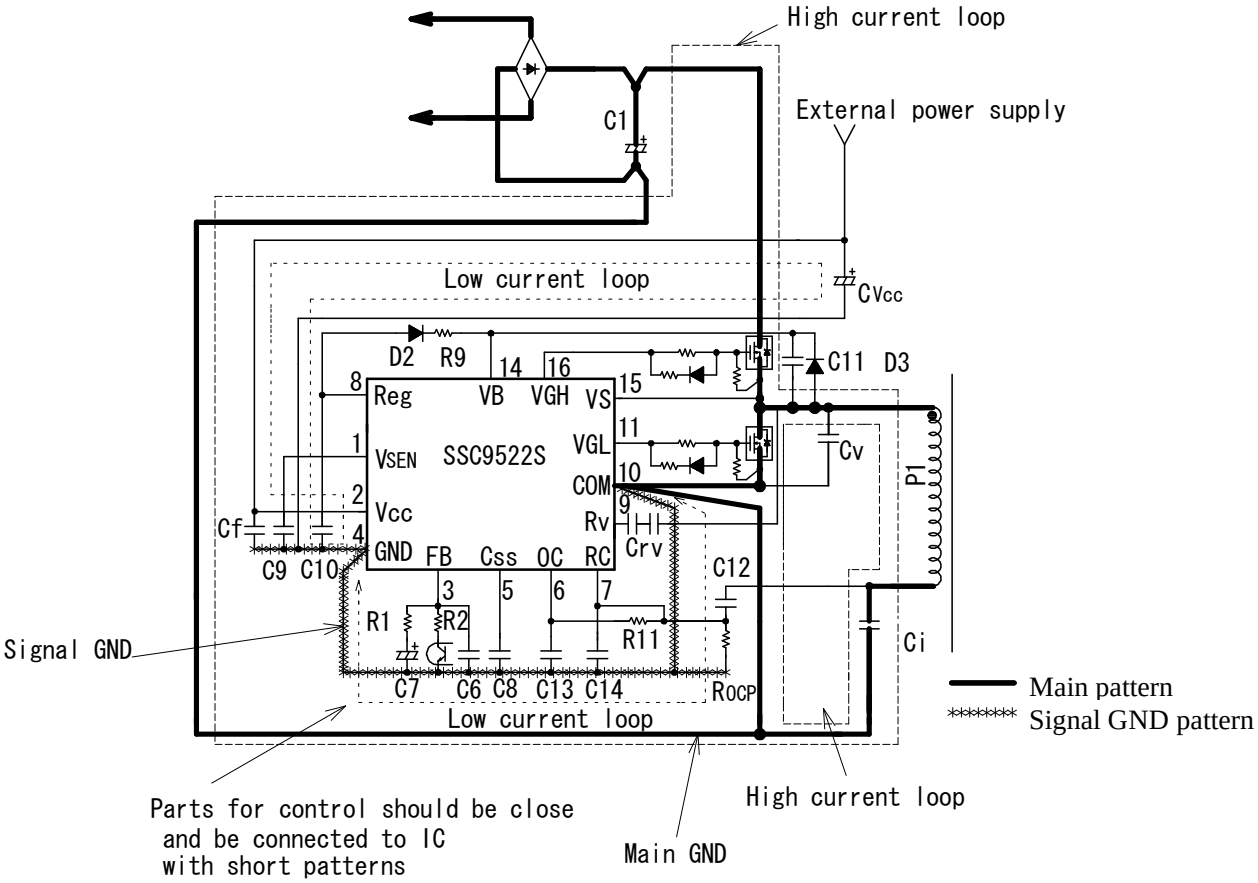


Figure 8-4 Layout design example

Figure 8-4 shows a circuit layout design example.

- Separate signal GND patterns from main current GND patterns because of reducing common impedance, and connect them at COM terminal (No.10 pin). Especially, connect GND (No.4) terminal to COM (No.10) terminal with the shortest pattern possible to prevent main resonant circuit current from flowing into the patterns for control.
- Place a C_f (film capacitor of about 0.1μF) close to the IC to prevent malfunctions caused by noise, when the distance between C_{VCC} and V_{CC} terminal becomes long.
- Connect control parts for the IC close to the IC with the shortest patterns possible.

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