

High Performance Non-Isolated Buck PFC Controller

FEATURES

- | Low Cost LED Driver Solution with Non-Isolated Buck PFC
- | Quasi-Resonant Switching to Achieve >90% Efficiency
- | Accurate LED Output Current $\leq \pm 1\%$ Control with Universal Input
- | Proprietary Constant On-time Control for $PF > 0.97$
- | Proprietary ZCD Method to Save Auxiliary Winding Design
- | Building-in Complete Protection:
 - o LED Open and Short Protection
 - o Cycle-by-Cycle Over Current Protection
 - o OVP for IC Bias Voltage
 - o Maximum and Minimum Switching Frequency Limit
 - o Built-in Thermal Protection
- | RoHS Compliant and Halogen Free
- | Available with SOT23-6 Package

APPLICATIONS

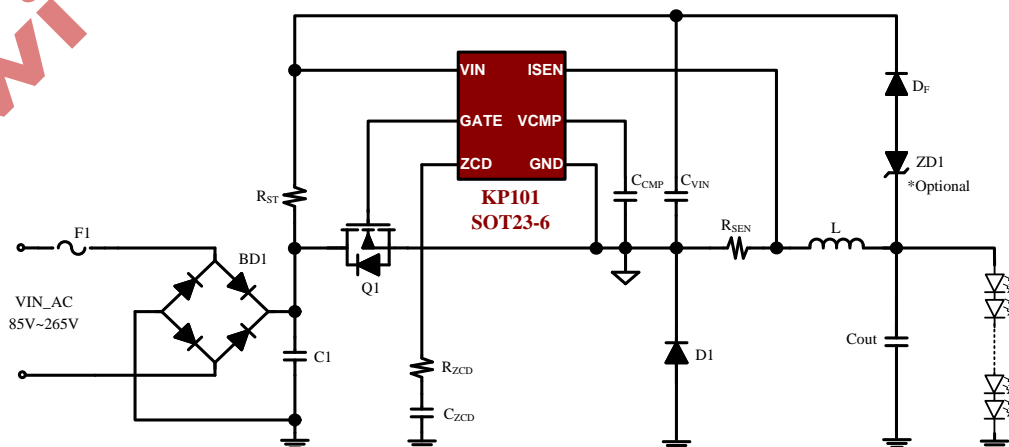
- | LED Driver Power Supplies
- | Commercial and Residential LED Fixtures
- | Non isolated Applications E27, PAR30,
- | Offline LED Lights
- | 5w-35w typical application.

GENERAL DESCRIPTION

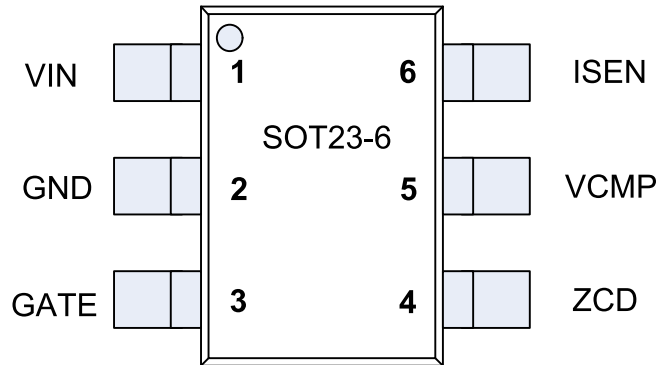
KP101 is a pulse-width modulated (PWM) controller with integrated high side floating gate driver. This switching mode power supply controller is intended for driving low to medium power single stage power factor corrected (PFC) LEDs. The devices operate in boundary mode and are suitable for buck topologies. Constant on-time boundary mode control scheme guarantees high power factor and low gate turn-on loss. Build-in gate control limits the switching frequency range from 16 kHz to 200 kHz, solving the audible noise and high switching loss issue inherited from boundary mode operation: the switching frequency will change with variation of line voltage, load voltage or load current.

The devices feature a gate driver, duty cycle limiter, error amplifier, PWM control circuitry and protection functions, as well as the proprietary zero cross detection (ZCD) technique required to implement a boundary mode switch power supply. The accurate output LED current is achieved by an average current feedback loop. The fault protection features include Under Voltage Lockout (UVLO), Over Current Protection (OCP), Over Voltage Protection (OVP) and thermal protection function (OTP). Moreover, for high efficiency, the device features low startup current enabling fast, low loss charging of the VIN capacitor.

TYPICAL APPLICATION



Pin Configuration



Pin Description

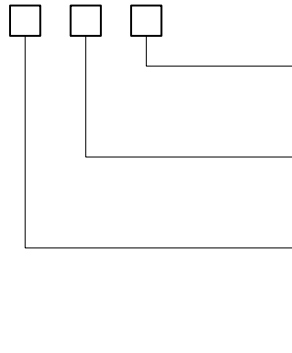
Pin Num	Pin Name	I/O	Description
1	VIN	I	Power Supply Pin of the Chip. The circuit starts to operate when VIN goes above 16V and turns off when VIN goes below 8V. After startup, the operating range is recommended to be from 10V to 18V.
2	GND	P	Ground of the Chip.
3	GATE	O	Gate Driver for External MOSFET Switch.
4	ZCD	I	Zero-Current-Direction Pin. Typically a 2M ohm resistor and a 1pF capacitor are recommended to be connected between ZCD Pin and Power Ground of the LED output, which needs fine-tuned in actual design.
5	VCMP	I	Control loop Compensation Pin.
6	ISEN	I	LED Current Sense Input Pin. Typical internal current reference threshold is -90mV and a resistor is used to sensing the averaged output current.

Ordering Information

Part Number	Description
KP101LGA	SOT23-6, Halogen free in T&R, 3000Pcs/Reel

Marking Information

KP101



Pack:

Blank: Tube

A: Tape

Package material:

P: RoHS compliance

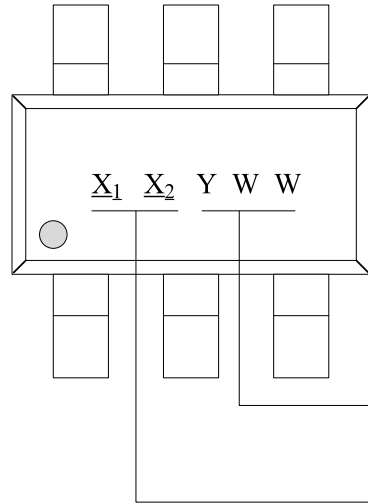
G: halogen free

Package type:

L: SOT-26

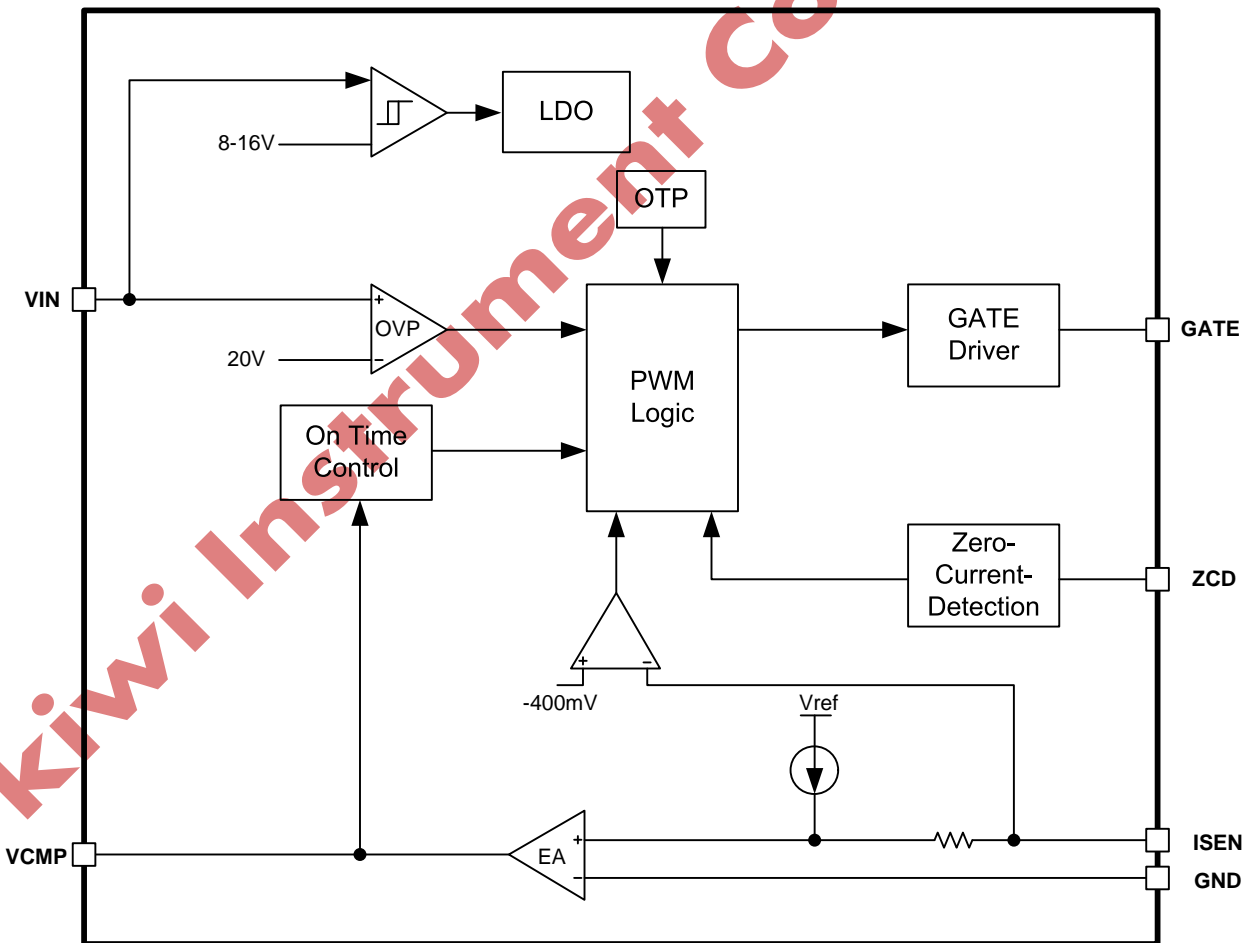
Part number

SOT-26 Mark Spec



Year & week code
 Y: 3 for 2013
 WW: 0-52
 Part number
 Underline means RoHS
 Default is Halogen free

Block Diagram





KP101

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Absolute Maximum Ratings (Note 1)

Rating	Symbol	Value	Unit
Supply Input Voltage	VIN	20.5	V
GATE Voltage	GATE	14	V
ZCD Voltage	ZCD	6	V
Compensation Voltage	VCMP	6	V
Current Sense Voltage	SENSE	-0.350 to 6	V
Power dissipation, @ TA = 25°C SOT-23-6	PD	0.350	W
Package Thermal Resistance SOT-23-6 (Note 2)	RθJA	255	°C/W
Junction Temperature	TJ	150	°C
Lead Temperature (Soldering, 10 s)	TL	260	°C
Storage Temperature Range	TSTG	-65 to 150	°C
ESD Susceptibility (Note 3)			
ESD Capability, HBM (Human Body Model)	HBM	3500	V
ESD Capability, MM (Machine Model)	MM	350	V

Recommended Operation Conditions (Note 2)

Rating	Symbol	Value	Unit
Supply Input Voltage	VIN	10.2 to 20	V
Junction Temperature	TJ	-40 to 150	°C
Operating Ambient Temperature	OAT	-40 to 125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Start-up voltage	V _{IN_ON}		--	16	--	V
Under Voltage Lockout Threshold	V _{IN_OFF}		--	8	--	V
Maximum Startup Current	I _{ST(MAX)}		--	---	150	uA
Input Supply Current	I _{CC}	After Start-Up with switching, VCC = 15V	--	1	3	mA
Input Quiescent Current	I _{QC}	After Start Up without switching, VCC = 15V	--	100	--	uA
Input Over Voltage Protection threshold	V _{IN_OV}		--	20	--	V
Current Sense Reference Voltage	V _{I_ref}		--	90	--	mV
Maximum Switching Frequency	f _{SW_MAX}		--	200	--	kHz
Minimum Switching Frequency	F _{sw_MIN}			16		kHz
Over current protection level	V _{OCP}			-400		mV



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Minimum Turn-On Time	$t_{ON(MIN)}$		--	300	--	ns
Maximum On Time	t_{ON_MAX}			13.6		us
GATE Pin Voltage	V_{GATE}		--	13.5	--	V
GATE Drive Rise and Fall Time	T_R/T_F	1.0nF Load at GATE	--	--	100	ns
GATE Drive Source / Sink Peak Current	I_{Source} / I_{Sink}	1.0nF Load at GATE	--	0.5 / 0.8	--	A
Thermal Shutdown Temperature	T_{SD}			--	140	°C
Thermal Shutdown Hysteresis	T_{SDH}			80		°C

Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note2. $R_{\theta JA}$ is measured in natural convection at $T_A = 25^\circ\text{C}$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note3. Devices are ESD sensitive. Handling precaution is recommended.

Note4. The device is not guaranteed to function outside its operating conditions.

OPERATION DESCRIPTION

The KP101 is a high side buck type PWM LED driver controller for high performance non-isolated LED application. Its high side floating gate driver is used to control the buck converter via an external MOSFET and regulate the constant output current. The KP101 can achieve high accuracy LED output current via the average current feedback loop control and high power factor by the constant on time Active PFC control.

I Start-Up Operation

Before the operation, the VIN Cap is charged through the start-up resistor for KP101. When the VIN voltage reaches the threshold of V_{IN_ON} (16V typically), the chip is enabled and GATE begins to switch; after that the VIN cap is to be discharged due to the increased operation current of the IC which will be continued until the VIN cap voltage is taken controlled by the built-up output voltage.

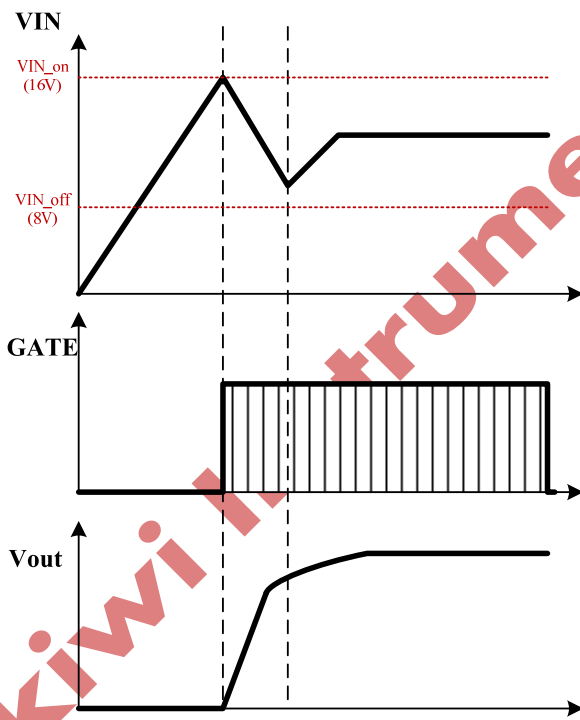


Fig. 1

I Quasi-Resonant Operation Mode

KP101 utilized the Quasi-Resonant Operation Mode to achieve high efficiency and better EMI performance compared with conventional PWM

Control.

Internally a resistor R_{INT} is connected between GND Pin and ZCD Pin which is used to sense the dynamic current flowing through the IC GND Pin and the Output Ground. Shown as Fig.2, a resistor and a capacitor are also needed to be connected between the ZCD Pin and the output Ground. When the inductor current reaches zero, the polarity of the voltage source V_{source} is changed from $+V_F$ to $-V_o$ which will cause a negative current flowing through the resistor of R_{INT} and ZCD Pin voltage starts to fall down. When the voltage of ZCD pin is lower than its internal threshold, the set signal will be triggered by its internal ZCD block and next cycle of GATE signal begins.

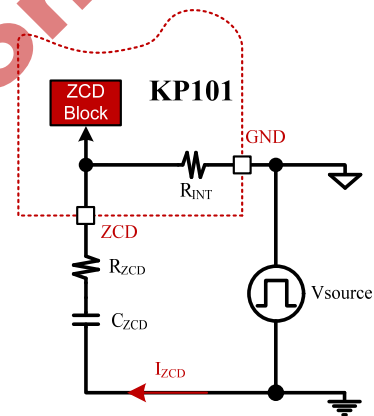


Fig. 2

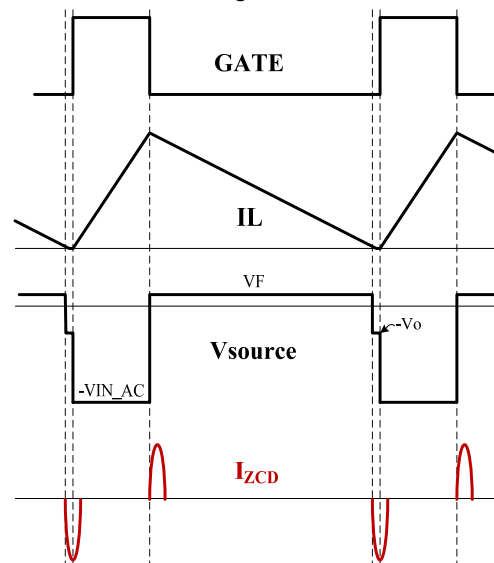


Fig. 3

I Active Power Factor Correction

In KP101, the on time of GATE signal is controlled as a constant within a line cycle and the off time of GATE is controlled by the ZCD signal. By this method, the switching frequency varies with the real-time value of AC input voltage and the averaged input voltage becomes sinusoidal to achieve high PF value, which is shown in Fig.4. Normally a large capacitor, such as 100nF, is recommended to be connected to VCMP Pin to keep low bandwidth control loop for High PF.

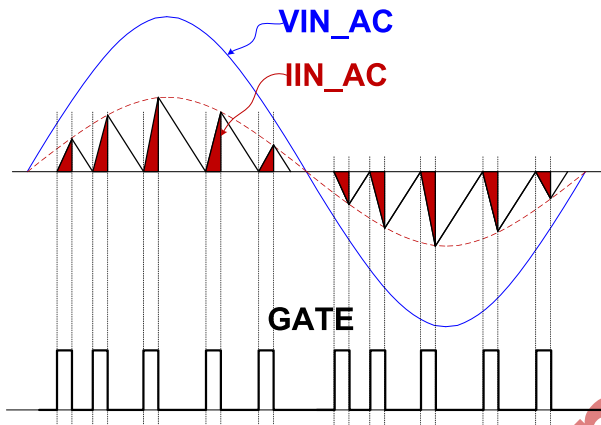


Fig. 4

I Setting Average Output Current

The output current that flows through the LED string is set by an external resistor, R_{SEN} , which is connected between the GND and ISEN Pin. The relationship between average output current, I_o , and R_{SEN} is shown below:

$$I_o = \frac{90mV}{R_{SEN}}$$

I LED Open Protection

Normally the power supply of the chip is taken by the AC Line input through the start-up resistor at the beginning of system start and taken by the output voltage through the feedback diode after output voltage becomes high enough.

If the LED is opened, the output current will be charged into the output capacitor only which causes the output voltage and the IC VIN Pin rise up quickly. When the threshold of V_{IN_OV} is triggered, internal logic and GATE signal is shut

down. Then the system is latched and next start-up is initiated only by re-plug the AC input.

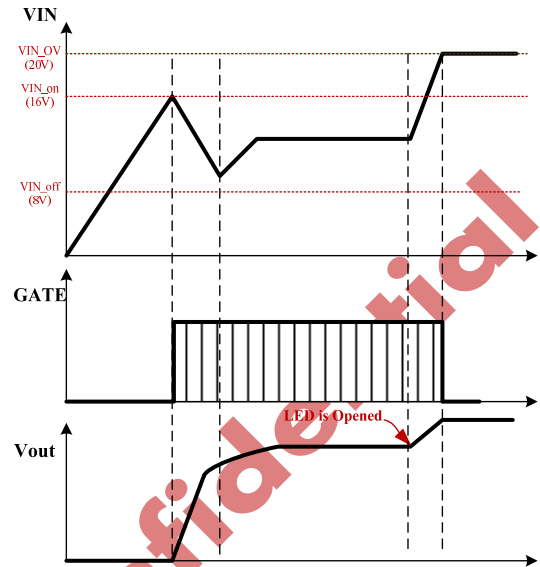


Fig. 5

I LED Short Protection

After the LED is short, the output voltage becomes too small to charge the VIN Capacitor and the VIN starts to fall down. When the threshold of V_{IN_OFF} is triggered, GATE stops switching and VIN is recharged due to the decreased IC operation current through the start up resistor. When the threshold of V_{IN_ON} is triggered, the GATE starts to work again which will be repeat continuously until the fault condition is removed. By the function, the auto-recovery is realized for LED short Protection in KP101.

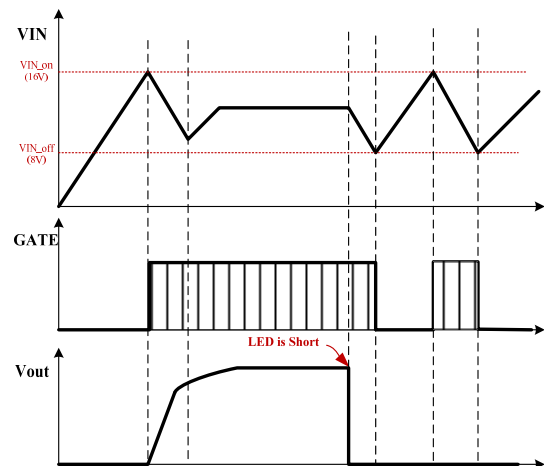


Fig. 6

I Cycle by Cycle Current Limit (OCP)

To limit the peak inductor current value, an internal -400mV threshold is designed in KP101. After the turn on of GATE signal, the inductor current rises up and the ISEN Pin voltage starts to falls down. If the inductor current is too large to cause the ZCD Pin voltage to be lower than -400mV, the GATE will be blocked immediately and next switching cycle will be triggered by the ZCD signal.

I Minimum and Maximum Switching Frequency

For constant on time PFC control, the switching frequency varies with the real-time AC input. With the increase of the AC input, the switching frequency becomes smaller; with the decrease of the AC input, the switching frequency becomes larger. To avoid audio noise and decrease the requirement of the EMI filter design, the minimum and maximum switching frequency is limited as 20 kHz and 200 kHz internally in KP101.

I Thermal Shut Down

When the IC temperature is over 140 °C, the IC shuts down. Only when the IC temperature drops to 80 °C, the IC restarts to work again.

COMPONENTS SELECTION

I Start-Up Resistor (R_{ST})

Make sure the current flowing through the R_{ST} is larger than the IC start-up current I_{ST} (150uA typically).

$$R_{ST} < \frac{V_{in_min}}{I_{ST}}$$

Where:

V_{in_min}: the minimum peak value of AC input voltage. For universal input, V_{in_min} is 120V.

I VIN Capacitor (C_{VIN})

To meet the requirement of the start-up time T_{ST} (from AC input added to IC starts to work), the VIN capacitor is recommended to be selected by the following equation:

$$C_{VIN} < \frac{(\frac{V_{in_min}}{R_{ST}} - I_{ST}) \cdot T_{ST}}{V_{IN_ON}}$$

Normally too much small value of C_{VIN} will cause too short start-up time. But too much small value of C_{VIN} will cause the first time start-up failed. If the capacitor of C_{VIN} is not big enough and secondary-start-up happens, go back to re-select the start-up resistor until the ideal start-up sequence is obtained.

I VCMP Capacitor (C_{COMP})

Generally a large enough capacitance of C_{COMP} is needed to achieve high power factor (100nF typically). Usually larger capacitance of C_{COMP} can provide bigger phase margin for the control loop which also make the start-up time larger at the same time.

I PFC Inductor Design(L_{PFC})

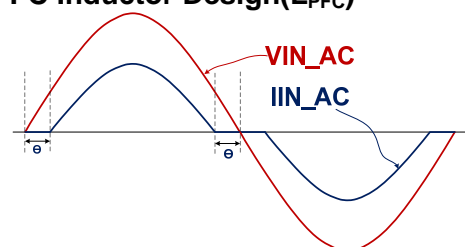


Fig. 7

For buck PFC converter, a dead conduction angle always exists when the real-time input voltage is smaller than the output voltage. Then the input power can only be transferred to the output within the conduction angle of $\pi-2\theta$. According to the power balance rule, the PFC inductor can be calculated by the following equation:

$$L_{PFC} = \frac{V_o \cdot h}{2p \cdot F_{sw_min} \cdot I_o} \left(\frac{p}{2} - \frac{V_o}{V_{in_min}} \cdot \sqrt{V_{in_min}^2 - V_o^2} - \arcsin\left(\frac{V_o}{V_{in_min}}\right) \right)$$

Where:

V_{in_min} : The minimum peak value of AC input voltage. For universal input, V_{in_min} is 120V.

F_{sw_min} : The pre-set minimum switching frequency. 40 kHz is recommended for universal input and 80 kHz for narrow input.

V_o : The DC output voltage

I_o : The averaged output LED current.

η : The pre-set overall efficiency, 0.95 is recommended as typically value.

The peak current for the PFC inductor, Power MOSFET and Diode is:

$$I_{PK} = \frac{V_{in_min} - V_o}{F_{sw_min} \cdot L_{PFC}} \cdot \left(\frac{V_o}{V_{in_min}} \right)$$

I Output Capacitor (C_{out})

For PFC converter, two times of AC line frequency voltage ripple should be observed on the output capacitor which value is related to the output current I_o , peak to peak output voltage ripple ΔV_o , AC line frequency f_{ac} and system efficiency η :

$$C_{out} = \frac{I_o}{h \cdot 4p \cdot f_{ac} \cdot \Delta V_o}$$

I MOSFET and Diode Selection

When the circuit is working with the maximum AC line input voltage, the voltage stress of the MOSFET and Diode is maximum; when the circuit is working with minimum AC line input voltage and full load condition, the current stress is maximum.

For MOSFET: $V_{DS_MAX} = \sqrt{2} \cdot V_{ac_max}$

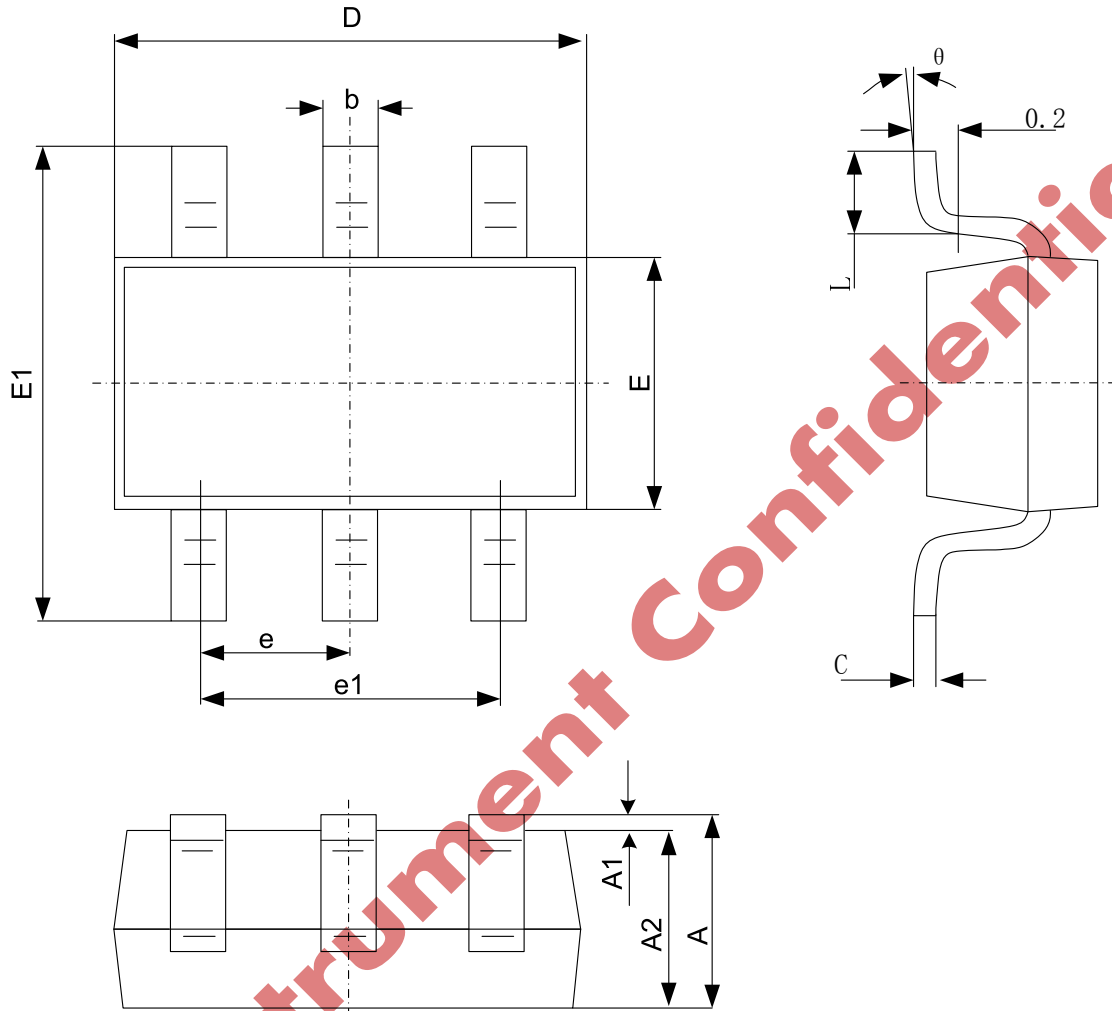
$$I_{DS_MAX} = I_{PK}$$

For Diode: $V_{DR_MAX} = \sqrt{2} \cdot V_{ac_max}$

$$I_{DF_MAX} = I_{PK}$$

Package Dimension

SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.047
A1	0.000	0.150	0.000	0.006
A2	0.900	1.100	0.035	0.043
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



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